CESAR: Cryogenic Electronics for Space Applications

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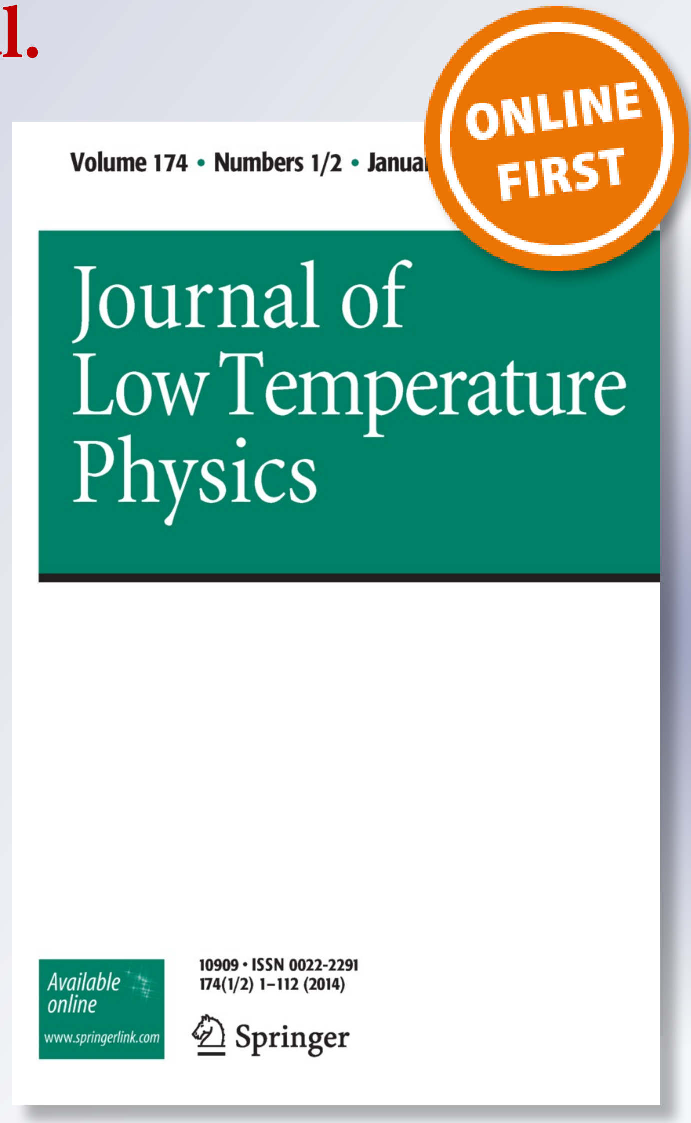

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Abstract Ultra-low temperature sensors provide unprecedented performances in X-ray and far infrared astronomy by taking advantage of physical properties of matter close to absolute zero. CESAR is an FP7 funded project started in December 2010, that gathers six European laboratories around the development of high performances cryogenic electronics. The goal of the project is to provide far-IR, X-ray and magnetic

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sensors with signal-processing capabilities at the heart of the detectors. We present the major steps that constitute the CESAR work, and the main results achieved so far.

Keywords Cryogenic electronics · High impedance detectors · X-ray microcalorimeters · Far-infrared bolometers

1 Introduction

In the coming decade, the European Space Agency has scheduled programs in X-ray and far infrared astronomy with improved detector arrays (number of pixels and signal sensitivity). This is a consequence of the great successes of the XMM-Newton, Planck and Herschel missions launched by ESA in 1999 and 2009. Nevertheless these developments are slowed down by the restricted amount of available power, at low temperature, in space conditions. The power budget is mainly consumed by the ever-growing number of wires that link the cooled detectors to the distant (~10 m) warm electronics. A possible solution is the development of the signal processing functions at the heart, or close to the detectors themselves. The development of such cryogenic and complex electronics is the goal of CESAR. The three steps are presented below: cryogenic front-end electronics with intrinsic properties as good as the detector ones, complex electronics circuits (amplifiers, filters, multiplexers, DACs and ADCs) working at or below 4 K, and combination of both developments and end-to-end tests on large 2D arrays (multiplexed X-ray microcalorimeters, far-infrared bolometers and magnetometers). One of the CESAR peculiarities is this three level complementarity and dependence between the different technical work packages: components/circuits/physical applications.

2 Elementary Components

2.1 AsGa HEMTs

During the last decades, silicon JFETs have been the transistors of choice for the low-frequency and high impedance readout electronics with low noise performances (~1nV/Hz$^{1/2}$). But these devices cannot operate below 100 K and therefore often require long cables between the focal plane containing the detectors and the readout electronics stage. To avoid the limitations due to these cables, new generation

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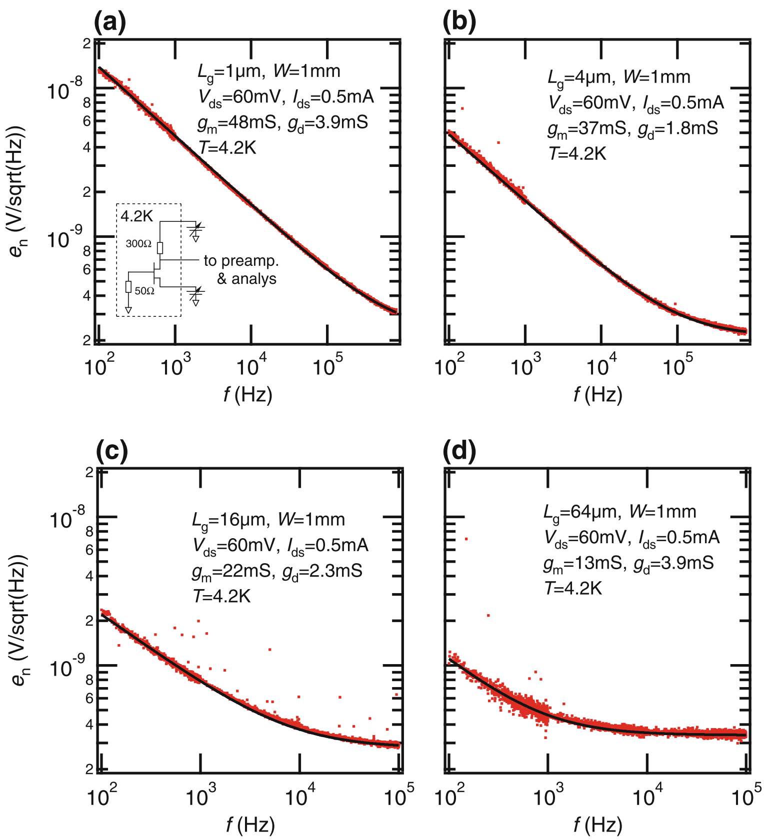

Fig. 1 Input voltage noise measured at 4.2 K for four different gate geometries, see Refs. [1–3] for more details. (Color figure online)

transistors will have to work at cryogenic temperatures (i.e. between 50 mK and 2 K). High electron mobility transistors have already been used at very low temperature and with very low noise, but never at low frequencies. In the CESAR framework, CNRS/LPN (France) has studied AsGa HEMTs specially designed for the requirements of low-frequency/high-impedance detectors (with low gate leakage current and low input voltage noise).

Various heterostructures have been grown by molecular beam epitaxy and HEMTs with different gate geometries have been fabricated and characterized at low temperatures [1–3] (gate length $L_g = 1, 2, 4, 8, 16, 32$ and 64 µm), see Fig. 1. Measurements showed that with an increase of L_g, a significant decrease of the capacitance C_{gs} is observed [3].

Experimental results show that the equivalent input noise voltage e_n in HEMTs at 1 kHz and 4.2 K is approximately inversely proportional to the square root of their input capacitance C_{gs}. For example for C_{gs} of about 20 and 100 pF, the corresponding e_n are of about 1 and 0.46 nV/Hz$^{1/2}$, respectively. Typical value for dissipation is of the order of a few tens of µW around 1 K.

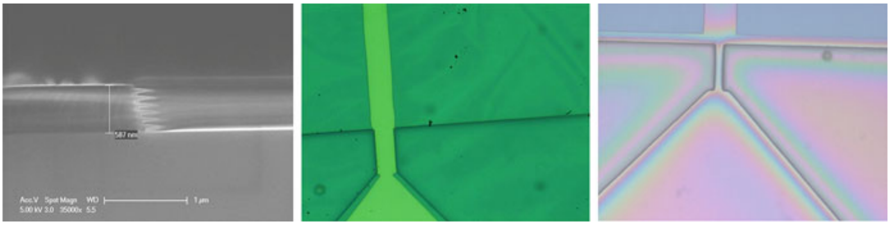

Fig. 2 *Left* SEM image of a Bragg mirror used for the GILD process, after etching. *Middle* optical image of the gate area after developing and before removing the photoresist on the Bragg mirror. *Right* gate area after opening of source and drain areas in the second Bragg mirror. (Color figure online)

2.2 Ge JFETs

The CNRS-IEF (France) partner is developing Ge based JFETs fabricated via an original approach based on laser doping of source, drain and gate areas. In contrast with the classical doping by ion implantation, the laser doping technique developed at IEF [4] results in sharp interfaces similar to that obtained by epitaxial growth (Fig. 2). The first part of the CESAR project was dedicated to preliminary experiments and design studies. The main issues to be addressed were the cleaning of germanium substrates before epitaxial growth of the JFET channel, the UHV-CVD homoepitaxial growth of doped germanium, the superficial gas immersion laser doping (GILD), the formation of ohmic contacts on n and p types doped germanium. It must be emphasized that the obtainment of an ohmic contact on n-type Ge is rather challenging. Several advances have been achieved in particular in the GILD development, and the group is pursuing the developments in particular in the improvement of the design.

3 Complex Circuits

3.1 Circuits Based on SiGe Bipolar Transistors

CEA/SEDI (France) is developing readout electronics based on SiGe CMOS/BiCMOS technology (commercially available at AMS foundry, using its 0.35 μm BiCMOS technology) mainly for the needs of X-ray cryogenic microcalorimeters [5]. The specific constraints for this application are: high impedance ($\sim$1 MΩ), low input capacitance (not to slow down the signal, bandwidth = 100 Hz to 10 kHz), ultra low noise ($\sim$1 to 2 nV/Hz$^{1/2}$ at 1 kHz) and very low dissipation ($<$1mW per output signal). During the first half of the project, several ASICs have been tested in a cryogenic environment (4.2 K), in association with HEMTs produced by the LPN group. This first generation ASICs have showed good results, fulfilling the requirements of a future X-ray space mission with microcalorimeters:

- Cut-off frequency = 9.3 kHz for a 1 MΩ input load.
- Noise = 2.4 nV/Hz$^{1/2}$ at 1 kHz, 0.9 nV/Hz$^{1/2}$ at 10 kHz.
- Power switching and multiplexing = tested at 100 kHz and 1 MHz with good performances.

– Anti charges injection system (compensation system to avoid charges injection on the detector) = tested at 100 kHz and 1 MHz with good performances.

3.2 CMOS Circuits

The IMEC Institute (Belgium) develops complex circuits for high impedance, low-frequency IR/submm detectors, such as cryogenic low power DAC, ADC, amplification and filtering circuitry [6]. The first test circuits have been successfully designed to the preliminary specifications and have been processed in the foundry and tested.

The first part of the project consisted in an explorative phase for parameter extraction at cryogenic temperature (both simulation and tests). Several foundries have been considered to provide the commercial 0.35 μm 0.18 μm CMOS technologies depending on their cryogenic expected behaviors (e.g. threshold voltage, transient effects, noise) and process availability (Europractice Service). Several circuits have been tested at Konkoly Institute (Hungary) at low temperature. The first IMEC readout circuit connected to a cryogenic bolometer array will be tested later in 2013.

4 Applications

4.1 X-ray Microcalorimeters

The CEA group in Saclay (France), together with UNIPA (Italy), develop high sensitivity microcalorimeters [5] for the next generation X-ray space missions. The work is based on the technology developed for low-temperature bolometers for Herschel/PACS (see below). The goal is to have a large focal plane (32×32 pixels) with 2–3 eV resolution on a full 6×6 arcmin field of view. A baseline for the design of the demonstrator has been established. First measurements of a SiGe ASIC connected to HEMTs have been performed in the test bench in Saclay. More details can be found Jean-Luc Sauvageot's paper in this conference.

4.2 Far-infrared Bolometers

The (sub)millimeter group at CEA Saclay develops detectors (bolometers) and instruments [7] for submillimeter and millimeter astronomy that operate in ground-based telescopes and space observatories. The requirements for next generation space missions (SPICA, COrE/PRISM, FIRI) are extremely challenging compared to state of the art technology developed for Herschel for example (improvement by two orders of magnitudes for sensitivity, ~10 times more detectors,...). To achieve such performances the bolometers have to operate at very low temperatures (~20–50 mK). Therefore, along with the work on detectors itself, the performances of the entire electronic readout chain have to be demonstrated at very low temperatures, with a particular focus on the power consumption. The final product of this work package is a demonstrator of a complete analogue cryogenic chain to be integrated with a detector array (16×18 bolometers, see Fig. 3) working below 300 mK. The minimum

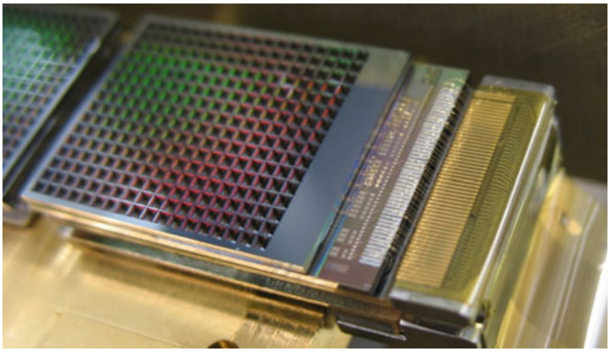

Fig. 3 A 16 × 18 bolometer arrays used in the submillimeter ArTMiS camera. (Color figure online)

readout chain should have 2 channels (minimum) with 16 pixels sampled at 20 kHz. In particular, the DACs need to work with 8 bits (0–3 V) and the ADC with 12 bits (DAC and ADC work at 4 K, dissipating a few mW in total).

4.3 Magnetometry

Imperial College London and CEA/SPEC have been working on the development of highly sensitive magnetometers for space applications [8]. They have defined the specifications required for a three-axis magnetometer in three specific cases: outer planet orbiter, outer planet lander and shadowed Nanosat. The design is based on CEA's GMR sensor (giant magnetoresistance, one-axis) for high sensitivity/low frequency specifications [9]. The sensor comprises four GMR elements assembled in a Wheatstone bridge configuration. Each of the sensor has the following dimensions: 1 mm (length) × 50 µm (width) × 50 nm (stack thickness). Increasing the GMR volume allows reducing the 1/f noise which is usually dominant below few hundreds of Hz, limiting the performances of small size GMR sensor for static field or low frequency field measurements. Furthermore, the four elements are mounted by pairs with opposite hard layer direction to form a bridge. This ensures compensation of the resistance offset and of the thermal drift of the sensor. This sensor has been tested in terms of sensitivity and noise at low frequency. The sensitivity is 30V/T for 1 V on the bridge at room temperature and 48V/T at 77 K. Tests at lower temperature using cryogenic SiGe electronics developed by CEA/SEDI are ongoing.

5 Conclusions

All the activities of the CESAR project are progressing well, with some impressive results (extremely high performances of HEMTs transistors for example). The very challenging development of Ge-JFETs is ongoing and will go on until the end of the project. The first versions of elementary components and complex circuits have been tested in good cooperation with the applications groups. Full demonstrators will be realized during the coming year, as originally planned. The CESAR developments have found applications to the medical and scientific domain through the magnetometric brain imaging [10]. The association of the cold electronics circuits with giant magnetoresistive sensors could efficiently compete with current techniques.

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