A Simple Software-based Resolver To Digital Conversion System

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***Abstract*—In this paper, a software-based resolver to digital converter (RDC) is proposed. The hardware signal conditioning circuit is realized using common electronic components, while the algorithm can be implemented either using a microcontroller or an FPGA. Its validation and performance analysis has been carried out using an interior permanent magnet synchronous machine drive and, with comparative purposes, an LTN Servotechnik 1024 ppr incremental encoder. Tests show that the proposed RDC is characterized by a good dynamic response and precision, moreover, due to low computational demand, it can be successfully adopted without significant extra cost.**

Keywords—Resolver, Resolver to Digital Converter, Electric Drives, speed measurement.

I. INTRODUCTION

Closed-loop drives require, among other things, sensors for speed and position measurement. Resolver is a position sensor widely used in various applications such as robots, machine tools, radars, and other systems like aircraft, satellite antennas, and electromechanical braking systems [1]. In fact, it is characterized by a simple and robust design, it has low sensitivity to vibrations and offers fine resolution and accuracy, low output impedance, wide temperature range, small size, weight, and negligible power consumption [2].

The resolver is essentially a bi-phase electrical machine, whose rotor is excited by a sinusoidal voltage waveform at a few kHz. Rotational resolvers can be classified on the base of rotor typology in wound rotor and variable reluctance rotor. The first one is characterized by higher accuracy and a more complex structure, higher weight and size, while the second one has a simpler structure, higher reliability and smaller size and weight, but it is influenced by manufacturing tolerance and high installation requirements [3]-[4]. Several studies on resolver electrical winding design have been carried out to improve resolver performance [5]. Also, low-cost hall-effect sensors have been used to emulate resolver sensors, to control machines not equipped with speed sensors [6].

Resolver output voltage waveforms can be processed in order to extract the rotor absolute position signal. Several methods have been developed to achieve this goal. The most common and commercially solution used is the integrated circuit (IC) RDC, characterized by high cost, and additional hardware stages which determine low reliability, extra board space, and a low versatility [7]-[9]. Many commercial solutions employees integrated components such as the AD2S1210 whose hardware stages, such as buffer or conditioning circuit for resolver excitation and output resolver signals acquisition, include a high number of additional passive components [10]. Although several studies have been conducted to realize performant, versatile and low-cost full-analog integrated circuits, nowadays, the most common approach is to integrate hardware and software RDC solutions. In detail, the resolver output voltage waveforms are digitalized by an ADC and the acquired signals are processed by a DSP, or an FPGA or a microcontroller. This approach leads to a cheaper, more reliable, and more versatile system. Most common software-based RDCs are designed taking into account Phase Locked Loop (PLL) [12]-[13] or Angle Tracking Observer (ATO) algorithms [14]-[15]. Also with this approach, the hardware interface presents a complex structure with a high number of electronic components that result in expensive implementation. By way of example, in [16] a high precision resolver-to-angle converter is proposed but it presents a complex demodulator and sinewave and trigger generator circuits that employ several operational amplifiers (OAs), transistors and passive electronic components.

In [17]-[18], the authors describe a software-based low-cost RDC implemented in the dSPACE system: in detail, hardware conditioning circuits are realized to adapt both excitation signal to resolver features and output waveforms to dSPACE ADC, and the used ATO algorithm is explained. Although the demodulation and processing algorithm is extremely simple and functional, the conditioning circuit has high power losses and tends to heat up a lot, therefore a heatsink is required. Furthermore, conditioning circuits are employed to adapt the resolver output signals to ADC features for acquisition purposes. In this paper, the ATO algorithm presented in [18] is implemented on sbRIO 9651 FPGA controller, and a novel excitation circuit is presented. The hardware interface of the proposed RDC system is only composed of an excitation buffer circuit, and it has been designed to obtain resolvers output signals which can be directly acquired with typical ADCs without conditioning circuits. The goal is to minimize both analog excitation circuit power losses and costs since the excitation circuit is entirely realized with common electronic components. The paper is structured into the following sections: Section II describes the resolver operation principle; Section III presents the hardware excitation and the software RDC implementation; Section IV presents experimental results and the RDC performance; Section V addresses the RDC cost analysis.

II. OPERATION PRINCIPLE

The resolver is a speed sensor based on the principle of mutual induction; it is a rotating electric machine with a primary rotor winding that allows the sensor excitation, and two secondary stator windings with magnetic axes 90° electrical degrees displaced. The resolver is mechanically

coupled with the motor shaft and supplied by a sinusoidal voltage waveform. When the shaft starts rotating, two amplitude-modulated sinusoidal voltage waveforms v_{sin} and v_{cos} are induced in the stator windings. According to [9], they can be expressed as:

$$\begin{cases} v_{sin} = kv_e\left[\sin(\theta)\cos(\omega_r t) + \dfrac{1}{\omega_r}\dfrac{d\theta}{dt}\cos(\theta)\sin(\omega_r t)\right] \\ v_{cos} = kv_e\left[\cos(\theta)\cos(\omega_r t) + \dfrac{1}{\omega_r}\dfrac{d\theta}{dt}\sin(\theta)\sin(\omega_r t)\right], \end{cases} \quad (1)$$

where k is the resolver transformation ratio, θ is the rotor absolute angular position, ω_r is the angular frequency of the excitation voltage. Since the excitation frequency is chosen equal to a few kHz resulting in $\omega_r >> d\theta/dt$, the second term in (1) can be neglected, leading to:

$$\begin{cases} v_{sin} = kv_e[\sin(\theta)\cos(\omega_r t)] \\ v_{cos} = kv_e[\cos(\theta)\cos(\omega_r t)]. \end{cases} \quad (2)$$

The resolver output waveforms $v_{sin}(\theta)$ and $v_{cos}(\theta)$ are sampled by an analog to digital converter (ADC) connected with the digital controller. The acquisition is led with a sampling frequency equal to the resolver excitation frequency and the acquisition must be executed when the excitation signal reaches the maximum value. In this way, the two acquired signals describe the $v_{sin}(\theta)$ and $v_{cos}(\theta)$ envelopes, whose frequency is equal to rotor shaft frequency, as shown in Fig. 1.

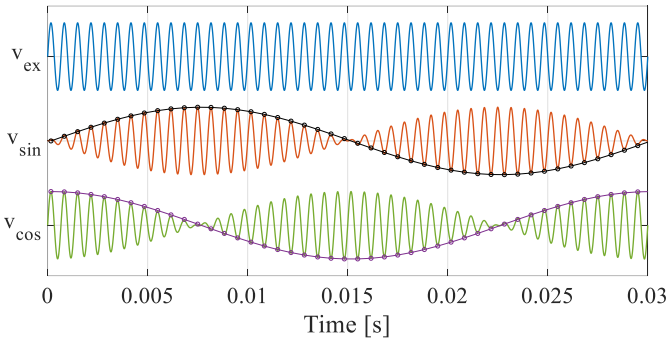


Fig. 1: Excitation signal and resolver output signals.

The acquired demodulated signals are introduced into the Angle Tracking Observer (ATO) algorithm, synthesized in Fig. 2.

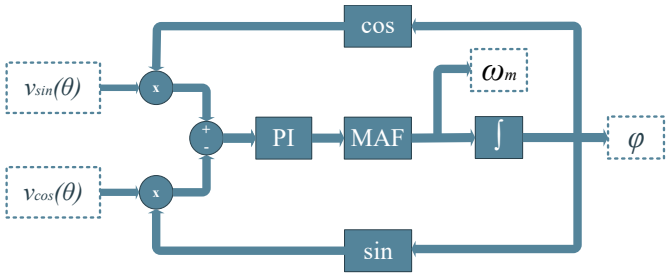


Fig. 2: ATO algorithm block scheme.

Demodulated signals $v_{sin}(\theta)$ and $v_{cos}(\theta)$ are multiplied by $cos(\varphi)$ and $sin(\varphi)$, respectively, where φ is the estimated absolute angular position. The obtained signals are compared to each other and the error generated is sent to a PI regulator that returns the speed signal. This signal is filtered by a Moving Average Filter (MAF) to eliminate the ripple; the filtered signal ω_m is integrated and the estimated angular position is obtained.

III. Hardware and Software Implementation of RDC

In this section, the resolver sensor, the hardware conditioning circuit, the RDC algorithm, and the digital controller are discussed. Table I summarizes resolver features.

TABLE I. Main Data of Resolver ARTUS S26SM19RX452CO1F

Data	Value
Input voltage/frequency	10 V at 5 kHz
Transformation ratio	0.5 ± 10%
Max. electrical error	±10’
Max. null Voltage	20 mV_{RMS}
Operating Temperature	-55°C +155°C
Max. operating speed	10 000 rpm
Mass	0.34 kg

The main purpose of this section regards the description of the proposed simplified RDC hardware interface that allows the acquisition of resolver output signals directly through typical ADCs and the respective demodulation procedure. By way of example, to validate the proposed approach, a System on Module (SoM) sbRIO 9651 produced by National Instruments has been chosen as a controller. It consists of two different cores, an Artix 7 FPGA unit, used for high-speed control implementation, and an ARM Cortex-A9 processor, used for real-time process management. FPGA and DSP cores can be programmed individually in the LabVIEW environment with a graphical programming language (G-Language). The sbRIO 9651 is fully integrated into a power electronics and drives board (PED Board), that allows simple interaction with SoM thanks to a set of peripherals such as ADCs, digital I/Os and PWM Channels. It makes the implementation of power electronics and electric drive systems control extremely easy and user-friendly. In Fig. 3, the resolver to digital conversion block scheme is presented:

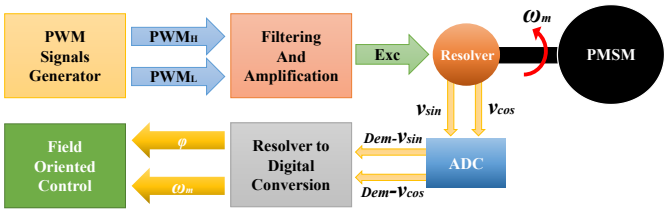


Fig. 3: System under study: excitation, conditioning, acquisition and RDC.

A. Excitation signal generation

The excitation signal is generated starting from two 5 V PWM signals, generated by the FPGA controller; the PWM generation scheme, illustrated in Fig. 4, is the Unipolar PWM, largely used to control single-phase H-Bridge Inverters.

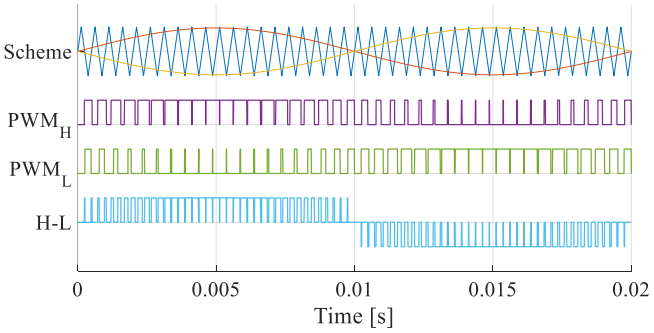


Fig. 4. Unipolar PWM Modulation scheme, PWM signals and excitation signal H-L.

Defining the switching frequency f_{sw} as the triangular carrier frequency and f as the sinusoidal modulating signal frequency, the frequency modulation index m_f is defined as:

$$m_f = \frac{f_{sw}}{f}. \tag{2}$$

Two generated PWM signals, called PWM_H and PWM_L are electrically subtracted from each other and the H-L signal is obtained. Choosing an even m_f value, H-L signal harmonics are arranged around $2m_f$ harmonic order and its multiples. This propriety makes the generated signals extremely simple to be filtered. Although the resolver nominal frequency is 5 kHz, a 10 kHz sinusoidal modulating signal is generated, for control needs. m_f is chosen equal to 40, so PWM signals are generated by the comparison of a 400 kHz triangular and two opposite phase 10 kHz sinusoidal modulating signals.

A block scheme of the RDC software implemented on the FPGA controller is presented in Fig.5. It must be underlined that, in order to avoid signal loss and real-time delay, the entire control algorithm is implemented on the FPGA target. The RT target is adopted for auxiliary functions such as signal representation and speed set point variations.

The triangular carrier and the two sinusoidal modulating signals are generated in the same way discussed in [19]. In detail, the triangular carrier is generated by an up-down counter, the modulating sinusoidal signals are generated thanks to a sinusoidal block memory and an address counter that extract elements by the memory. The address counter is also used to generate an auxiliary clock signal thanks to the acquisition is synchronized with the excitation signal, in order to execute the $v_{sin}(\theta)$ and $v_{cos}(\theta)$ demodulation.

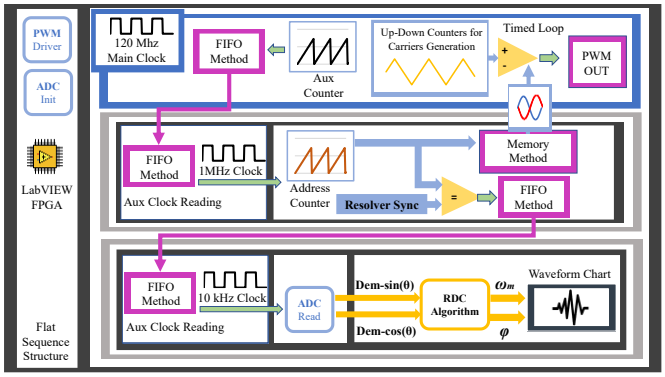


Fig. 5: RDC software block scheme implemented on FPGA controller.

Generated PWM signals are sent to the filtering and amplification circuit, presented in Fig. 6. It consists of three different stages: passive filtering, active filtering, pre-amplification and power amplification. The first stage is realized by a passive RC filter with a 16 kHz cut-off frequency; the second stage consists of an op-amp in a differential configuration with a 4.7 gain and 15.4 kHz cut-off frequency, and the last stage consists of another op-amp in inverting configuration with adjustable gain and a class B BJT based power amplifier, which feeds the required current to the excitation circuit. The output gain can be tuned, in order to match the resolver excitation voltage, thus, a 10 V 10 kHz sinusoidal signal is obtained. Bipolar ADCs have been used to directly acquire the resolver output signals without using any other stage and, therefore, simplifying further the RDC hardware interface.

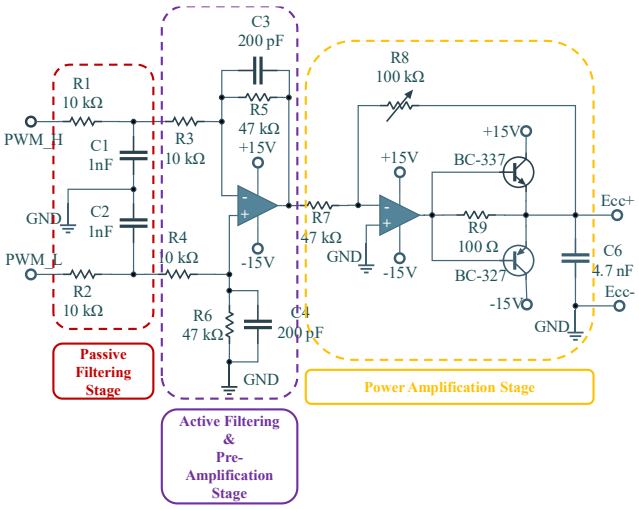


Fig. 6: Signal conditioning circuit.

B. *Demodulation and Resolver to Digital Conversion*

Resolver output signals are directly sent to the ADC without any kind of conditioning, since it has been observed that no considerable harmonic distortion is presented and no amplification/attenuation is required, in fact, signals fall into the ADC voltage input range. The synchronization between the acquisition stage and the sinusoidal excitation waveform has a vital role in the resolver to digital conversion algorithm. In order to realize it, the address counter is used to generate a 10 kHz auxiliary clock that enables the acquisition. Since the PWM signals are sent to an analog conditioning circuit, delays are introduced by the filters; to compensate delays, the synchronization is realized manually by the user, adjusting the *Resolver Sync* value in the Graphic User Interface (GUI), which triggers the acquisition. In detail, synchronization is realized when is maximized the signal v_m, defined as:

$$v_m = \sqrt{{v_{D_{sin}}}^2 + {v_{D_{cos}}}^2} \tag{3}$$

where v_{Dsin} and v_{Dcos} are the demodulated resolver output signals. Since the resolver transformation ratio is 0.5, synchronization is acceptable when v_m is equal to 5 V. Furthermore, the same signal is used to detect possible loss of the resolver phase. In Fig. 7 the resolver to digital conversion algorithm implemented on the FPGA controller is presented.

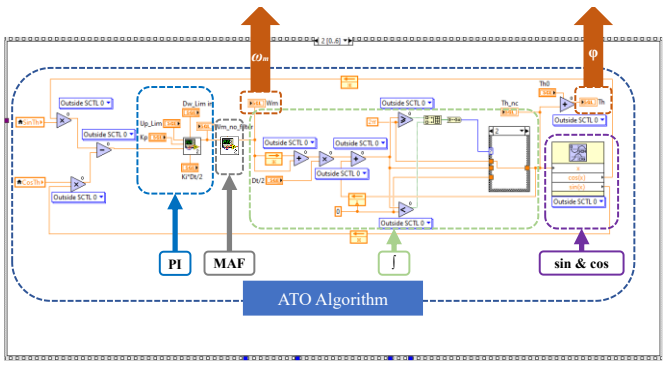


Fig. 7: Resolver to Digital conversion software implemented on FPGA controller.

The RDC algorithm is entirely implemented in Single Precision Floating Point data, following the block diagram presented in Fig. 2. PI controller and integration states are implemented with a discrete trapezoidal integration method,

in order to reduce the integration numerical error. A 40 points MAF is placed. Once the position and speed signal are obtained, they are sent to a closed-loop control algorithm and can be eventually displayed in the RT target GUI.

In Table II, the RDC algorithm required computational resources are presented. It must be noted that the algorithm presented in Fig. 5 represents the starting point for the realization of any closed-loop electric drive control. The desired control has to be put into the slowest cycle and can be implemented in single precision floating point data.

TABLE II. RDC ALGORITHM COMPUTATIONAL COST

Device Utilization	Available resources	Percent
Total slices	13300	37.8
Slice registers	106400	13.3
Slice LUTs	53200	27.3
Block RAMs	140	5.0
DSP48s	220	3.6

IV. EXPERIMENTAL RESULTS

In this section, the test bench is presented and experimental results are discussed. A Printed Circuit Board (PCB), shown in Fig. 8, has been realized to interface circuits with the FPGA. It is mounted on the PED-Board and linked with the required peripherals for this application. The test bench setup is reported in Fig. 9.

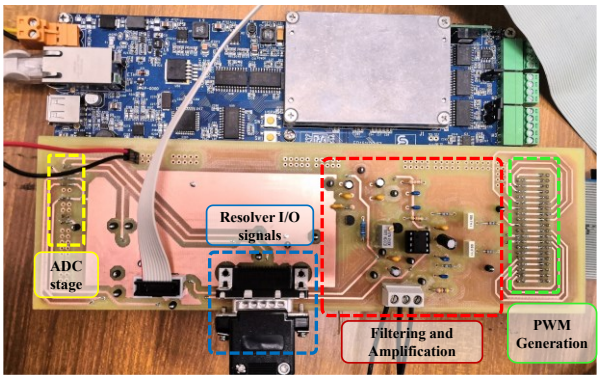


Fig. 8: PED-Board interface PCB.

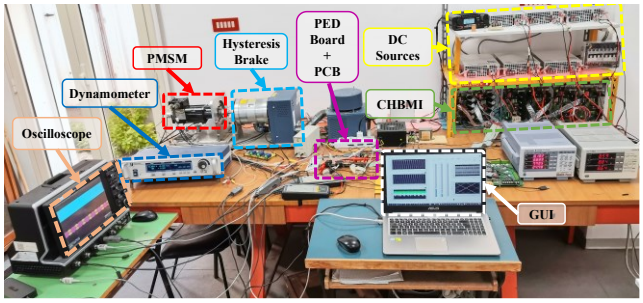
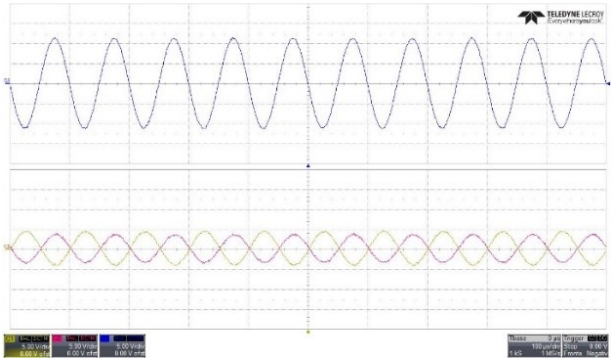


Fig. 9: Test bench.

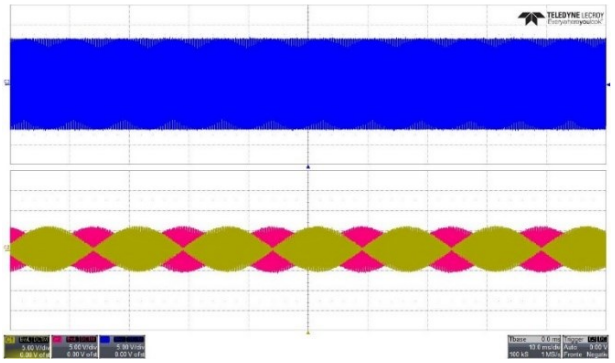
It consists of an electric drive composed of a DigiPower three-phase five-levels Cascaded H-Bridge Multilevel Inverter (CHBMI) with six H-Bridges, six DC power supply RSP-2400 whose technical data are reported in [19], and permanent magnet brushless motor (PMSM), whose technical data are presented in Table III. The electric drive is controlled by a Field Oriented Control (FOC), entirely implemented on the sbRIO 9651. A MAGTROL HD-715 hysteresis brake is used to apply a load torque to PMSM, its maximum load torque is 6.2 Nm and the maximum speed is 30000 rpm. Furthermore, an incremental encoder (LTN Servotechnik, 1024 ppr, type G36 W) is employed for validation purposes. To perform a dynamic comparison analysis with an accurate speed sensor, an X4 encoding approach has been used to obtain 4096 ppr. As a way of example, some results are reported below, including resolver output signals analysis and dynamic comparison between resolver measured speed and encoder measured speed acquired by the PED-Board ADC.

TABLE III. PERMANENT MAGNET BRUSHLESS SERVOMOTOR

Quantity	*Symbol*	*Value*
Nominal speed	n_{MAX}	4000 rpm
Back EMF constan	K_{Ep}	33 V/krpm
Rated Torque	T_N	1,8 Nm
Rated current	I_N	3,6 A
Maximum Torque	T_p	7,2 Nm
Maximum current	I_p	14.4 A
Pole pairs	p	3



(a)



(b)

Fig. 10: Resolver excitation and output voltage waveforms detected in rotor block test, x-axis 100 µs/div, y-axis 5 V/div, 1MS/s (a) and 2000 rpm speed test, x-axis 10 ms/div, y-axis 5 V/div, 1MS/s (b).

In Fig. 10, the resolver excitation and output voltages, acquired by Teledyne Lecroy WaveRunner 640Zi oscilloscope at rotor block test (a) and speed test at 2000 rpm, are reported. It can be seen that, although the excitation signal is made by two PWM signals, the obtained waveform is sinusoidal. These results validate the effectiveness of the filtering stage of the proposed hardware interface.

In Fig. 11, the demodulated resolver output voltage waveforms, PMSM dq-axes voltages and currents and a comparison between encoder and resolver speed measurements obtained during a 0-2000 rpm PMSM acceleration test are reported. It can be noticed that the resolver and encoder speed trends are very similar and the encoder speed signal is more affected by disturbances. These

are due to the torsional vibrations generated by the MAGTROL hysteresis brake.

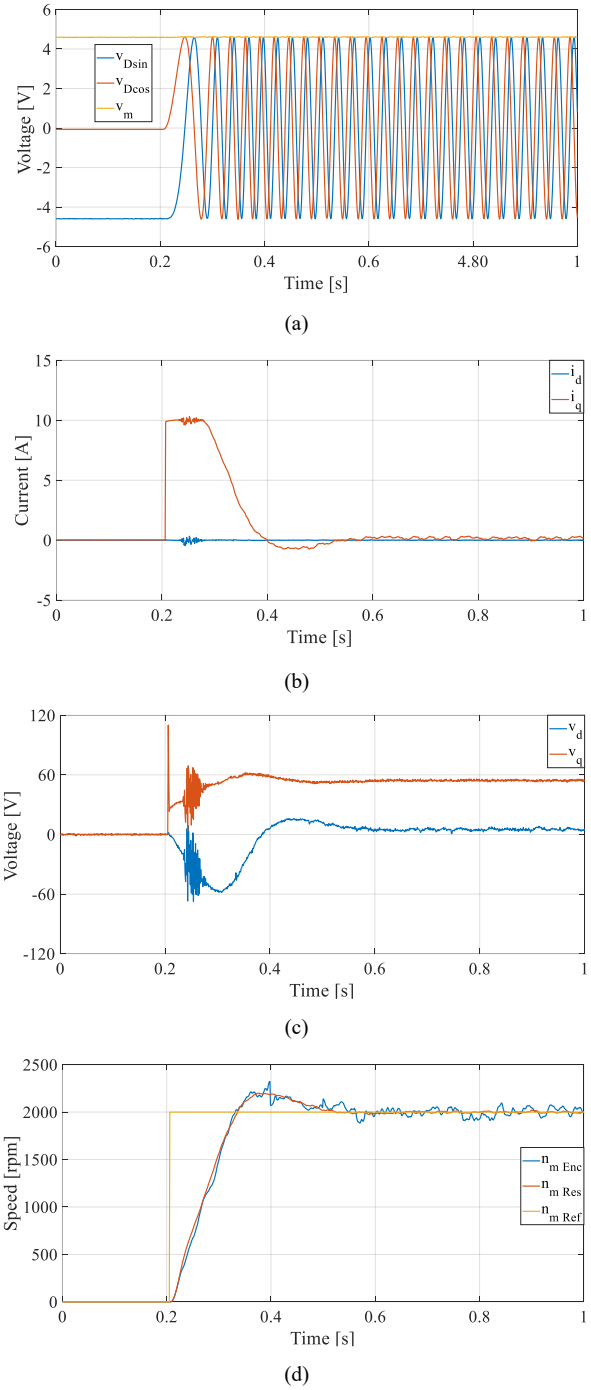


Fig. 11: PMSM drive output signals during a 0-2000 rpm acceleration test: demodulated resolver output signals(a); dq-axes currents (b); dq-axes voltages (c); speed signals (d).

In Fig. 12 another speed measurements comparison during a 0-4000 rpm acceleration is presented. Also, in this case, previous considerations are valid, thus, resolver measurements can be considered reliable and characterized by a fast and accurate response. In Fig.13 other two-speed comparisons are shown for validation purposes. In detail, in Fig.13 (a) a 1.5 Nm load torque has been applied and removed during PMSM operation at 2000 rpm. Similarly, the rated torque of 1.8 Nm has been applied and removed during PMSM operation at 3000 rpm. In this case, it is possible to highlight that the resolver measure is characterized by a lower ripple and noise than the encoder one.

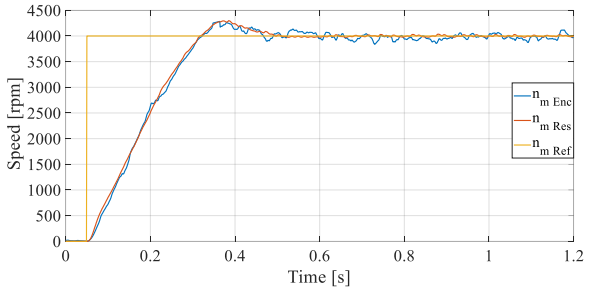


Fig. 12: Resolver and incremental encoder measured speed comparison for 0-4000 rpm acceleration.

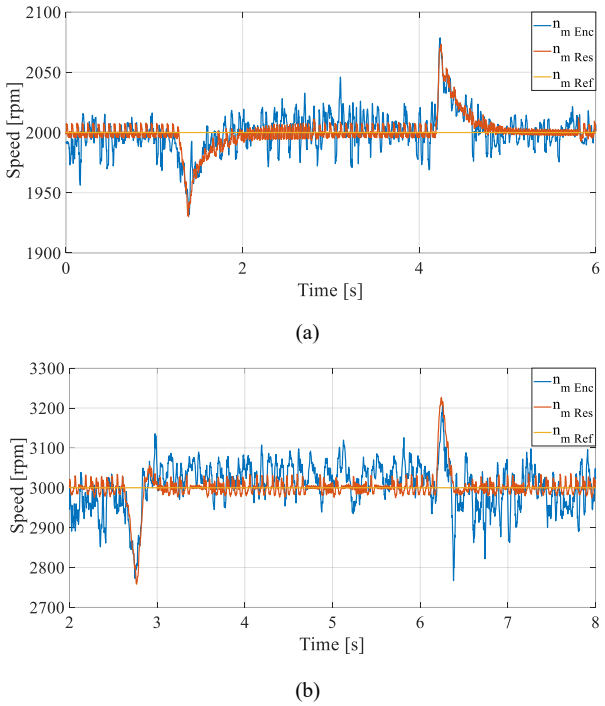


Fig. 13: Resolver and incremental encoder measured speed comparison with step load torque variation at 2000 rpm (a) and 4000 rpm (b).

TABLE IV. COST ANALYSIS

Electronic component	*Required number*	*Cost per unit [€]*
Resistors 10 kΩ	4	0.086
Resistors 47 kΩ	4	0.071
Resistors 100 Ω	1	0.086
Capacitor 1nF	2	0.25
Capacitor 200pF	2	0.163
Capacitor 4.7nF	1	0.34
Trimmer 100 k	1	2.39
Transistor NPN	1	0.254
Transistor PNP	1	0.271
TL 082	1	0.98
D-sub 15 pins	1	2.59
PCB terminal block 3 ways	1	1.66
Connector 72 pins 2.54mm step	1	2.61
PCB board		1.08
Total		**13.71**

V. COST ANALYSIS

In Table IV the required electronic components and the total price for the excitation voltage conditioning circuit are summarized. Although the PCB realization of the conditioning circuit is carried out homemade with LPKF

milling machine, the cost analysis includes the commercial cost of required electronic components and PCB board realization. The total cost is equal to € 13.71. In this evaluation, a stock of 100 units has been considered for each component and for the PCB board. This price has been evaluated as the average price of each electronic component by referring to well-known electronic components sellers, such as [20]-[22]. Obviously, if an industrial use is considered, the purchase of such components in large quantities results in a further cost reduction. For comparison purposes, the average market cost of an RDS AD2S1210 is € 29.15 [23]-[24] which is double that of the proposed RDC hardware interface and does not include the costs of the necessary buffer circuits. Hence, the system not only offers similar or better performance but is much cheaper.

VI. Conclusions

In this paper, a very simple and very low-cost resolver to digital converter has been presented. The resolver hardware and software realization has been discussed. Experimental results regarding speed comparison purposes validate the proposed RDC system that is characterized by good dynamic behaviour and presents lower noise than the incremental encoder. Cost analysis showed that the introduced RDC system is cheaper than the common IC RDCs. The proposed RDC system is extremely versatile, since the excitation voltage amplitude can be adjusted easily by a trimmer, and PI parameters can be set by the user, affecting the speed measurement and, as a consequence, the electric drive control. Since the PCB is made of electronic through-hole components, it is easy to repair and modify by the user if required. The RDC software has been implemented on a sbRIO9651 FPGA controller. Anyway, the illustrated system can be easily implemented on every FPGA, DSP, and microcontroller system because the conditioning electronic circuit can be powered with the desired DC voltage, depending on the resolver to excite and the available DC supply. These aspects make the proposed RDC a modular and extremely versatile solution.

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