Comprehensive Modelling and Experimental Testing of Fault Detection and Management of a Non-Redundant Fault-Tolerant VSI

***Abstract*—This paper presents an investigation and a comprehensive analysis on fault operations in conventional Voltage Source Inverters. After an introductory section dealing with power converter reliability and fault analysis issues in power electronics, a generalized switching function accounting for both healthy and faulty conditions and an easy and feasible method to embed fault diagnosis and reconfiguration within the control algorithm are introduced. The proposed system has simple and compact implementation. Experimental results, obtained using a test bench realized using a dSPACE® system and the fault tolerant inverter prototype operating both at open and closed loop current control, show that the proposed solution is effective and feasible and makes all faults easily managed by the control system itself.**

***Index Terms*—Fault diagnosis, Fault tolerance, Power converters, Inverters, Control, Pulse width modulation**

List of Symbols

S_{j+}; S_{j-}: switching functions of the *j-th* upper (+) or lower (-) leg device
$\hat{S}_{j+}$; $\hat{S}_{j-}$: generalized switching functions of the upper (+) or lower (-) leg device
i_j: load current in *j-th* phase
v_{jN}: inverter output voltage in *j-th* phase
h_{j+}; h_{j-}: Healthy Device Binary Variable (HDBV) for *j-th* upper(+) or lower (-) leg device
R; L: load resistance and inductance
h_{Lj}: Healthy Leg Binary Variable (HLBV) for the *j-th* phase
$\mathbf{v}_{kN}$: inverter output voltage vector (line to neutral)
$\hat{\mathbf{S}}_{k+}$; $\hat{\mathbf{S}}_{k-}$: generalized switching functions vectors of the upper (+) or lower (-) devices
u_1; u_2: partial voltages of the DC Link capacitors
i_0: input inverter current (before the DC Link)
C: capacitance value for each DC Link capacitor
$\boldsymbol{T}$: Topological inverter matrix
$\mathbf{H}_k$: square diagonal matrix of the HLBVs
$\mathbf{x}^t$: vector $\mathbf{x}$ transpose
i_α; i_β: load current components in stationary $\alpha-\beta$ reference frame
$\hat{i}_\alpha = \frac{i_\alpha}{\sqrt{i_\alpha^2+i_\beta^2}}$; $\hat{i}_\beta = \frac{i_\beta}{\sqrt{i_\alpha^2+i_\beta^2}}$: normalized $\alpha-\beta$ components of the load current in stationary reference frame
ε: security bandwidth for diagnosis algorithm
u^*_{ref1}; u^*_{ref2}; u^*_{ref3} U^*_{ref1}; U^*_{ref2}; U^*_{ref3}: post fault reference voltages of healthy legs and their corresponding phasors
$U_{inv,(j)}$: inverse voltage component for fault in the *j-th* phase
U_{RMS}: Root Mean Square of the voltage u
$\alpha = e^{j\frac{2}{3}\pi}$: complex operator for symmetrical components
$U_{inv(A.B.C)}$: voltage inverse phasors after fault and reconfiguration on phase A, B, C respectively
φ: generic displacement angle between post fault reference voltages
$\mathbf{u}_{ref}$: inverter pre-fault reference voltages vector
$\mathbf{u}^*_{ref}$: inverter post-fault reference voltages vector
$\mathbf{h}_L < \bar{\mathbf{h}}_L$: HLBVs and negated HLBVs vectors
$\lceil x \rceil$ approximation of x to the next integer ;
$v_{sD,}$ v_{sQ} stator voltages components in the rotating DQ reference frame;
$i_{sD,} i_{sQ}$ stator current components in the rotating DQ reference frame;
$\Psi_{sD,}$ Ψ_{sQ} stator fluxes components in the rotating DQ reference frame;
ω speed of the rotating reference frame, synchronous pulsation;
R_1 stator resistance (per phase) of the induction motor;
P_p Induction motor pole pairs.

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I. Introduction

THE ULTIMATE GOAL of fault tolerant inverters is either to ensure continuous operations, eventually at reduced performance, or to quickly stop operations in case of failures, thus preserving overall safety. This feature is particular relevant not only in hazardous environments or mission critical applications such as underwater or submarine applications [1], aerospace applications [2], [3], but in numerous situations of practical interest in industry, transportation etc.

Power converter reliability depends on the adopted components, hardware design, and on how control software has been conceived, developed and tested. However, it has been estimated that at least 80% of faults are due to semiconductors failures, as consequence of short circuits, interruptions, open circuits, driver misfiring) etc. [4]–[8],— [7], [9]–[14].

Fault tolerant inverters have been investigated for several years, and significant progresses have been attained with this regard. The huge technical literature can be categorised within some specific subject areas, in particular some articles concern inverter topologies for fault tolerant operation [7], [15]–[17]. Redundant and non redundant topologies [5], [13], [18], [19],

multilevel inverters [15], [18], [20]–[24] and matrix converters with fault tolerant capabilities [18], [19], [25]–[27] have been equally considered. Redundant topologies with additional components or parts of the circuits operating only in case of failures, have been investigated too. Nowadays it is universally recognized that these latter ones offer the best performance since they do not lead to degradation of the supplied electrical power; on the contrary, non redundant topologies, assuming temporary performance degradation, on the basis of some modified control strategies exploit the possibility of minimum additional components for reconfiguration and operation [5], [13], [18], [19].

Other interesting technical papers concerning the application of fault tolerant inverters, investigate around the limits of performance or control issues taking into account the specific application field *i.e.* industrial drives , automotive, distributed generation systems, etc [8], [21], [28]–[32]. Control algorithms and fault diagnosis systems, more or less integrated within the operational range of the system are addressed in [4], [13], [16], [33], [34].

By developing a relationships between pre-fault and post-fault equations, an easy and effective integration of the fault diagnosis and the inverter reconfiguration becomes possible within the original control system scheme. In this paper, a non redundant fault tolerant inverter topology has been considered and a fault tolerant operational approach has been introduced, which is characterised by high level of integration among analysis, modelling, control and monitoring issues [10], [13], [14], [34]–[38]. The fault tolerance algorithm can be easily embedded within the control system and implemented using the same microcontroller. It is based on the normalized Park's current vector [22], [39]–[42], the general inverter mathematical model and some relationships between pre and post-fault conditions. The resulting faulty-mode mathematical model allows a prediction of the effects on both the internal (DC Link) and the external behavior (i.e. load voltages and currents), and returns voltages and current waveforms in good accordance with the experimental results.

The hereafter presented mathematical model is based on the definition of some appropriate variables which rescue the informations about the healthy or the faulty inverter state. These variables also suggests a fault-tolerant reconfiguration control strategy for the inverter and, at the same time, a way for the fault diagnosis. These variables have been called Healthy Device Binary Variables (HDBV) and Healthy Leg Binary Variables (HLBV), respectively [36], [38].

A practical usage of the mentioned variables in an inverter test bench gets in touch both the diagnosis of the fault, and the reconfiguration strategy of the inverter, making control in fault tolerant mode very simple and immediate, with evidence of experimental data reported at the end the article.

In the following, Section 2 summarizes problem formulation showing the generalized approach with state variables, hence introduces HDBV and HLBV.

Section 3 deals with control and fault diagnosis system for fault tolerant mode based on the same HLBV. Fault tolerant control is designed to be immediately integrated with other closed-loop controls, *i.e.* the external control system, dedicated to the main task of the apparatus, continues to operate according to its usual modes, even in the presence of a fault except for a very short transient.

Section 4 shows some results obtained using a laboratory setup.

Finally, Section 5 summarizes some conclusions and remarks making some analysis and drawing future work.

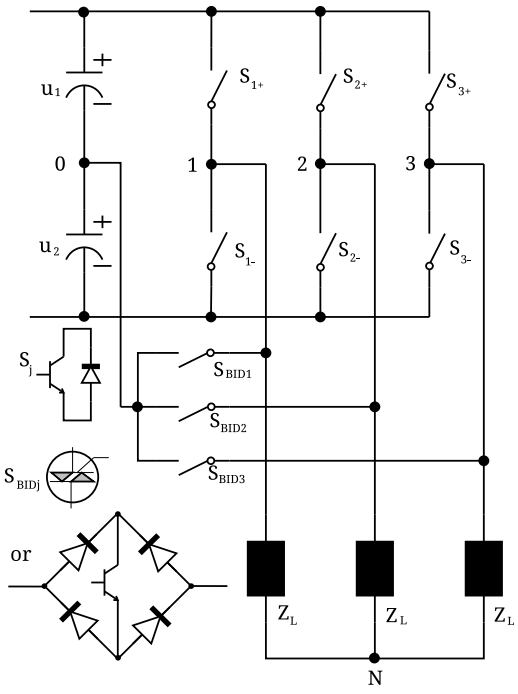


Figure 1: Non redundant fault tolerant inverter topology.

II. Inverter model during healthy and faulty mode

The topology of a non-redundant fault tolerant inverter is shown in Fig. 1. The primary switches are IGBTs with antiparallel free-wheeling diodes. Additional bidirectional switches S_{BIDj} (see Fig. 1) add fault tolerant operations by connection of the load poles with the DC link midpoint. They could be TRIACs but, since they exhibit high susceptibility to fast changing and pulsating voltages, IGBTs with single phase rectifier bridges are preferred, thus allowing unidirectional currents with alternating load currents.

As discussed in [15], [38], in order to take into account potential faults, conduction across free-wheeling-diodes should taken into account, hence the following switching functions $\hat{S}_{j+/-}$ has to be introduced:

$$\begin{cases} \hat{S}_{j+} = & [S_{j+} \wedge (i_j > 0)] \vee \left[\overline{S}_{j-} \wedge (i_j < 0)\right] \\ \hat{S}_{j-} = & [S_{j-} \wedge (i_j < 0)] \vee \left[\overline{S}_{j+} \wedge (i_j > 0)\right] \end{cases} \quad (1)$$

where $S_{j+}$and S_{j-} $\left(S_{j-} = \overline{S}_{j+}\right)$ are complementary switching functions $(S_{j+} = 1/0)$ for the upper/lower device of the

$j-th$ phase and $\vee$, $\wedge$ represent "OR" the "AND" logical operators, respectively.

In (1) the term at the left hand of the OR operator represents the condition for which the controllable devices are turned on while the right one is that relative to diode conduction.

To fix the ideas, let's the upper free-wheeling diode is conducting if the load current is negative and, at the same time, if the lower IGBT is switched off, otherwise it'll carry on the current. Similar consideration applies to other conditions.

If a fault occurs to the upper IGBT then S_{j+} vanishes and the negative current is conducted by the free-wheeling diode or by the lower IGBT, so the generalized switching function for the upper switch reduces to the term: $\left[\overline{S}_{j-} \wedge (i_j < 0)\right]$.

To depict the general case, it is sufficient to introduce a *Healthy Device Binary Variable* (HDBV) defined as follows:

$$\begin{cases} h_{j\pm} = & 1 \text{ if the upper (+)/lower (-) device is healthy} \\ h_{j\pm} & 0 \text{ otherwise.} \end{cases} \tag{2}$$

The introduction of such variables makes the definition of the generalized switching function very simple:

$$\begin{cases} \hat{S}_{j+} = & [h_{j+}S_{j+} \wedge (i_j > 0)] \vee \left[h_{j-}\overline{S}_{j-} \wedge (i_j < 0)\right] \\ \hat{S}_{j-} = & [h_{j-}S_{j-} \wedge (i_j < 0)] \vee \left[h_{j+}\overline{S}_{j+} \wedge (i_j > 0)\right] \end{cases} \tag{3}$$

In fact, it is sufficient to multiply each $S_{j\pm}$ by the corresponding variable $h_{j\pm}$. The same principle holds in case both transistor and diode are broken. However, in this case the signal coming from the expression $\left[\overline{S}_{j-} \wedge (i_j < 0)\right]$, or similar, is used to reset the integrators used in the load simulation. The load equation is:

$$v_{jN} = Ri_j + L\frac{di_j}{dt} \tag{4}$$

while its integral form is:

$$i_j = \frac{1}{L}\int_0^t (v_{jN} - Ri_j)\, dt. \tag{5}$$

Notice that, in order to correctly model converter behavior, in case of simultaneous fault to one IGBT and its free-wheeling diode ((5)) has to be reset. In this way, the load current is forced to zero every time the bottom device is turned off. Finally, the proposed HDBVs approach holds even if an entire inverter leg becomes faulty.

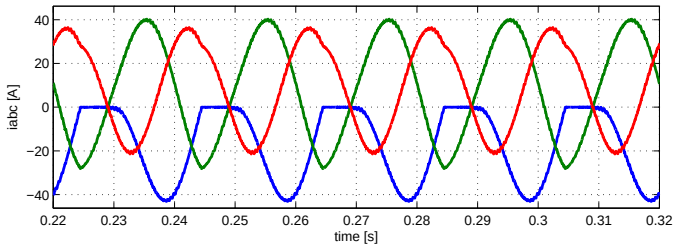
By introducing the *Healthy Leg Binary Variables* (HLBVs):

$$h_{Lj} = h_{j+} \wedge h_{j-} \tag{6}$$

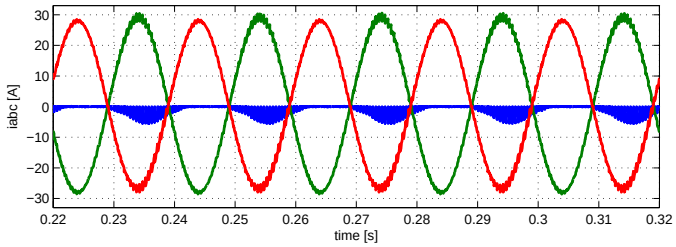
a general inverter model including both faults and post fault reconfiguration can be obtained through the following matrix equations [13], [38]:

$$\mathbf{v}_{kN} = \mathbf{T}\mathbf{H}_k \left(u_1\hat{\mathbf{S}}_{k+} - u_2\hat{\mathbf{S}}_{k-}\right) \tag{7}$$

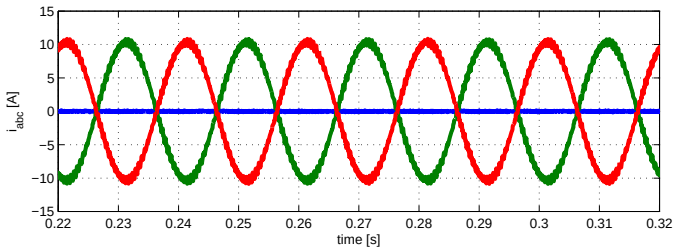
$$\begin{cases} u_1 = & \frac{1}{C}\int_0^t \left(i_0 - \hat{\mathbf{S}}_{\mathbf{k+}}^{\mathbf{t}}\mathbf{H}_{\mathbf{k}}^{\mathbf{t}}\mathbf{i}_{\mathbf{k}}\right) dt \\ u_2 = & \frac{1}{C}\int_0^t \left(i_0 + \hat{\mathbf{S}}_{\mathbf{k-}}^{\mathbf{t}}\mathbf{H}_{\mathbf{k}}^{\mathbf{t}}\mathbf{i}_{\mathbf{k}}\right) dt \end{cases} \tag{8}$$



(a) Current simulation after a single upper IGBT fault.



(b) Current simulation after an upper simultaneous IGBT and diode fault.



(c) Current simulation after a complete phase disconnection fault.

Figure 2: Output inverter current in three different cases of open circuits faults.

being:

$$\mathbf{T} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \tag{9}$$

$$\mathbf{H}_k = \begin{pmatrix} h_{L1} & 0 & 0 \\ 0 & h_{L2} & 0 \\ 0 & 0 & h_{L3} \end{pmatrix} \tag{10}$$

It should be observed that if the inverter is healthy, $\mathbf{H_k}$ is a diagonal unitary matrix and previous equations reduce to the well known model of a three-phase inverter. Equations (7) and (8) are arranged in equivalent form, thus resulting more understandable than those in [43].

The proposed model is capable to simulate failures or breakages of a single IGBT and/or its free-wheeling diode and can be easily implemented using either an equation-oriented simulation tool (e.g. Matlab/Simulink®, Octave ...); or a circuit-oriented simulator (e.g. Sim Power System® or PSIM®). The first solution has been preferred here, due to its higher simulation speed and the absence of convergence problems during integration algorithms.

III. Fault detection and reconfiguration algorithm

The proposed fault detection algorithm is based on the analysis of the normalized Park's current space vector. It is important to distinguish between three distinct cases:

1) An open-circuit fault affects only one device: the current flowing across the faulted phase can circulate only during half wave, closing its pattern through the free wheeling diode and/or the second device of the leg. The fault condition could persist long enough causing a degradation in performance (see also Fig. 2a)
2) An open circuit fault affects an IGBT and its free wheeling diode companion: in this case the current on the faulted phase vanishes, unless it is conducted by the remaining IGBT (see Fig. 2b). The load current conducted by the healthy IGBT is highly pulsating
3) An entire leg of the inverter is disconnected due to the fault: this may happens if the fault occuring to one device is propagated to the second device of the same leg. This case is typical of packaged modules or due to the intervention of fast fuses or another protection. For the damage to an entire leg, the current flowing across the faulted phase becomes zero (see also Fig. 2c).

It is worth notice that in all cases the average trajectory of the current space vector changes. In particular, in case 1, the space vector trajectory consists of two distinct parts: (i) an half circle, if all phase currents circulate, and (ii) a segment, if the current through the faulty phase is null (see e.g. Fig. 3a).

In case 2., an IGBT failure and a diode break occur simultaneously. The trajectory becomes a segment (See Fig. 3b). Previous considerations can be extended to case 3.

If the average vector trajectory becomes a segment and not related with the nature of fault:

$$\begin{cases} i_\alpha = 0 & \text{if the faulted phase is 1} \\ i_\alpha = \sqrt{3} i_\beta & \text{if the faulted phase is 2} \\ i_\alpha = -\sqrt{3} i_\beta & \text{if the faulted phase is 3} \end{cases} \tag{11}$$

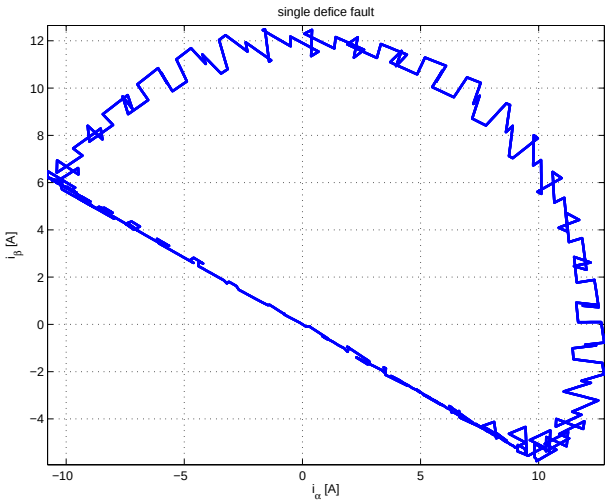
i.e. during a phase fault, from trajectory slope follows faulty phase knowledge.

In order to improve reliability and robustness, especially at very low load current (rev.3), the normalized current space vector components are considered and (11) is modified as follows:

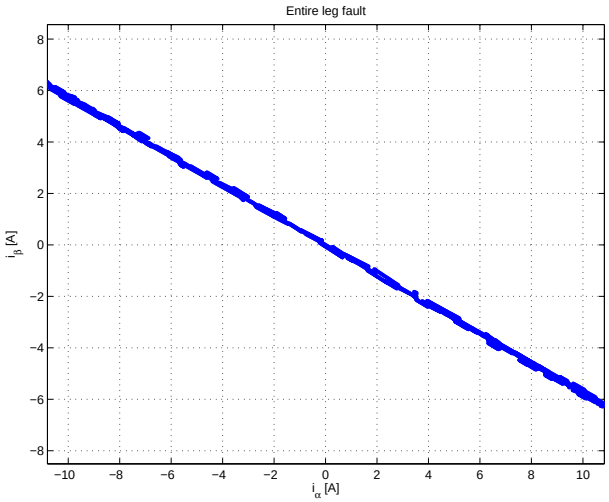
$$\begin{cases} |\hat{i}_\alpha| \leq \varepsilon & \text{if faulted phase is 1} \\ |\sqrt{3}\hat{i}_\beta - \hat{i}_\alpha| \leq \varepsilon & \text{if faulted phase is 2} \\ |\sqrt{3}\hat{i}_\beta + \hat{i}_\alpha| \leq \varepsilon & \text{if faulted phase is 3} \end{cases} \tag{12}$$

where ε is a coefficient accounting for noisy measurements and current ripple.

A full exploitation of filtered current samples helps to strengthen the diagnosis algorithm (rev. 2, rev. 3). Assuming N sampled currents per period and considering a healthy inverter, each relationship in (12) is satisfied within $\frac{2N}{\pi}\varepsilon$ samples at most. Therefore, the diagnosis process can use a pulse counter operating with the same clock used for current sampling. Such a counter is reset every time (12) are no longer verified. A threshold Γ, much higher than $\frac{2N}{\pi}\varepsilon$, is chosen as fault index.



(a) IGBT fault



(b) Simultaneous IGBT-diode or entire leg fault

Figure 3: Current space vector trajectories after fault occurrence (single devices or entire leg).

(rev.1, rev.3) Figure 4 shows the simulation of the diagnosis based on the sample counting principle. When (12) become true for each phase, counters start working until conditions hold, hence they stop and reset. Counter outputs are always compared with Γ. Clearly, for healthy legs counters stop within $\frac{2N}{\pi}\varepsilon$. For the faulted phase, instead, the counter operates for longer time and certainly overcomes Γ, highlighting fault occurrence and triggering inverter reconfiguration. After reconfiguration, the counter is reset and counting process restarts.

Figure 4 shows a simulation of a healthy inverter at 3 kHz sampling frequency and $\Gamma = 26$. The diagnosis system counts three samples at most. In practical cases, current ripple has to be taken into account, therefore Γ should be high enough to avoid the risk of false positive tests.

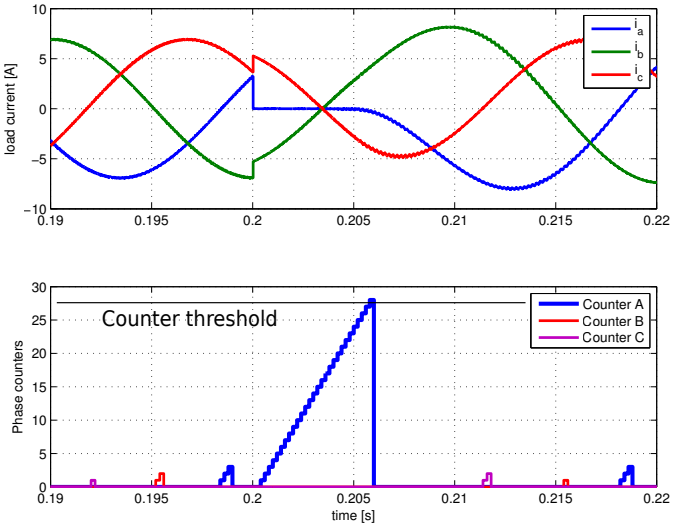


Figure 4: Fault detection operating principle based con current samples counting.

A simple calibration performed according to the highest expected current ripple should be sufficient to eliminate the problem. It is worth notice that any new incoming fault will be detected but the system cannot be further reconfigured, hence the inverter must be shutdown. Laboratory tests presented in Section IV suggest that a good trade-off is to choose a threshold $\Gamma = \Gamma^*$, between $\frac{N}{4}$ and $\frac{N}{2}$, at the highest output frequency. If the counter output is $\frac{2N}{\pi}\varepsilon \leq N \leq N_{th}$, this may indicate a pre-fault condition due to a possible gate drive failure. This abnormal condition could be reported as a pre-fault signal, useful to schedule a check and/or a maintenance operation.

It is worth notice that whatever the fault and its occurence, the time needed for its diagnosis is bounded within half period. Hence, while operating at 50 Hz, any incoming fault is diagnosed in 10 ms at most.

In fault-tolerant mode, after disabling the faulted phase, inverter control uses only two reference voltages with displacement angle $\pi/3$ to achieve a null inverse component in the output voltages.

This can be easily demonstrated by calculating the inverse component module of a pair of reference voltages $u^*_{ref1} = \sqrt{2}U_{RMS}\sin(\omega t)$ and $u^*_{ref2} = \sqrt{2}U_{RMS}\sin(\omega t - \varphi)$, where U_{RMS} is the voltage root mean square. The phasor expressions of the reference voltages are:

$$\begin{cases} U^*_{ref1} = U_{RMS}e^{j0} \\ U^*_{Ref2} = U_{RMS}e^{-j\varphi} \end{cases} \tag{13}$$

The inverse components in the three possible fault cases are:

$$\begin{aligned} U_{inv,(A)} &= \alpha U_{ref1} + \alpha^2 U_{ref2} \\ U_{inv,(B)} &= U_{ref1} + \alpha^2 U_{ref2} \\ U_{inv,(C)} &= U_{ref1} + \alpha U_{ref2} \end{aligned} \tag{14}$$

The inverse components magnitudes are:

$$|U_{inv,(j)}| = \sqrt{2}U_{RMS}\sqrt{1 + cos(\varphi \pm \frac{2\pi}{3})}; \quad j = \{1,\ 2,\ 3\} \tag{15}$$

in which the sign "+" applies for phase "1" or "3" fault, while the sign "-" applies for phase "2". In both cases, the minimum inverse factor is reached if $\varphi \pm \frac{2\pi}{3} = \pi$ i.e. for $\varphi = \pm\frac{\pi}{3}$, just resulting $|U_{inv}| = 0$.

Hence, in a faulted inverter, if the load is symmetrical and if reference voltages for healthy legs consist of a couple of sinusoidal signals with a $\pi/3$ phase displacement, the inverter output voltages and currents are both symmetrical.

By using the *HLVBs*, it is possible to synthesize a general control law for the fault-tolerant inverter including both faulted and healthy conditions. (rev. 2) The modified reference voltages u^*_{ref1}, u^*_{ref2} , u^*_{ref3}, after the inverter reconfiguration, are as follows:

$$\begin{cases} u^*_{ref1} = u_{ref1}h_{L1}h_{L2}h_{L3} + \sqrt{3}\left(\overline{h}_{L3}u_{ref2} - \overline{h}_{L2}u_{ref3}\right) \\ u^*_{ref2} = u_{ref2}h_{L1}h_{L2}h_{L3} + \sqrt{3}\left(\overline{h}_{L1}u_{ref3} - \overline{h}_{L3}u_{ref1}\right) \\ u^*_{ref3} = u_{ref3}h_{L1}h_{L2}h_{L3} + \sqrt{3}\left(\overline{h}_{L2}u_{ref1} - \overline{h}_{L1}u_{ref2}\right) \end{cases} \tag{16}$$

These equations are general. In fact, for the three fault different cases it results:

$$\begin{cases} \text{for } h_{L1} = 0 \rightarrow & \boldsymbol{u}^*_{ref} = [0,\ \sqrt{3}u_3, -\sqrt{3}u_2]^t \\ \text{for } h_{L2} = 0 \rightarrow & \boldsymbol{u}^*_{ref} = [-\sqrt{3}u_3,\ 0,\ \sqrt{3}u_1]^t \\ \text{for } h_{L3} = 0 \rightarrow & \boldsymbol{u}^*_{ref} = [\sqrt{3}u_2, -\sqrt{3}u_1,\ 0]^t \end{cases} \tag{17}$$

For the healthy case, instead $u_{ref} = [u_1,\ u_2,\ u_3]$

Previous (18), expressed in vectorial form becomes:

$$\mathbf{u}^*_{ref} = \lambda\mathbf{u}_{ref} + \sqrt{3}\left(\overline{\mathbf{h}}_L \times \mathbf{u}_{ref}\right) \tag{18}$$

where: $\lambda = h_{L1}h_{L2}h_{L3} = \det(\mathbf{H_k})$. A direct application of (18) guarantees inverter reconfiguration but introduces a $\pi/2$ phase displacement in reference voltage space vector with respect to non reconfigured reference voltages. This undesired displacement leads to additional current transients and in case of grid connected inverters may lead to loss of synchronization.

In order to avoid abrupt changes of current angles after the reconfiguration, (18) can modified as follows:

$$\mathbf{u}^*_{ref} = \lambda\mathbf{u}_{ref} + \sqrt{3}\left(\overline{\mathbf{h}}_L \times \mathbf{u}_{ref}\right)e^{-j\frac{\pi}{2}} \tag{19}$$

In fact, during healthy mode operations $\mathbf{u}^*_{ref} = \mathbf{u}_{ref}$ while during fault-tolerant mode $\mathbf{u}^*_{ref} = \sqrt{3}\left(\overline{\mathbf{h}}_L \times \mathbf{u}_{ref}\right)e^{-j\frac{\pi}{2}}$, *i.e.* phase displacement correction is active only during fault-tolerant operations.

IV. Experimental results

A test bench consisting of a dSPACE® control board and an INFRANOR® converter has been set up to demonstrate the effectiveness of the proposed fault tolerant control strategy. Over-current and under-voltage protections were not disabled

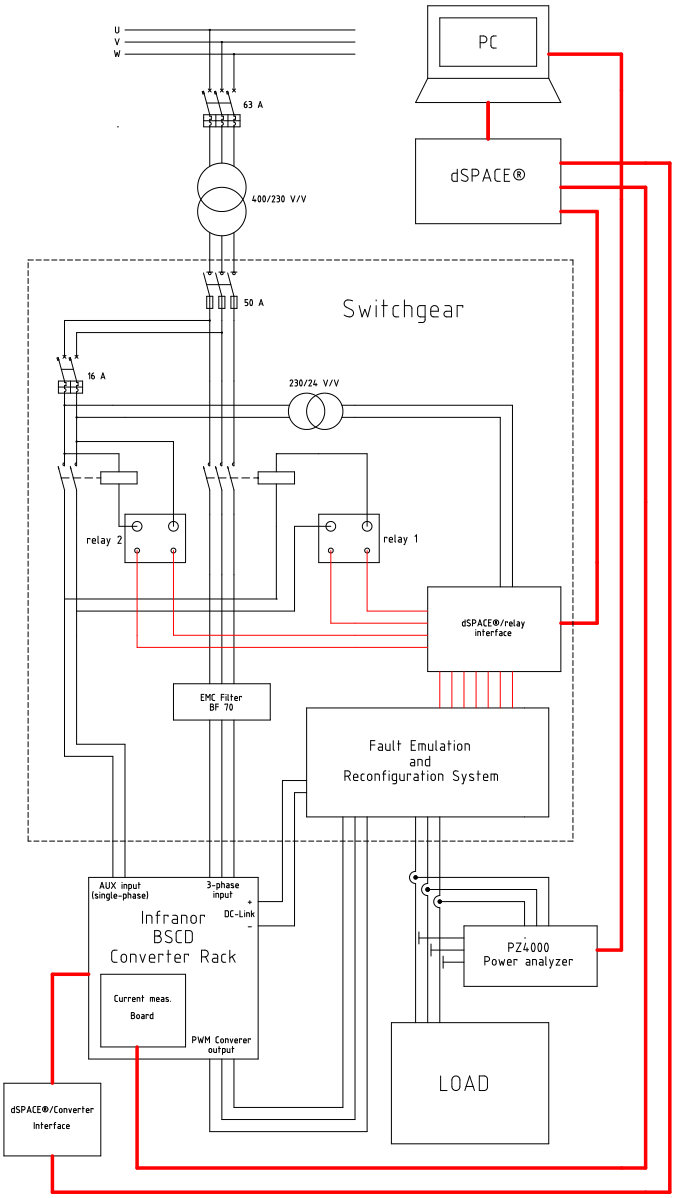
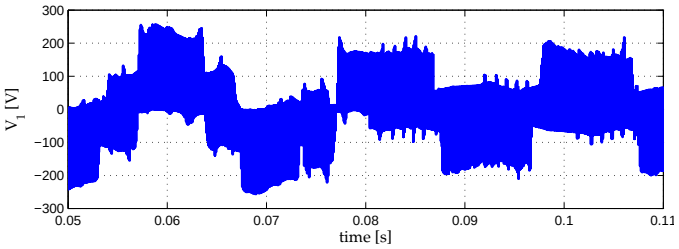


Figure 5: Laboratory setup.

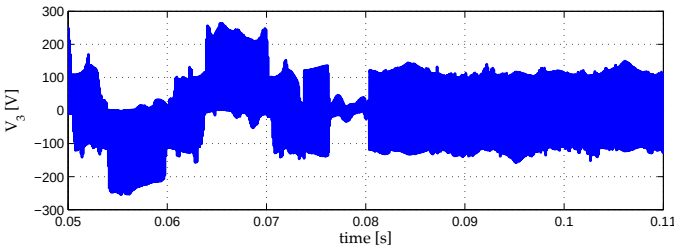
in order to demonstrate the fast and affordable operation of the fault tolerant algorithm. As a matter of fact, during almost all tests the proposed algorithm has performed faster than factory protections. Only in few cases (approximately 5%) and due to unpredictable supply network disturbances uncorrelated with the emulated fault, inverter protections disconnected the system from the network earlier than fault tolerant algorithm operation.

Table I: Rated values of the induction motor used as load

MOTOR	PARAMETERS
Power	5.5 kW
Speed	2870 rpm
Frequency	50 Hz
Torque	18.3 Nm
Voltage	400 V
Current	16 A



(a) Healthy phase



(b) Faulted phase

Figure 6: Load voltage before and after fault and reconfiguration (reference voltage 150 V, linear range, fault at 0.07 s).

(rev.1, rev. 2) Fault emulation has been realized using normally-closed relays connected between inverter output terminals and load and operated by the dSPACE® board. Anti-parallel thyristors reconnect the faulted phase pole with the DC Link mid-point.

An induction motor, whose rated values are summarized in Tab. I, and an electromagnetic brake have been used as a load.

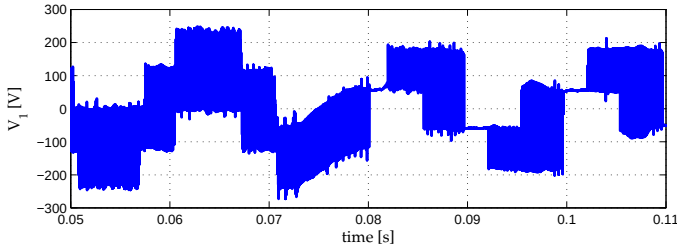
Test results have been recorded by Yokogawa® PZ4000 power analyzer and successively plotted with MATLAB®. A scheme of the test bench is shown in Fig. 5. The experimental tests have been realized both in open and closed loop current control, thus verifying the different behavior of the fault tolerant inverter in these different situations.

A. *Open loop tests*

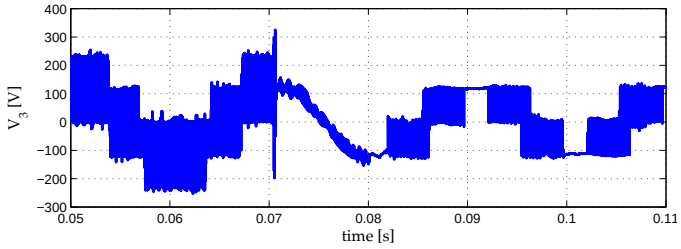
During open loop tests the converter fed the motor without speed and current loops. Hence, a fault was emulated on phase 3 ("*W*" in Fig. 5) of the converter. Tests were realized at different values of output voltages and currents and at different switching frequencies. In absence of disturbance in main supply, all tests were successful, i.e. the system performed proper diagnosis and prompt inverter reconfiguration as well.

Figure 6 depicts typical voltage patterns before and after fault and reconfiguration, on the faulty and healthy phases, respectively. Test were performed at 50 Hz, reference voltage equal to 150 V, 10 kHz switching frequency and V_{DC} =380 V. Fault detection and reconfiguration were achieved within less than half period. A similar test was also made choosing 230 V reference voltage to test the over-modulation range too (see fig. 7).

Figures 8 and 9 show induction motor stator currents at no-load and at load. After fault detection and reconfiguration, stator currents ripple is higher than before the fault, but still acceptable in most applications. Currents are affected by light

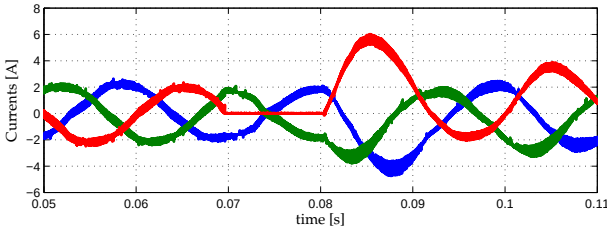


(a) Healthy phase

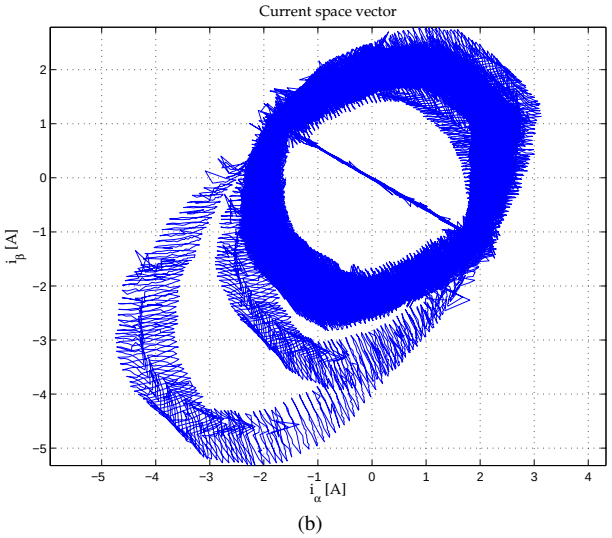


(b) Faulted phase

Figure 7: Load voltage before and after fault and reconfiguration (reference voltage 230 V, over-modulation range, fault at 0.07 s).

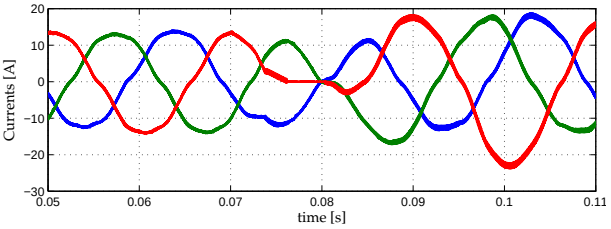


(a)

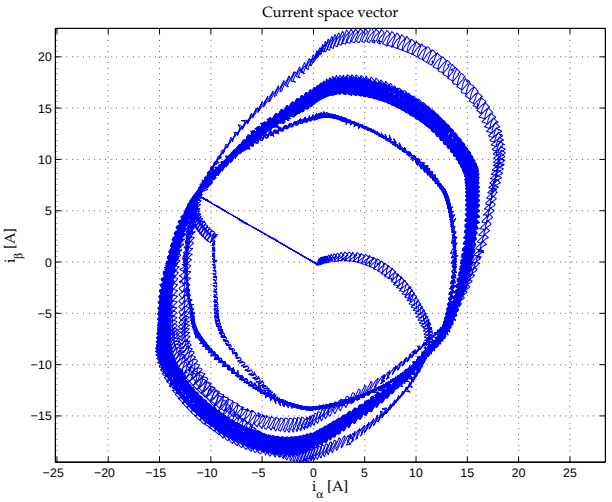


(b)

Figure 8: Motor currents at no-load (a) and space vector trajectory before and after the fault and the reconfiguration (b).



(a)



(b)

Figure 9: Motor currents at load (a) and space vector trajectory before and after the fault and the reconfiguration (b).

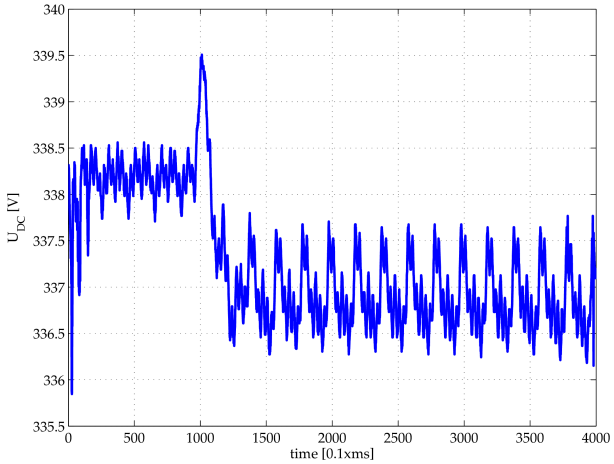


Figure 10: DC Link voltage swing before and after the inverter reconfiguration.

unbalance due the fluctuation of the DC Link voltage after reconfiguration, caused by circulation of faulted phase current across DC Link capacitors (see fig. 10).

There are several strategies for DC link voltage unbalance compensation, such as that proposed in [44]. As discussed in Section IV-B, the closed-loop current controller can implement a self compensating action just with a proper generation of the reference voltages by the current controllers.

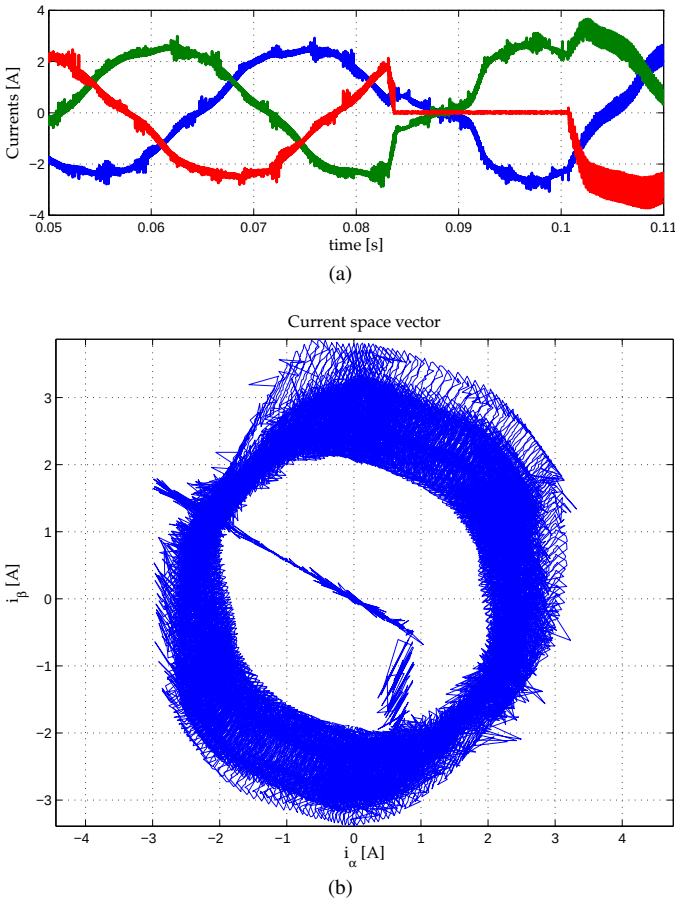


Figure 11: Motor currents at no-load (a) and corresponding space vector trajectory at closed loop before and after the fault (b).

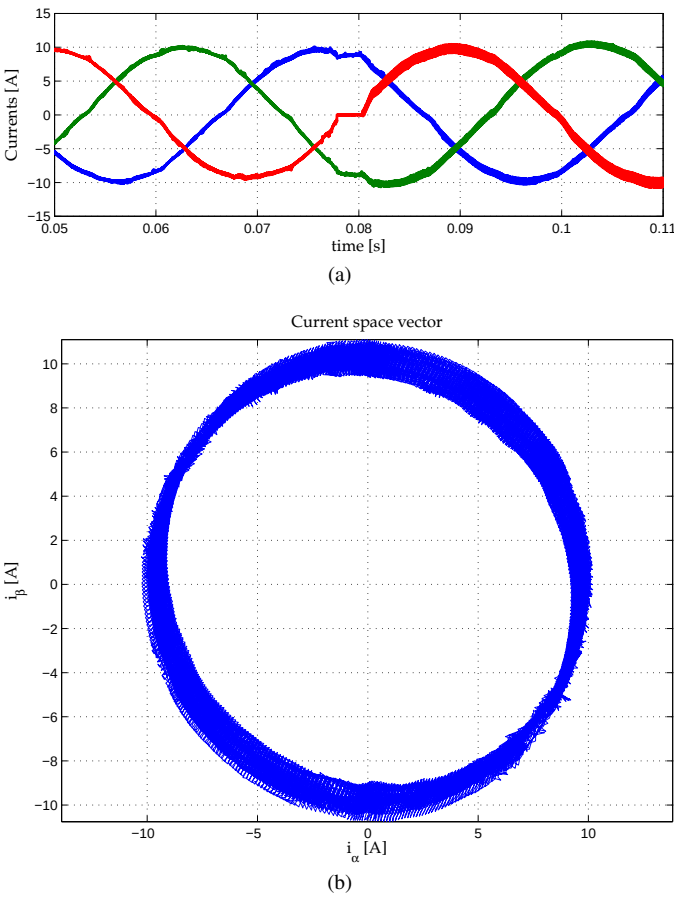


Figure 12: Motor currents at load (a) and related space vector trajectory at closed loop before and after the fault (b).

B. *Closed loop tests.*

Motor speed and current closed loop operations have also been performed. An electromagnetic brake impose different motor currents, monitored by the power analyzer.

Thanks to current regulation, the system has better behavior than during open loop operations, with special regards to current patterns. Since no blatant difference can be observed in output voltages with respect to open loop operations, only stator currents during no-load and load conditions are hereafter reported.

During no-load operations (see fig. 11) motor current ripple is still higher than before the fault, but with a smaller amount with respect to the open loop tests. As shown in Fig. 12, load currents are very satisfacoty; also current unbalance is smaller than during open loop test.

Figure 14 shows the estimated motor torque in case of closed loop test at 10 A and 50 Hz. The same figure shows that a deterioration of torque after the fault and the reconfiguration is not significant and confirms the relevance of the introduction of fault tolerant operations.

The motor torque has been estimated with a post-processing of the measured voltages and currents, using a motor model defined in a dq synchronous reference frame (20):

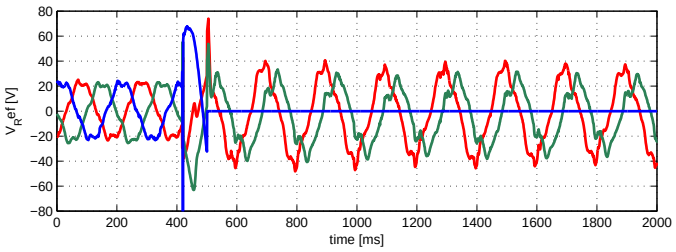


Figure 13: Reference voltages generated by current controllers before and after fault.

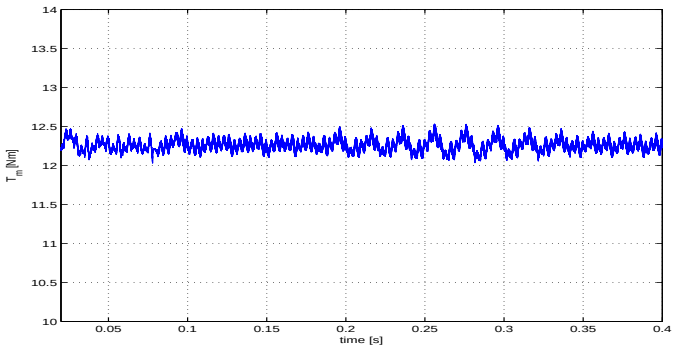


Figure 14: Estimated motor torque during the closed loop test. Fault at 0.07 s.

$$\begin{cases} \frac{d}{dt}\Psi_{sd} = v_{sd} - R_1 i_{sd} + \omega\Psi_{sq} \\ \frac{d}{dt}\Psi_{sq} = v_{sq} - R_1 i_{sq} - \omega\Psi_{sd} \\ T_m = P_p \cdot (\Psi_{sd} i_{sq} - \Psi_{sq} i_{sd}) \end{cases} \quad (20)$$

Figure 13 shows the reference voltages at the output of the reconfiguration algorithm block, generated by the current regulators, as before the faults, and rearranged according to (19) after the fault. The reference voltages of the current regulator remain almost unchanged. It is worthwhile to note that in closed loop test the $\pi/3$ phase displacement between the reference voltages remain unchanged, but a slight difference in peak voltages is evident. This difference compensates the DC link voltage unbalance and improves the load current balancing. This test confirms what has been demonstrated in [44], [45], *i.e.* introducing a proper unbalance in reference voltages, both load current unbalance and DC link voltage swinging are reduced.

V. Conclusions

This article has presented a comprehensive theoretical and an experimental testing of a non-redundant fault tolerant inverter. After introducing the generalized switching functions *HDBV* (Healthy Device Binary Variables) and the *HLBV* (Healthy Leg Binary Variables), a general dynamic model suitable for simulation of voltage source inverter both in healthy and faulty conditions has been introduced. In particular, *HDBV* and *HLBV* allow modelling of healthy, faulted and reconfigured mode operations.

The introduced variables also allow a very simple and practical formulation of a fault diagnosis algorithm based on the recognition of the Park's normalized current space vector trajectory. At the same way it enables the setting of a reconfiguration system in which the new voltage references are computed from those previously used before the inverter failure. (rev. 1, rev. 2) The strong conceptual bound between *HDBV*, *HLBV*, inverter model and post fault reconfiguration algorithm provide a great facility to realize systems in which fault tolerant control can be easily embedded within the whole system This may help to expand fault tolerance operations in all many cases of practical interest.

System reconfiguration converts pre-fault reference voltages into a two-phase reference system with $\pi/3$ phase displacement, capable to ensure a load current balance, which is often affected by significant fluctuation and the unbalancing of the DC Link voltage. However, simple compensating open loop strategy or PI regulators in closed loop current controls are able to correct the unbalance effects by introducing a slight difference in the amplitude of the post fault reference voltages.

Experimental results confirm the validity of *HDBV* and *HLBV* definitions and show how these variables simplify implementation and set up of fault tolerant control strategy In this way, traditional systems could be used even with fault tolerant inverter topologies, without the need to upset the control system itself.

References

[1] G. Flury, B. Gollentz, and C. Conilh, "Fault-tolerant inverter for subsea applications," in *EPE '09. 13th European Conference on Power Electronics and Applications, 2009.*, Sept 2009, pp. 1–10.

[2] J. Guitard, F. Richard, and K. Bouallaga, "Fault-tolerant inverter with real-time monitoring for aerospace applications," in *(EPE/PEMC), 2010 14th International Power Electronics and Motion Control Conference*, Sept 2010, pp. T9–1–T9–6.

[3] J. Restrepo, A. Berzoy, A. Ginart, J. Aller, R. Harley, and T. Habetler, "Switching Strategies for Fault Tolerant Operation of Single DC-link Dual Converters," *IEEE Trans. Pow. Electron.*, vol. 27, no. 2, pp. 509–518, 2012.

[4] D. Kastha and B. Bose, "Investigation of fault modes of voltage-fed inverter system for induction motor drive," in *Conference Record of the 1992 IEEE Industry Applications Society Annual Meeting, 1992.* IEEE, 1992, pp. 858–866 vol.1.

[5] R. Errabelli and P. Mutschler, "Fault-Tolerant Voltage Source Inverter for Permanent Magnet Drives," *IEEE Trans. Pow. Electron.*, vol. 27, no. 2, pp. 500–508, 2012.

[6] J. Li, A. Huang, Z. Liang, and S. Bhattacharya, "Analysis and design of active npc (anpc) inverters for fault-tolerant operation of high-power electrical drives," *IEEE Trans. Pow. Electron.*, vol. 27, no. 2, pp. 519–533, 2012.

[7] B. Welchko, T. Lipo, T. Jahns, and S. Schulz, "Fault tolerant three-phase AC motor drive topologies: a comparison of features, cost, and limitations," *IEEE Trans. Pow. Electron.*, vol. 19, no. 4, pp. 1108–1116, 2004.

[8] B. Vaseghi, N. Takorabet, J. Caron, B. Nahid-Mobarakeh, F. Meibody-Tabar, and G. Humbert, "Study of Different Architectures of Fault-Tolerant Actuator Using a Two-Channel PM Motor," *IEEE Trans. Ind. Appl.*, vol. 47, no. 1, pp. 47–54, 2011.

[9] E. dos Santos, C. Jacobina, and M. B. R. Correa, "Fault tolerant ac-ac single-phase to three-phase dc-link converter," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 1707–1713.

[10] A. Gaeta, G. Scelba, and A. Consoli, "Sensorless Vector Control of PM Synchronous Motors During Single-Phase Open-Circuit Faulted Conditions," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 1968–1979, 2012.

[11] E. Ribeiro, A. Cardoso, and C. Boccaletti, "Fault-Tolerant Strategy for a Photovoltaic DC–DC Converter," *IEEE Trans. Pow. Electron.*, vol. 28, no. 6, pp. 3008–3018, 2013.

[12] B. Lu and S. Sharma, "A Survey of IGBT Fault Diagnostic Methods for Three-Phase Power Inverters," in *Proceedings of the 2008 International Conference on Condition Monitoring and Diagnosis, Beijing, China*, April, 21 - 24 2008.

[13] F. Genduso and R. Miceli, "A general mathematical model for non-redundant fault-tolerant inverters," in *2011 IEEE International Electric Machines Drives Conference (IEMDC), .* IEEE, 2011, pp. 705–710.

[14] A. Di Tommaso, F. Genduso, and R. Miceli, "A geometrical simple approach for power silicon devices fault detection and fault-tolerant operation of a voltage source inverter," in *2012 XXth International Conference on Electrical Machines (ICEM),.* IEEE, 2012, pp. 1526–1532.

[15] I. Lorzadeh, E. Farjah, and O. Lorzadeh, "Fault-tolerant matrix converter topologies and switching function algorithms for AC motor drives with delta connection windings," in *2010 International Symposium on Power Electronics Electrical Drives Automation and Motion (SPEEDAM),.* IEEE, 2010, pp. 1651–1657.

[16] M. Naidu, S. Gopalakrishnan, and T. Nehl, "Fault-Tolerant Permanent Magnet Motor Drive Topologies for Automotive X-By-Wire Systems," *IEEE Trans. Ind. Appl.*, vol. 46, no. 2, pp. 841–848, 2010.

[17] M. Parker, L. Ran, and S. Finney, "Distributed Control of a Fault-Tolerant Modular Multilevel Inverter for Direct-Drive Wind Turbine Grid Interfacing," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 509–522, 2013.

[18] S. Kwak, "Four-Leg-Based Fault-Tolerant Matrix Converter Schemes Based on Switching Function and Space Vector Methods," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 235–243, 2012.

[19] D.-F. Chen, K. Nguyen-Duy, T.-H. Liu, and M. Andersen, "A fault-tolerant modulation method to counteract the double open-switch fault in matrix converter drive systems without redundant power devices," in *IPEC, 2012, Conference on Power Energy*. IEEE, 2012, pp. 65–70.

[20] S. Ceballos, J. Pou, J. Zaragoza, J. Martin, E. Robles, I. Gabiola, and P. Ibanez, "Efficient modulation technique for a four-leg fault-tolerant neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1067–1074, 2008.

[21] M. Barcaro, N. Bianchi, and F. Magnussen, "Faulty operations of a pm fractional-slot machine with a dual three-phase winding," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3825–3832, 2011.

[22] R. Ventura, A. Mendes, and A. Cardoso, "Fault detection in multilevel cascaded inverter using park's vector approach with balanced battery power usage," in *Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011)*, Aug 2011, pp. 1–10.

[23] M. Ruba and D. Fodorean, "Analysis of fault-tolerant multiphase power converter for a nine-phase permanent magnet synchronous machine," *IEEE Trans. Ind App.*, vol. 48, no. 6, pp. 2092–2101, 2012.

[24] M. Aleenejad, H. Iman-Eini, and S. Farhangi, "Modified space vector modulation for fault-tolerant operation of multilevel cascaded h-bridge inverters," *Power Electronics, IET*, vol. 6, no. 4, pp. 742–751, 2013.

[25] S. M. A. Cruz, A. M. S. Mendes, and A. J. M. Cardoso, "A New Fault Diagnosis Method and a Fault-Tolerant Switching Strategy for Matrix Converters Operating With Optimum Alesina-Venturini Modulation," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 269–280, 2012.

[26] K. Nguyen-Duy, T.-H. Liu, D.-F. Chen, and J. Hung, "Improvement of Matrix Converter Drive Reliability by Online Fault Detection and a Fault-Tolerant Switching Strategy," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 244–256, 2012.

[27] E. Ibarra, J. Andreu, I. Kortabarria, E. Ormaetxea, and E. Robles, "A fault tolerant space vector modulation strategy for matrix converters," in *35th Annual Conference of IEEE Industrial Electronics, 2009. IECON '09.* IEEE, 2009, pp. 4463–4468.

[28] R. Spee and A. Wallace, "Remedial strategies for brushless dc drive failures," *IEEE Trans. Ind. App.*, vol. 26, no. 2, pp. 259–266, 1990.

[29] S. Bolognani, M. Zordan, and M. Zigliotto, "Experimental fault-tolerant control of a pmsm drive," *IEEE Trans. Ind. App.*, vol. 47, no. 5, pp. 1134–1141, 2000.

[30] R. de Araujo Ribeiro, C. Jacobina, E. R. C. Da Silva, and A. Lima, "Fault-tolerant voltage-fed pwm inverter ac motor drive systems," *IEEE Trans. Ind. Electron.*, vol. 51, no. 2, pp. 439–446, 2004.

[31] B. Welchko, T. Jahns, and T. Lipo, "Fault interrupting methods and topologies for interior pm machine drives," *Power Electronics Letters, IEEE*, vol. 2, no. 4, pp. 139–143, 2004.

[32] W. Wang, M. Cheng, B. Zhang, Y. Zhu, and S. Ding, "A fault-tolerant permanent-magnet traction module for subway applications," *IEEE Trans. Pow. Electron.*, vol. 29, no. 4, pp. 1646–1658, 2014.

[33] G. Brando, A. Dannier, and A. Del Pizzo, "Failure adapted techniques to improve service dependability in systems using fault-tolerant converters," in *IEEE International Symposium on Diagnostics for Electric Machines, Power Electronics and Drives, 2007. SDEMPED 2007.* IEEE, 2007, pp. 64–69.

[34] A. Gaeta, G. Scelba, and A. Consoli, "Modeling and control of three-phase pmsms under open-phase fault," *IEEE Trans. Ind. App.*, vol. 49, no. 1, pp. 74–83, 2013.

[35] A. Di Tommaso, S. Favuzza, F. Genduso, R. Miceli, and G. Ricco Galluzzo, "Development of diagnostic systems for the fault tolerant operation of Micro-Grids." in *2010 International Symposium on Power Electronics Electrical Drives Automation and Motion (SPEEDAM)*. IEEE, 2010, pp. 1645–1650.

[36] C. Cecati, F. Genduso, R. Miceli, and G. Ricco Galluzzo, "A suitable control technique for fault-tolerant converters in Distributed Generation," in *2011 IEEE International Symposium on Industrial Electronics (ISIE)*. IEEE, 2011, pp. 107–112.

[37] F. Genduso, R. Miceli, and G. Ricco Galluzzo, "Flexible power converters for the fault tolerant operation of Micro-Grids," in *2010 XIX International Conference on Electrical Machines (ICEM)*. IEEE, 2010, pp. 1–6.

[38] A. Di Tommaso, F. Genduso, R. Miceli, and G. Ricco Galluzzo, "Experimental validation of a general model for three phase inverters operating in healthy and faulty modes," in *2012 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM),*. IEEE, 2012, pp. 50–55.

[39] B.-G. Park, K.-J. Lee, R. young Kim, T.-S. Kim, J.-S. Ryu, and D.-S. Hyun, "Simple Fault Diagnosis Based on Operating Characteristic of Brushless Direct-Current Motor Drives," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1586–1593, 2011.

[40] A. Mendes and A. Cardoso, "Voltage source inverter fault diagnosis in variable speed ac drives, by the average current park's vector approach," in *International Conference IEMD '99 Electric Machines and Drives, 1999.*, May 1999, pp. 704–706.

[41] F. Zidani, D. Diallo, M. Benbouzid, and R. Nait-Said, "A fuzzy-based approach for the diagnosis of fault modes in a voltage-fed pwm inverter induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 586–593, Feb 2008.

[42] J. Estima, N. Freire, and A. Cardoso, "Recent advances in fault diagnosis by park's vector approach," in *2013 IEEE Workshop on Electrical Machines Design Control and Diagnosis (WEMDCD)*, March 2013, pp. 279–288.

[43] A. Di Tommaso, F. Genduso, R. Miceli, and G. Ricco Galluzzo, "A general mathematical model for the simulation of common faults in three-phase voltage source inverters," *International Journal of Automation and Power Engineering*, vol. 2, no. 1, pp. 1 –11, January 2013.

[44] M. Beltrao de Rossiter Correa, C. Jacobina, E. Cabral da Silva, and A. Lima, "A general pwm strategy for four-switch three-phase inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1618–1627, Nov 2006.

[45] F. Salmasi, T. Najafabadi, and P. Jabehdar-Maralani, "An Adaptive Flux Observer With Online Estimation of DC-Link Voltage and Rotor Resistance For VSI-Based Induction Motors," *IEEE Trans. Pow. Electron.*, vol. 25, no. 5, pp. 1310–1319, 2010.