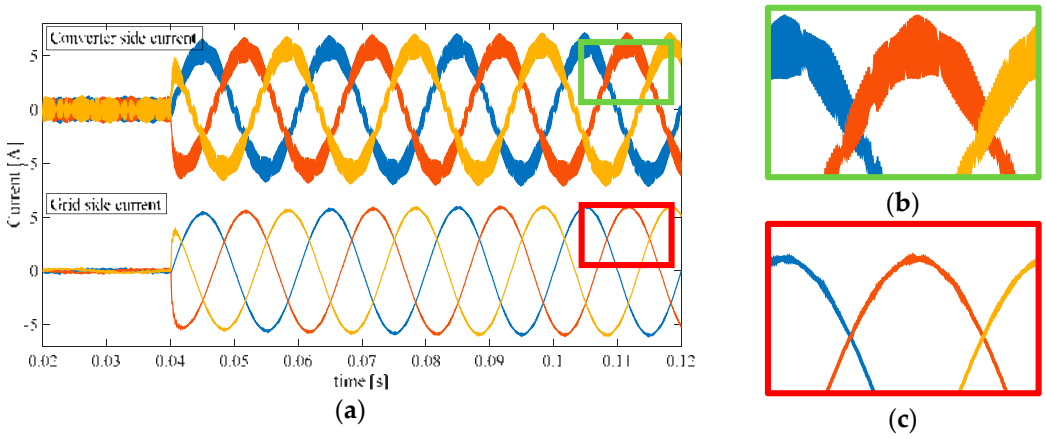


Figure 21. Converter side and grid side three-phase current with THIAPOD. (**a**) Transient behavior in multiple cycles; (**b**) Ripple magnification for converter side current; (**c**) Ripple magnification for grid side current.

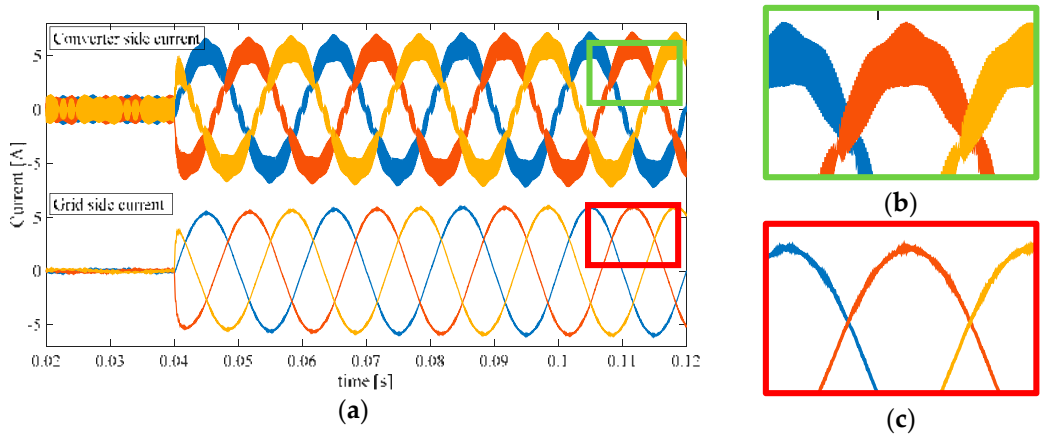


Figure 22. Converter side and grid side three-phase current with SFOAPOD. (**a**) Transient behavior in multiple cycles; (**b**) Ripple magnification for converter side current; (**c**) Ripple magnification for grid side current.

As before, the grid currents trend presents a THD% less then 5% according to IEEE 1574 and IEC 61727, but it is necessary to study the lower order harmonics and the ones around the switching frequency, in order to investigate in depth the performances. Figure 23 shows the low order harmonics (from third to fortieth harmonic) in grid side current I_{ga} obtained with SPOD, THIPOD, SFOPOD, SAPOD, THIAPOD, and SFOAPOD, respectively.

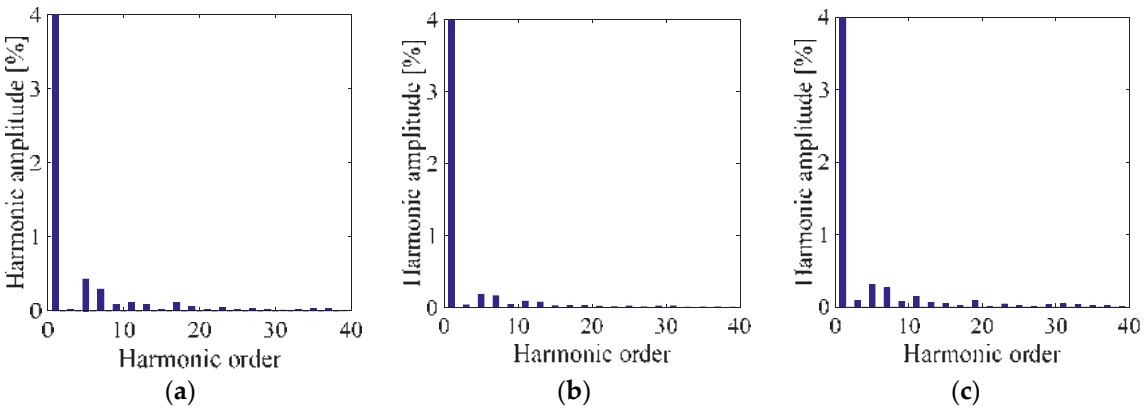


Figure 23. *Cont.*

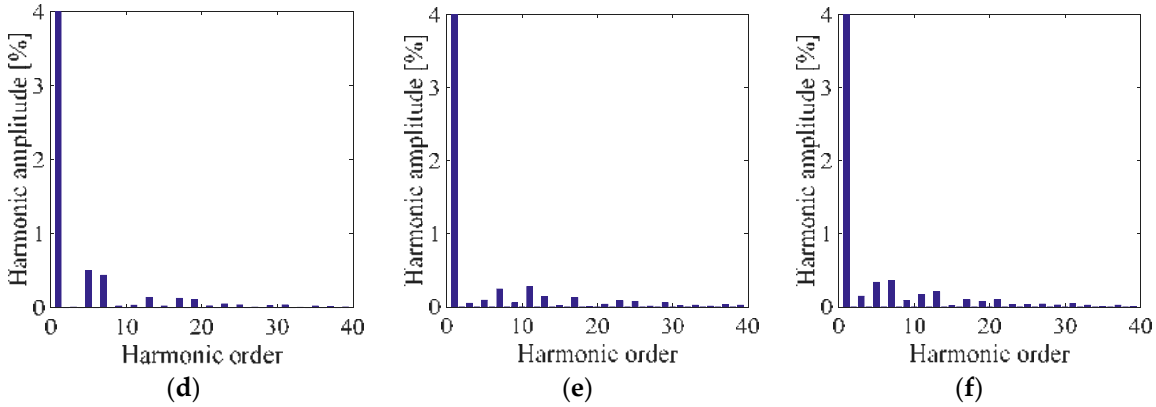


Figure 23. Low order harmonics on the grid side current *Iga* for (**a**) SPOD, (**b**) THIPOD, (**c**) SFOPD, (**d**) SAPOD, (**e**) THIAPOD, and (**f**) SFOAPOD.

It should be noted that the amplitude of the lower order harmonics are below of the standard harmonic current limits defined by IEEE 1574 and IEC 61727 at the PCC. Interesting results were obtained with THIPOD (Figure 23b) considering that are visible only fifth and seventh components with the lower amplitude compared to others modulation techniques POD and APOD based. Moreover, this is the best results also compared with modulation techniques PD based. This phenomenon is also explained by the higher values of the LCL filter parameters.

Figure 24 shows a comparison among harmonic spectra centered around the switching frequency of 10 kHz among line voltage V_{ab} (blue bars), converter side current I_a (red bars) and grid side current I_{ga} (yellow bars) obtained with SPOD, THIPOD, SFOPOD, SAPOD, THIAPOD, and SFOAPOD, respectively.

The lower values of the grid side current harmonics, less of 0.3% referred to the fundamental amplitude, demonstrate the LCL filter effectiveness. While, the predominant pair of the side band harmonic that appear in all harmonics spectra explains the higher values of the LCL filter parameters compared with modulation techniques PD or PS based. An interesting consideration is about the grid side current, the values are very lower respect to the modulation techniques PD based.

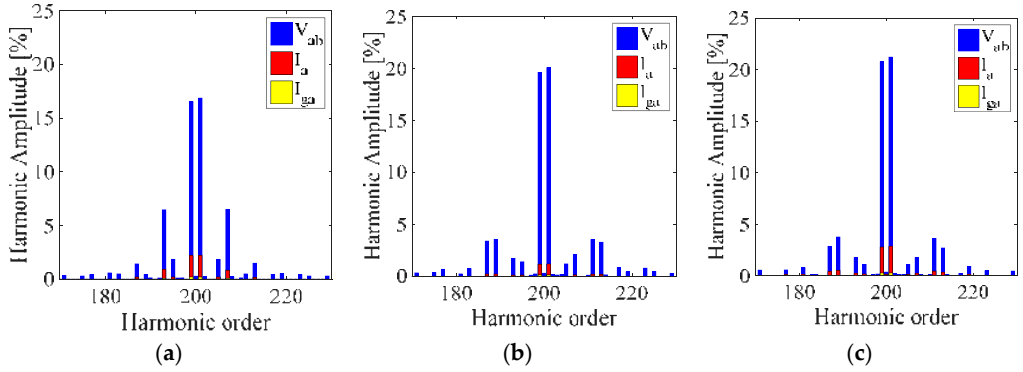


Figure 24. *Cont.*

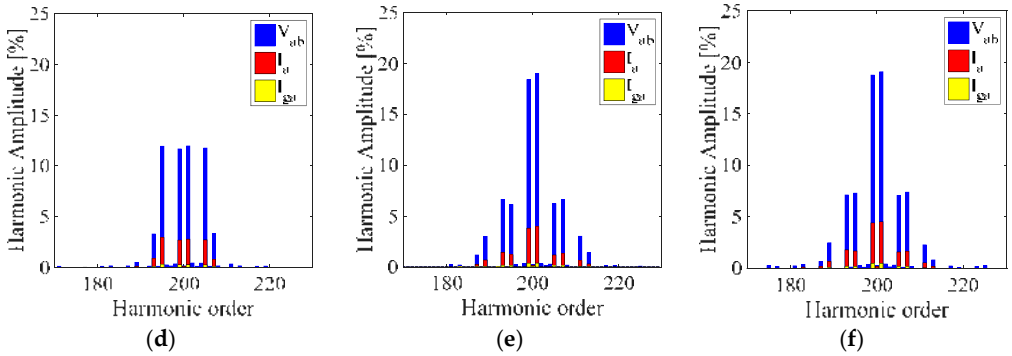


Figure 24. Comparison of line voltage harmonic spectra V_{ab}, converter side current I_a and grid side current I_{ga} centered around the switching frequency (10 kHz) in percent respect to the fundamental amplitude for (**a**) SPOD, (**b**) THIPOD, (**c**) SFOPOD, (**d**) SAPOD, (**e**) THIAPOD, and (**f**) SFOAPOD.

In Table 9 are reported the values of the PTHD% for line voltage V_{ab}, converter side current I_a and grid side current I_{ga}.

Table 9. *PTHD*% values obtained with SPOD, THIPOD, SFOPD, SAPOD, THIAPOD, and SFOAPOD.

	V_{ab}	I_a	I_{ga}
SPOD	25.62%	3.37%	0.33%
THIPOD	29.12%	1.72%	0.18%
SFOPOD	30.60%	4.12%	0.40%
SAPOD	24.17%	5.68%	0.53%
THIAPOD	29.78%	6.16%	0.61%
SFOAPOD	30.65%	7.21%	0.77%

As expected, the *PTHD*% relatively of the line voltages present higher values compared with modulation techniques PD based. While, the low values of *PTHD*% relatively of the currents are similar respect to the values calculated with modulation techniques PD based.

2.4.3. Phase Shifted Disposition

Last type of the carrier signals analyzed in this work is the Phase Shifted PS that allows shifting the harmonic to 2*nHB* times of the switching frequency. In the case of the five-level converter, *nHB* is equal to 2, so the harmonic content is shifting to four times the switching frequency (40 kHz). Moreover, the harmonics are centered around four times the switching and are present only side band harmonics like in modulation techniques POD and APOD based. Figure 25 shows the harmonic spectra, centered around four times of the switching frequency, obtained with SPS, THIPS, and SFOPS, respectively.

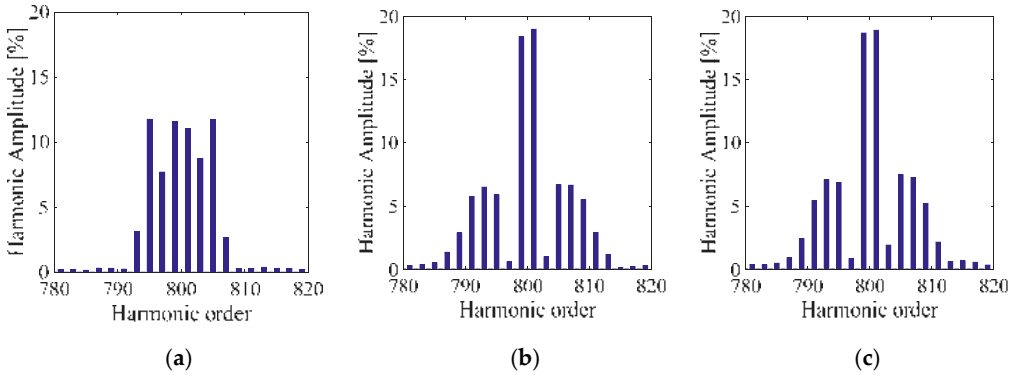


Figure 25. Phase voltage harmonic spectra centered around four times of the switching frequency (10 kHz) in percent respect to the fundamental amplitude of (**a**) SPS, (**b**) THIPS, and (**c**) SFOPS.

The harmonic spectra are similar respect to the harmonic spectra obtained with POD and APOD but the amplitude of the predominant harmonics are lower.

Figures 26–28 show the transitory of the converter side currents and grid side currents from zero to the rated current obtained with SPS, THIPS, and SFOPS, respectively.

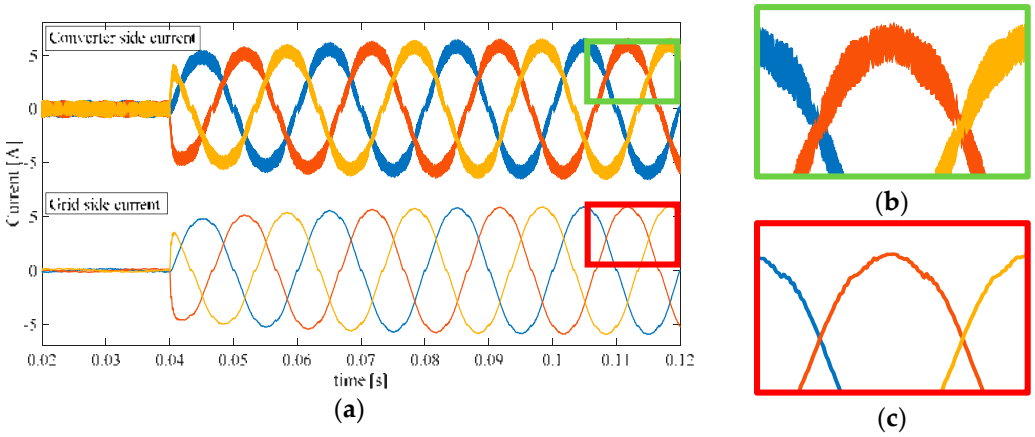


Figure 26. Converter side and grid side three-phase current with SPS. (**a**) Transient behavior in multiple cycles; (**b**) Ripple magnification for converter side current; (**c**) Ripple magnification for grid side current.

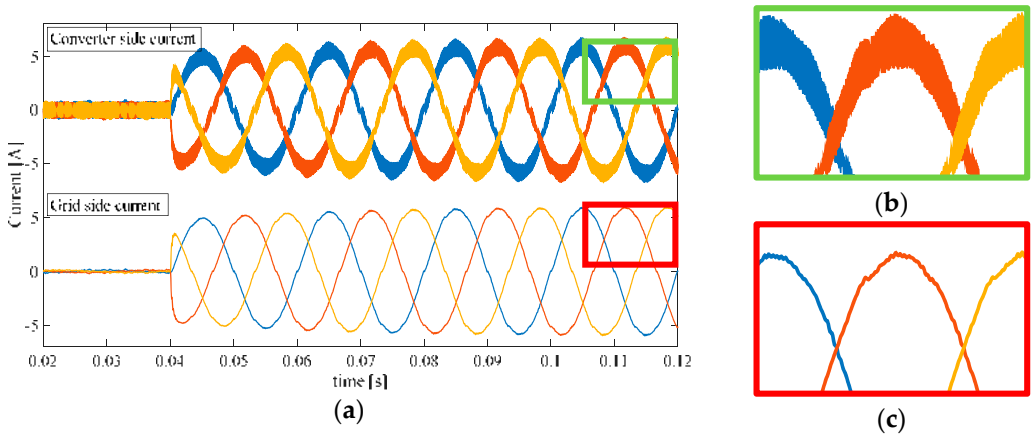


Figure 27. Converter side and grid side three-phase current with THIPS. (**a**) Transient behavior in multiple cycles; (**b**) Ripple magnification for converter side current; (**c**) Ripple magnification for grid side current.

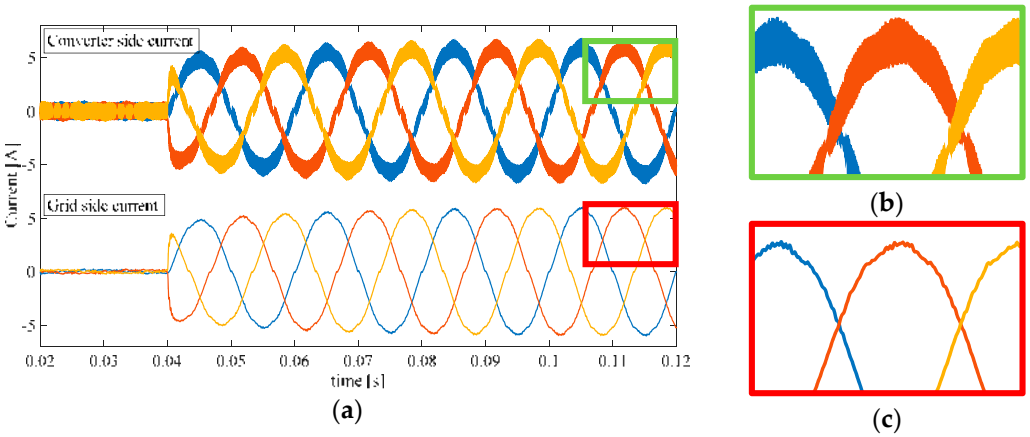


Figure 28. Converter side and grid side three-phase current with SFOPS. (**a**) Transient behavior in multiple cycles; (**b**) Ripple magnification for converter side current; (**c**) Ripple magnification for grid side current.

As previously noted, the grid currents trend presents a THD% less then 5% according to IEEE 1574 and IEC 61727 but observing the grid currents trend is evident the presence of low order harmonics.

Figure 29 shows the low order harmonics (from third to fortieth harmonic) in grid side current I_{ga} obtained with SPS, THIPS, and SFOPS, respectively.

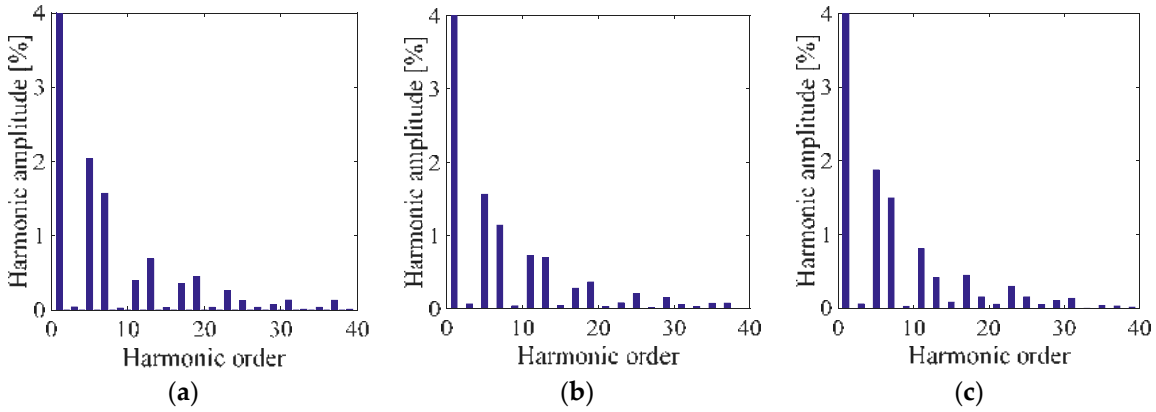


Figure 29. Low order harmonics on the grid side current I_{ga} for (**a**) SPS, (**b**) THIPS, and (**c**) SFOPS.

As presumed, by analyzing Figure 29, low order harmonics contents are present, in particular the fifth, seventh are predominant respect to the others, which anyway are under the harmonics current limits. Modulation techniques PS based have the higher values of the lower order harmonics compared with all modulation techniques previously described. Figure 30 shows a comparison among harmonic spectra centered around the switching frequency of 10 kHz among line voltage V_{ab} (blue bars), converter side current I_a (red bars) and grid side current I_{ga} (yellow bars) obtained with SPS, THIPS, and SFOPs, respectively.

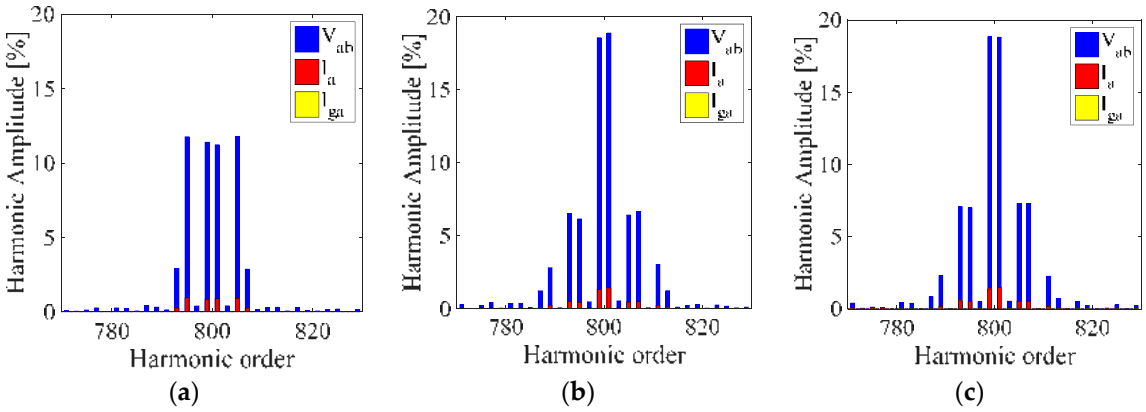


Figure 30. Comparison of line voltage harmonic spectra V_{ab}, converter side current I_a and grid side current I_{ga} centered around the switching frequency (10 kHz) in percent respect to the fundamental amplitude for (**a**) SPS, (**b**) THIPS, and (**c**) SFOPS.

Also for modulation techniques PS based, the grid side current harmonics are less than 0.3% referred to the fundamental amplitude demonstrating the LCL filter effectiveness. In terms of harmonic spectra of the line voltage, there are a pair of the predominant side band harmonics that are present also in the current spectra. In order to compare the performance were evaluated the *PTHD*% where the values are summarized in Table 10.

Table 10. *PTHD*% values obtained with SPS, THIPS, and SFOPS.

	V_{ab}	I_a	I_{ga}
SPS	23.51%	1.80%	0.0095%
THIPS	29.84%	2.16%	0.0117%
SFOPS	30.51%	2.35%	0.0124%

As shown in Table 10, the values of the *PTHD*% are lower compared with other values previously calculated. These are interesting results because on the grid side current are present only low order harmonics that are under the current limits (IEEE 1574 and IEC 61727).

In conclusion, modulation techniques PD based allow obtaining good results in terms of the harmonic content on the grid current with the lower values of the LCL filter parameters. In particular, SPD represent the best solution. Interesting results have been obtained also with modulation techniques PS based thanks to the feature that allows to shift the harmonic content respect to the switching frequency. In fact, have been obtained the lower values of the *PTHD*% about the grid side currents among all the modulation techniques taken into account. Moreover, modulation techniques PS based allow to control the power flow from the DC sources because each level can be controlled as a single-phase converter. This feature is important in very applications like PV systems for example. In the next section the experimental validation to confirm the simulation results were reported.

3. Experimental Validation

The purpose of this section is to provide all the useful information to describe the employed of a prototype CHBMI.

The first aim of the experimental validation is to validate the model of the system previously described and to confirm the effectiveness of the LCL filter design and the control strategy. In particular, the experimental tests have been executed with a prototype of a three-phase five-level multilevel converter with topology structure cascaded H-bridge inverter. Moreover, also the control board FPGA based is a prototype designed for power electronics applications. In this section were reported detailed descriptions of the test bench, control algorithm design and the experimental results. By the simulation

analysis, reported in section "2.4 Performances Evaluation", the experimental validation was focused on SPD and SPS modulation techniques.

3.1. Test Bench

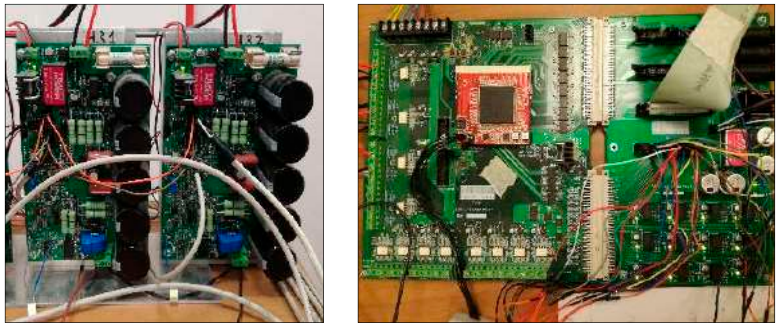
In order to carry out the experimental analysis, a three-phase, five-level multilevel inverter prototype with a CHB circuital structure were assembled.

The test bench is shown in Figure 31 and it is mainly composed by:

- a prototype of FPGA-based control board (produced by DigiPower s.r.l);
- Six prototypes of H-bridges (produced by DigiPower s.r.l);
- A Three-phase LCL filter especially designed (produced by SDESLAB and LEAP of the University of Palermo);
- Six DC sources with 24 V of rated voltage;
- Three-phase variac to grid interface;
- A Teledyne LeCroy WaveRunner 6Zi, scope, employed for the real-time acquisition of the waveforms and monitoring of the system.

Figure 31. A photograph of the test bench.

Figure 32a shows the prototype of the H-Bridge that is based on power Mosfet (International Rectifier—model IRFB4115PbF [57]) whose technical features are reported in Table 11. While, Figure 32b shows the FPGA-based control board where the FPGA is produced by Altera—model Cyclone III and the features reported in [58,59].



(**a**) (**b**)

Figure 32. A photograph of the prototype (**a**) H-Brides and (**b**) field programmable gate array (FPGA) control board.

Table 11. Technical features of the IRFB4115PBF device [57].

Voltage V_{dss}	150 V
Resistance $R_{ds(on)}$	9.3 mΩ
Current Id (silicon limited)	104 A
Turn on delay $t_{D(on)}$	18 ns
Rise time t_R	73 ns
Turn off delay $T_{D(off)}$	41 ns
Fall time t_F	39 ns
Reversal recovery t_{RR}	86 ns

Figure 33 shows the three-phase LCL filter especially designed and assembled with commercial components at SDESLAB and LEAP laboratories of the University of Palermo. For the converter and grid side inductance have been used commercial inductance of 560 μH with rated current of 4A in parallel connected to obtain an inductance then 280 μH with rated current of 8A.

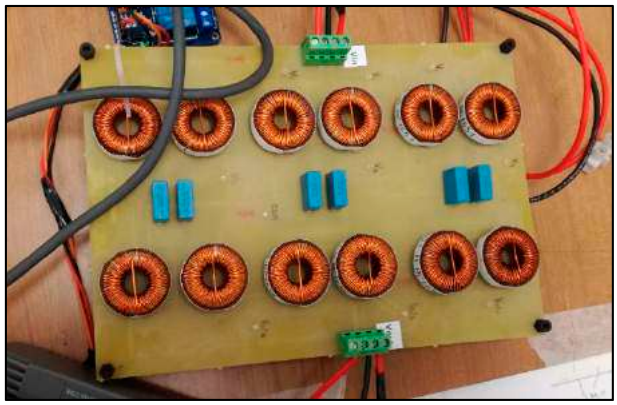


Figure 33. Tree-phase LCL filter.

While, for the capacitor filter have been used the ceramic capacitors of 4.7 μF with rated voltage of 100 V in parallel connected to obtain a capacitor of 9.4 μF.

3.2. Control Algorithm Design

The FPGA is commonly used in order to implement complex functions, such as arithmetic logic unit (ALU), memories, communication units and so on [16]. The main difference with other programmable systems used in industrial applications (μ-controller or DSP) is that through a software programming it is possible to describe an especially designed hardware for specific application. For this reason, the FPGA allows to obtain high flexibility and very fast execution time that allows using in very large of applications field. Actually, in power electronics application the complexity of the control algorithms, due also to the application type is increasing. For example, in grid connected applications there are very different control algorithm to control the power flow, power quality, synchronization with the grid, parallel control of the DC side and AC side and so on. Thus, are necessary programmable systems with fast execution time and the clock of the digital system should be adapted to the specific application. Aim of this section, is to investigate on the use of the FPGA for grid-connected application in order to validate the simulation analysis previously described and to optimize the control algorithm for the application under test. The control algorithm was implemented by means of an FPGA Altera Cyclone III EP3C40Q. The control software is Quartus II by Altera and the used programming language is the VHDL [60–62].

The structure of the control algorithm implemented can be explained by means the schematic block diagram shown in Figure 34.

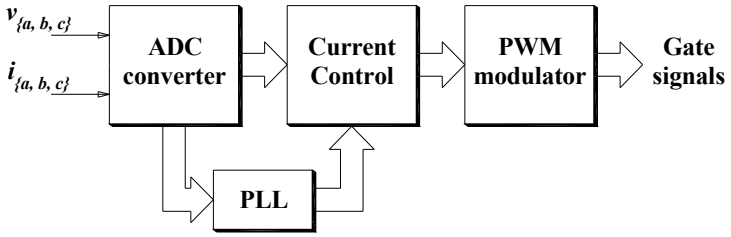


Figure 34. Schematic block diagram of the control algorithm.

The block named "ADC converter" represent the algorithm to manage the acquisition of the electrical quantities. In the prototype FPGA-Based control board is available an ADC converter with 16 channel (no simultaneously), 1 MSPS, 12 bit successive approximation ADC produced by Analog Devices model AD7490 16. The conversion process is managed by a clock signal reference with a frequency at 10MHz and conversion time (analog to digital signal) is equal to 2 µs. For the system under test, three voltage (v_a, v_b and v_c) and three current (i_a, i_b and i_c) are acquired; the conversion process is subdivided in two sub-conversion process relatively for the voltages and currents with a conversion time equal to 6 µs, respectively. In this way, the operation are executed in parallel, so when finished the first sub-conversion process relatively to the voltages, the mathematic elaborations for PLL with voltages samples start jointly with the second sub-conversion process relatively to the currents. After the conversion process, the mathematic elaboration with a resolution of 32 bit Floating Point (FP) single precision and a clock reference equal to 100 MHz starts. In Table 12 are summarized the execution time of the main mathematic operation.

Table 12. Execution time of the mathematic operation in FP 32bit.

Mathematic operation	Time
Conversion Integer to Floating (Integer 13 bit, FP 32bit)	60 ns
Sum or subtraction (FP 32 bit)	140 ns
Product (FP 32 bit)	110 ns

It should be noted that between two operations there is a delay time equal to 10 ns in order to stabilize and address the digital signals.

The equivalent schematic block diagram of the PLL to describe the implementation in VHDL is shown in Figure 35.

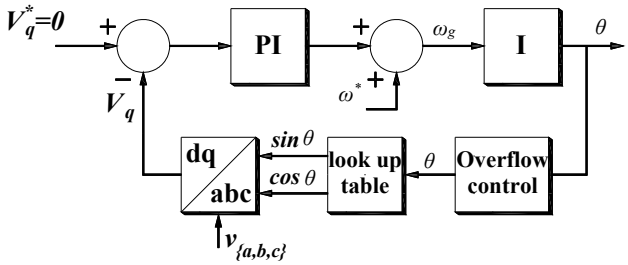


Figure 35. Equivalent schematic block diagram of the PLL. PI: proportional-integral; I: integral.

The PI regulator have been implemented in the discretion form as:

$$u(k) = k_p e(k) + \frac{k_p T}{T_i} e(k) + u_i(k-1) \tag{26}$$

where k indicate the k-sample, $u(k)$ is the output term of the PI regulator, $e(k)$ is the error, T is the sampling time, T_i is the time-integral and $u_i(k-1)$ is the $k-1$ integral output. In order to optimize the execution time to evaluate the $sin\theta$ and $cos\theta$, where θ is the instantaneous phase of the space

vector voltage, a look-up table was used. Each value of the instantaneous phase was used as an address (from 0 to 6280) to determinate the values of the $sin\theta$ and $cos\theta$. In the look-up table there are only a quarter of the sine waveform with a number of the sample equal to 1570 and it is possible to determinate the $sin\theta$ and $cos\theta$ values through a logic circuit. The block "Overflow Control" is necessary to limit the instantaneous phase value to 2π. In this way, the instantaneous phase of the space vector voltage θ assumes the sawtooth trend. In Table 13 are summarized the execution time of the main block of the PLL algorithm.

Table 13. Execution time main block of the PLL.

Operation	Time
ABC to DQ transformation (FP 32bit)	880 ns
PI regulator (FP 32 bit)	540 ns
Integral (FP 32 bit)	270 ns
Overflow control and look-up table (FP 32 bit)	450 ns

The total execution time algorithm from the end of the acquisition voltage to the instantaneous phase θ is equal to 3 µs. Figure 36 shows the experimental PLL effectiveness through a comparison of the grid voltage (red trend) and phase voltage of the converter (yellow trend) before carrying out the parallel with the grid.

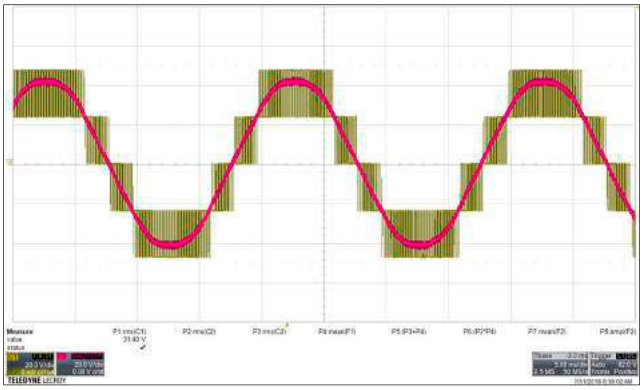


Figure 36. Experimental PLL effectiveness.

Figure 37 shows the execution time of the current control scheme where the total execution time is 3.13 µs.

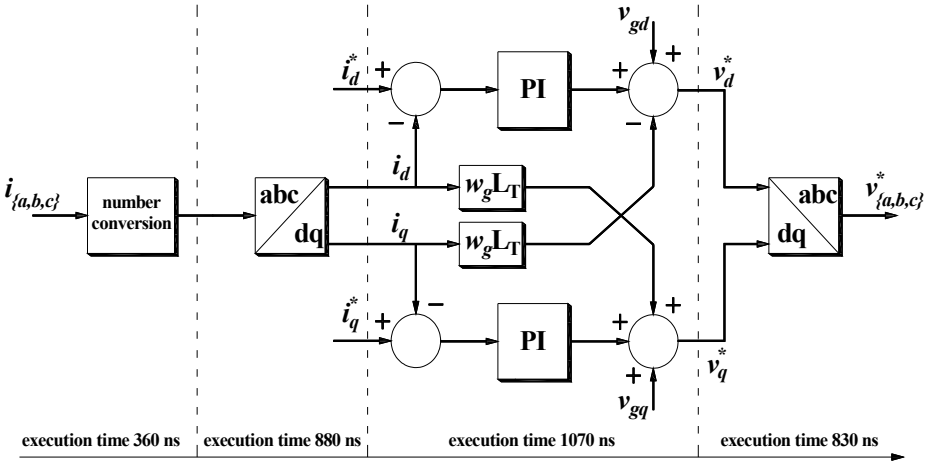


Figure 37. Execution time of the current control scheme.