Predictive Dead Time Controller for GaN Based Boost Converters

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ABSTRACT

A dynamic dead time controller is presented, specifically intended to operate in synchronous boost converters based on GaN FET switches. These transistors have a reduced stored charge with respect to silicon MOSFETs with similar breakdown voltage and series resistance, and can operate at higher frequencies with reduced switching losses. On the other hand, the voltage drop in reverse conduction is typically more than doubled with respect to silicon devices resulting in relevant power losses during the free-wheeling phases. Therefore dynamic control of dead time can be profitably applied even in converters operating in the tens of volts range. The device presented in this paper controls the switching delays taking into account both variations of the fall/rise times and of the turn-off/on delays, in order to keep dead time within a range of a few nanoseconds above its minimum value. A discrete-components prototype was designed, built in a synchronous boost converter and extensively tested at 1-2 MHz switching frequency, in a range of operating parameters corresponding to significant variations of the switching times (currents in the 1-6A range, output voltage up to 50V). The prototype demonstrated the capability to match dead time to actual operating conditions with a smooth and fast transient response.

1. INTRODUCTION

The efforts to increase power density of switching converters are stimulating a wide interest in GaN based FET devices, as they are expected to enable relevant increases of operational frequencies [1] or/and efficiencies [2], [3], [4] with respect to state-of-the-art silicon MOSFETs. In fact they provide large reductions of the switching times [5], due to peculiar GaN properties allowing to reduce die size, and consequently capacitance, with respect to silicon devices with similar breakdown voltage [6].

GaN transistors for low voltage applications, like the eGaN FET$^{(TM)}$ manufactured by EPC, can be grown on Silicon substrates. Their operation is quite similar to lateral MOSFETs, but reverse conduction in the OFF state relies on a low-conductivity channel [7], where voltage drop can largely exceed the typical forward voltage of body diodes. This effect can be particularly harmful in synchronous converters and in bridge legs where the switches go in reverse conduction at any switching cycle, during the excess dead time. Actually the analysis of the switching sequence reported in Sec. II distinguishes between the dead time, when no transistor is in direct conduction, and the excess dead time, when one of the transistors is biased in reverse conduction.

As both turn-off and turn-on processes are affected by current level, voltage, temperature and parametric variations, in ~~the~~ absence of dynamic control the delay between turn-off and turn-on commands has to be conservatively set to the maximum required in any operating conditions [8], resulting in a superfluous excess dead time in any other condition. This approach is not suitable for high-frequency GaN based converters, because the excess dead time may be a relevant part of the conduction period and the voltage pulses arising during reverse conduction may result in large power losses and EMIs. Basically such voltage peaks could be clamped by external Schottky diodes, but in this case the additional capacity and parasitic inductance of the related interconnections would easily impair the improvements in transient behaviour provided by GaN technology.

The effects of dead time have been investigated with reference to several applications. Specific techniques for its management have been proposed for full bridges [9], bridge legs [10], buck converters [11], shunt power filters [12], PWM amplifiers [13], [14].

In three-phase PWM inverter-fed induction motor systems the dead time tends to distort current waveforms and to cause torque ripples [15], [16]. This circumstance is especially relevant in case of high frequency ratio between PWM and the reference wave because the small distortions generated during each switching event tend to cumulate over a half period [17], [18]. The approaches proposed to mitigate the related effects were mostly intended to modify the reference signal either a priori [19] or on-the-line by detecting voltage zero crossing [20], [21]. Effectiveness and complexity of the proposed techniques have been evolving in parallel with performance of digital systems [11], [22-24].

In dc-dc converters different effects are observed. In buck converters during dead time the switching node voltage is driven negative by the voltage drop on a switch in reverse conduction. In low-voltage converters the negative peak can be a relevant fraction of the output voltage, and could even induce current reversal in case of Discontinuous Current Mode operation [25]. Differently, in boost converters during reverse conduction the switching node voltage tends to exceed the output voltage. The excess dead time may affect operation of the stage mainly via the duration of the phase of energy transfer to the load, which is linked to the maximum voltage gain. On the other hand, to our knowledge at present no results have been published on dynamic dead time control in boost converters: just in [26] a thorough theoretical analysis was presented, but the problem of dynamically adjusting dead time on the basis of variable operating conditions was not faced. Otherwise, several approaches were proposed for dynamic control of dead time duration in buck converters, aimed to keep it at the minimum value needed to avoid shoot-through in the specific operating conditions.

Adaptive control of dead time adjusts its duration by generating the turn-on command as soon as complete current quenching in the driven-off transistor is detected. Originally proposed in [27], it was incorporated in a commercial device in 1998 [28]. This approach, even in its most recent variants [29], [30] is not suitable for converters operating at switching frequencies larger than few tens of kHz, as the minimum dead time is clamped by the delay introduced by gate drivers and voltage comparators [31].

Predictive control [32] overcomes this limitation by setting the delay between gate commands on the basis of the dead time observed in the last switching event. Digital predictive techniques can provide either high accuracy or fast response in adjusting dead time duration. In fact, predictive unit-bit-delay adjustment techniques [33] increase the delay by small steps at each switching cycle. They achieve high resolution by relatively simple digital circuits, but are affected by poor transient response. Otherwise, one-step-delay predictive adjustment techniques [34] can update dead time in a single cycle: they are capable to track fast-changing loads, but are affected by rough digital delay quantisation.

The issue of delay quantisation in digital control of dead time and its trade-off with circuit complexity and power absorption has been faced in different ways. The baseline is a binary scheme where the delay is selected between two values on the basis of the operating conditions. Resolution is improved in [35] by a DSP-based system, where the delay is selected in a Look Up Table (LUT). Further improvements were achieved in [36] where the delay provided by a LUT was used as a first-guess to be successively refined. A remarkable amount of computational load was required for the optimisation algorithm in charge of estimating efficiency from voltage/current measurements and searching its maximum according to a kind of Perturb & Observe algorithm. Otherwise, the sensorless approach proposed in [33] finds the optimal dead time by searching for the maximum efficiency in buck converters on the basis of duty cycle

minimization. The main limitation of this approach is the assumption that the converter operates in stationary conditions, necessary to establish the link between duty cycle and efficiency.

Analog predictive techniques were reported by several authors. Some of them set the dead time on the basis of a predetermined relation between the turn-on delay and the current measured either on the load [37] or in a switch [38]. These approaches neglect the effects of voltage and temperature on the switching times and are affected by parametric variations. Better accuracy was achieved by controlling the time elapsing between the gate turn-off command and the zero crossing of the drain-source voltage on the driven-on transistor [25], [39], [40]. This approach is affected by variations of the turn-off delay so that the resulting accuracy of the controlled excess dead time hardly can be better than a few tens of nanoseconds.

On the other hand, efficient operation in the multi-MHz switching frequency range in the presence of wide load and/or voltage variations requires that dead time is controlled in the nanoseconds range, especially in boost converters. This could be achieved by the proposed device, allowing direct control of the duration of the excess dead time based on detection of the reverse bias of the power switches. This approach, together with predictive control, allowed us to achieve in the same controller both a precision in the nanoseconds range, comparable with that provided by the most precise competitors, and a dynamical response in the tens of microseconds range with reduced circuit complexity. Moreover, the proposed device is, to our knowledge, the first dynamical dead time controller experimentally tested in operation with boost converters.

The principles of operation are introduced in Sec. II. A prototype was specifically designed for GaN-based boost converters, demonstrating correct operation and a quite fast and smooth transient response. An analysis of the experimental results is reported in Sec. III.

2. THE PROPOSED SYSTEM

The proposed dead time controller is intended to be embedded in the control loop of a synchronous boost converter, according to the schematic outlined in Fig. 1. It receives the complementary signals U_{G1} and U_{G2}, setting the duty cycle of the synchronous transistors M_1 and M_2, respectively, from an independent duty cycle generator fitted to implement the desired control law for the converter. Correspondingly, the dead time controller generates the pair of non-overlapping gate commands V_{G1} and V_{G2} to be applied to M_1 and M_2.

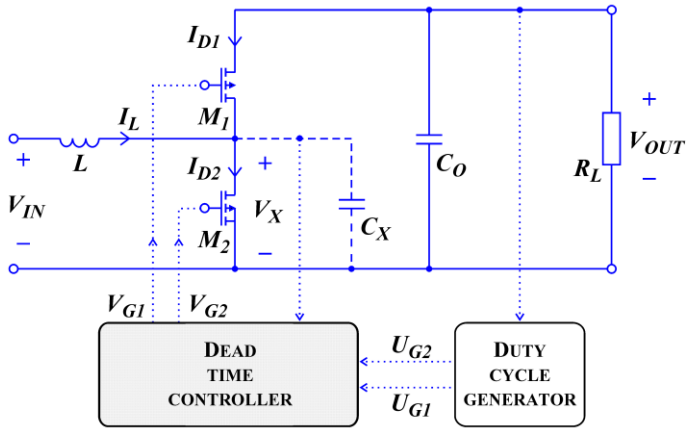


Figure 1.

Outline of the system.

Specifically, as illustrated in Fig. 2, the controller modulates the delay t_d between the turn-off and turn-on gate commands so that a finite dead time τ with no transistor in direct conduction is provided in the switching sequence, regardless of variations of turn-on (t_{ON}) and turn-off (t_{OFF}) times:

$$\tau = t_d + t_{ON} - t_{OFF} \tag{1}$$

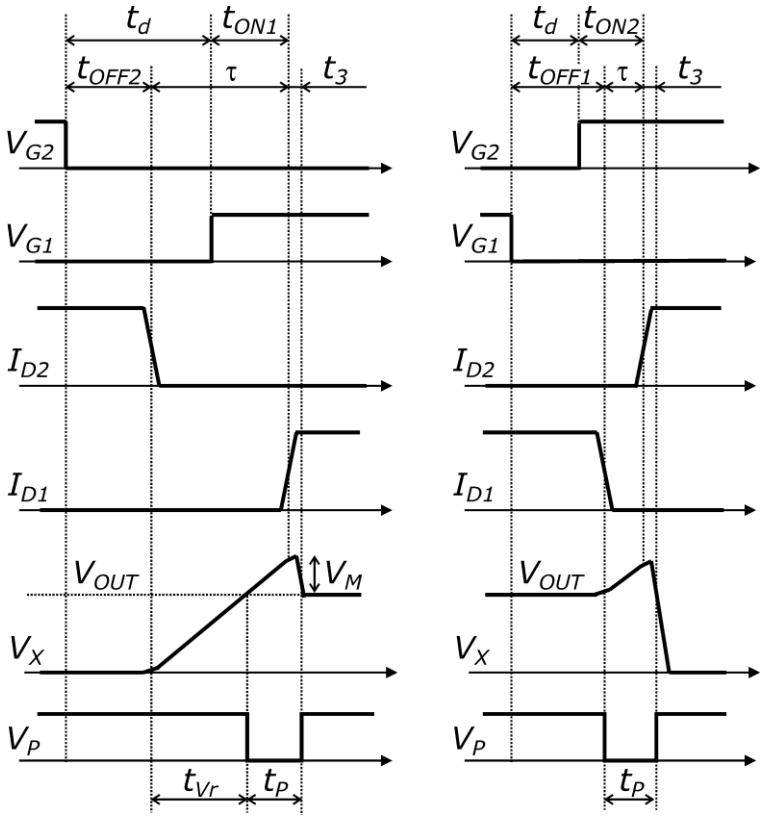


Figure 2.

Timing diagrams and definitions for dead time generation. I_{D1}, I_{D2} are the currents in M_1 and M_2, respectively. V_P is the output of the pulse detector, as detailed in Fig. 3.

Fig. 2 outlines the waveforms related to both transitions in boost converters. The dead time starts when current actually quenches in the commanded-OFF switch. From then on, the inductor current I_L charges the switching-node capacitance C_X until its voltage V_X exceeds the output voltage V_{OUT}.

When τ is long enough, M_1 goes in reverse conduction, and V_X saturates at a level dependent on the operating conditions and on the transistor in use: in case of GaN FET switches the voltage peak $V_M = V_{X(MAX)} - V_{OUT}$ can reach several volts.

Otherwise, if the synchronous switch is turned on before reverse conduction starts in M_1, V_X exceeds V_{OUT} for just a short time t_p. In this case the peak amplitude V_M can be expressed as:

$$V_M \approx \frac{(t_p - t_3)(I_L \pm \Delta I_L/2)}{C_x} \approx \frac{t_p\,(I_L \pm \Delta I_L/2)}{C_x} \tag{2}$$

where ΔI_L is the ripple current in I_L. The overvoltage duration t_p can be expressed as:

$$\begin{aligned} t_p &= \tau - t_{Vr} + t_3 \\ &= t_d + t_{ON} - t_{OFF} - C_X\,\Delta V / I_L + t_3 \end{aligned} \tag{3}$$

where t_{Vr} is the time needed for voltage to reach V_{OUT} and ΔV is either V_{OUT} in the transient following M_2 switch-off or zero after M_1 switch-off. The drop time t_3 , as defined in Fig. 2, is typically short and barely affected by the operating conditions.

According to (1) and (3), any variation of t_d directly reflects in a similar variation of τ and t_p, so that for the sake of small-signal analysis it is possible to assume:

$$\frac{d\tau}{dt_d} = \frac{dt_p}{dt_d} = 1 \tag{4}$$

The control action of the proposed system consists in modulating t_d to compensate for the variations of t_p with the operating conditions.

The dead time controller can be split in two stages: a dead time sensor, providing a precise measurement of the overvoltage duration t_p , and an adjustable delay generator, intended to accordingly modulate the delay t_d to be applied during the next switching cycle.

In order to make operation of the dead time controller independent of the output voltage, the circuit is fed by a power supply floating below the output positive line and is interfaced to the converter controller and to the transistor gate drivers by means of suitable optocouplers.

2.1. DEAD TIME SENSOR

A schematic of the Dead Time Sensor is reported in Fig. 3.

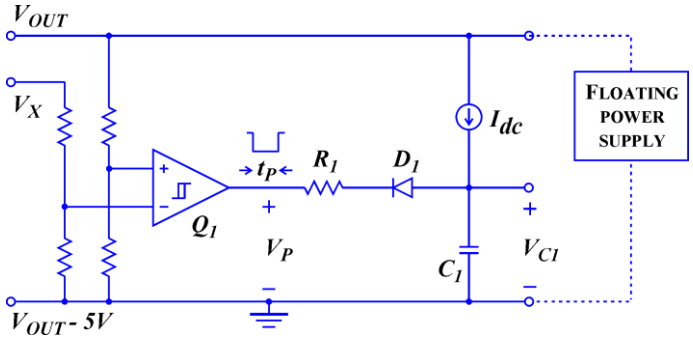


Figure 3.

Schematic of the Dead Time Sensor.

The input stage is a high speed comparator Q_1 set for emitting a negative voltage pulse on V_P in response to the voltage peak developed on V_X. Correspondingly, a charge proportional to the pulse duration t_p is removed from the capacitor C_1 via R_1 and D_1. The charge Q_{C1} on C_1 is then restored by a constant current I_{DC}, providing a reference charge $Q_{RIF} = I_{DC}$ T_{SW} during every switching period T_{SW}. As a result, at the beginning of the $k+1$ switching period the stored charge on C_1 is:

$$Q_{C1(k+1)} = Q_{C1}(0) + k\,Q_{RIF} - \sum_{j=1}^{k} \int_0^{t_{pj}} \frac{\left(\frac{Q_{C1}(t)}{C_1} - V_{LOW} - V_\gamma \right)}{R_1} dt \tag{5}$$

where V_{LOW} is the negative output level of the comparator Q_1 and V_γ is the forward voltage of D_1.
In stationary conditions both Q_{C1} and t_{pj} have constant values: $Q_{C1(k+1)} = Q_{C1(k)} \equiv C_1 V_{C10}$ and $t_{pj} = t_{p0}$. They are linked by the balance of positive and negative charges:

$$V_{C10} \cong \left(R_1\, I_{dc}\, \frac{T_{SW}}{t_{p0}} + V_{LOW} + V_\gamma \right) \tag{6}$$

In proximity of a determined operating point t_{p0} the small-signal transfer characteristic can be linearised as:

$$V_{C1} \approx V_{C10} - \lambda_R\, t_p \tag{7}$$

where λ_R is dependent on the operating point t_{p0}:

$$\lambda_R = \frac{R_1\, I_{dc}\, T_{SW}}{t_{p0}^2} \tag{8}$$

Example 1

When f_{SW} = 1 MHz, I_{dc} = 2.8 μA and R_1 = 280 Ω, if a small-signal Schottky diode is used with V_γ = 0.2V, the stationary value of V_{C1} corresponding to t_p = 2.5ns is V_{C10} = 2V. In the same conditions the slope of the transfer characteristic is λ_R = 0.2 V/ns.

2.2. *ADJUSTABLE DELAY GENERATOR*

The Adjustable Delay Generator is outlined in Fig. 4: it is basically a delay cell propagating the pulses received from the duty cycle generator U_{G2} to the MOSFET gates with a delay t_d in the rising edge. Two optocouplers are needed in order to allow the ground of the dead time controller to float with the output voltage of the converter.

The time constant t_C for charging the capacitor C_2 is modulated on the basis of the input voltage V_{C1}:

$$t_C = C_2\left(R_3 + r_{ds3}\left(V_{C1}\right)\right) \tag{9}$$

where $r_{ds3}(V_{C1})$ is the series resistance of M_3. Specifically, the series resistance of M_3, polarised in triode, is controlled by the amplifier Q_2, having a gain ($-G_2$). An high output impedance is needed for this amplifier, in order to avoid appreciable discharging of the Gate-Source capacitance of M_3 during t_d. The transfer characteristic t_d Vs. V_{C1} can be linearised in proximity of the operating point to derive the gain $\lambda_F = \dfrac{d\,t_d}{d\,V_{C1}}$ as:

$$t_d \approx t_{d0} + \lambda_F V_{C1} \tag{10}$$

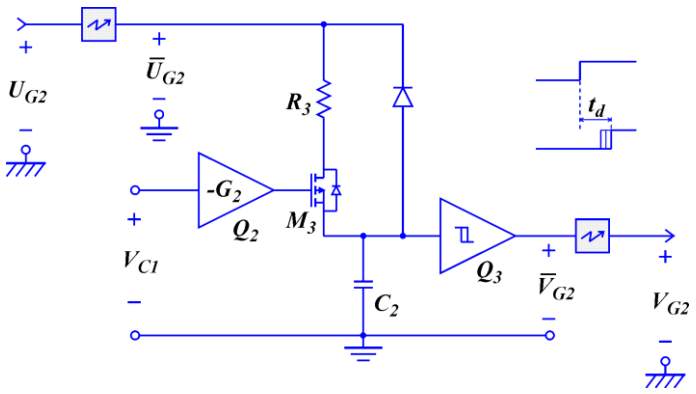


Figure 4.

Schematic of the Adjustable Delay Generator.

The small-signal analysis provides:

$$\lambda_F \equiv \frac{d\,t_d}{d\,V_{C1}} \cong \frac{d\,t_C}{d\,V_{C1}}\,\frac{V_{th}}{V_H} = C_2\,\frac{d\,r_{ds}}{d\,V_{gs}}\,\frac{d\,V_{gs}}{d\,V_{C1}}\,\frac{V_{th}}{V_H} = C_2\,\frac{d\,r_{ds}}{d\,V_{gs}}\,(-G_2)\,\frac{V_{th}}{V_H} \tag{11}$$

Where V_{th} is the switching threshold of the comparator Q_3 and V_H is the positive level of the $\overline{U}_{G2}$ signal. The derivative $\frac{d\,r_{ds}}{d\,V_{gs}}$ depends on the transistor in use and on its operating point.

Example 2

When V_{C1} is 2 V and G_2 = 6, the MOSFET M_3 is biased at a point where $d\,r_{ds} / d\,V_{gs}$ = 0.45 Ω/mV. In an adjustable delay generator with C_2 = 100 pF and V_H = 5V, setting the threshold of Q_3 to V_{th} = 3.7 V provides λ_F = 200 ns/V.

2.3. THE CONTROL SYSTEM

According to the predictive approach, a closed loop system adjusts t_d on the basis of the pulse duration t_p detected in the previous switching events. Fig. 5 outlines the relevant waveforms in response to a sudden variation of the switching times caused by a current increase. Such variation results in a sudden rise of the excess dead time, which is detected by the comparator Q_1 making t_p pass from t_{pA} to t_{pB}. The resulting longer discharge of C_1, amplified by Q_2, increases the gate bias on the transistor M_3. Thus, in the following switching events the charging rate of capacitor C_2 will be increased, bringing to a shorter delay t_d. The negative feedback action drives back the excess dead time towards its starting value in a few switching cycles, depending on the controller parameters.

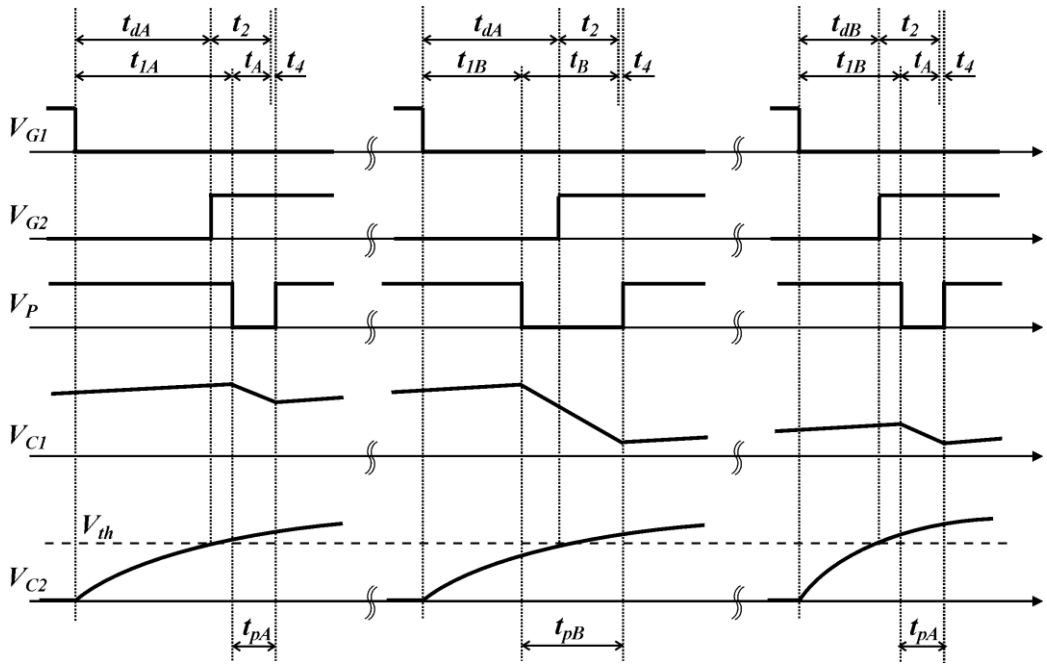


Figure 5.

Response to a variation of the switching times induced by a sudden load variation.

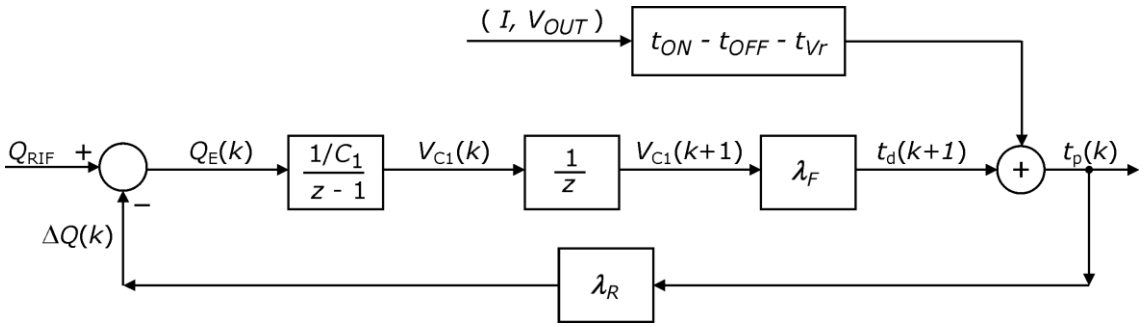


Figure 6.

The control loop.

The closed loop behaviour can be represented by the block diagram reported in Fig. 6.

Loop analysis was carried out on the basis of small-signal perturbation of nonlinear variables:

$$\begin{aligned} t_p &= t_{p0} + \hat{t}_p \\ t_d &= t_{d0} + \hat{t}_d \\ V_{C1} &= V_{C10} + \hat{V}_{C1} \end{aligned} \tag{12}$$

Thus, taking into account (4), (10), (11), the overall loop gain $T(z)$ can be derived as:

$$T(z) = \frac{\hat{t}_d(z)}{\hat{V}_{C1}(z)} \frac{\hat{V}_{C1}(z)}{\hat{t}_p(z)} \frac{\hat{t}_p(z)}{\hat{t}_d(z)} \frac{1}{z} = \frac{\lambda_F \lambda_R}{z} \tag{13}$$

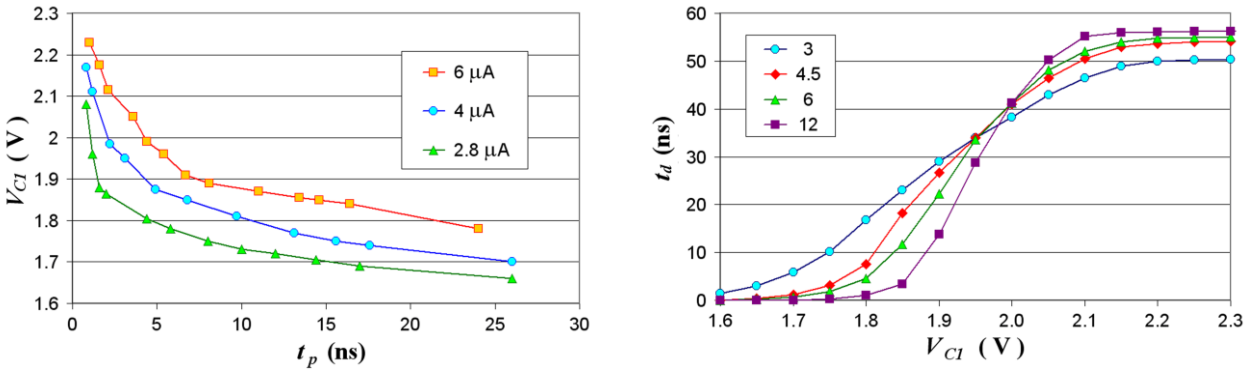
The system behaves as a simple PI controller, where integration is intrinsic in storing information about t_p along successive switching events. As $T(z)$ contains a single pole, it provides sufficient phase margin for smooth transient behaviour.

3. EXPERIMENTAL VERIFICATION

In order to demonstrate correct operation of the proposed dead time controller a prototype was built and tested. It was embedded in the control loop of a synchronous boost converter, with switching frequency in the MHz range, voltage gain 2× and output voltage up to V_{OUT} = 50V. The switches were EPC2001 eGaN FETs, with 100V drain-to-source breakdown voltage, 25A maximum continuous drain current and 8nC total gate charge. The gate drivers were LM5114 devices manufactured by Texas Instruments. The dead time controller was fed by a 5V power supply floating below the positive line of the converter output and had a power absorption lower than 150 mW. It was interfaced to the duty cycle control circuit and to the gate drivers by means of IL710 high-speed digital isolators. As a result of the predictive approach, sub-nanosecond response time was only required for the input comparator Q_1, and the ADCMP553 was

selected. The prototype also included HSMS2820 diodes, NX3020NAKT MOS transistors as amplifiers, and a LMV7219 as the output comparator Q_3.

Fig. 7(a) reports the experimental transfer characteristics of the Dead Time Sensor stage for different values of the parameter I_{DC} defined in Fig. 3. It is shown that the slope of the curves V_{C1} Vs. t_p tends to decrease at high t_p , with a trend loosely reproducing the theoretically predicted $1/t_p$ law. The deviation may be ascribed to some simplifying assumptions adopted to derive eq. (8). In fact a precise analysis would take into account the complete impedances of all components involved in the fast charge exchanges with C_1 . At the operating point $t_{p0} \approx$ 2ns, using I_{DC} = 2.8 µA and C_1.> 50 pF, the observed slope was $\frac{dV_{C1}}{dt_p} = \lambda_R \cong -0.2\, V/ns$. The value of I_{DC} was set by means of a current mirror configuration, capable to minimise its fluctuations with temperature and parametric variations to less than 5% in the worst case. On the basis of the experimental results reported in Fig. 7(a), such modifications entail an uncertainty lower than 2ns about the reference value of t_p .



(a) (b)

Figure 7.

Transfer characteristics of: (a) dead time sensor for different values of I_{DC} (b) adjustable delay generator as a function of the gain G_2.

Fig. 7(b) shows the transfer characteristics of the adjustable delay generator for different values of the gain G_2. It can be observed that, despite severe nonlinearities in operation of single subcircuits in the stage, the transfer characteristic t_d Vs. V_{C1} has a quite smooth trend.

When G_2 is increased attempting to improve precision of the control loop, the range of linear operation is reduced. Thus, the trade-off between precision and range of linear operation was heuristically investigated, obtaining a satisfactory performance for G_2= 6. This value provided a slope $\frac{dt_d}{dV_{C1}} = \lambda_F \cong 200\, ns/V$ at an operating point V_{C1}=1.95

V. Not shown in the figure, an additional delay offset has been introduced in order to align the high-gain region with the desired operating point.

Controller operation is analysed on the basis of the waveforms shown in Fig. 8, referred to the switching transition occurring after the M_2 turn OFF. The figure reports a mosaic of the typical waveforms of the switching node voltage V_X observed on a converter with a fixed delay set at 30 ns (Fig. 8(a) and 8(b)) and with a dynamically controlled dead time (Fig. 8(c)), for input currents ranging from I_L=1 A to I_L=5 A. The edge of the turn-off command $\overline{U}_{G2}$ is also reported for reference.

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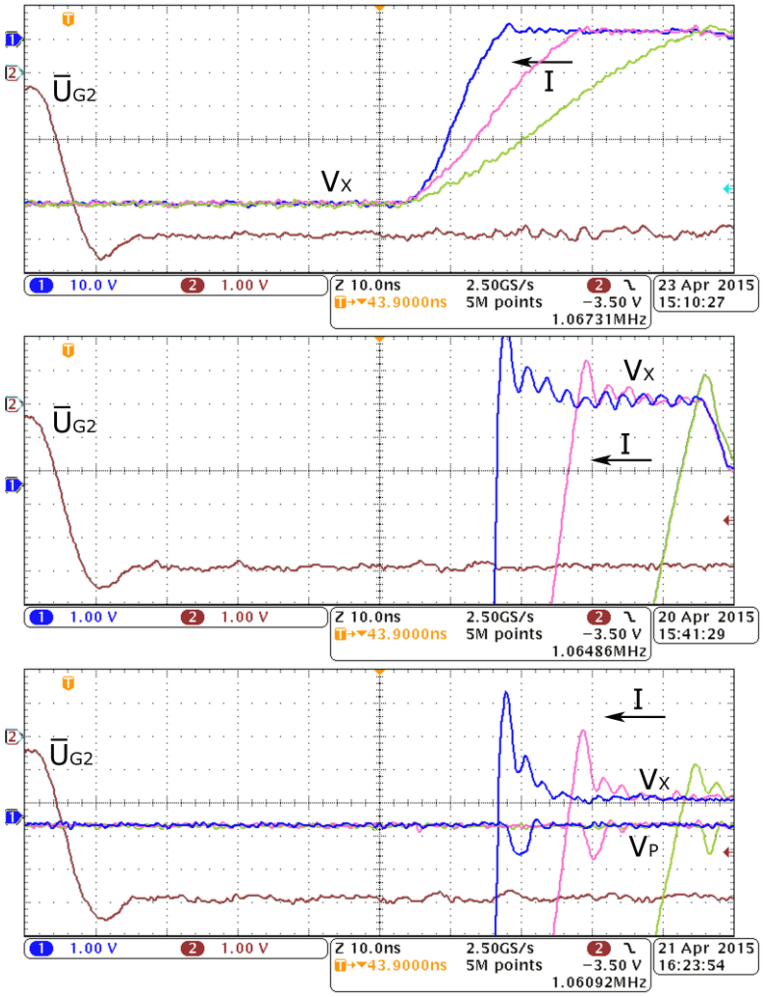

Figure 8.

Waveforms for input currents varying from 1 A to 5 A: (a) V_X with fixed turn-on delay t_d (10V/div); (b) the same as (a) with 1V/div vertical scale; (c) V_X and V_P with controlled t_d (1V/div). The reference voltage for the traces in (b) and (c) was the output voltage, V_{OUT} = 50V.

Fig. 8(a) illustrates the link among I_L and t_{OFF} via the slew rate of V_X in the presence of a fixed delay. In this condition the duration of the reverse conduction of M_1 can vary by several tens of nanoseconds, as better appreciated in an

expanded scale in Fig. 8(b). It is possible to observe that, after an inceptive voltage peak, V_X stabilises nearly 2V above V_{OUT} , due to reverse conduction of M_1 . Then, when M_1 itself starts to conduct direct current, V_X is short-circuited to the output node via the series resistance $R_{ds(ON)}$. It can be noted that both amplitude and duration of the inceptive voltage peak are dependent on I_L . Otherwise, when the dead time is controlled by the proposed device, M_1 never enters in reverse conduction (Fig. 8(c)). Actually V_X just undergoes a short voltage peak, with reduced amplitude and stable duration in the few nanoseconds range. Position of the peak is shifted with the load, according to the modulation of t_d applied in response to variations of the transistors switching times

Fig. 8(c) also reports the voltage pulses V_P emitted by the comparator Q_1, showing that the controller succeeded in keeping the peak duration nearly unvaried at t_p < 4ns.

A similar behaviour could be observed during the switching transition after the M_1 turn OFF [41]. The main difference, as outlined in Fig. 2, arises from the amplitude of the voltage to be swept during switch turn-off and the related variations of the delay times to be introduced.

The transient behaviour of the developed system is shown in Fig. 9, reporting the delay t_d and the pulse duration t_p along a load transient with I_L increasing from 1A to 5A in nearly 500µs. It can be observed that the system promptly reacts to the load variation, reducing t_d until a new stationary condition is reached. The observed t_p changed from 1.7ns to 3.2ns with a small overshoot, remaining always smaller than 5ns. The experimental tests reveal that, corresponding to the considered transient, the dead time variations follow the converter current with delays barely appreciable in the scale of hundreds of microseconds.

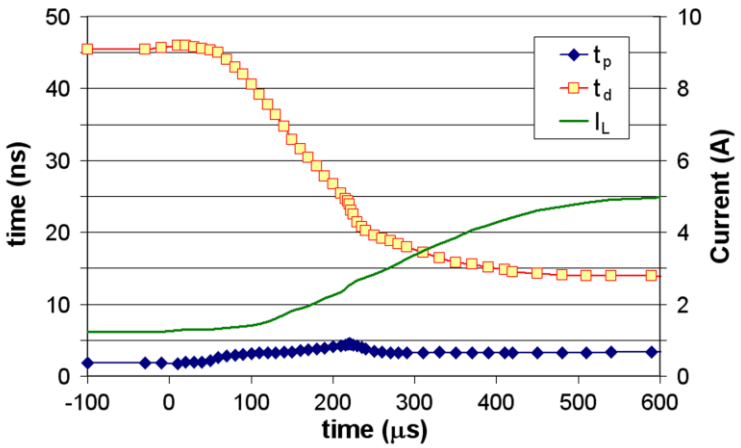

Figure 9.

Delay t_d and pulse duration t_p during a load transient forcing the inductor current I_L to rise from 1A to 5A in nearly 500µs.

A similar behaviour is observed when the variations of switching times are induced by voltage modifications.

The switching losses can be appreciably reduced by the proposed device, as demonstrated by Fig. 10, where the conversion efficiencies achieved with dynamically controlled and fixed dead time are reported in comparison. The data were obtained by a 10/20 V boost converter operating at 1-2 MHz switching frequencies. In the presence of the dynamic controller the conversion efficiency underwent a sharp improvement, increasing with load current and switching frequency: at 6A/2MHz the improvement exceeded 1%. The trend of the efficiency improvement with load current can be explained taking into account that when the dead time is fixed [3]: 1) the reduction of switching times with current causes a symmetrical increase of the excess dead time, with increased losses by reverse conduction of M_1; 2) the higher power dissipation causes a rise of junction temperature in transistors, still persisting when M_1 is in direct condution, and therefore results in a larger $R_{DS(on)}$. At increased frequency, switching times become a relevant part of the switching period, also increasing the beneficial effects of the dynamic dead time control.

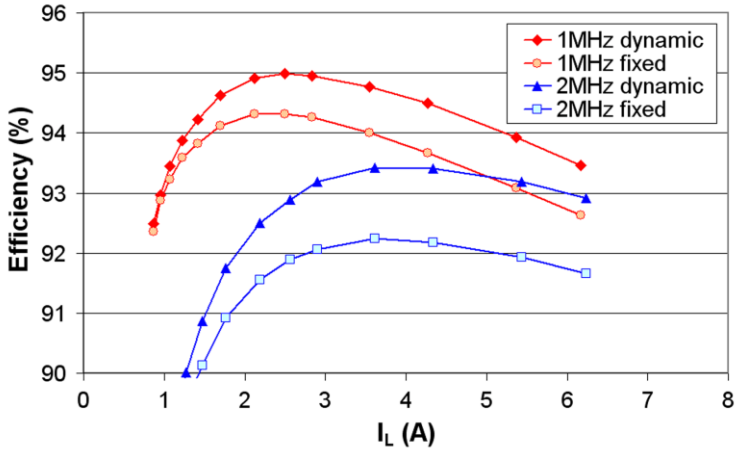

Figure 10.

Conversion efficiency Vs. load at different switching frequencies (V_{OUT}= 20V).

4. CONCLUSIONS

This work for the first time reports a dynamic dead time controller for GaN-based boost converters. It takes advantage of a predictive approach to stabilize excess dead time against both variations of the fall/rise times and of the turn-off/on delays. A discrete-components prototype was built and extensively tested at 1-2 MHz switching frequencies with various loads and voltages. The dynamic control succeeded to avoid both shoot-through and switch reverse conduction in the presence of significant variations of the switching times. It kept dead time within a range of a few nanoseconds above its minimum value, matching actual operating conditions with a smooth and fast transient response. Though specifically developed for GaN-based boost converters, the proposed controller could operate with minor modifications in any synchronous switching converter stage and other kind of switches.

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