

Modeling and simulation of a digital control design approach for power supply systems

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Abstract – Electronic designers need to model and simulate system features as close as possible to its effective behaviour. Moreover, today, electronics systems are often composed of mixed analog and digital components. The increasing complexity has led to the use of different simulation softwares, each one specific for a particular level of abstraction: mathematical, circuital, behavioural, etc. In order to simulate the entire system these softwares should work together: co-simulation is necessary for digitally controlled power electronics systems. In this paper, the modeling of a digitally controlled switching power supply system using MATLAB/Simulink, ALDEC Active-HDL and Powersys PSIM is presented. The power converter is modelled in PSIM, the digital control is described in VHDL by using Active-HDL, and the complete system is simulated in MATLAB/Simulink environment. This design approach presents all the advantages of each used software and all its features will be discussed. The comparison between simulation and experimental results of the digitally controlled step-down converter prototype are reported.

Index Terms – simulation, modeling, digital control, power supply, design approach, co-simulation.

I. INTRODUCTION

Power supply systems can be divided into two parts: power section with power converter, drivers and other electric devices, and analog or digitally implemented control section. The development of such systems needs powerful simulators specific for each level of abstraction. Recently, there has been a growing interest in digital control for power converters, due to its low power consumption, high immunity to noise and components aging, easiness of integration with other digital systems. Among the advantages of digital approach, design flexibility is the most valuable one. So, today, electronic industries and university researchers try to develop digital control for power conversion systems, using new micro-controller and digital signal processors (DSPs). The control algorithm is often described at a functional level using hardware description language, as VHDL or Verilog. ASICs or FPGAs standard-cells can be generated by VHDL code, using sophisticated simulation, synthesis and verification tools.

Behavioural simulations are commonly used to first validate electronics systems, to shorten the overall design process and to study parameter change effects on system working. Simulation allows to plot voltage and current waveforms and estimate dynamic and steady-state performances. Computer simulation results don't substitute experimental ones but are essential to speed design process and to shorten system time-to-market.

Electronic designers need to model and simulate system features as close as possible to its effective behaviour. Moreover, today, electronics systems are often composed of mixed analog and digital components. The increasing complexity has led to the use of different simulation softwares, each one specific for a particular level of abstraction: mathematical, circuital, behavioural, etc. Specific simulation tools are available on the market and each one of these is oriented to a specific abstraction level. In order to simulate the entire system these softwares should work together: co-simulation is necessary for digitally controlled power electronics systems [1-4].

Powersys PSIM is an electronic simulation software used to analyze and design power systems. Simulating the complete system using PSIM is necessary to work at circuital abstraction level, increasing design complexity and simulation total time. In the worst case, the simulation may not be able to proceed because of possible convergence error. On the other hand, the only use of MATLAB/Simulink often leads to increasing model complexity, even if powerful electronic toolboxes do exist, although Simulink libraries are less accurate than PSIM ones. The digital control implementation is easier if realized by a VHDL description, i.e by using ALDEC Active-HDL. VHDL source code can be easily implemented into ASIC or FPGA to test control logic design. Each software is optimized for a specific abstraction level. Both PSIM and Active-HDL have co-simulation toolboxes for Simulink.

This paper presents an innovative co-simulation design approach applied to a digitally controlled power system. The power converter is modeled in PSIM and the digital control is implemented in VHDL by Active-HDL. Thanks to PSIM and Active-HDL co-simulation toolboxes for Simulink, the complete system is simulated in MATLAB environment. The

goodness of this design approach will be shown in terms of simulation and experimental results matching.

II. ADVANCED CO-SIMULATION ENVIRONMENT

In this section, a brief description of the used softwares is reported.

Simulink is a MATLAB software package for multi-domain simulation and model-based design of dynamic systems. It enables the user to model, simulate and analyze the most significant signals. First of all the designer need to create a system model using Simulink editor, obtaining a block diagram model of the dynamic system described by a set of algebraic, differential and/or difference equations. After creating the model by using Simulink libraries components, the designer can run simulation, fixing a specified start and stop time. The interactive graphical environment and the customizable/specialized set of available libraries make Simulink a versatile and powerful instrument for researchers and engineers. Even if a SimPowerSystems library is available it is very difficult to create a simple model to simulate the effective system behaviour: the more detailed model, the more complicated equations and the higher model complexity. Obviously all system components, digital ones included, must be described by using mathematical equations and libraries blocks.

Powersys PSIM is an electronic simulation software used to analyze and design power systems, including switching power supplies, rectifiers, inverters, UPS systems, battery chargers, PFC, active filters, reactive power compensator and motor control systems, thanks to electrical engineering library.

In the basic package, PSIM consists of three programs:

1. PSIM Schematics, full-featured schematic-entry program;
2. PSIM Simulator, schematic simulation program;
3. SIMVIEW, advanced schematic simulated waveforms viewer program.

In addition, many add-on modules are provided, such as Digital Control Module for discrete and digital systems and SimCoupler Module for co-simulation with MATLAB/Simulink. In particular, the Digital Control Module is provided to analyze control systems in z-domain and it can be used to simulate the performances of digital control loops, study digital filters, and evaluate various effects in digital control, such as truncation errors, sampling/hold delay and computational delay. The producer recommend the use of this module to simulate digital control schemes with microprocessors or DSP implementation, and to perform digital signal processing. Unfortunately, it is not possible to describe a digital control loop by a VHDL or Verilog source code. The second add-on module, SimCoupler Module, is provided for PSIM and MATLAB/Simulink co-simulation [5]. In fact, this module allows the designer to use the SimCoupler block, implementing the PSIM circuit netlist, adding it in a specific Simulink library, making system co-simulation possible. So, a system part is implemented in PSIM while the entire system is simulated in MATLAB/Simulink. Circuit voltage and

current waveforms can be displayed by using both PSIM SIMVIEW and Simulink scope blocks.

The ALDEC Active-HDL is a totally integrated environment for digital IC design and verification, by which circuits can be described by C/C++ code or hardware description languages, as VHDL or Verilog. An intuitive graphical or efficient text-based design entry tools are available to implement system. The use of highly efficient, vendor independent and easy-to-use tools provides engineers and designers a powerful instrument to implement and test the designed digital systems. While defining a new workspace, a specific technology can be declared, fixing the vendor and the device type. By using a single Active-HDL simulation kernel mixed designs with libraries objects and hardware or SystemC source codes can be modeled. Signal history, data flow analysis, debug step-by-step source codes and view memory contents can be displayed, too. Indeed, the greatest advantage of Active-HDL is MATLAB/Simulink co-simulation: by using the Active-HDL Co-Sim block, a link between Active-HDL and Simulink is created, whenever simulation in Simulink starts. Simulink acts as top-level model simulator, Active-HDL acts as Simulink model VHDL blocks controller [6].

Both PSIM and Active-HDL have co-simulation toolbox for MATLAB/Simulink environment, so Simulink acts as an interface.

III. SIMULATION AND EXPERIMENTAL RESULTS

In order to test co-simulation procedure advantages, a single-phase step-down converter, whose block diagram is shown in Fig. 1, is modeled.

The entire system is divided into four parts, each one described using its “optimal” software. The DC/DC converter and the electronic load are modeled in PSIM, the digital control loop and the switching logic is implemented in VHDL and the analog-to-digital converters (ADCs), the digital-to-analog converter (DAC) and the PWM comparator are implemented in Simulink.

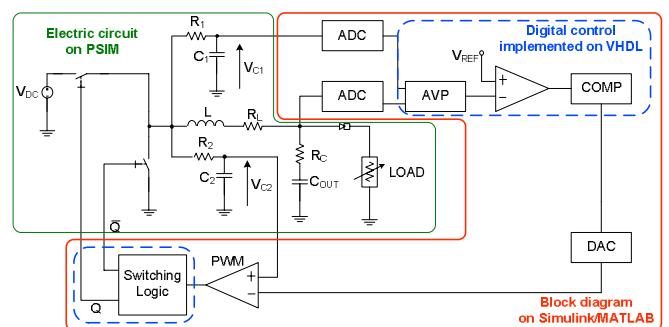


Fig. 1: Block diagram of the modeled step-down converter.

The PSIM section is shown in Fig. 2. Regulated voltage and the phase-node voltage are PSIM output and Simulink input signals and power MOS driver signals are Simulink outputs and PSIM inputs.

The Simulink section is shown in Fig. 3. SimCoupler and Active-HDL Co-Sim blocks are shown.

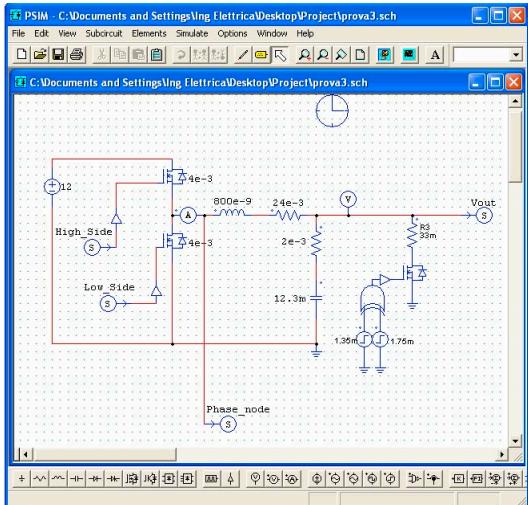


Fig. 2: PSIM section of the modeled system.

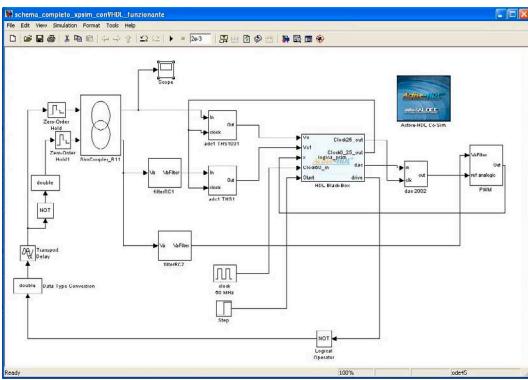


Fig. 3: MATLAB/Simulink section of the modeled system.

The digital control loop with its specific functions as soft-start, voltage and current protection, etc. is implemented by VHDL in Active-HDL section. In Fig. 4 an extract from VHDL source code is shown.

```

library IEEE;
use IEEE.STD.TEXT.all;
use IEEE.STD.TEXT.TEXT.all;
use IEEE.STD.TEXT.TEXT.all;
entity logic_intern is
    port(Vout : out std_logic_vector(10 downto 0);
        Vout_Latched : out std_logic_vector(10 downto 0);
        Clock50_in : in std_logic;
        Reset : in std_logic;
        Clock50_out : out std_logic;
        Vout_Error : out std_logic;
        decision : out std_logic_vector(11 downto 0);
        driver : out std_logic);
end entity logic_intern;

architecture Behavioral of logic_intern is
begin
    Vout := conv_std_logic_vector(0,11);
    Vout_Latched := conv_std_logic_vector(0,11);
    Clock50_out := '0';
    Vout_Error :='0';
    decision :='0';
    driver :='0';

    process(Clock50_in,Reset)
    begin
        if(Reset = '1') then
            Vout := conv_std_logic_vector(0,11);
            Vout_Latched := conv_std_logic_vector(0,11);
            Clock50_out := '0';
            Vout_Error := '0';
            decision := "000000000000";
            driver := '0';
        elsif rising_edge(Clock50_in) then
            if(Vout_Error = '1') then
                decision := "111111111111";
                driver := '1';
            else
                decision := "000000000000";
                driver := '0';
            end if;
            Vout := conv_std_logic_vector(decision,11);
            Vout_Latched := conv_std_logic_vector(decision,11);
            Clock50_out := '1';
        end if;
    end process;
end architecture Behavioral;

```

Fig. 4: Extract from VHDL code in ALDEC Active-HDL.

In Fig. 5, regulated output voltage and inductor current waveforms on PSIM SIMVIEW and, in Fig. 6, the output voltage on Simulink scope are reported under typical system working conditions (start up and load changes).

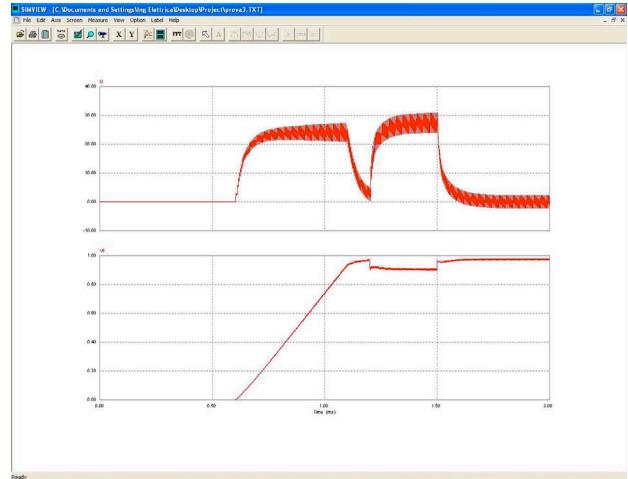


Fig. 5: V_{OUT} and I_L waveforms on PSIM SIMVIEW.

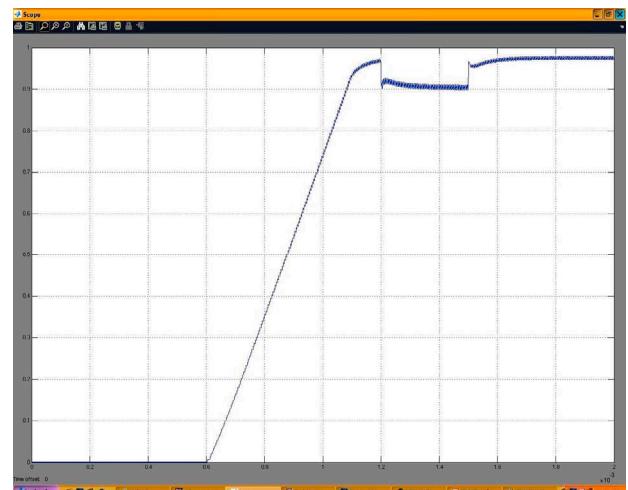


Fig. 6: Output voltage V_{OUT} on MATLAB/Simulink scope.

Performed tests underlined that co-simulation procedure does not influence the total simulation process time.

Fig. 7 shows the regulated output voltage and inductor current during system start-up.

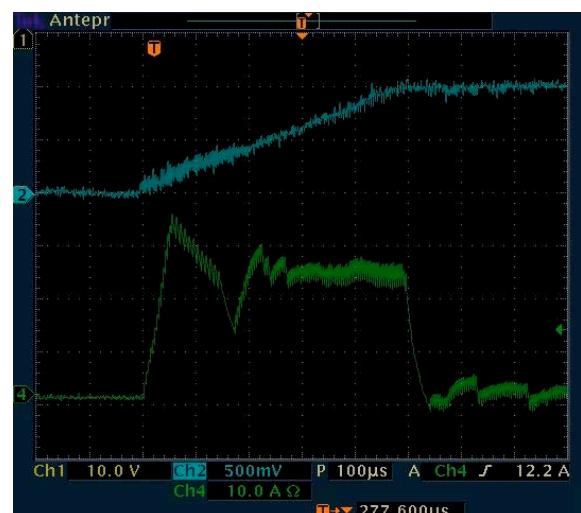


Fig. 7: V_{OUT} and I_L waveforms under soft-start.

Fig. 8 shows the regulated output voltage and inductor current under 20A load change. In spite of measured noise, co-simulation results match experimental ones.

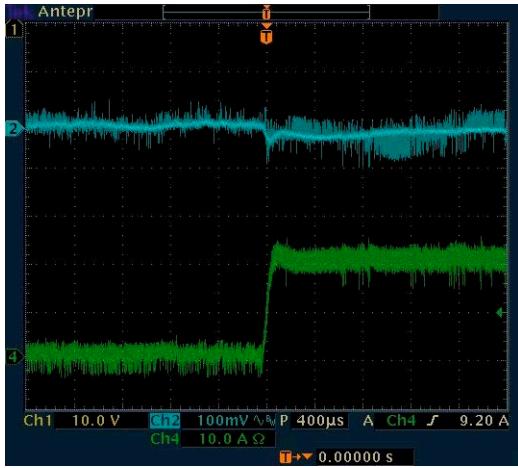


Fig. 8: V_{OUT} and I_L waveforms under 20A load change.

IV. CONCLUSION

In this paper, the modeling of a digitally controlled switching power supply system using MATLAB/Simulink, ALDEC Active-HDL and Powersys PSIM has been presented. The entire system was divided into three section: power, analog-to-digital and digital-to-analog interface, and digital control loop. In order to obtain a detailed model, as

close as possible to the effective behaviour, each section has been modeled by its “optimal” software, optimal in terms of the specific abstraction level. Modeling each section by its specific software results in more accurate and simpler model than using only one software. Active HDL and PSIM simulation softwares work together through Simulink that acts as co-simulation process supervisor. Simulation and experimental results has been shown.

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