UNIVERSITÀ DEGLI STUDI DI PALERMO

Dottorato di Ricerca in *Information and Communication Technologies*
Dipartimento di Energia, ingegneria dell'Informazione e modelli Matematici (DEIM)
Settore Scientifico Disciplinare ING-INF/01 - Elettronica

GRAPHENE-BASED TRANSISTORS AND DETECTORS: FABRICATION AND CHARACTERIZATION

IL DOTTORE

Antonio Benfante

Antonio Benfante

IL COORDINATORE

Prof.ssa Ilenia Tinnirello

IL TUTOR

Prof. Alessandro Busacca

I CO TUTOR

Prof. Enrico Calandra

Dr. Salvatore Stivala

CICLO XXX
ANNO CONSEGUIMENTO TITOLO 2018

UNIONE EUROPEA
Fondo Europeo di Sviluppo Regionale

Ministero dell'Istruzione, dell'Università e della Ricerca

Ministro per la Coesione Territoriale

Ministero dello Sviluppo Economico

Progetto: TECLA - "Ricercatori ed Esperti Di Alta Tecnologia e Innovazione Tecnologica Applicata al Settore dei Beni Culturali" a valere sull'Avviso n. 713/Ric. del 29 ottobre 2010
TITOLO III
"CREAZIONE DI NUOVI DISTRETTI E/O NUOVE AGGREGAZIONI PUBBLICO - PRIVATE"
Codice identificativo progetto: PON03PE_00214_1/F7

Contents

Introduction

Carbon and carbon-based systems have always attracted great attention thanks to the almost unlimited different structures they can be arranged in and the equally varied physical properties they own. These characteristics are mainly related to the flexibility of carbon bonding, which makes carbon an extremely versatile "building block" material. Most of the typical properties of each carbon-based system are mainly associated with the dimensionality of the structure itself. In this framework, graphene, the first two-dimensional atomic crystal available to the scientific community, has revealed to play a key role in terms of fundamental physics and potential applications, despite its short story. Its exceptional properties, like electrical and thermal conductivity, high carriers mobility and saturation velocity, mechanical strength and elasticity, wavelength-independent optical absorption coefficient and so on, suggest that graphene could replace, in the next years, more conventional materials in many fields, such as high-frequency electronics and photonics.

This thesis describes the author's work with graphene, developed throughout the PhD program. During this period, most of the research activity has been dedicated to the design, fabrication and characterization of microwave Graphene Field Effect Transistors (GFETs). In particular, three different fabrication runs have been carried out, investigating the role of different transistor layouts, of the substrate and of the dielectric material in the devices' performance. The above-mentioned transistors have been fabricated at the Institute of Nanotechnology (INT) of the Karlsruhe Institute of Technology (KIT), Germany. Extensive GFETs characterizations, including DC/microwave, optical and thermoelectric ones, instead, have all been performed at the Laboratorio di Elettronica delle Microonde (LEM) of the University of Palermo. Concerning this last aspect, great attention has been paid to the development of a reliable, automated, multifunctional microwave/optical measurement bench through the implementation of a complete set of HTBasic software modules.

Furthermore, graphene optical transparency and low resistivity have been exploited to develop a novel kind of X-ray detector based on polycrystalline grade diamond substrate and Reduced Graphene Oxide (RGO) contacts. Graphene electrodes

are, in fact, basically X-ray transparent, thus introducing an almost negligible perturbation of the incoming beam. These characteristics, together with the high resistivity, high mobility, radiation hardness and high thermal conductivity shown by diamond substrates, make the RGO/diamond detector a very promising solution for *in situ* beam monitoring. In addition, a novel Graphene Oxide (GO) rapid thermal reduction process has been developed, combining the advantages of all typical thermal reduction processes (like the absence of toxic agents and the parallel reduction of several GO-coated substrates) with an unequalled reduction speed and without compromising the film quality. Detector design and preliminary X-ray tests showing detection capability of these devices have been performed at the SLAC National Accelerator Laboratory, Menlo Park, CA (USA), while fabrication has been carried out at the Stanford Nanofabrication Facility (SNF) and at the Stanford Nano-Center (SNC), part of the Stanford Nano Shared Facilities.

Chapter 1
Theoretical background

Theoretically studied for over seventy years, graphene, a single layer of carbon atoms bounded into a two-dimensional honeycomb lattice, has been valued for most of the time as an "academic" material, useful to describe properties of more conventional carbon-based stuff. In fact, until 2004, 2D crystals were believed not to exist without their corresponding 3D base (i.e., in the free state), due to their theoretically thermodynamic instability [1]–[3]. Actually, conventional thin films show a melting temperature decreasing with the material thickness leading to films that become unstable at thicknesses of almost twelve atomic layers. These characteristics explain why atomic monolayers have been known so far usually only as films epitaxially grown on top of bulk monocrystals with matching lattices [1], [4], [5]. Nevertheless, starting from 2004 [6], graphene and other free-standing 2D-atomic crystals were finally experimentally obtained on top of non-crystalline substrates [7], as suspended membranes [8] and in liquid suspension [9]. This apparent disagreement with theory has been then clarified considering that the small size and strong interatomic bonds of the produced 2D crystals prevent thermal fluctuations to produce crystal defects even at elevated temperature; that is, 2D crystals can lie in a metastable state since they are extracted by a 3D structure by gently collapsing the third dimension [1], [8].

Since most of the peculiarities of single-layer graphene are related to its unusual electronic structure, an overview of graphene electronic properties is presented.

1.1 – Physics of graphene

As briefly already anticipated before, graphene is made out of carbon atoms arranged in a hexagonal structure, i.e., an honeycomb net (Fig. 1.1a). From the Molecular Orbital Theory point of view, σ and π carbon-carbon bonds contribute to the graphene lattice formation. Each carbon atom, in fact, bonds with three carbon atoms through in plane σ-

bonds formed between sp^2 hybridized orbitals while a highly delocalized π-orbital originates from the remaining p_z-orbitals locating perpendicularly to the sp^2-plane and allows its electron to move freely (Fig. 1.1b). Graphene honeycomb net can be thought as formed by two interpenetrating triangular lattices whose unit vectors can be written as $\boldsymbol{a_1} = \frac{a}{2}(3, \sqrt{3}), \boldsymbol{a_2} = \frac{a}{2}(3, -\sqrt{3})$, with $a \approx 1.42$ Å indicating the lattice constant, while the reciprocal-lattice vectors are $\boldsymbol{b_1} = \frac{2\pi}{3a}(1, \sqrt{3}), \boldsymbol{b_2} = \frac{2\pi}{3a}(1, -\sqrt{3})$.

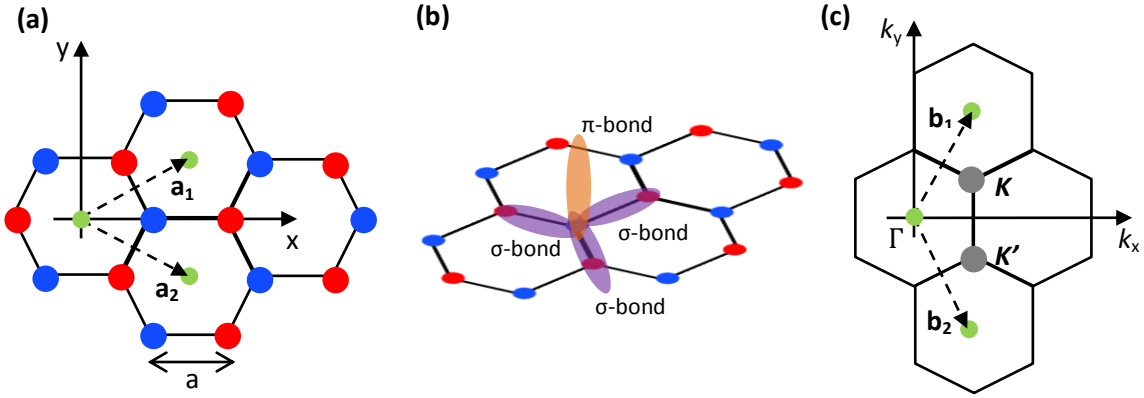


Fig. 1.1 – (a) Graphene hexagonal lattice showing its unit vectors ($\mathbf{a_1}$ and $\mathbf{a_2}$). (b) The C-C σ and π bonds distribution contributing to graphene lattice formation. In (c), the corresponding Brillouin zone is shown. ***K*** and ***K'*** refer to the Dirac points position while $\mathbf{b_1}$ and $\mathbf{b_2}$ are the reciprocal-lattice vectors (adapted from [10]).

The introduction of the reciprocal-lattice is of particular interest since it allows to define two points, ***K*** and ***K'***, located at the corners of graphene Brillouin zone (Fig. 1.1c): the Dirac points (or neutrality points), whose position in momentum space can be written as: $\boldsymbol{K} = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right), \boldsymbol{K}' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right)$ [10]. The choice of this name for the above-mentioned points is related to the need of employing Dirac equation to describe the electronic behavior in their vicinity, as it will be discussed more in detail later. The Dirac points play a key part in the electronic transport of graphene, quite similar to the role of Γ-points in direct band-gap semiconductors. Actually, all of the physics that will be discussed in this background chapter concerns the physics of graphene carriers close to the Dirac points. A tight-binding Hamiltonian can be used to describe electrons in graphene and then employed to derive the material energy bands distribution, which is given by (assuming to use units such that $\hbar = 1$) [11]:

$$E_{\pm}(\boldsymbol{k}) = \pm t\sqrt{3 + f(\boldsymbol{k})} - t' f(\boldsymbol{k}) \qquad (1.1)$$

where t (2.8 eV) is the nearest-neighbor hopping energy (i.e., between different sublattices), t' is the next nearest-neighbor hopping energy (i.e., in the same sublattices) and $f(\boldsymbol{k})$ has the form:

$$f(\boldsymbol{k}) = 2\cos\left(\sqrt{3}k_y a\right) + 4cos\left(\frac{\sqrt{3}}{2}k_y a\right)\cos\left(\frac{3}{2}k_x a\right) \qquad (1.2)$$

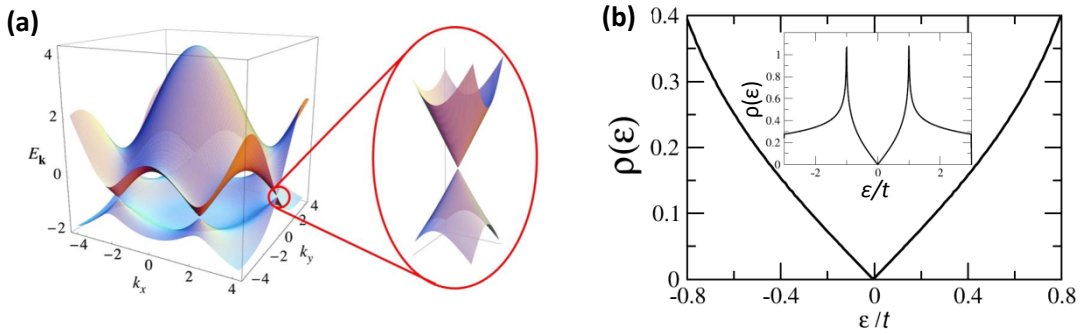


Fig. 1.2 – (a) Graphene energy spectrum and detail of the energy bands near the Dirac points [10]. (b) Density of states approaching the Dirac point and over the full electron bandwidth (inset) [12].

In particular, the plus sign in (1.1) refers to the upper band (π^*) and the minus sign to the lower band (π). The value of t' in (1.1), instead, has been found to lie in the range $0.02t \leq t' \leq 0.2t$, depending on the tight-binding parametrization [13] although the almost universally used graphene band dispersion at long wavelength assumes $t' = 0$ [12]. In Fig. 1.2a, the full band structure in units of t is reported.

As it can be noticed, valence band (formed by π states) and conduction band (formed by π^*states) touch at six points, which exactly coincide with the Dirac points. Due to band structure symmetry around the Dirac point, electrons and holes in defect-free graphene should have the same properties. This rather unique band structure is of course strictly related to graphene hexagonal honeycomb lattice. The energy dispersion close to one of the Dirac points, $\boldsymbol{K}$ (or $\boldsymbol{K'}$), can be analytically extracted from equation (1.1) by writing $\boldsymbol{k} = \boldsymbol{K} + \boldsymbol{q}$, with $|\boldsymbol{q}|<<|\boldsymbol{K}|$, thus obtaining [11]:

$$E_{\pm}(\boldsymbol{q}) \approx \pm v_F|\boldsymbol{q}| + O[(q/K)^2] \qquad (1.3)$$

where $\boldsymbol{q}$ is the momentum measured relatively to the Dirac points and $v_F = 3ta/2 \approx 10^6$ m/s, is the Fermi velocity [11]. A zoom of the energy bands close to $\boldsymbol{K}$ (or $\boldsymbol{K'}$) point in the Brillouin zone is also depicted in Fig. 1.2a. From (1.3), if we limit our considerations to low energies, which are the most relevant in graphene electron

transport, we can infer that the bands have a linear dispersion and their structure can be seen as two cones touching at the Dirac points with no energy gap. This causes graphene to be usually described as a zero-gap semiconductor with a linear rather than quadratic wavelength energy dispersion for both charge carriers. Moreover, as found in literature [10], the energy dispersion reported in (1.3) looks like the energy of ultrarelativistic particles which are normally described by the massless Dirac equation. In other words, graphene electrons interaction with the periodic potential of the honeycomb lattice causes these particles to behave as zero rest-mass, relativistic Dirac Fermions.

Graphene density of states per unit cell $\delta(\varepsilon)$ can also be extracted from the tight-binding Hamiltonian [11], [14]. Its trend as a function of energy, in units of t, is reported in Fig. 1.2b for $t' = 0$, showing a semimetallic behavior. A simplified analytical expression for the density of states per unit cell can be derived, assuming to be located close to the Dirac point and for $t' = 0$ [10]:

$$\delta(E) = \frac{2A_C}{\pi}\frac{|E|}{v_F^2} \qquad (1.4)$$

where A_c is the unit cell area. As it can be noticed, unlike the constant density of state of 2D systems which show parabolic dispersion, graphene density of state increases linearly with energy. The above-mentioned graphene peculiarities in terms of band-structure and density of states, of course, are strongly connected with the charge carriers transport characteristics, as it will be discussed in the following section.

1.2 – Charge transport in graphene

The control of materials electronic properties from outside, for example through a voltage signal, is the base of modern Electronics. Most of the time, exploiting the electric field effect allows the designer to tailor semiconductors carrier concentration thus changing the flow of electric current through them. In graphene, electric field effect has been widely proved and can be used to induce electrons and holes in concentrations up to 10^{13} cm^{-2} and with a room-temperature mobility of ~ 10^5 $cm^2/V{\cdot}s$ by simply applying a gate voltage [6]. A typical dependence of graphene sheet resistivity (ρ) on

gate voltage (V_G) is reported in Fig. 1.3a, for a simple graphene-based device in which graphene is deposited on top of a silicon dioxide layer and a voltage is applied between the metal pads and a back-gate located underneath [1], [6].

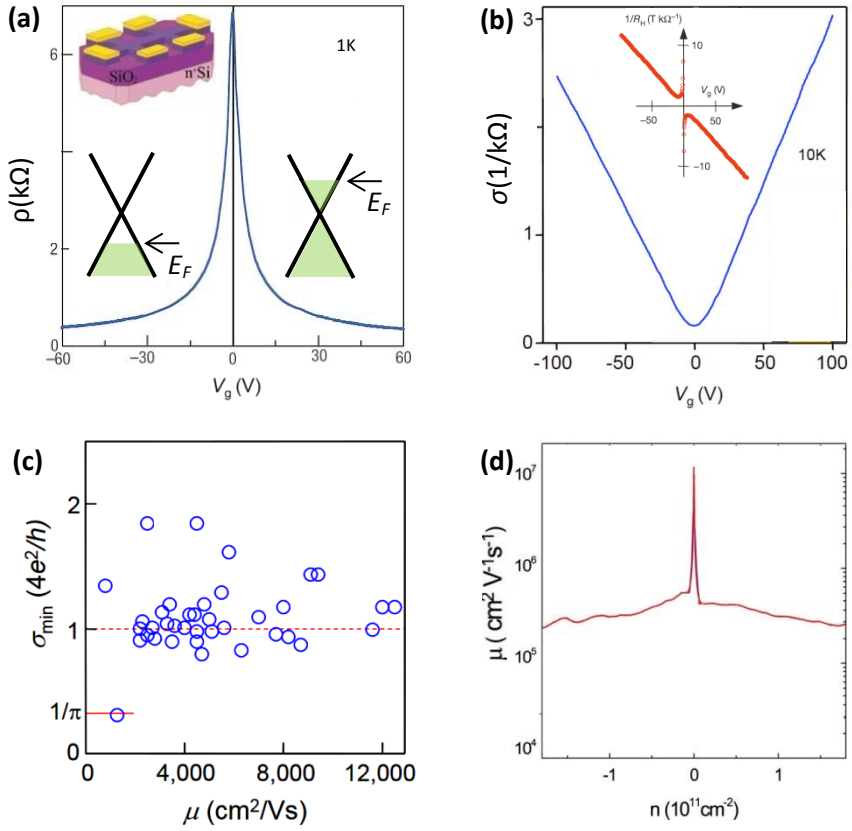


Fig. 1.3 – (a) Resistivity modulation as a function of the gate voltage showing the typical bipolar electric field effect of single-layer graphene. The corresponding variations in the position of the Fermi level are also reported (adapted from [1], [6]). (b) Associated change in graphene conductivity and in the Hall coefficient (inset), adapted from [15]. (c) Not null minimum of graphene conductivity at the neutrality point (adapted from [1]). (d) Graphene mobility vs. carrier density *n* depicting the typical mobility divergence due to the nominal zero carrier concentration shown by graphene at the Dirac point (adapted from [16]).

As it can be noticed, the curve shows a really pronounced peak at the Dirac point. Conductivity plot is also depicted in Fig. 1.3b, exhibiting a linear increase with V_G going away from the neutrality point. This behavior approximates the ambipolar field effect of conventional semiconductor materials although there is no zero conductance region, normally related to a Fermi level pinned inside the band-gap [6]. In the case of a few-layer graphene, these trends can be quantitatively explained by modelling graphene as a 2D metal with valence and conductance bands slightly overlapping [6]. In this structure, the gate voltage can be employed to induce a surface charge density $n =$

$\frac{\varepsilon_0 \varepsilon V_G}{te}$, where ε_0 and ε are the dielectric constant of free space and SiO_2, respectively, t is the thickness of SiO_2 and e is the electron charge. Assuming a voltage V_G = 100 V, this leads to a surface charge density $n \approx 10^{13}$ cm^{-2} for a 300 nm thick SiO_2 layer [6]. Of course, inducing a charge density causes the Fermi level to be moved thus changing graphene electronic transport properties. Focusing on the physics of ideal (i.e., single layer) graphene, doping through an electric field allows the designer to transform the material into either a complete electron (with Fermi level located inside the conduction band) or hole (with Fermi level located inside the valence band) conductor. In between, a condition of large resistivity is obtained for a particular value of voltage (the so called *Dirac voltage*, V_{Dirac}) in which a zero density of states causes no carriers to contribute to the electronic transport (Fig. 1.3a) [6]. It is to be pointed out that, in the case of neutral graphene, $V_{Dirac} = 0$, while in the case of doped graphene sheets, this value is shifted depending on the dopant level, as it will be discussed later. Similarly to graphene conductivity, the Hall coefficient R_H also shows a particular behavior when V_G approaches V_{Dirac} with its value changing sign (Fig. 1.3b, inset). This trend confirms that an electron regime is induced for $V_G > V_{Dirac}$, while holes concentration is predominant if $V_G < V_{Dirac}$. Going away from the *Dirac voltage*, the inverse of the Hall coefficient, $1/R_H = ne$ (being n electrons or holes concentration and e the electron charge), grows linearly with V_G thus yielding to $n = \alpha \cdot V_G$ for neutral graphene, with $\alpha \approx 7 \cdot 10^{10}$ cm^{-2}/V. Since the electrical conductivity depends on carrier concentration as:

$$\sigma(V_G) = n_{e,h}(V_G) e \mu_{e,h} \qquad (1.5)$$

we get the linear dependence of conductivity as a function of the gate voltage as already reported in Fig. 1.3b [15]. In the previous expression, $n_{e(h)}$ and $\mu_{e(h)}$ refer to electrons (holes) concentration and mobility, respectively. It is to be pointed out here another pretty unique property of graphene related to the trend shown by conductivity when approaching the neutrality point: contrary to what might be expected, graphene conductivity does not vanish regardless of the zero carrier density at the Dirac point, but its value reaches a minimum around $\sigma_{min} = 4e^2/h$ [1], as depicted in Fig. 1.3c. This peculiarity is related to the nature of graphene charge carriers which behave as relativistic Dirac Fermions for which a minimum quantum conductivity has been predicted [17]–[21], although slightly different from the $\sigma_{min} = 4e^2/h$ value around which

most of experimental data cluster. Sample dependent σ_{min} values will be justified in the next section, where graphene non-idealities and, among them, scattering sources will be introduced.

Given the symmetric energy dispersion (1.3) in ideal graphene, hole and electron mobilities are expected to be equal. This property distinguishes graphene from conventional semiconductors, for which the hole mobility is quite lower than the electron mobility with the ratio μ_h/μ_e reaching around 0.3 for Si, 0.05 for GaAs and approaching 0.01 for narrow bandgap compounds like InAs and InSb [22]. From electrical conductivity and carrier density data (normally obtained via Hall effect measurements), carrier mobilities can be obtained from the (1.5). More in detail, their value is calculated in the high carrier density regime, i.e. in those conditions that guarantee an almost constant resistivity value despite the induced charge. A typical mobility plot as a function of the carrier density is reported in Fig. 1.3d. We observe that mobility tends to diverge at $V_G = V_{Dirac}$ since $n = 0$ nominally at the Dirac point. Mobility values of 10000 – 15000 $cm^2V^{-1}s^{-1}$ can easily be obtained for exfoliated graphene on SiO_2-covered silicon wafers [6], [23] while values up to 10^6 $cm^2V^{-1}s^{-1}$ have been reached by suspending single layer graphene [24] (see Table 1.1 for additional data). This value is higher than those normally obtained employing more conventional semiconductor materials (Fig. 1.4a [22], [25]), suggesting graphene use in high-speed devices fabrication, as it will be seen in the next chapter.

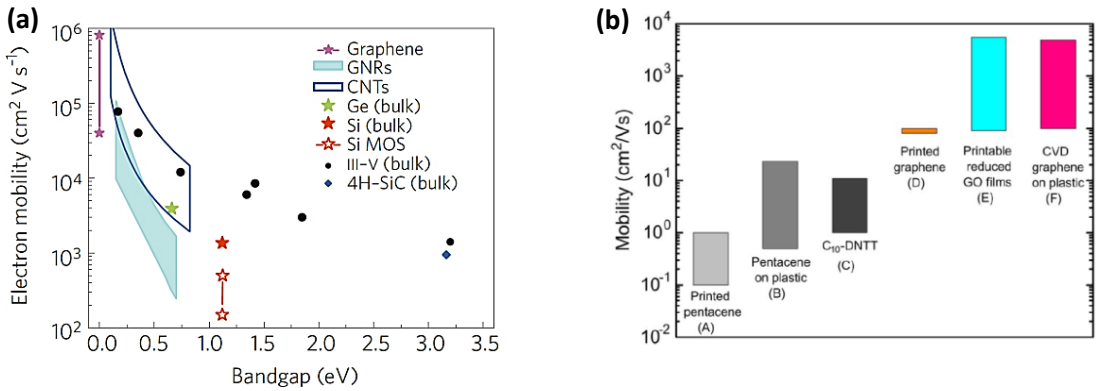


Fig. 1.4 – (a) Comparison of electron mobility vs. bandgap in low electric field regime between graphene and other conventional semiconductors [25]. (b) Electron mobility of printable and flexible graphene compared with some of the most used organic semiconductors [22].

It is worthwhile to point out that graphene mobility is strongly affected by the presence of impurity scattering. Interaction with the substrate, causing surface charge traps [26],

[27], interfacial phonons [23], and fabrication residues can heavily deteriorate carriers mobility, as it will be discussed in the next section. This leads to the need of employing high quality substrate or even no substrate at all, by using suspended structures over trenches [16].

A comparison of graphene with less common organic semiconductors can be also usefully made in terms of carriers mobility due to the emerging interest in making use of graphene for flexible and printable electronics, fields in which organic semiconductors lead. Organic materials, like pentacene, are in fact normally bendable and printable but they show low mobility. On the other hand, deposition of graphene on flexible substrates or the use of graphene ink for printable electronics allows for combining both characteristics (Fig. 1.4b) [22].

Additional theoretical material concerning graphene electronic and photonic properties will be introduced in Chapter 2, where graphene-based devices will be described.

1.3 – Dealing with graphene non-idealities

1.3.1 - Overview

In the previous sections, most of the attention has been paid to the physics of ideal graphene. Nevertheless, some of the above-mentioned almost unique properties can be even deeply modified when dealing with "real" graphene. For example, scattering by random charged impurity centers (long-range scattering or Coulomb scattering) or by lattice defects (short-range scattering), phonon scattering, effects of unintentional doping as well as strain and corrugation of the graphene layer induced by the substrate [28], [29], can all induce significant changes in graphene properties and, in principle, transform a 2D metal into an insulator. Having a finite (not null) value of V_{Dirac}, for example, could indicate that there exists an unintentional graphene doping, whose cause can be electrostatic or related to charge impurities [30]. In general, unintentional intrinsic p-doping of graphene has been mainly found to be caused by adsorbed water and oxygen molecules or contamination arising on the graphene surface [31], which

behave as electrons acceptors [32]. Increasing the ambient exposure, in fact, causes the hole-doping to get larger and, then, the V_{Dirac} to shift to more positive voltages [33]. Also, curvature and corrugation of the graphene sheet, together with modulation of hoppings due to elastic strain, modify the Dirac equation. As a direct consequence, a change in graphene transport properties is observed, causing alterations of the energy dispersion curve (which varies from linear to a conventional quadratic one), band-gap opening, mid-gap states induction and changing in the Dirac point location (in terms of position shifting and energy raising) [28], [34], [35]. Some examples are reported in Fig. 1.5.

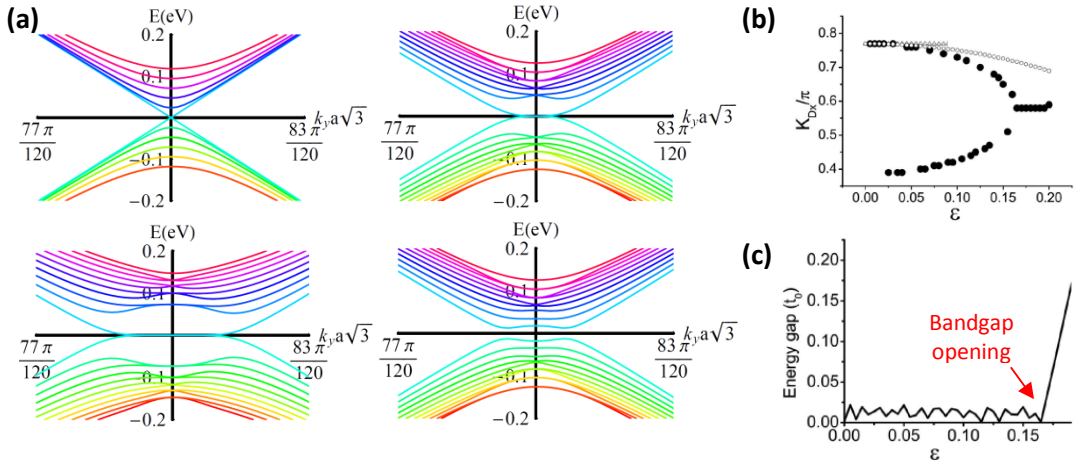


Fig. 1.5 – (a) Change in graphene low energy states induced by a ripple for increasing values of the hoppings modulation [34]. (b) Modification of a Dirac point under shear strain (ε), black circle points refer to numerical results while blank circle points to analytical data [35]. (c) Graphene energy gap modification vs. shear strain (ε) showing the band gap opening occurring under severe strain application (ε > 0.15) [35].

Mobility limiting value (i.e., the mobility value defined in the large carrier density limit, n ~ $4 \cdot 10^{12}$ cm^{-2}) can also be considered as a sample quality figure of merit together with the carrier density dependent conductivity $\sigma(n)$ [30]. Generally speaking, samples with a poorer quality show lower mobility and a broad conductivity minima close to the charge neutrality point. Nevertheless, in the case of unintentional doping, either an improvement or degradation of carrier mobility may occur, depending on the nature of the substrate impurities. In this case, in fact,

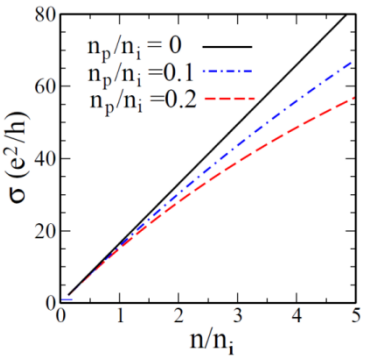


Fig. 1.6 – Graphene conductivity vs. carrier density calculated for different concentrations of charge impurity (n_i) and short-range scatterers (n_p) [36].

elements causing unintentional doping can potentially screen substrate impurities and help mitigation of carrier scattering [33].

Differences in terms of $\sigma(n)$ trends can then be noticed in samples having different quality and can give indications on the predominant scattering mechanism involved. In Fig. 1.6 [36], graphene conductivity as a function of carrier density is reported, assuming to include both charge impurity (n_i) and short-range scatterers (n_p). As it can be noticed, a linear dependence of $\sigma(n)$ (commonly found in most experiments) relates to a higher charged impurity concentration (small n_p/n_i), while, in the case of a predominant defect scattering (large n_p/n_i), a flattening of the conductivity curve can be observed, leading to the so-called *sub-linear* conductivity. Strictly speaking, point defects produce a constant conductivity, while charged impurity scatterers cause σ to grow roughly linearly in n/n_i. Of course, in any realistic graphene samples, both scatterers are present and the relative ratio determines in which kind of regime the sample is. Herein it is to be pointed out that Coulomb scattering time τ_C grows as ~ $\sqrt{n}$, while, in the case of short range scattering, $\tau_S \sim 1/\sqrt{n}$ [36], thus justifying the dominant effect of point defects (Coulomb scattering) in the large (low) carrier density regime. Deposition of potassium on graphene samples in Ultra High Vacuum (UHV) has been used to investigate the dependence of electronic transport properties of graphene on the density of charged impurities [26]. Summarizing, this leads to: a decrease of carriers mobility, a more linear dependence of $\sigma(V_G)$ on the gate voltage, an increase of holes mobility compared with electron mobility (i.e., $\mu_h/\mu_e \neq 1$), a shift of the gate voltage minimum conductivity to more negative gate voltage, a broaden of the width of the minimum conductivity region [26]. All the above-mentioned effects are summarized in Fig. 1.7. Defect scattering has also been deeply analyzed, for example, by ion-induced formation of lattice defects via Ne and He irradiation. Defect scattering causes the conductivity to be proportional to charge carrier density and mobility to decrease as the inverse of the ion dose, as reported in Fig. 1.8 [37]. Modification of Raman spectrum due to defects introduction is also depicted with the appearance of the D band indicating intervalley scattering.

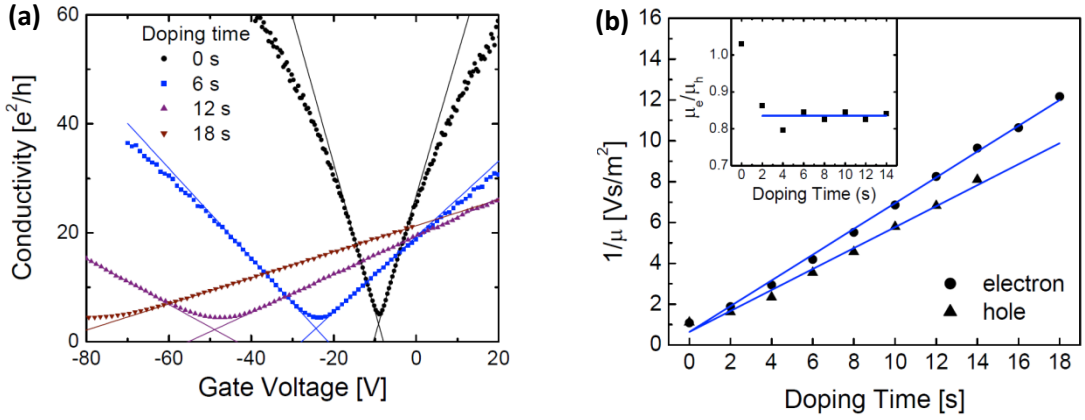


Fig. 1.7 – (a) Graphene conductivity plots under different K-doping concentration and (b) inverse of charge carriers mobility at different doping time. The inset reports the variation of the ration of μ_e and μ_h as the doping reaction proceeds [26].

Phonon scattering (i.e., lattice vibration) can also influence carrier transport of graphene and, being an intrinsic scattering source, can limit mobility at finite temperatures when all extrinsic scattering sources are removed. Three different phonon scattering mechanisms can be distinguished: intravalley acoustic phonon scattering, intravalley optical phonon scattering and intervalley scattering. Usually, intravalley phonon scattering, which causes an electronic transition within a single valley through acoustic or optical phonons, gives small contribution in graphene. On the other hand, intervalley scattering, which is responsible for electronic transition between different valleys, may be important, but only at high temperature [12].

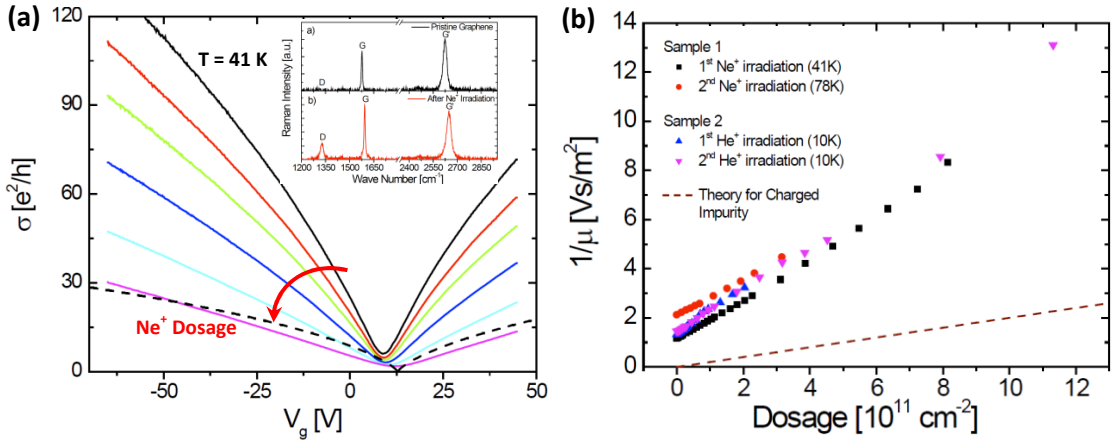


Fig. 1.8 - (a) Graphene conductivity plot and (b) inverse of charge carriers mobility for different Ne^+ irradiation dosage. The inset of picture (a) shows Raman spectrum alteration due to Ne^+ irradiation (adapted from [37]).

Summarizing, screened Coulomb scattering (or long-ranged charged impurity scattering) is found to be the most important scattering mechanism.

In fact, assuming an impurity density $n_i \approx 5 \cdot 10^{11}$ cm^{-2} for both scattering regimes, simple theoretical arguments lead to a scattering length $l > 1$ μm for short-range scatterers and $l \approx 50$ nm for charged impurity scatterers [30].

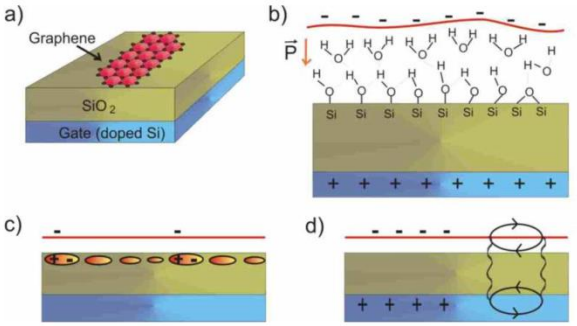


Fig. 1.9 – Main causes of interaction affecting (a) graphene deposited on SiO_2/Si substrates: (b) water molecules bonded to hydroxyl radicals at the substrate, (c) polar modes located at the surface of the substrate and (d) van der Waals bonds between graphene and the gate [27].

Of course, different kinds of electrostatic interactions may occur between graphene layers, the substrate and other materials, which may exist in the environment causing alterations of graphene properties. For the common case of graphene deposited on SiO_2, different causes can be found, like: interactions with molecules attached to hydroxyl radicals at the substrate, interactions with polar modes at the surface of the substrate, van der Waals interactions between the graphene sheet and the metallic gate (Fig. 1.9) [27]. For this kind of device structure, it has been experimentally shown that the most significant interactions are those related to graphene and the polar modes of the SiO_2 substrate and to graphene and water layers on top of the substrate [27].

I conclude this section with a brief discussion concerning the sample dependent value of the conductivity minimum, anticipated in the previous section (Fig. 1.3c). The variability of σ_{min} around the value $4e^2/h$, in fact, seems to be related to an inhomogeneous charge distribution in the low density limit near the Dirac point, where the carrier concentration becomes smaller than the charged impurity density and the system breaks up into puddles of electrons and holes (Fig. 1.10) [30], [38]. Then, charged impurities induce a residual density distribution in graphene sample that is responsible for the minimum

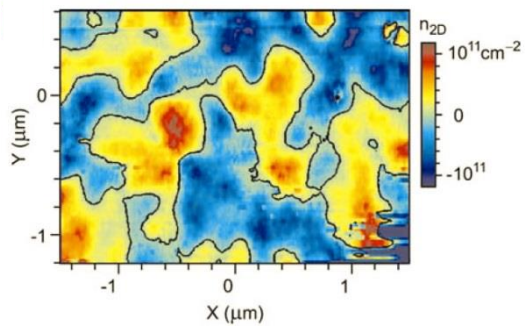


Fig. 1.10 - Two dimensional map of electrons (red areas) and holes (blue areas) spatial density for *Puddle model* assuming an average carrier density of zero. Zero density contours are marked with black lines [38].

conductivity thus justifying σ_{min} dependence on the impurity concentration (i.e., on the sample quality) [30].

From the analysis of what has been reported, it is clear that both the choice of the substrate and the reduction of fabrication contaminations are the key points required to allow ballistic transport over micron lengths, thus opening concretely the possibility of a new electronics based on quantum transport at room temperature.

1.3.2 - Hysteresis

In this section, some notes on the hysteretic behavior of graphene-based devices will be given. More in detail, hysteresis appears as a shift in the transfer characteristics under standard ambient conditions with respect to the gate voltage. It can play a significant role especially in the characterization of active devices, for which sweeping backward and forward the gate voltage is a usual procedure to tune the channel conductivity, as it will be shown deeper in the experimental section. Hysteresis in graphene relates again on the interaction between graphene and the surroundings, mainly due to the low density of states near the charge neutrality point, which makes graphene electronic properties really sensitive to the environment, and to the large surface-to-volume ratio, which promotes the bonding with adsorbates [31], [39]. Two mechanisms seem to be more likely responsible for hysteresis in graphene: charge transfer and capacitive gating [39]. Despite being conceptually different in the way they act, the two mechanisms both produce a shift of conductance curves due to a modification of graphene carrier density. In the first case (Fig. 1.11a), this happens due to a simple charge transfer from graphene to charge traps and vice versa. In the case of capacitive gating Fig. 1.11b, instead, the application of an external electric field causes ions with opposite charge to move toward graphene and dipoles to align along the external electric field. This charge redistribution alters the local electrostatic potential nearby the graphene channel, which then promotes the attraction of majority carriers through the metallic contact, thus increasing the carrier density [39].

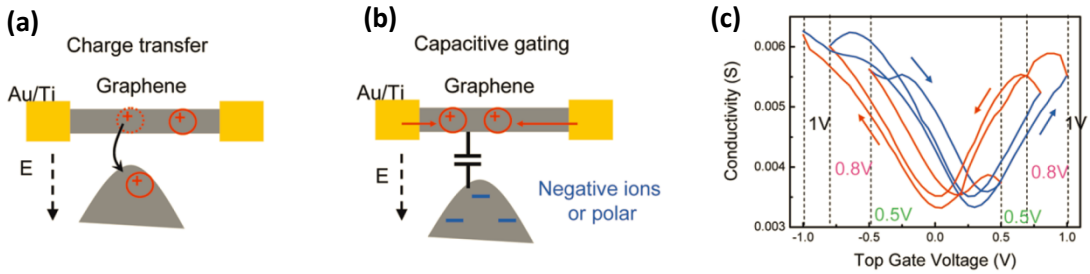


Fig. 1.11 - (a) Charge transfer phenomena and (b) capacitive gating effects causing hysteresis in graphene-based devices. (c) Conductivity plots vs. gate voltage under different sweepings conditions. The arrows show the voltage sweeping direction (adapted from [39]).

In general, both mechanisms affect graphene electronic transport on the seconds time scale and they both coexist in graphene-based active devices causing shifts of the conductivity curves with respect to the gate voltage Fig. 1.11c.

Vacuum treatments, thermal and current annealing and chemical hydrophobization of the substrate have been demonstrated to effectively suppress hysteresis [39]–[42], although most samples tend to return to their initial hysteretic state after a short time when back to ambient conditions.

1.4 - Graphene fabrication techniques

As it will be discussed in Chapter 3, in which the experimental part will be presented, in this work both transferred monolayer graphene obtained through chemical vapor deposition and reduced graphene oxide have been employed for devices fabrication. Of course, the choice of the starting graphene film can strongly influence devices performance and, in general, a compromise between material quality and cost needs to be reached, depending on the particular application to be designed. Due to the importance of this topic, in this section an overview of graphene fabrication techniques will be given [43], [44], while some notes on graphene oxide and its reduction methods will be presented further on. The latter aspect, in fact, plays an important role in this work since a part of the experimental activity has been dedicated to the development of a “green” and cheap reduction method, as it will be described deeply in Chapter 3.

As a general rule, the development of new materials deeply relies on the progress of the production techniques, due to the need of finding the best compromise for each particular application between quality and cost of the final product. This is also

true for graphene production, where additional difficulties arise from the intrinsic 2D nature. Up to now, according to literature, more than fifteen methods have been developed to produce graphene films of various dimensions, quality and cost as summarized in Fig. 1.12 and Table 1.1.

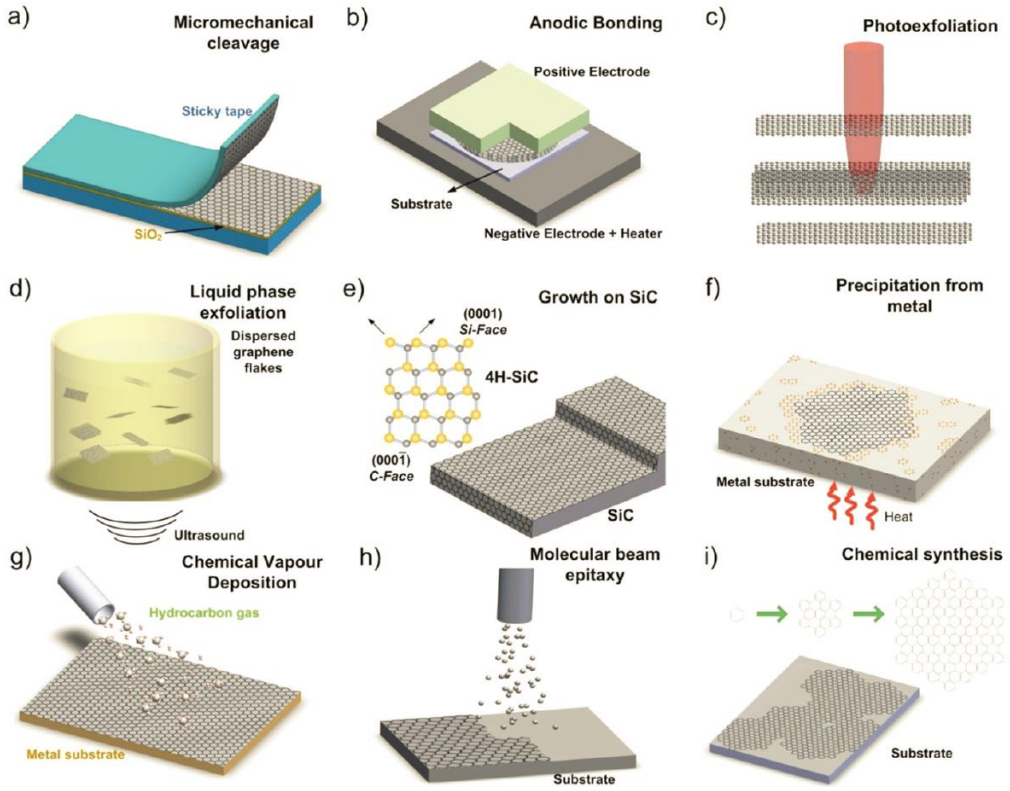


Fig. 1.12 – Main graphene fabrication techniques [43].

Among them, dry exfoliation has been one of the first production processing that has been historically developed. It consists in the splitting of the original layered material (e.g., graphite) into atomically thin sheets through mechanical (using adhesive tape [7], Fig. 1.12a), electrostatic (e.g., anodic bonding [45], Fig. 1.12b) or electromagnetic forces (laser ablation and photoexfoliation [46], Fig. 1.12c) in air, vacuum or inert environments. In particular, Micromechanical Cleavage (MC) can lead to very high quality layers production with graphene grains size limited by the single crystal grains of the starting graphite material (millimeters). Mobility up to 10^6 $cm^2V^{-1}s^{-1}$ have been reported for suspended graphene produced via MC [47] and this aspect suggests that,

even if not suitable for large-scale applications, MC is still the best choice for fundamental research and proof of principle devices.

Exfoliation can also be accomplished in liquid environments (Fig. 1.12d) involving generally three steps: dispersion in a solvent of the starting graphite material or any other layered material, exfoliation by sonication (which helps graphite splitting into individuals platelets) and final purification through ultracentrifugation. Chemical wet dispersions are generally employed for the exfoliation step while ultrasonication can be made both in aqueous [48] and non-aqueous solvents [49]. The solvent choice is generally quite critical due to the need of minimizing the interfacial tension between the liquid and the graphene flakes. Employing water is generally not a good solution due to its high interfacial tension for graphene and graphite dispersion [50], so alternative chemicals solutions need to be considered [49], [51]–[53]. The versatility of liquid phase exfoliation can also be exploited to exfoliate oxidized graphite pellets thus producing graphene oxide, as it will be discussed more in-depth in a separate section. Although less expensive for mass fabrication than other methods, liquid-phase exfoliation allows the production of lower quality graphene films.

Graphitic layers production from SiC (Fig. 1.12e) has a long tradition, with the first investigation started from 1960 [54]. Both the Si-terminated and the C-terminated surfaces have been proved to be suitable for graphitization since the growth mechanism basically relies on Si-atoms sublimation [55], [56], originally made only at high temperature and UHV conditions. Nevertheless, first attempts suffered from the non-self-limiting nature of the growth process, which led to the production of areas of high different film thickness. Now, the number of graphene layers that can be grown can be controlled and high quality graphene has been obtained with crystallites up to hundreds of micrometers in size [57]. Moreover, graphene growth on SiC could benefit from the well-established SiC technology for power electronics in the fabrication of new devices. Nevertheless, this approach has still some drawbacks for the large scale production due to SiC wafers cost (~ 30 times the cost of Si wafers of the same area) and small size (usually no larger than 4’’). Also, the common growth technique employs high temperature processing (above 1000 °C) which is not directly compatible with Si electronics technology. For these reasons, other options have been developed and are

currently underway [58], like the possibility of graphene growth on SiC surfaces via laser processing [59], [60].

Chemical Vapor Deposition (CVD) is currently employed for large-area uniform polycrystalline graphene film production (Fig. 1.12g). As it happens for most of materials normally grown through CVD, a wide variety of precursors, chamber pressures and temperatures can be used to produce graphene [43]. First attempts of growing graphene through thermal CVD on metals have been carried out employing Ir as substrate material, due to its low carbon solubility [61]. Nevertheless, it was immediately clear that new materials and processing needed to be found due to the difficulties in the subsequent graphene transfer procedure on top of the target substrate and to Ir cost. In 2009, polycrystalline Cu foils have been demonstrated to provide a good support for uniform, large area (~ cm^2) CVD growth of graphene films [62]. This process exploits thermal decomposition of methane, low carbon solubility and allows a self-limited growth since graphene formation mostly stops once the Cu surface is fully covered. Production of square meters of graphene via CVD has already been obtained [63] and, on a smaller scale, state-of-the–art devices employing CVD graphene films have been fabricated, showing transport properties comparable to those of exfoliated graphene on both SiO_2 and hexagonal boron nitride substrates [44]. Nevertheless, some difficulties arise from the high cost of the process and the high temperatures required (> 1000 °C), which make difficult to integrate graphene with standard CMOS processing. Also, due to the difference (an order of magnitude) in thermal expansion coefficients between Cu and graphene, a significant increase in wrinkle density upon cooling may appear, causing significant device degradation [64], [65]. Finally, other issues concern the subsequent graphene transfer process from the metal foil to the target substrate, which can often be as complicated as the growth itself and cause a significant degradation of the transport properties of the final device. For these reasons, the main target would be the development of graphene growth techniques on arbitrary substrates and at lower temperatures employing, for example, Micro Wave Chemical Vapor Deposition (MWCVD) [66], Plasma Enhanced CVD (PECVD) [67] and Inductively Coupled Plasma (ICP) CVD [68]. Through these techniques, in fact, graphene synthesis at lower temperature is, potentially, possible although improvements are still needed to reduce graphene damages caused by direct plasma exposure during growth.

Additional graphene production techniques can also be found in literature, although it is unlikely that they will become commercially feasible in the next years, mainly due to the much higher cost compared to the above-mentioned methods. Among them, Molecular Beam Epitaxy, Atomic Layer Epitaxy, chemical synthesis and precipitation from carbon containing metal substrates have been investigated. An overview of these methods can be found in [43].

Growth Technique	Crystallites size [μm]	Sample size [mm]	Mobility (at RT) [$cm^2V^{-1}s^{-1}$]	Price (for mass production)	Applications
Micromechanical cleavage	1000	1	10^5	$$$$	Research
LPE of graphite	0.01 – 1	0.1 – 1 (∞ as overlapping flakes)	10^2 (for a layer of overlapping flakes)	$	Inks, coatings, paints batteries, supercaps, solar cells, fuel cells, sensors, photonics, flexible electronics and optoelectronics, bio-applications
LPE of GO	> 1	> 1 (∞ as overlapping flakes)	1 (for a layer of overlapping flakes)	$	Inks, coatings, paints batteries, supercaps, solar cells, fuel cells, sensors, photonics, flexible electronics and optoelectronics, bio-applications
Growth on SiC	100	100 (6″)	10^4	$$$	High-frequency transistor and other electronic devices
CVD	50000	1000	10^4	$$	Photonics, nanoelectronics, sensors, bio-applications, flexible electronics

Table 1.1 – Overview of the main graphene growth techniques and related characteristics (adapted from [43], [44]).

1.5 – Graphene oxide

1.5.1 - Chemistry

Considered as an oxidized form of graphene, Graphene Oxide (GO) has proved to be a promising precursor of graphene-based materials, particularly when state of the art transport properties are not required and, on the other hand, a lower cost needs to be kept (e.g., for coatings, paint/ink and transparent conductive layers production). Although several techniques have been developed over the years to produce large quantities of GO, basically they all rely on the same technological steps: a first oxidation of inexpensive graphite powders by employing strong oxidants species (e.g., H_2SO_4, HNO_3, $KMnO_4$, $KClO_3$, $NaClO_2$), followed by exfoliation of graphite oxide through a variety of thermal and mechanical methods, among which sonication and stirring in water are the most widespread. In particular, during the last step, suspensions in which individual GO flakes can lay stable by mutual electrostatic attraction and repulsion forces are obtained. A schematic picture of GO synthesis is reported in Fig. 1.13a. Until today, three methods are most commonly used for the preparation of graphitic oxide, which basically differ for the oxidizing species used: Brodie, Staudenmaier and Hummer-Offemann, with the last one being the most recent and commonly used [69]. It is to be pointed out here that the choice of the oxidizing species can really make the difference between the production methods, since it strongly affects the GO structure, the residue contamination and, consequently, the final GO quality [70].

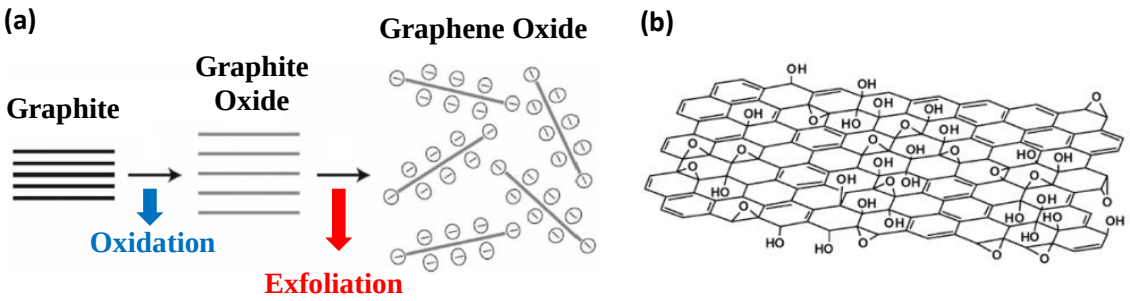


Fig. 1.13 - (a) Schematic representation of graphene oxide synthesis (adapted from [70]). (b) Lerf and Klinowski model of graphene oxide [71].

In Fig. 1.13b, a schematic of one of the most well-known and cited GO model, the one by Lerf and Klinowski [71], [72], is also reported.

Although no unambiguous model of GO exists, mainly due to its nonstoichiometric atomic composition, polar oxygen functional groups are always included, since they are responsible of the hydrophilic nature of graphite oxide, thus explaining the reason why it can be exfoliated in many solvents and disperses particularly well in water. Moreover, oxygen-containing functional groups, together with defects produced during the oxidation process, change the sp^2 carbon network typical of pristine graphene and, consequently, they can be considered as the main responsible of the different electrical behavior between GO and graphene. In fact, the disrupted sp^2 bonding network makes both graphite oxide and GO electrically insulating materials. Nevertheless, electrical conductivity can be recovered trying to restore the π-bonds network through reduction reactions; i.e., transforming GO into Reduced Graphene Oxide (RGO).

In this work, RGO has been employed to fabricate X-Ray transparent electrodes on diamond detectors and a new rapid thermal reduction process has also been specifically developed. For these reasons, as a support to the experimental work presented in Chapter 3, a review of the reduction techniques found in literature will be given in the next section. A synthesis of GO modelling, reduction methods and related experimental progress can be found in [70].

1.5.2 - Review of reduction methods

Similarities existing between RGO and pristine graphene in terms of electrical, thermal and mechanical properties, as well as surface morphology, explain why the reduction processes are among the most important reactions involving GO. Over the years, a huge variety of procedures has been developed, employing chemical, thermal and electrochemical approaches. Although the main target of every reduction reaction is the production of graphene-like material (i.e., as similar as possible to what can be obtained through more conventional graphene fabrication techniques), every reduction protocol has its own pros and cons, leading to final films that resemble pristine graphene with different degrees of approximation. Chemical reducing agents have been traditionally

employed and, among them, hydrazine (N_2H_4) has been the first and most commonly used due to its strongly reducing action under low temperature (~ 100°C), although its high toxicity prevents its use for mass production. Moreover, nitrogen species, effective in the oxygen functionality removal, tend to remain covalently bonded to GO surface and act as n-type dopants, thus deeply affecting the electronic properties of the resulting RGO film. For all these reasons, the possibility of employing other chemical reducing agents has been investigated and in particular: alcohol (C_2H_6O), sodium/potassium hydroxide (NaOH/KOH), sodium borohydride ($NaBH_4$), hydriodic acid and acetic acid (HI-AcOH). In general, electrical conductivity is found to be one of the main parameter used to evaluate the reduction reaction quality or, in other words, how the reduction process is able to restore the sp^2 network. GO conductivity usually ranges between 10^{-8} and 10^{-5} $S \cdot m^{-1}$ while, for RGO, values of the same order of magnitude of graphite can be reached (e.g., ~ 30400 $S \cdot m^{-1}$compared with ~ 84500 $S \cdot m^{-1}$ of graphite) [70], [73]. In [74], a sheet resistance as low as 15 kΩ/□ has been obtained via C_2H_6O reduction at high temperature (600 – 1000 °C), while typical values for hydrazine reduced sample lay around 800 kΩ/□. Lower temperature (50 – 90 °C) chemical reactions have also been proved in strongly alkaline conditions (NaOH/KOH). Combination of different chemicals can be employed as a possible way to try to improve films quality. In [75] a two-step reduction process, using a deoxygenation process with $NaBH_4$ followed by dehydration with concentrated sulfuric acid, has been reported. Both the reaction and the evolution of the conductivity values for the above-mentioned approach is reported below.

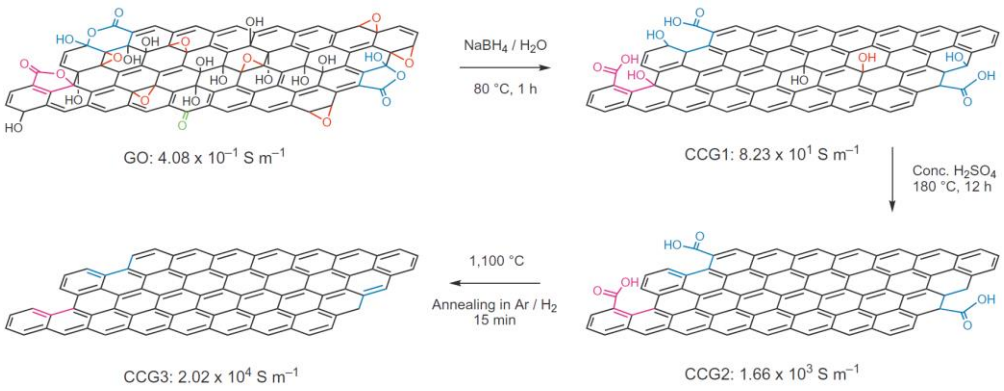


Fig. 1.14 – A GO chemical reduction example [75].

Although most of the chemical reduction methods reported previously reduce GO in suspensions, reducing agent vapors can also be used. Among them, HI-AcOH and HI vapors allow the production of RGO powder pellets with a conductivity of 30400 $S \cdot m^{-1}$ [73]. Reduction through metals (like iron, aluminum and iron powders) has also been reported in literature [76]. Although the wide choice of chemical reducing agents and the possibility of producing good quality RGO films, no chemical approach has been proved to be suitable for mass production. The reasons for that are mainly related to the toxicity of the reducing agents, multiple steps needed (i.e., reaction, washing, filtration and dispersion), long time required (from hours to days) and partial removal of the oxygen-containing groups, which causes low conductivity and increases the difficulties in restoring lattice defects such as missing carbon atoms or holes in the GO carbon network. In order to overcome these limitations, thermal reduction processes have been widely investigated. In this case, the oxygen-containing functional groups can be removed through the release of gas molecules of H_2O, CO_2, and CO, as depicted in Fig. 1.15a, where an example of temperature desorption spectra of thermally reduced GO through an heating rate of 30 $°C \cdot min^{-1}$ is reported [77].

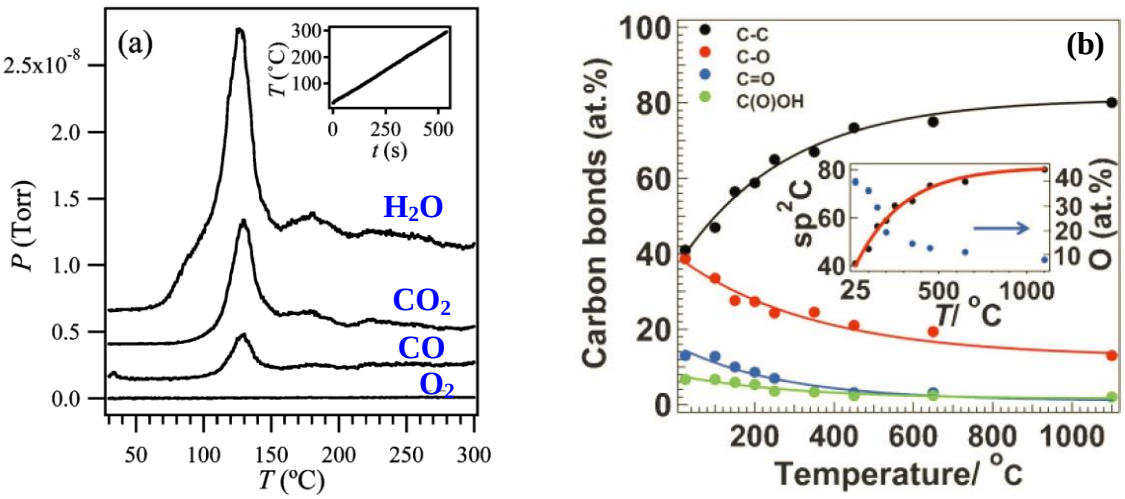


Fig. 1.15 – (a) Typical desorption spectra of thermally reduced GO; the inset shows the thermal heating rate employed (adapted from [77]). (b) Atomic concentration of different C-based species vs. annealing temperature; in the inset, a comparison between the percentages of oxygen and sp^2-carbon atoms during the reduction process is also reported [78].

In particular, water molecules formation relies on hydrogen dissociation from hydroxyls and subsequent recombination of nearby hydroxyls, which leads to H_2O molecules

formation while leaving the atop oxygen atoms to form epoxies [70]. The mechanism of CO_2 and CO creation, on the other hand, seems not to be perfectly clear yet. Complete O_2 removal, instead, seems not to be possible even when heating temperatures up to 1100 °C in ultra-high vacuum are employed, as summarized in Fig. 1.15b, where both the atomic percentage of the different carbon species involved and the oxygen concentration (inset) with respect to the annealing temperature are reported. This reduction inefficiency needs to be taken into account, since it may represent an intrinsic limit in the final RGO film electrical properties. A comparison of the electrical properties of GO films of different optical transparency after undergoing hydrazine, hydrazine/thermal and thermal reduction treatments is reported in Fig. 1.16 (left), showing how higher quality films can be obtained through thermal reductions. This is confirmed in Fig. 1.16 (right), which groups the high-resolution X-Ray Photoelectron Spectroscopy (XPS) analysis for the above-mentioned cases and shows how higher concentration of carbon-carbon species and absence of nitrogen groups can be reached via thermal treatments.

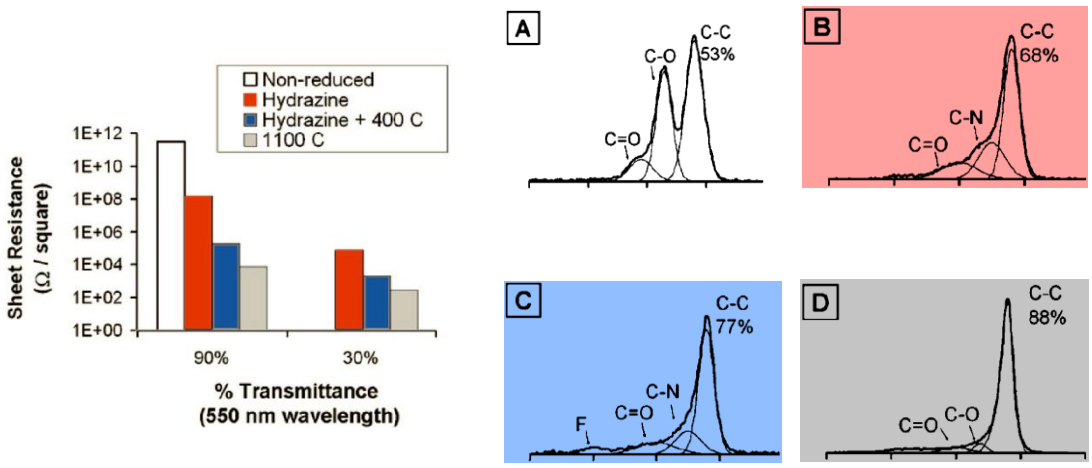


Fig. 1.16 - (Left) Comparison of the electrical properties, in terms of sheet resistance, of GO films reduced employing different reduction reactions. (Right) X-ray photoelectron spectroscopy analysis of the corresponding GO films (adapted from [79]).

From mass loss studies made during thermal reduction processes, two main temperature intervals have been demonstrated to play a significant role: the first one, around 150 °C, in which epoxies and hydroxyls can be removed, and the second one, around 600 °C, in which all the other functional groups are involved and the real thermal reduction takes

place [70]. In general, thermal approach may introduce significant mass loss between GO and RGO, so great care needs to be taken in the choice of the starting GO film thickness. A typical mass loss of ~ 30% can be noticed when reaching 200 °C followed by an almost linear decrease of weight [79]. The atmosphere in which the thermal reaction takes place may also influence the final product and gives the technologist additional degrees of freedom to tailor RGO properties. For example, thermal reductions in UHV or Ar prevents adsorbates or contaminants, while nitrogen-containing gaseous mixtures (e.g., NH_3 or hydrazine) allow the production of n-type RGO films. P-type behavior, instead, can be obtained via H_2 atmosphere. Combinations of different techniques to increase the reduction level have also been reported [70], [80]. Accordingly to what previously described, the critical issues of thermal treatments appear clear especially in terms of thermal cycles (regime maximum temperature and heating/cooling rates), atmosphere and reduction time choices. For these reasons, different thermal combinations can be found in literature, like single cycles (400 °C for 3h at a rate of 20 °C/min in Ar flow) or combined cycles (100 °C at ambient pressure, then 1100 °C for 3h at 20 °C/min in vacuum) [79]. Apart from both the atmosphere and the temperature cycles, the heating sources may also have a significant role in RGO production. Together with more conventional thermal reduction processes in furnaces described previously, other sources such as chemical-free flash light [81], laser [82]–[84] and electron beam [85], [86] have been reported. Reduction through microwave, plasma and heated atomic microscope tip can also be found [70]. Clearly, the choice of the heating source needs to be made by taking into account not only the quality of the final product but also the size of the samples, since a necessary compromise between speed, quality and control of the reduction area needs to be found.

From what has been previously presented, thermal reduction, compared with the chemical approach, has the clear advantage to be more controllable and safe through the choice of heating temperature, gas environment and duration although the highest reduction levels have been achieved employing hybrid (chemical/thermal) methods. In general, a compromise between film quality, size of reduction area and reaction duration needs also to be found. The particular solution developed during my visiting period at SLAC exploits Rapid Thermal Annealing (RTA) systems to combine the advantages of all typical thermal reduction processes (e.g. absence of toxic agents and

parallel reduction of several GO coated substrates) with an unequalled reduction speed and without compromising the film quality. These results will be presented in Chapter 3. A summary of GO reduction processes is reported in Table 1.2. I refer to [70] for additional details.

Sample	Forms	C:O (atomic ratio)	Conductivity [$S \cdot m^{-1}$]
Graphite	Pellet	20	84500
		72.5	1160 – 140000
Graphene	Film	Unknown	$5 – 6.4 * 10^{6}$
GO	Film	2.6	$6 * 10^{-5}$
		2.2	$6.8 * 10^{-8}$
GO/N_2H_4, RT	Pellet	10.3	200
GO/N_2H_4, RT	Film	12.5	9960
GO/N_2H_4, RT	Paper	11	1700
150 °C			16000
GO/N_2H_4, 1100 °C	Film	Unknown	55000
GO/N_2H_4 + NH_3, RT	Paper	Unknown	7200
220 °C			11800
500 °C			35000
GO/N_2H_4 + KOH, RT	Paper	3.1	690
GO/N_2H_4 +$C_{16}H_{10}$, RT	Paper	Unknown	200
GO/N_2H_4 +$C_6H_{15}N$, 500 °C	Paper	> 2.6	1700
GO/N_2H_4 +$NaBH_4$, RT	Film	Unknown	1250
GO/$NaBH_4$, RT	Pellet	4.8	82
180 °C		8.6	1660
1100 °C		> 246	20200
GO/$NaBH_4$, RT	Film	8.6	45
GO/$Na_2S_2O_4$ + NaOH, 80°C	Film	Unknown	1377
GO/$NaHSO_3$, RT	Paper	6.48 – 7.89	6500
GO/HI and AcOH, RT	Pellet	6.7	30400
GO/HI, RT	Film	12	29800
GO/NMP, RT	Paper	5.15	374
250 °C		Unknown	1380
500 °C		Unknown	5330
1000 °C		6.03	57300
GO/$C_4H_6O_3$, 250 °C	Paper	6.8 – 8.3	2640 – 5230
GO/ C_7H_8O, RT	Pellet	30	4600
GO/Fe, RT	Paper	7.9	2300
GO/Al, RT	Paper	18.6	2100
GO/vitamin C, RT	Film	12.5	7700
GO/150 °C	Paper	4.7	230
GO/1050 °C	Film	9.7	1000 – 2300
GO/1100 °C	Film	Unknown	55000
GO/Flash	Film	4.2	1000
GO/Microwave	Paper	5.46	200
GO/Microwave	Pellet	2.75	274
GO/Laser	Film	Unknown	26000

Table 1.2 – Overview of the main GO reduction reactions. Listed temperatures are either drying temperatures or heating temperatures while RT stands for room temperature. Adapted from [70] and [83].

Chapter 2
Graphene in Electronics and Photonics

A first theoretical background concerning graphene properties has been given in Chapter 1. In this chapter, additional graphene peculiarities, which play a significant role in the development of graphene-based devices, will be presented. The main target of this section is giving to the reader a more complete idea of graphene multifunctionality. In particular, most of the attention will be paid to the electrical and optical properties that make graphene a starting material for high-frequency transistors, photodetectors and transparent conductive electrodes fabrication, as all these subjects have been widely handled in the experimental work of this thesis.

2.1 - Graphene for transistors fabrication

2.1.1 - Overview

The possibility of employing graphene as semiconductor material for high-frequency transistors fabrication has been intensively investigated since the very beginning of its discovery. Clearly, in this field, graphene has to fight with more mature technologies, such as III-V materials, so it is not difficult to foresee that we still have to wait some years before seeing graphene entering in the high-frequency devices market consistently. This is particularly awaited, since projections show that III-V materials will not be able to fulfill the next requirements in terms of both current and power modulation [44]. Theoretically speaking, an ideal semiconductor should guarantee to have the following properties: wide bandgap, excellent carrier transport properties and high thermal conductivity, possibility of being "friendly" produced on large-area substrates with processes compatible with Si CMOS technology, possibility of interfacing with good dielectric materials without affecting its carrier transport close to the dielectric interface, low contact resistance [22]. Therefore, now, the question that arises is if graphene peculiarities meet these requirements. Concerning the first point, I

have already anticipated that natural, large-area graphene behaves like a semimetal with zero bandgap with cone-shaped valence and conduction bands touching each other at the Dirac point. This property leads to devices that cannot be switched off and, therefore, that are not suitable for logic applications. Nevertheless, graphene bandgap opening can be performed (that is, band structure can be modified) constraining large-area graphene in one dimension (forming the so-called nanoribbons), biasing bilayer graphene, applying strain or irradiating graphene with an ion beam [22], [25]. For example, in the case of gapless bilayer graphene, theoretical investigations and experiments have demonstrated that gaps up to 250 meV can be reached in high fields conditions (~ 10^7 V·cm^{-1}) [87], [88], while gaps around 300 – 400 meV have been obtained employing graphene nanoribbons [89], [90] which are slightly close to the suggested minimum gap of 360 – 500 meV needed for digital logic [22]. All these matters are summarized in Fig. 2.1a. In terms of mobility, graphene advantages over more conventional semiconductors have already been described in Chapter 1 (Fig. 1.4a has been reported here for the sake of clarity).

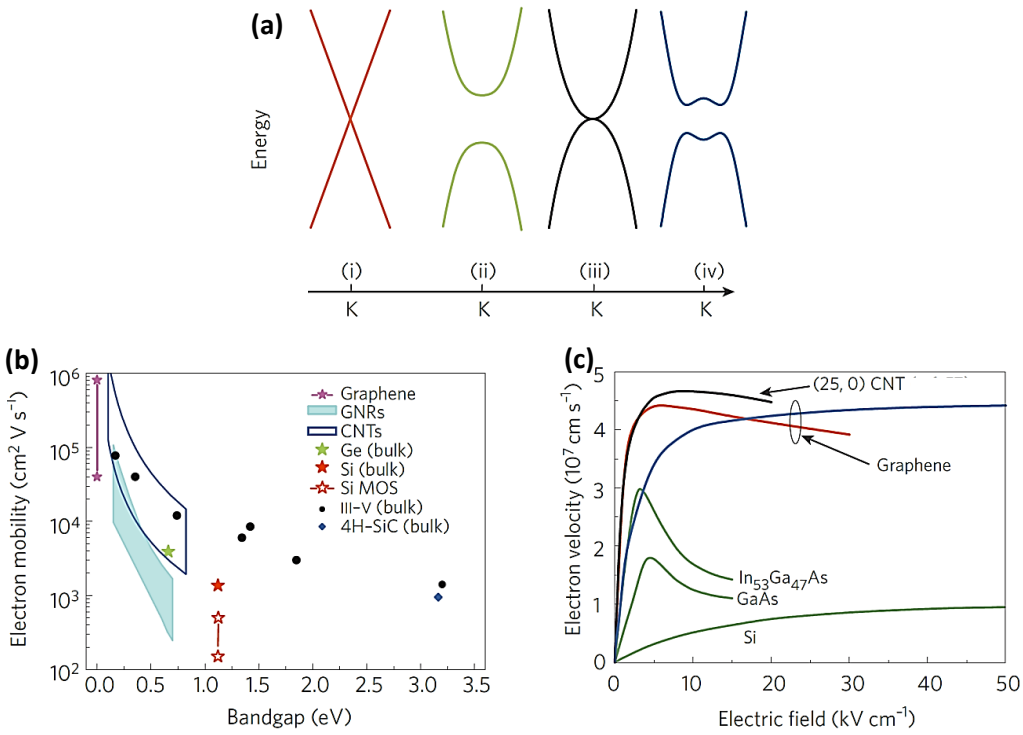


Fig. 2.1 – (a) Graphene band structure close to the Dirac point of (i) large-area graphene, (ii) graphene nanoribbons, (iii) unbiased bilayer graphene and (iv) biased bilayer graphene. (b) Comparison of electron mobility vs. bandgap in the low electric field regime between graphene and other conventional semiconductors. (c) Electron velocity plots vs. electric field of graphene, carbon nanotubes (CNT) and some common semiconductors [25].

Such high values, together with the peculiarity of having both holes and electrons mobilities almost equal, make graphene quite attractive for high-speed devices fabrication. Nevertheless, additional considerations on mobility data need to be made since high values often adversely affect other properties or can even not be the only limiting parameter for high-frequency devices. Strictly speaking, mobility numbers are normally referred to large-area gapless graphene. Actually, as it is known from conventional semiconductors, the electron mobility tends to increase as the bandgap decrease (Fig. 2.1b) and the same trend has been predicted for graphene nanoribbons [91], [92]. This means that, even if high-frequency operation can potentially be obtained with graphene, this comes at the expense of the possibility of switching properly the devices off (i.e., higher static power consumption is expected for CMOS configuration) [25]. Mobility however is not the only (or maybe not the most appropriate) measure of the speed of carrier transport, which makes graphene appealing for high-speed devices. Short gate lengths employed nowadays in modern FETs, in fact, can easily lead to high fields in a fairly large channel area. For example, considering a FET with 100 nm-long gate, a drain-source voltage of 1 V and a 0.3 V drop across the series resistances, a field of ~ 70 $kV \cdot cm^{-1}$ can be found in the channel. In this high field conditions, the influence of mobility in the device performance becomes less significant due to the saturation of the steady-state carrier velocity which, on the other hand, becomes a relevant figure of merit of carrier transport. In Fig. 2.1c, a comparison of electron velocity versus the electric field is reported for graphene and conventional semiconductors. As it can be noticed, graphene films show a carrier velocity two times higher than GaAs and four times higher than Si and, in the high field regime, its carrier velocity does not decrease as fast as in the III-V semiconductors. Moreover, according to the scale theory, having a material that allows thin channel region fabrication, helps to suppress short-channel effects thus giving the opportunity to scale MOSFETs to very short gate length. Graphene obviously provides the thinnest possible channel so graphene MOSFETs should be, in principle, more scalable than their direct competitors [25]. All these aspects justify the advantage shown by graphene over conventional semiconductors in terms of carrier transport properties and, consequently, the scientific community interest in graphene high-frequency transistors fabrication. This is summarized in Fig. 2.2, where the cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) have

been chosen as high-frequency figures of merit [93]. In particular, f_T values are impressive especially considering the relative young age of graphene with the longer timescale of other technologies. Graphene FETs have now indeed overtaken the best silicon MOSFETs and are approaching InP HEMTS and GaAs mHEMT performance. An apparent contradiction, instead, appears when looking at the f_{max} values. This discrepancy, however, seems to be due to a weak saturation of the drain current which, combined with high source-drain resistances, deteriorate seriously the power gain and, consequently, the f_{max} value while leaving unaffected the current gain. More details concerning the weak saturation regime typical of graphene transistors will be given later in this section. A more analytical approach on the dependence of both f_T and f_{max} on DC bias conditions will be found in Appendix A.

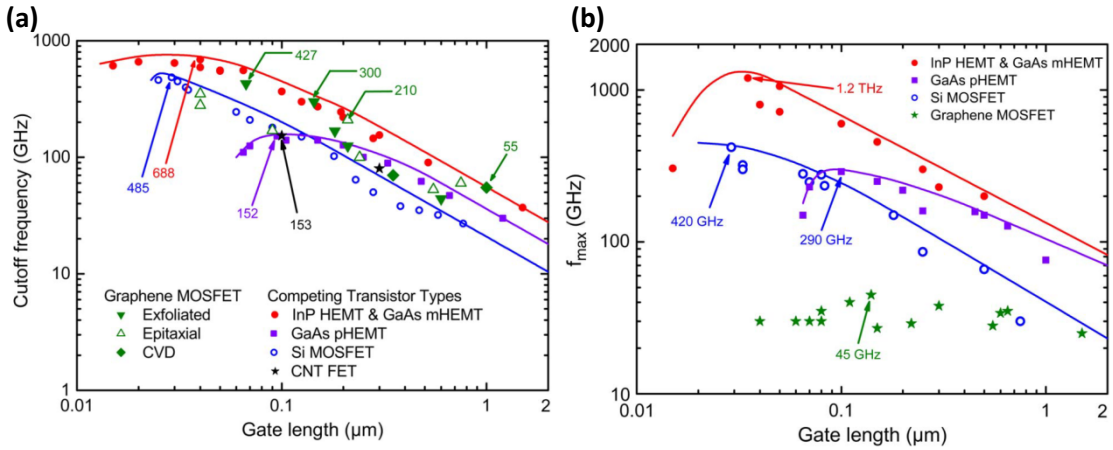


Fig. 2.2 – (a) Cut-off frequency (f_T) and (b) maximum frequency of oscillation (f_{max}) of graphene MOSFETs compared with competitive classes of RF FETs vs. gate length [22].

As for the carrier density, the requirement of providing enough carriers for appropriate FET operation is definitely fulfilled, with carrier sheet densities in excess of 10^{12} cm^{-2}, similar to what can be obtained in more conventional FETs [22].

Requirements concerning heat dissipation are also met due to the excellent graphene thermal conductivity (30 – 50 $Wcm^{-1}K^{-1}$ [94], that is almost one order of magnitude higher than copper) although often the heat transfer through the substrate can be the real limiting factor.

Finally, the contact resistance between source and drain contacts and the graphene channel needs to be considered due to its crucial role for proper transistor operation. Considering this aspect, graphene transistor still show lower performance

(e.g., contact resistance almost ten times higher) if compared with Si and III-V FETs [95], [96]. Nevertheless, a proper choice of the metal [97] and the application of contact patterning in the form of cuts in the contact regions of a graphene device [98] may help in decreasing resistances values.

Differences between graphene and conventional MOSFETs can be found in DC output characteristics, with graphene-based devices showing a linear shape with no saturation or only weak saturation (Fig. 2.3).

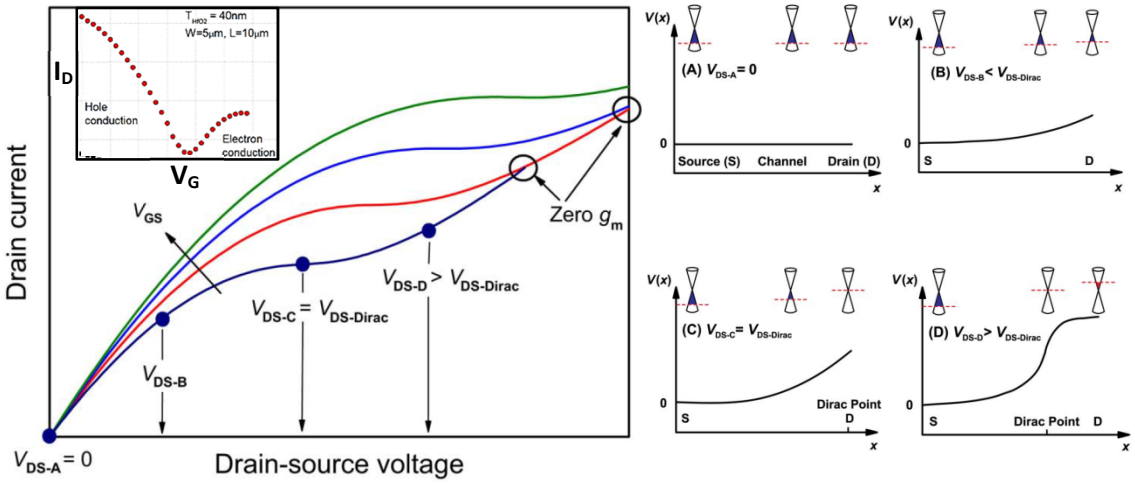


Fig. 2.3 – (Left) Typical output characteristic of a n-type GFET vs. the drain-source voltage, showing the main transistor operating regions. The curves are parametrized in terms of the gate-source bias. In the inset, a qualitative shape of a GFET transfer characteristic is depicted. (Right) Potential distribution and position of the Fermi energy (red dotted lines) of transistors for different biasing conditions (adapted from [22] and [99]).

Three regions can be distinguished in the I_D vs. V_{DS} curve (Fig. 2.3, left panel).

For $V_{DS-A} < V_{DS} < V_{DS-B}$ (Region I), the transistor is found to work in the first linear region. Then, increasing V_{DS}, the output characteristics start to saturate ($V_{DS-B} < V_{DS} < V_{DS-C}$, Region II) until the inflection point, $V_{DS} = V_{DS-C} = V_{DS-Dirac}$ (where $V_{DS-Dirac}$ refers to the drain-source voltage required for the Dirac condition), is reached. Then, for $V_{DS} > V_{DS-Dirac}$, a change in the conductivity type can be observed (from p-type to n-type or vice versa) and the transistor starts operating in a second linear region (Region III). It is to be pointed out that, for sufficiently high V_{DS} values, the output curves for different V_{GS} may cross, leading to a zero transconductance, which means that the gate is not controlling anymore the current flow. This apparent anomaly is a direct consequence of dealing with gapless channels. The potential distribution along

the channel and the Fermi level (red dashed line) for $V_{DS} = V_{DS-A}$, V_{DS-B}, V_{DS-C} and V_{DS-D} are also grouped in the right panel. An initial carrier density decrease when moving in the channel from source to drain for $V_{DS-A} < V_{DS} < V_{DS-C}$ (Fig. 2.3, right panel, figures (A) and (B)) can be noticed. Then, when the potential conditions correspond to those of the Dirac point, the change in the conductivity type (Fig. 2.3, right panel, figure (C)) is observed, followed by a new carrier density increase for higher values of the drain-source voltage (Fig. 2.3, right panel, figure (D)), causing the peculiar second linear region in the output characteristic. As already anticipated, current saturation is required to reach competitive power gain performance and high values of $f_{max.}$ This can be done by opening a bandgap in the channel material, although a degradation in terms of mobility needs to be expected [22].

In the inset of Fig. 2.3, left panel, a typical current-voltage transfer characteristic of a large-area graphene transistor is depicted. Both the carrier density and the carrier type are affected by the voltage drop between the gates and the channel, with large positive (negative) values leading to electrons (holes) accumulation. The two operating regions are separated by the Dirac point, whose position may be influenced by several factors, as already discussed in Chapter 1.

2.1.2 - Evolution of graphene-based transistors

The first proof-of-concept graphene MOSFET by Novoselov et al. [6] made use of a back-gated topology (Fig. 2.4a), with a 300 nm SiO_2 gate dielectric layer and a highly doped silicon substrate as a back-gate. Although useful for proving field effect in graphene, this structure suffered from too large parasitic capacitances, resulting, moreover, not easily integrable with other components. For this reason, a top-gate structure has been designed (Fig. 2.4b) and fabricated for the first time in 2007 [100]. Other solutions have also been adopted, employing a top-gate topology on semi-insulating substrates (Fig. 2.4c). Nevertheless, in all these cases, the subsequent oxide deposition may deteriorate mobility. This drawback can be avoided exploiting local bottom-gate structures (Fig. 2.4d) in which graphene is deposited on the top of both the gate and the oxide layer, although, in this case, a flat graphene deposition can be tricky.

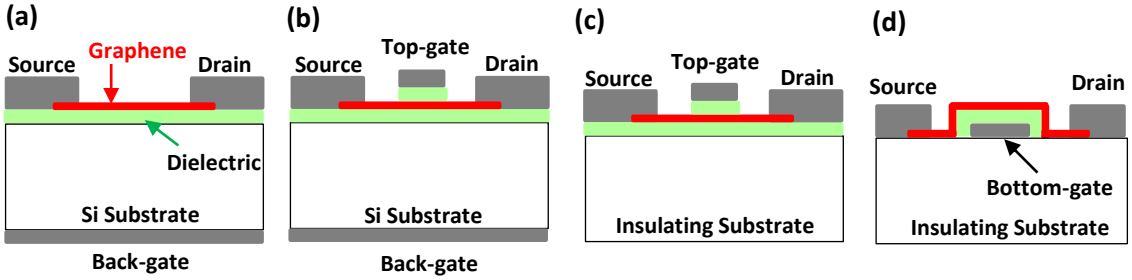


Fig. 2.4 – Some examples of GFETs structures, including: (a) back-gate topology, (b) top-gate topology, (c) top-gate topology on insulating substrate, (d) local bottom-gate topology.

After four years from the first proof-of-principle GFET, the first graphene MOSFET showing a cut-off frequency in the GHz range was reported [101]. It was soon followed by a 350-nm-gate MOSFET on a SiO_2/Si stack and cut-off frequency of 50 GHz obtained through the optimization of the oxide deposition process and the reduction of series resistance (Fig. 2.5, left panel) [102]. Nevertheless, both these solutions made use of mechanically exfoliated graphene, which is known to be not a suitable solution for mass production. In early 2010, a MOSFET from wafer-scale epitaxial graphene was reported (Fig. 2.5, right panel). In this case, epitaxial graphene grown on the Si face of a semi-insulating SiC wafer was used, combined with a 10-nm-thick HfO_2 gate dielectric and a 240-nm-long gate, leading to a cutoff frequency of 100 GHz [103].

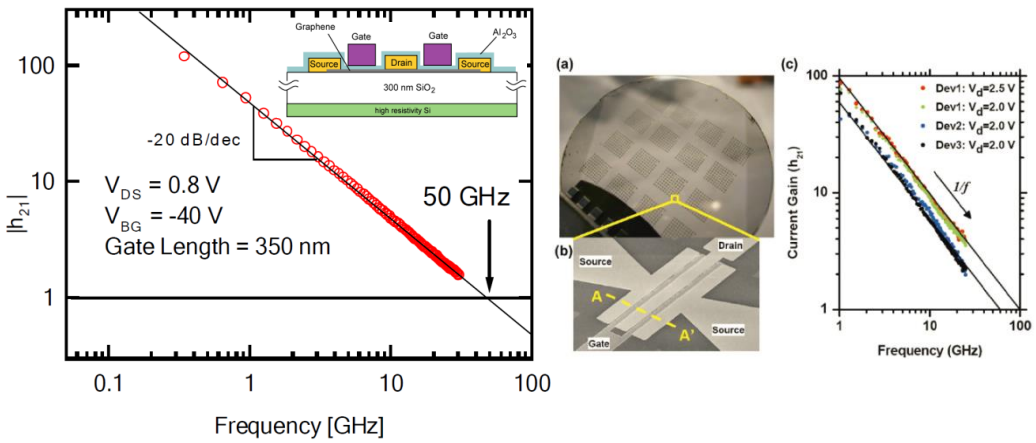


Fig. 2.5 - (Left) One of the first graphene MOSFET showing a cut-off frequency higher than 10 GHz [102]. (Right) The first example of MOSFET employing wafer-scale epitaxial graphene [103].

In 2012, IBM presented 300 GHz MOSFETs based on both wafer-scale CVD grown graphene and epitaxial graphene on SiC, thus surpassing any previous records on any

graphene material (Fig. 2.6a) [104]. In this work, they developed devices with optimized architecture, exhibiting voltage and power gains up to 20 dB. Then, they showed how, also in graphene MOSFETs, cut-off frequency increases by decreasing the channel length *L* according to the typical 1/*L* trend (inset). Subsequently, in 2012, Cheng et al.[105] developed a damage-free transfer process of CVD graphene and self-aligned device structure through which they were able to fabricate 67-nm-gate transistors on glass with an f_T of 427 GHz (Fig. 2.6b). In [106], quasi-free-standing bilayer graphene on SiC substrate with a gate length of 60 nm and ultra-thin gate dielectric have been fabricated by an improved, self-aligned process. This allowed good gate coupling and significant suppression of parasitic parameters, leading to an f_T of 70 GHz and to an f_{max} of 120 GHz, which are the highest extrinsic values reported so far. In addition to conventional planar devices, in which the current flows along the graphene sheet parallel to the substrate, more exotic graphene transistor topologies have also been investigated, like vertical structures, with the current (a tunneling one) flowing normal to the substrate surface. Additional information on these topics can be found in [22].

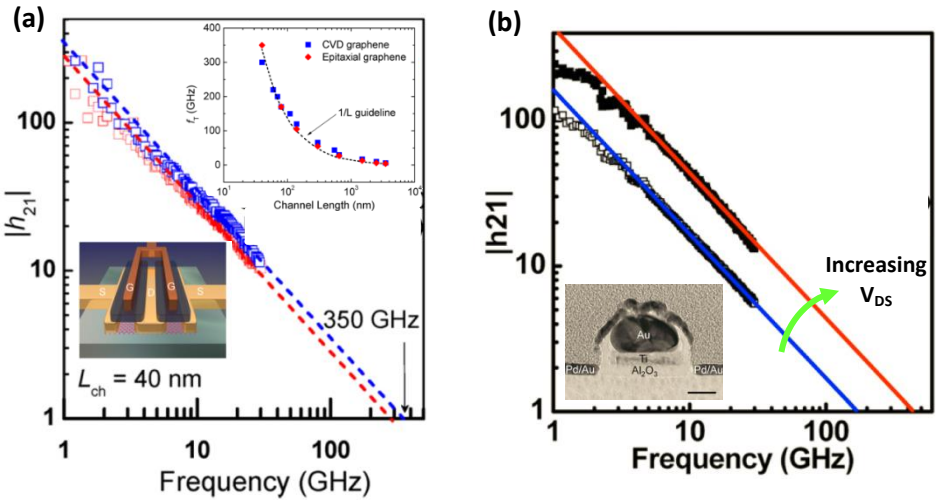


Fig. 2.6 - (a) Small-signal current gains versus frequency of two GFETs, with a 40-nm-long channel, fabricated by IBM, employing epitaxial graphene on SiC. The inset shows the scaling behavior of the cut-off frequency as a function of the gate length [104]. (b) In [105], self-aligned transistors with transferred gate stacks employing CVD graphene have been fabricated, reaching a cut-off frequency higher than 400 GHz.

2.2 - Graphene photonics

2.2.1 - Overview

Graphene electronic properties introduced in Chapter 1 have clearly an influence also on its optical characteristics. The massless, two-dimensional particles behavior of electrons in graphene leads to a consistent, wavelength-independent, optical absorption for normal incident light below 3 eV [44]. More in detail, applying the Fresnel equations in the thin film limit to single layer graphene, the transmittance *T* is found to be ~ 97.7%. Since graphene incident light reflection settles around 0.1%, the optical absorption of each single layer can be estimated ~ 2.3% (that is, the absorption coefficient α is ~ $7 \cdot 10^5$ cm^{-1}, much higher than conventional semiconductor materials). These values are valid over the entire visible spectrum, while they grow proportionally to the number of layers [107] (Fig. 2.7a, b). In particular, the absorption spectrum has a quite flat trend from 300 nm to 2500 nm, showing a peak in the UV region around 270 nm [108]. High light transmission coefficient and low sheet resistance suggest the use of graphene as a transparent conductive electrode for a plethora of applications, like solar cells and detectors, flat panel displays, touch screens and OLEDs. For the sake of clarity, Indium Tin Oxide (ITO), which is the most common choice for the above-mentioned devices, has a sheet resistance < 100 Ω/□ and an optical transparency lower than 90%, besides being expensive and brittle [109]. On the other hand, graphene, with sheet resistance values as low as 30 Ω/□ for the same optical transparency, has proved to be feasible [63] (Fig. 2.7c). In addition, having a high absorption coefficient over a wide wavelength interval and a zero bandgap semiconductor nature, allows graphene to be potentially employed as a wide spectral range detector, unlike what normally happens to more conventional semiconductors, which are transparent to photons having energy smaller than their bandgap (Fig. 2.7d). For example, Si-based photodetectors are limited to visible light sensing, due to the high Si bandgap, which prevents its use for IR detection, while materials currently used for longer wavelengths suffer from both expensive and complex fabrication processes. Another advantage of graphene over the other materials is the potential high operating bandwidth, a property that has important

consequences in the use of graphene-based devices for high-speed data communications. This aspect relates once again to graphene high carrier mobility and high saturation carrier velocity, which allow fast extraction of photogenerated carriers, and it also benefits from the peculiarity of having both electrons and holes with almost the same high mobility values. Transit time limited bandwidth of graphene photodetectors has been calculated to be 1.5 THz [110]. Although the maximum bandwidth would be limited by the capacitive delay associated with the parasitic components, a value of 640 GHz has been found, which is almost four times the transit time limited bandwidth of a 200 nm thick InGaAs layer used as photodetection material [110].

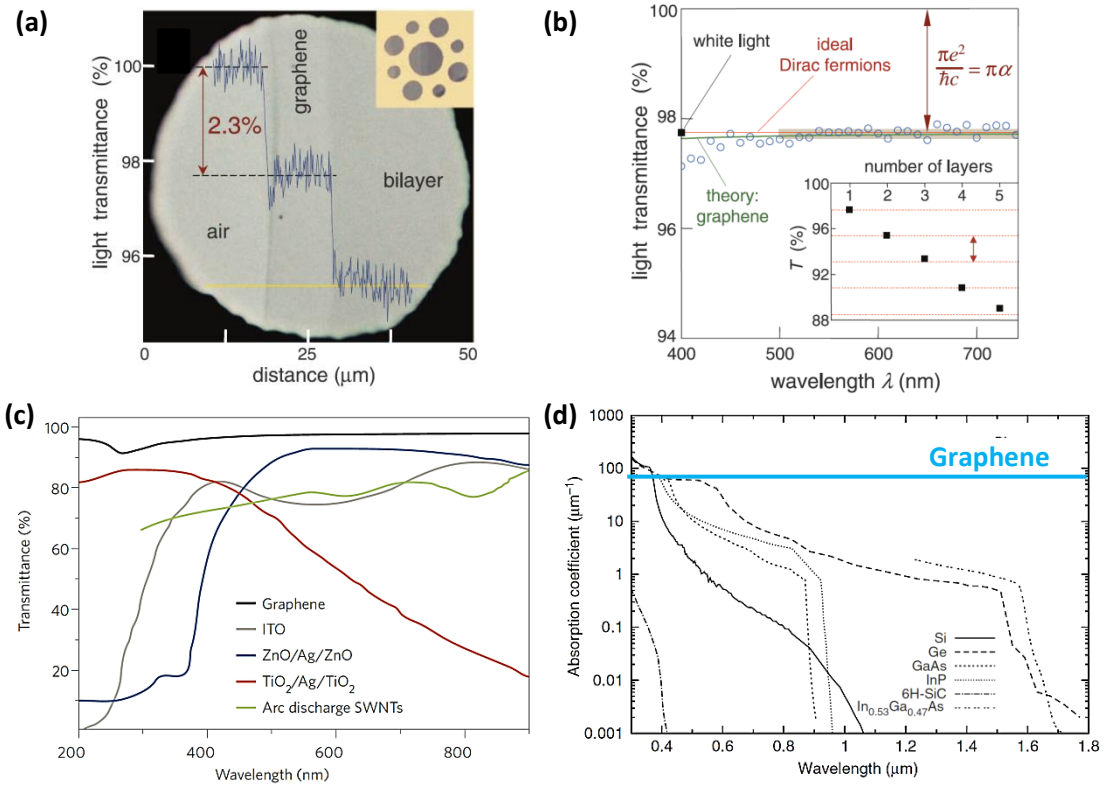


Fig. 2.7 – (a) Micrograph of a 50 μm aperture covered with both single layer and bilayer graphene showing the intensity of transmitted white light (blue scan) along the yellow line [107]. (b) Single-layer graphene transmittance spectrum (open circles) compared with ideal Dirac fermions and theoretical studies. The inset also shows the transmittance of white light as a function of the number of graphene layers [107]. (c) Comparison between transmittance spectra of graphene and different transparent conductors (SWNTs denotes the Single-Walled carbon Nano Tubes) [108]. (d) Comparison between absorption coefficients of graphene and common semiconductors [111].

It is important to point out that the ~ 2.3% single layer graphene absorption coefficient, although impressive for a one–atom thick material, is not sufficient for competitive photodetection applications. Moreover, the zero bandgap nature, essential for broadband detection, leads to a short lifetime of excitons, which is unfavorable for the exciton separation itself. These characteristics cause the responsivity values of pure single layer graphene to be limited to a few mA/W [112]. Nevertheless, several ways to overcome these limitations can be found, as it will be shown later.

As well-known from theory, the main mechanism on which photodetection and optoelectronic applications are based is the conversion of absorbed photons into an electrical signal. Different principles through which this process can be done in graphene have been reported, like photovoltaic, photo-thermoelectric, bolometric and photogating effects (Fig. 2.8), and they will be briefly described in the next section [112], [113]. It is important to underline here that other mechanisms may also apply in photodetection, depending on the type of graphene-based device, and that, quite often, more than one process can be thought to be involved in the detection mechanism.

2.2.2 - Mechanisms enabling photodetection in graphene

Photovoltaic (PV) current generation relies on the separation of photogenerated electron-hole pairs caused by a built-in electric field applied at the junctions between p-type and n-type doped regions of graphene or between differently doped sections [113]. The same effect could definitely be obtained through a source-drain bias voltage although this solution is generally undesired, due to the high dark current related to the graphene semimetal nature [112], [113]. The doping causing the built-in field may be generated exploiting different approaches, such as: the work-function difference between graphene and the contacting metals [114], [115], a local chemical doping [116] or electrostatically, through the use of split gates [115], [117].

Considering the first case, it has been demonstrated [118] that an intimate contact between graphene and a metal allows the Fermi level to be shifted in a remarkable way since the density of states in the vicinity of the neutrality point is low (Fig. 1.2b) due to the linear energy-momentum relationship in graphene [112].

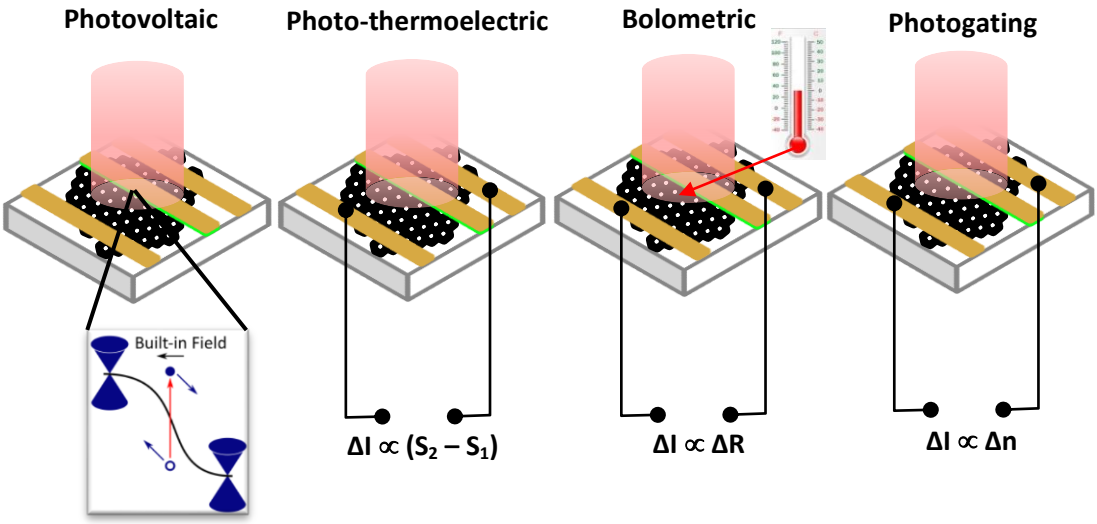


Fig. 2.8 – Main mechanisms involving photodetection in graphene (adapted from [113]).

Of course, if an external gate bias is applied, doping tuning can be performed according to the applied voltage, while, in the case of the metal-graphene junction, the doping typology of the contacted region is fixed (that is, p-type for metals having a work-function higher than the 4.45 eV of the intrinsic graphene). It is useful also to point out that the photovoltaic component is important only near the charge neutrality point where it determines the sign of the overall current [119].

Photo-Thermoelectric Effect (PTE) can also play an important role due to the significant hot-carrier assisted transport in graphene. The reason for that can be explained in these terms: due to the strong e-e interactions in graphene [120], photoexcitation of e-h pairs causes a fast heating of the carriers. However, due to the high graphene optical phonon energy (~200 meV) [121], electrons cooling by acoustic phonons is highly inefficient, causing hot carriers created by the incident radiation to remain at a temperature T_e, higher than that of the lattice, for many picoseconds [113]. Therefore, the PTE is basically a Seebeck effect in which photogenerated hot electrons cause a photovoltage $V_{PTE} = (S_1 - S_2)\Delta T_e$, where $S_{1,2}$ are the Seebeck coefficients in the two graphene regions having different doping and ΔT_e is the electron difference temperature between the two regions [122]. Application of the thermoelectric theory leads to an estimate of a significant thermoelectric photocurrent close to the Dirac point, while, away from that, the effect is expected to be less significant due to the reduced electrochemical potential asymmetry with increasing Fermi level [119].

In the case of the bolometric effect, heating associated with the incident photons produces a change in the transport conductance. In other words, this mechanism manifests as the dependence of conductivity on temperature. The thermal resistance (R_h = dT/dP, where T is the temperature and P the optical power) and the heat capacity C_h define the quality of a bolometer with the former giving an indication on its sensitivity and the latter on its response time ($\tau = R_hC_h$). The small volume for a given area and the low density of states cause graphene to have small values of C_h, while the inefficiency of the electrons cooling process by acoustic phonons leads to high values of R_h. This means that fast and highly sensitive bolometers are in principle feasible employing graphene. Of course, since in the bolometric effect a change in conductance is sensed and there is no direct current generation, an external bias is needed, while there is no need of introducing p-n junction (i.e., bolometric effect can be exploited on homogeneous graphene). Photoresponse due to bolometric mechanism can be expressed as: $\Delta V = I_{DC}\Delta R = I_{DC}(dR/dT)\Delta T$, where I_{DC} is the above-mentioned DC current applied [113]. It dominates, in general, the photocurrent contribution away from the Dirac point where the bolometric coefficient $\beta(V_G)$, defined as $\beta(V_G) = \Delta I(V_G)/ \Delta T(V_G)$, is found to be close to zero [119].

As it happens in the bolometric effect, also in the photogating mechanism a light-induced change in the transport conductance is shown. However, in this case, the effect is based on a photo-induced modification of the carrier density Δn, according to the expression: $\Delta\sigma = \Delta nq\mu$, where μ is graphene mobility. Of course, photoconductive gain can be enhanced if using graphene, due to its high charge carriers mobility [113].

Other phenomena, like the plasma-wave-assisted mechanism, need to be introduced to understand properly how graphene-based devices work, for example, in THz detection. I refer to [113] for additional insights on this topic.

2.2.3 - Some graphene-based photonic devices

In the last section of this chapter, an overview of graphene-based photonic devices will be given [112]. I will start with some notes on the design evolution of graphene photodetectors aimed at overcoming the low responsivity limit introduced in the previous section. Subsequently, a fast overview of other possible photonic applications will be given.

First approaches to photoresponse improvement make use of device geometry optimization. For example, by gating with a third electrode a photoconductor, a phototransistor can be made, where the additional vertical bias can be employed to either open a bandgap in bilayer graphene or control the Fermi level in graphene-based material. Then, adding a second gate, areas with different Fermi levels can be induced, which help the carrier transport and the PTE [112]. In a work reported by Ryzhii et al. [123], a device model for dual-gate graphene nanoribbon photodetector for infrared radiation has been studied (Fig. 2.9a). In this case, a combination of a common back gate and a center-only top gate was used to obtain an energy barrier between the center and the edge of graphene, thus facilitating photocarriers transport. Nevertheless, the above-mentioned solutions make use of the same material for the electrodes fabrication and this choice can be harmful, since it can lead to two symmetric and reverse electric fields that hinder the carriers extraction. In [124], titanium and palladium have been employed as electrodes material to form a band profile distribution that helps electrons transport from source to drain (Fig. 2.9b). In the same work, an interdigitated layout has also been employed and this choice helps increasing the effective detector area, since photocurrent is generated at the metal-graphene interface, leading to responsivity of 6.1 mA/W under 1.55 μm irradiation. A proper choice of the substrate can also strongly influence detectors performance. By making use of suspended graphene structures (Fig. 2.9c), this issue can be solved, as reported in [125], in which a higher responsivity (~ 10^{-2} A/W), compared with other PTE-based detectors, has been reached.

Photodetector integration with photonic structures may also be useful in improving responsivity, by the enhancement of light absorption, that is by the increase of the graphene-light interaction path. Different solutions have been proposed to integrate graphene with *ad hoc* structures that help confining photons and increasing

responsivity, like: waveguides (Fig. 2.9d) [126], microcavities (Fig. 2.9e) [127], and plasmonic structures (Fig. 2.9f) [128].

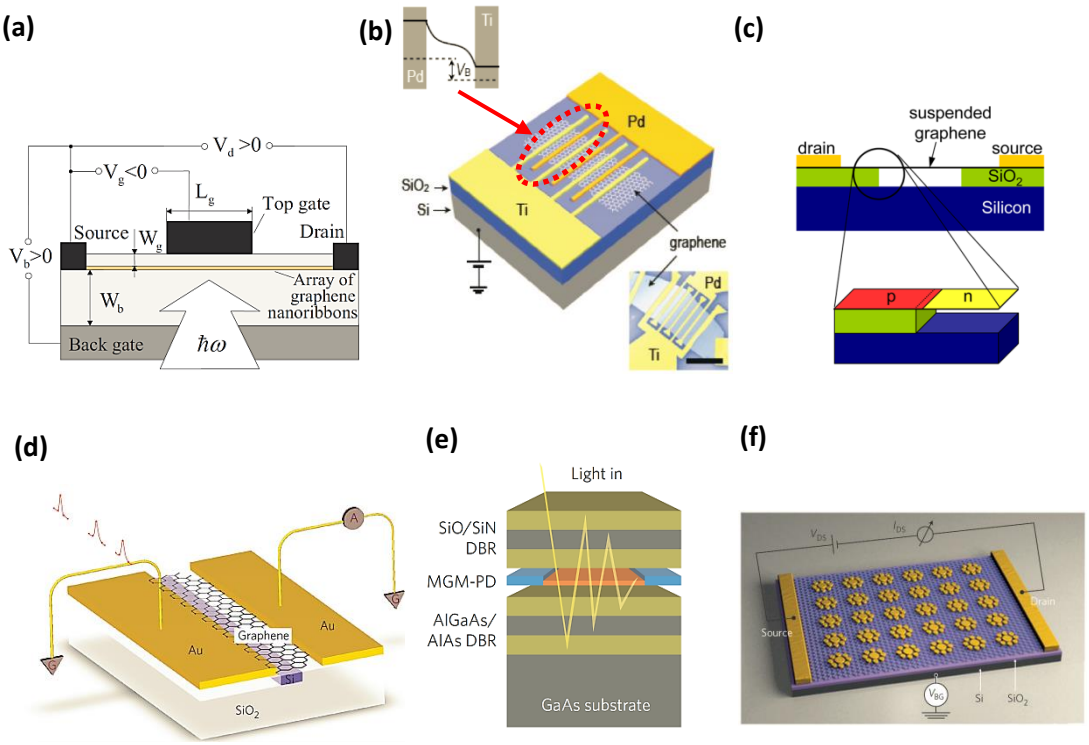


Fig. 2.9 - (a) A device model for a dual-gate graphene nanoribbons IR photodetectors [123]. (b) An interdigitated detector employing two different metals as electrodes material to form a band profile helping electrons transport along the graphene channel [124]. (c) Suspended graphene structures can be used to reduce the influence of the substrate in graphene properties [125]. (d) Waveguides [126], (e) microcavities [127] and (f) plasmonic structures [128] have also been investigated to help photons confinement.

In order to modulate graphene photoresponse and help reducing the main disadvantages of more conventional solutions, other approaches may be found. Among them, it is important to mention the use of: graphene quantum dots, chemically doped graphene and reduced graphene oxide, heterostructures and hybrids (by chemical growth and physical deposition of materials, showing highly light-harvesting properties). Nevertheless, although the above-mentioned approaches represent an effective way to improve both sensitivity and selectivity of graphene-based detectors, this comes at the expense of the operation speed, due to long carrier transfer and trap times caused by the introduction of additional chemical species and treatments. Hence, this kind of devices could be more suitable for application requiring high responsivity but less demanding in terms of response speed (such as sensors) [112]. I refer to [112] for additional insights

on these topics. In Table 2.1 [112], the main properties of the most representative graphene-based photodetectors are summarized.

Graphene multifunctionality can also be exploited to produce many others photonic applications. As already anticipated, low sheet resistance and high transparency make graphene an ideal candidate for transparent electrodes fabrication (Fig. 2.10a). In principle, graphene could replace the current transparent semiconductor-based conductors (i.e., indium oxide, zinc oxide, tin oxide and indium tin oxide) for displays, light-emitting diodes and solar cells [108], [129]. In addition, it could represent an interesting alternative to noble metals as X-Ray beam monitoring electrodes material, due to its high transparency to X-Ray and radiation tolerance, as I will report in the experimental section of this work. In photovoltaic devices, graphene could also be employed as photoactive material, channel for charge transport and catalyst. Other applications include light-emitting devices (Fig. 2.10b), flexible smart windows (Fig. 2.10c), touch screens (Fig. 2.10d), antenna-coupled terahertz detectors (Fig. 2.10e), saturable absorbers, as well as optical modulators and frequency converters [108]. A schematic overview of graphene-based photonic applications is reported in Fig. 2.11.

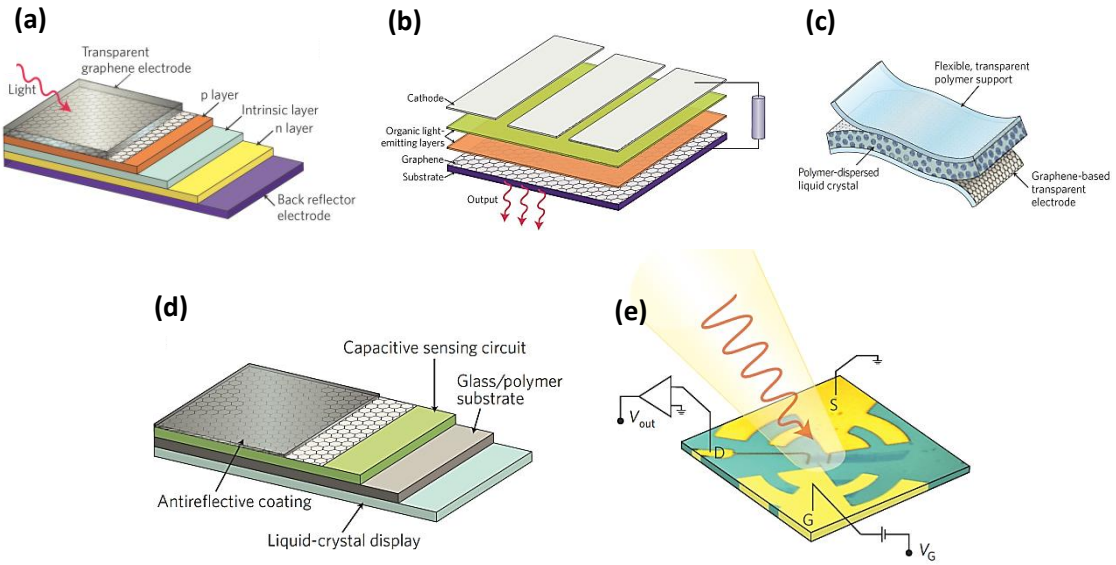


Fig. 2.10 – Additional examples of graphene-based photonic devices, including: (a) inorganic solar cells, (b) LEDs, (c) flexible windows, (d) capacitive touch screens [108] and (e) antenna-coupled graphene THz detectors [130].

Fig. 2.11 – Summary of the main applications of graphene Photonics and Optoelectronics.

Methodology	Material	Mechanism	Operation λ	Responsivity [A/W]	External bias [V]	Remarks
dual-gate	BLG	PV, PC	terahertz and infrared	800	4	$D = 4 \times 10^{12}$ Jones
	BLG	PTE	480—750 nm	~0.0015	0	—
	BLG	photo-bolometric	658—10600 nm	—	—	$t < 1 \times 10^{-9}$ s, ($T < 40$ K)
suspended	TLG[a]	PTE	476.5 nm, 514.5 nm	~0.01	0	—
	SLG (microribbons)	PC, PTE	532 nm	~0.4	0.1	—
integrated with photonic structures	BLG (microcavity)	PC	830—900 nm	0.021	2	—
	BLG (waveguide)	PC, PV	1450—1590 nm	0.108	1	—
	SLG (plasmonic array)	PV	400—700 nm	0.0061	0	—
shaped	GNR	PC	1550 nm	~1	2	$t > 160$ s
	GQD	PC	532 nm	8.61	0.1	$t > 100$ s
chemically doped	RGO	PC	370—895 nm	0.86 (370 nm) 0.7 (895 nm)	10 (370 nm) 19 (895 nm)	$t = 20$—52 s
hybrid and heterostructure	SLG, BLG (PbS QDs)	PC	532 nm, 1050 nm, 1600 nm	$\sim 5 \times 10^7$	5	$D = 7 \times 10^{13}$ Jones, $t > 0.01$ s (532 nm)
	SLG (few-layer MoS_2)	PC	635 nm	10^{10} at 130 K 5×10^8 at RT	0.1	—
uncategorized	SLG (Al_2O_3 passivation layer)	PC, PV	365 nm	10^5 (estimated)	0.1	—

[a] SLG, BLG, TLG: single-layer, bilayer, trilayer graphene. SL, FL: single-layer, few-layer. RT, room temperature; *D*, detectivity; *t*, response time. All the responses unspecified are data at room temperature.

Table 2.1 - Overview of the main photodetectors based on graphene (adapted from [112]).

Chapter 3
Experimental activity

Graphene can be thought as the common framework in which all the experimental activity carried out throughout my 3 years PhD program developed. In particular, two main experimental sections can be distinguished according to the tackled topic. The first one describes my work with Graphene Field Effect Transistors (GFETs), including: fabrications, performed at the Institute of Nanotechnology (INT) of the Karlsruhe Institute of Technology (KIT), design and electro/optical characterizations, performed at the Laboratorio di Elettronica delle Microonde (LEM) of the University of Palermo. The second section, instead, concerns the development of a novel kind of X-Ray detector, based on polycrystalline grade diamond substrate and Reduced Graphene Oxide (RGO) contacts, whose fabrication has been carried out at the Stanford Nanofabrication Facility (SNF) and at the Stanford Nano-Center (SNC), while design and preliminary tests have been performed at the SLAC National Accelerator Laboratory. Great attention has also been paid to the development of a dedicated software to automate the measurement benches and to facilitate the DC/microwave and optical characterizations of GFETs. An overview of the main implemented codes will be reported in Appendix B. Some notes on a supplementary study concerning the ring resonator method employed for the measurement of substrates dielectric constant will be briefly introduced in Appendix A.

3.1 - Graphene for field effect transistors

In this work, three different fabrication runs (namely Run #1, Run #2 and Run #3) have been carried out. Although each one differs from the others for specific details and will be described in a separate dedicated section, some steps concerning the fabrication procedures are the same and will be presented in the next two paragraphs. Details on the layouts employed will be presented instead at the beginning of each specific section. The measurement benches employed for GFETs characterizations will be also

introduced and then, the specific description of the results obtained from each run will be reported.

3.1.1 - Outline of GFETs fabrication

Transistors have been manufactured on C-Plane sapphire [131], [132] (Fabrication Run#1, Fabrication Run #2, Fabrication Run#3) and silicon (Fabrication Run #1) substrates, employing always a dual bottom-gate geometry. Details on the layout employed in each fabrication run will be given in the related specific sections. Due to the importance of reducing fabrication contaminants (see Chapter1), every fabrication procedure starts with the substrate cleaning (Fig. 3.1a). This has been performed by a first sonication step in acetone and isopropanol (IPA) followed by oxygen plasma cleaning (employing a flow of 10 sccm, 100 W power and 100 mTorr) and final hot plate baking at 200 °C for 15 minutes. Then, an eight steps lithography process follows to define devices geometry. This has been performed through a Raith eLine Electron Beam Lithography (EBL) system [133], in a 30 kV acceleration voltage, ~ $7 \cdot 10^{-10}$ mbar gun pressure and ~ $2 \cdot 10^{-6}$ mbar chamber pressure configuration. A 20 μm aperture, combined with a 100 μm writing field and 8 nm step size, has been used for high resolution writing steps (i.e., gates and drains patterning), while a 120 μm aperture, 400 μm writing field and 60 nm step size has been employed when lower resolution could be accepted (i.e., larger masks) and faster writing procedures required. Additional details on the optimization of other EBL system parameters will be given in a separate section. A ~ 200 nm thick, 4.5 wt% Poly(methyl methacrylate) (PMMA) film has been used as positive E-beam resist for all the lithographic steps, with the exception of the thick (300 nm) GFETs pads mask, for which a ~ 900 nm thick, 8 wt% PMMA layer has been required. After every PMMA-coating step, hot plate prebaking at 180 °C for 1 minute has been performed to facilitate the physical removal of PMMA casting solvent and improve resist adhesion on the sample. When EBL needed to be performed on sapphire substrates (that is, insulating ones), ESpacer conductive polymer has been spin coated after every PMMA deposition, followed by substrate N_2 drying and hot plate baking at 100 °C for 1 minute. This additional coating step helps preventing negative charge buildup which can occur on insulating substrates when exposed to an electron

beam, causing beam deflection and, as a consequence, pattern distortion. Although very expensive, ESpacer is a "user friendly" anti-charging method, as it can be easily removed before development by rinsing in water. In our case, ESpacer 300Z from Showa Denko K.K. has been used [134]. PMMA resist development has been performed through Methyl isobutyl ketone (MIBK). In particular, samples have been soaked in 1:3 MIBK:IPA solution for variable times (from 15 s to 45 s), depending on MIBK temperature and electron beam dose. Then, rinsing in IPA and N_2 drying followed. After the substrate cleaning procedure described at the beginning of this section, the lithography process starts with markers and dual gate geometry patterning by EBL followed by metal evaporation and lift-off in acetone (Fig. 3.1b).

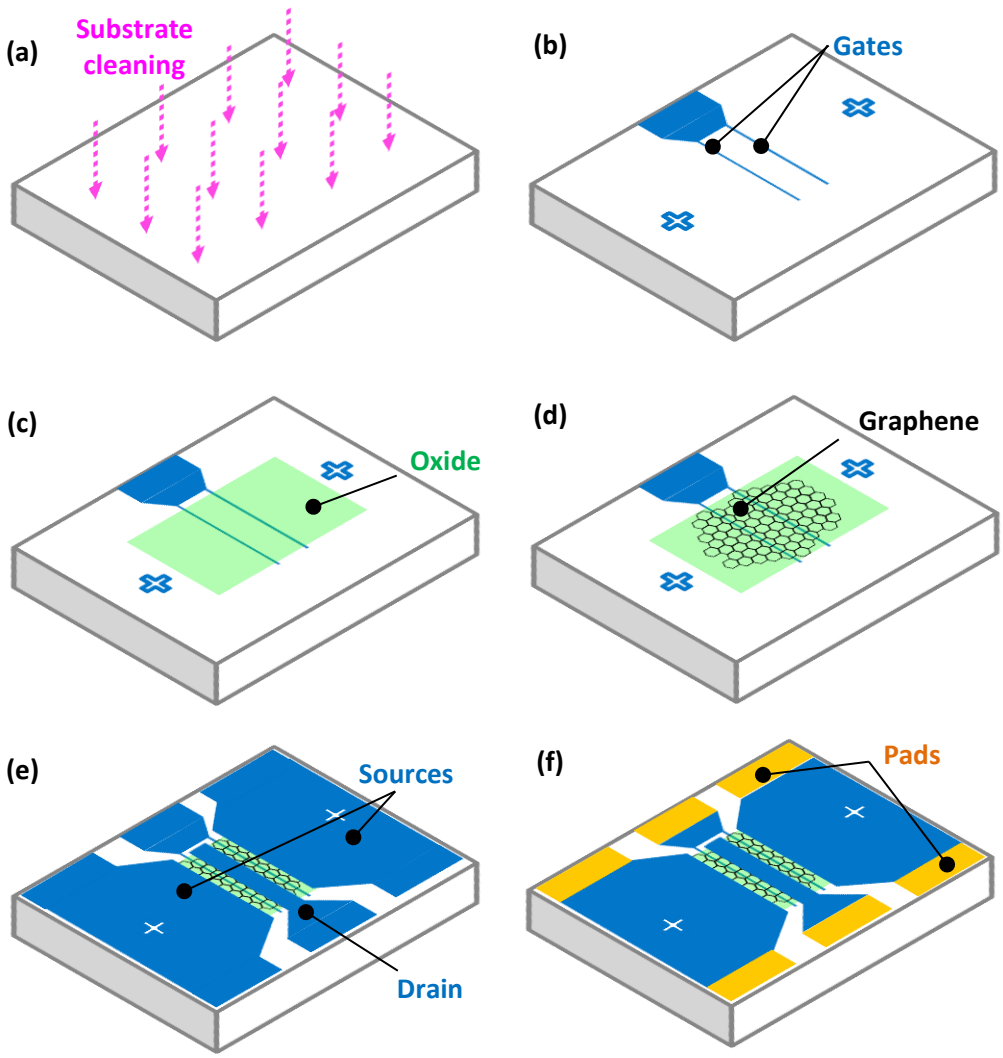


Fig. 3.1 – Outline of GFETs fabrication.

Details on the employed metal evaporation methods and deposition parameters for all the GFETs fabrication runs are summarized in Table 3.1. Then, oxide masks have been patterned and Atomic Layer Deposition (ALD) systems have been used to deposit ~ 10 nm high quality gate oxide (Fig. 3.1c). Scratching of the PMMA/oxide stack along the chip edges before oxide lift-off has shown to be necessary to facilitate acetone penetration underneath, due to the conformal nature of depositions performed by ALD. Additional details concerning this process are reported in Table 3.2.

Once the metal/oxide structure is ready, graphene transfer onto the chip can be performed, followed by graphene mask patterning by EBL (Fig. 3.1d). In particular, two graphene etching masks have been designed. In the former, a 40 μm x 20 μm rectangular mask has been used. In the latter, a meander geometry has been chosen in which rectangular cuts, 0.8 μm wide, have been patterned in those regions corresponding to the metal/graphene interface areas in order to reduce the contact resistance [98]. Micrographs of the above-mentioned graphene masks are reported in Fig. 3.2. Some details on the graphene transfer procedure will be presented in the next section.

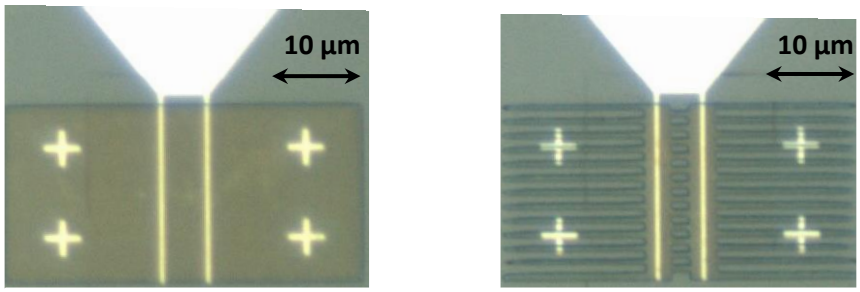


Fig. 3.2 – (Left) Rectangular and (right) meandered graphene etching masks.

Then, graphene patterning has been performed by Reactive Ion Etching (employing 15 sccm of O_2 at 30 W and a chamber pressure of 60 mTorr) for ~ 1 minute. After that, source and drain structures have been patterned and then metal deposition and lift off in acetone followed (Fig. 3.1e). Finally, contact pads have been deposited (Fig. 3.1f).

Run #1

	Metal	Thickness [nm]	Method	Rate [nm/s]
Gate	Ti	5	E-Beam	0.03
	Pd	40	E-Beam	0.12
Source/Drain	Ti	5	E-Beam	0.03
	Pd	100	E-Beam	0.12
Pads	Cr	5	Thermal	N/A
	Au	300	Thermal	N/A

Run #2

	Metal	Thickness [nm]	Method	Rate [nm/s]
Gate	Ti	5	E-Beam	0.03
	Au	40	E-Beam	0.12
Source/Drain	Ti	5	E-Beam	0.03
	Au	100	E-Beam	0.12
Pads	Au	300	E-Beam	0.12

Run #3

	Metal	Thickness [nm]	Method	Rate [nm/s]
Gate	Cr	3	E-Beam	0.02
	Pd	50	E-Beam	0.15
Source/Drain	Ti	3	MBE	0.008
	Al	50	MBE	0.12
Pads(*)	-	-	-	-

(*) No pads deposition has been possible due to a failure in the E-Beam evaporator.

Table 3.1 – Main deposition parameters employed for electrodes fabrication.

Run#	Oxide	Precursors	Cycles	Thickness [nm]	ALD System
1	Al_2O_3	TMA/H_2O	160 at 100°C	11	R-200 Advanced [135]
2	Al_2O_3	TMA/H_2O	160 at 100°C	11	R-200 Advanced
	TiO_2	$TiCl_4$/H_2O	220 at 100 °C	13	R-200 Advanced
	HfO_2	TEMAH/H_2O	107 at 120 °C	11	R-200 Advanced
3	Al_2O_3	TMA/H_2O	91 at 90 °C	10	Savannah [136]

Table 3.2 – ALD parameters for gate oxide depositions performed for each fabrication run.
TMA refers to Trimethylaluminum, TEMAH to Tetrakis(dimethylamido)hafnium.

3.1.2 - Graphene transfer process

In this work, monolayer CVD-grown graphene films have been used for GFETs fabrication. They have been provided by Prof. Jang and Prof. Ahn from Yonsei University, on SiO_2/Si substrates after being grown on copper foils and then transferred on the SiO_2/Si wafer [137]. Then, an additional transfer procedure is needed to transfer graphene film on the final target substrate. Great care is required during this technological step since it can strongly influence final graphene properties. An overview of graphene transfer procedure from the starting SiO_2/Si substrate to the target chip is depicted in Fig. 3.3. As it can be noticed, a combination of wet and dry transfer techniques has been used.

The transfer procedure has been performed as follows:

- A 800 nm PMMA layer is spin coated on top of the starting chip (Fig. 3.3a);
- After scratching the edges, the chip is soaked in a 1 mol NaOH water solution to etch the SiO_2 layer underneath the graphene film (Fig. 3.3b, Fig. 3.4). Just before the SiO_2 layer has completely dissolved, the chip is put in ultrapure distilled water;

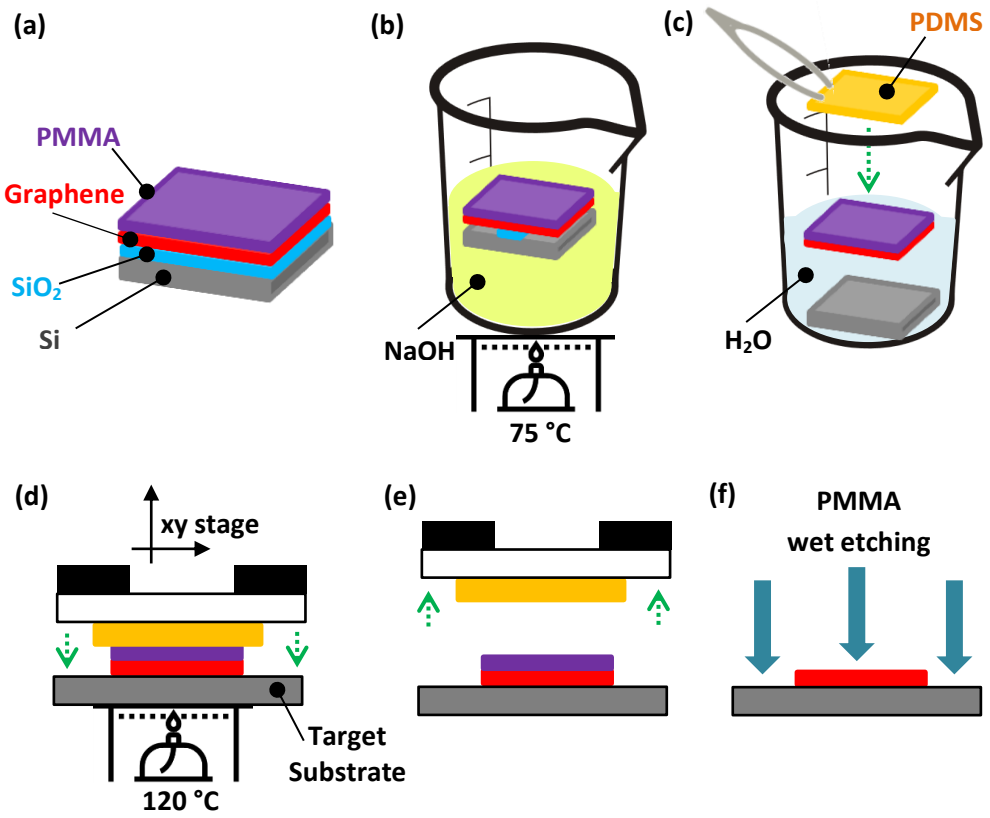


Fig. 3.3 – Overview of graphene transfer procedure from the original Si/SiO_2 support to the target substrate.

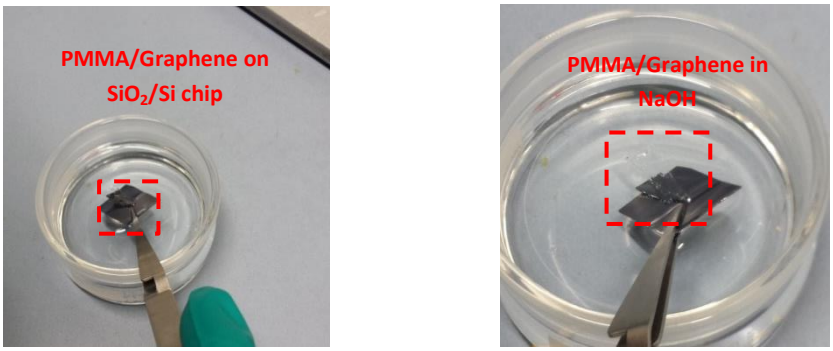


Fig. 3.4 – The PMMA/graphene film deposited on top of SiO_2/Si chip is soaked in a NaOH water solution (left) to facilitate SiO_2 etching and, consequently, the separation from the support substrate (right).

- Once in water, the PMMA/graphene is gently stirred to help the separation of the assembly from the Si support. A flexible PDMS substrate is used to "fish" the PMMA/graphene assembly and, then, the PDMS/PMMA/graphene stack (now simply called "the stack") goes through an overnight drying (Fig. 3.3c, Fig. 3.5);

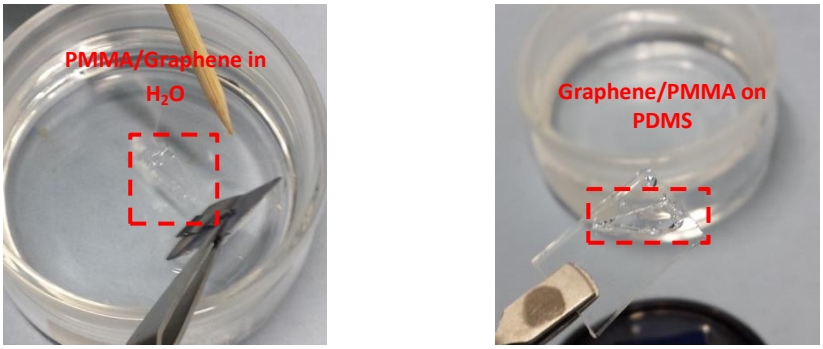


Fig. 3.5 – Once PMMA/graphene has been almost completely removed from the original substrate, the chip is gently stirred to help the separation from the Si support (left). Then, a flexible PDMS substrate is used to "fish" the PMMA/graphene assembly (right).

- The target substrate is fixed into a microscope stage, heated up to 60 °C and then the stack is aligned on it;
- Once the stack is put on top of the target substrate, the microscope stage is heated up to 120 °C and both the stack and the substrate are left in contact for 10 minutes (Fig. 3.3d);
- The stack is lifted up, leaving the PMMA/graphene assembly on top of the target substrate (Fig. 3.3e);
- The substrate is cleaned in acetone and IPA to remove the PMMA layer while leaving the graphene film on top of it (Fig. 3.3f).

3.1.3 - Graphene film characterization

Raman spectroscopy has been employed to provide a fast, non-destructive analysis on graphene films after the transfer procedure. In Fig. 3.6a, a typical Raman spectrum of graphene deposited on top of the gate/oxide stack is shown. In fig. 3.6b, instead, the spectrum is measured outside the patterned graphene area after undergoing the O_2-plasma reactive ion etching cycle. The distinctive G (~ 1587 cm^{-1}) and 2D (2680 cm^{-1}) peaks shape shown in Fig. 3.6a confirm the quality of the transferred monolayer graphene [138], while the flat spectrum reported in Fig. 3.6b proves the effectiveness of the etching recipe. In Fig. 3.6c, from [139], the same characterization has been reported for graphene transferred on top of the three different oxides employed during GFETs Fabrication Run #2 (*i.e.*, Al_2O_3, TiO_2 and HfO_2 respectively).

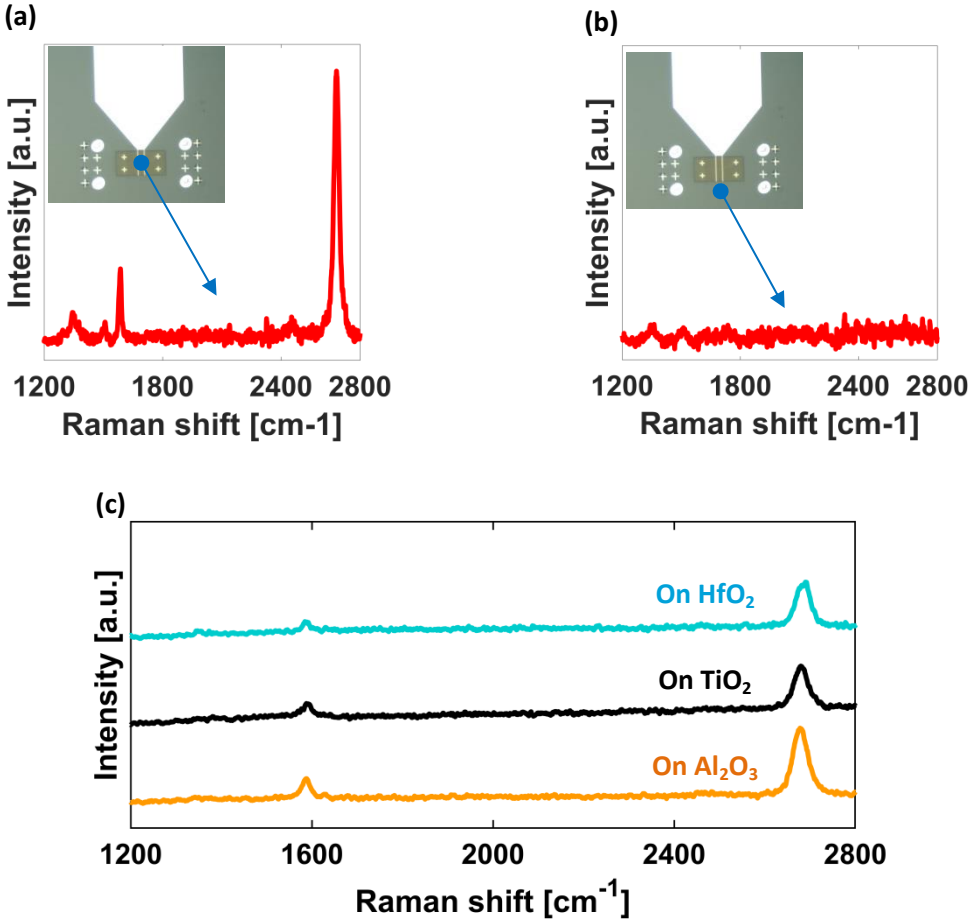


Fig. 3.6 – (a) A typical Raman spectrum of the employed graphene films after the transfer procedure, showing the distinctive G and 2D peaks, and (b) after the etching process. The dots in the arrows give a generic indication of the point where the spectra have been collected. In (c), from [139], Raman spectra of graphene deposited on top of the different oxides employed during the Fabrication Run #2 are also reported.

3.1.4 - Some notes on E-Line parameters optimization

A wrong choice of E-Line parameters (like aperture, writing field size, dose, etc.) may strongly influence the final device geometry. Moreover, when several subsequent lithography steps are required and several devices need to be written for each step, misalignment issues can also make EBL writing tricky. In our case, an automatic alignment procedure has been performed for each lithography step. During this process, the system, after a first raw manual alignment, performs some automatic E-beam line scans in the x- and y- directions, in order to find the user-defined markers (i.e., alignment crosses). A threshold-based algorithm, aimed at detecting light intensity change is then used to exactly determine the crosses location and to properly perform the writing field alignment (Fig. 3.7a). Markers position choice can potentially help this procedure. In our work, layouts with different positions of the most inner markers (i.e., the ones used to align the gate and the source/drain masks) have been tested to find the best alignment capabilities of the EBL system in our operating conditions.

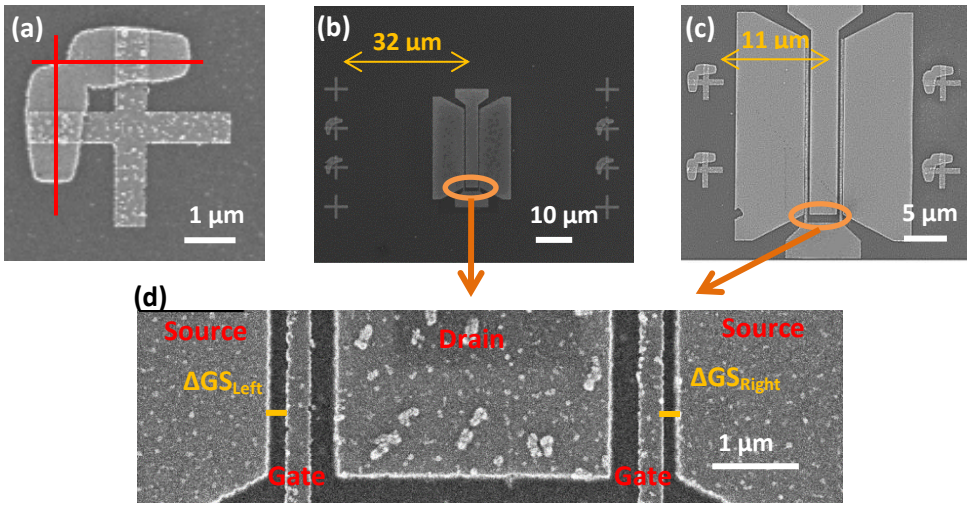


Fig. 3.7 – (a) A typical marker employed during the EBL writing field alignment procedure in which the system performs automatic scans (red lines) to locate the user-defined alignment crosses. (b) and (c) show two different markers locations tested to minimize misalignment issues. In (d) a detail of the GFET active region considered to evaluate writing field misalignment is reported.

The shift between the left and right gate/source distances (ΔGS_{Left} and ΔGS_{Right}, respectively) has been considered as the misalignment measurement, that is $\Delta Shift$ =

$|\Delta GS_{Left} - \Delta GS_{Right}|$ (Fig. 3.7b-d). In particular, the location of the above-mentioned markers has been moved from 32 μm to 11 μm (Fig. 3.7b, c). Nevertheless, no less than ~ 50 nm misalignment error (i.e., ΔShift) has been found. This limit is assumed to be related to both the high aspect ratio of the layout employed and to some pattern distortions caused by the insulating nature of the substrate employed, despite the use of the ESpacer. In order to guarantee a proper geometries development after PMMA exposure, before starting devices fabrication some E-beam dose tests have also been performed (considering the gate structures, which are the most critical geometries to be exposed). As example, some results are grouped in Fig. 3.8.

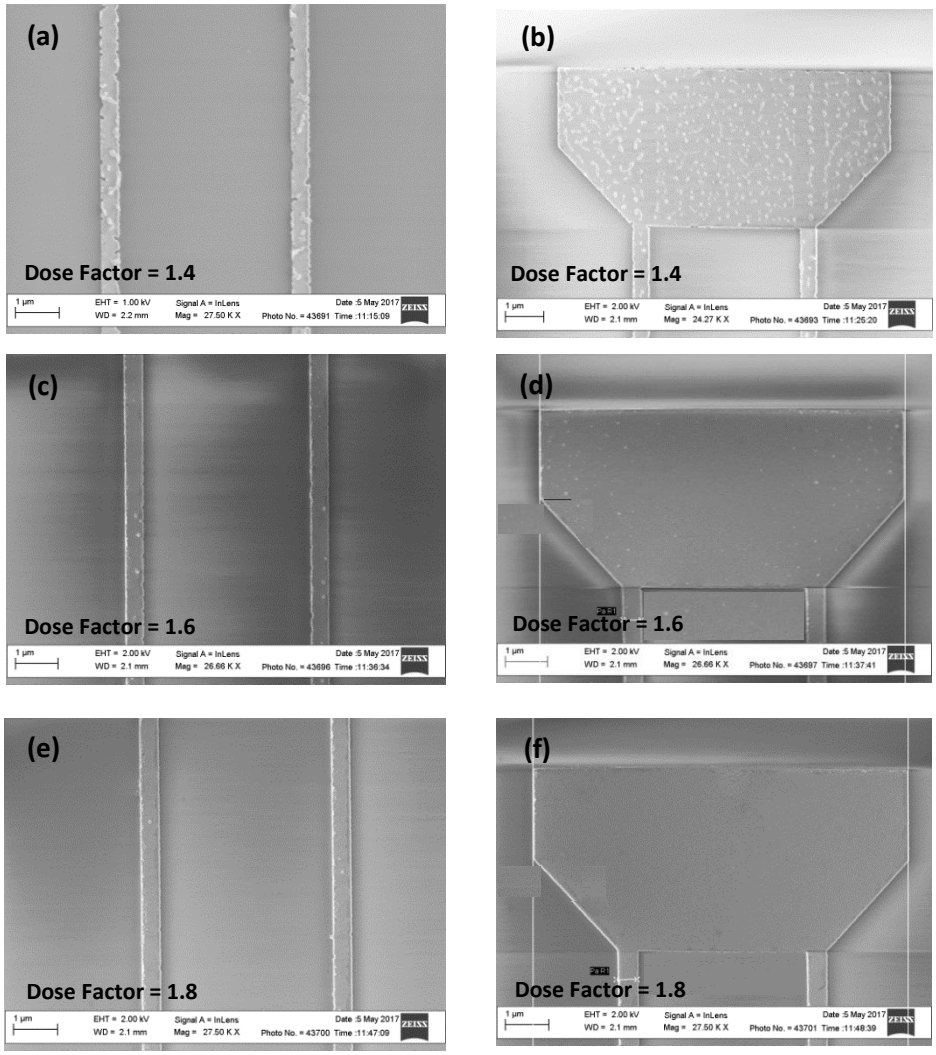


Fig. 3.8 – An example of E-beam dose optimization performed before the beginning of every fabrication run to guarantee a proper development after PMMA exposure. (a), (c) and (e) depict the gate fingers in the middle of the channel while (b), (d) and (f) refer to the end of the gates launcher.

3.1.5 - Measurement set-up description

Both DC/microwave and optical (IR) characterizations have been performed on the fabricated transistors. Details on the specific results for each fabrication run will be presented in subsequent relevant sections. In this paragraph, a description of the employed measurement set-up will be given. A multifunctional bench has been developed at LEM to satisfy the requirement of evaluating flexibly both DC/microwave and optical responses of our transistors. A schematic of the complete set-up is reported in Fig. 3.9.

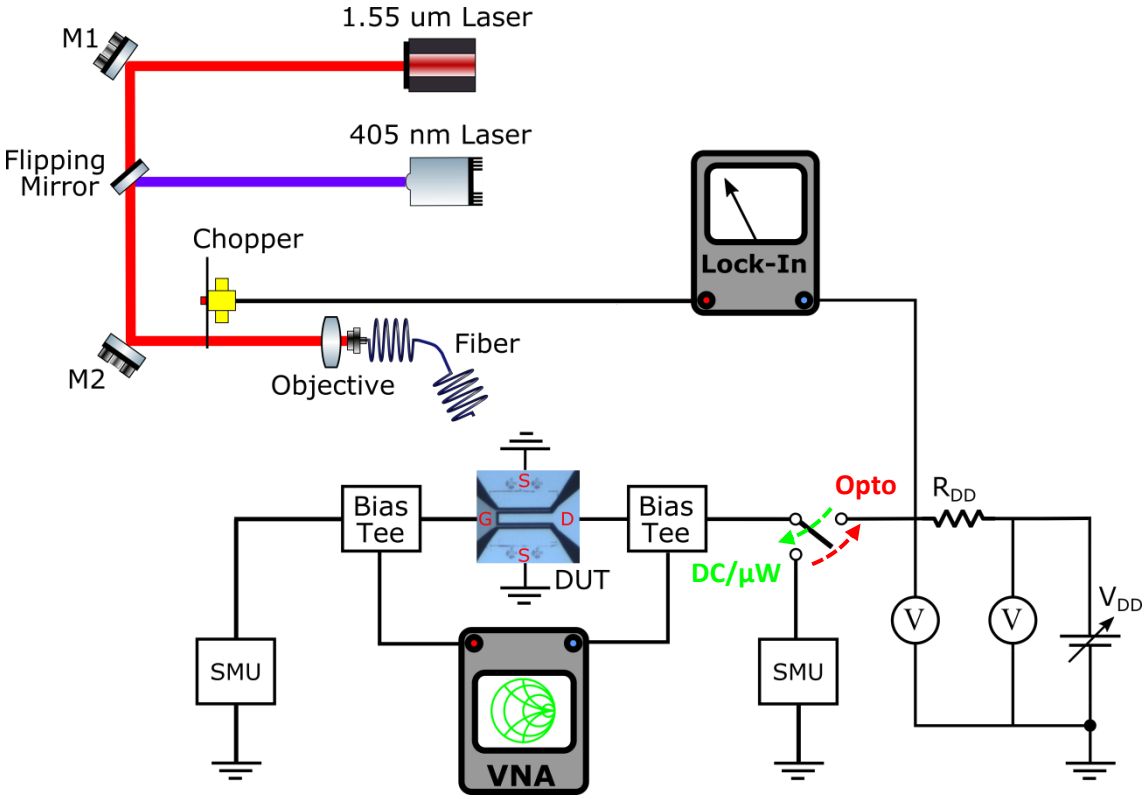


Fig. 3.9 – Simplified diagram of the multifunctional microwave/optical bench developed to perform GFETs characterizations.

First, the DC/microwave section of the bench will be described. A Keysight N5232A Vector Network Analyzer (VNA) [140], combined with a Cascade Summit 9000 wafer-probe station, has been used to measure GFETs Scattering parameters (S-parameters). Measurements have always been performed in the frequency range [300 kHz, 20.003

GHz] employing Cascade ACP40 probes (for Fabrication Run #1 and Fabrication Run #2 devices) and Cascade Infinity probes (for Fabrication Run #3 devices, due to the aluminum-made electrodes) [141] while connection between the probes and the VNA has been guaranteed employing high-stability coaxial cables. Device Under Test (DUT) bias (i.e., gate and drain voltages) has been performed through two Keithley 2400 Source Meter Units (SMUs) [142] as well as the measurements of both gate and drain DC currents. Separation between DC and RF sections has been obtained employing two external bias-tee networks from Pulsar [143].

The optical part of the bench has been implemented in order to perform IR optical characterization of GFETs simultaneously to the DC/microwave measurements. A 1.55 μm erbium fiber laser (IPG Photonics ELT-1-CL-SF-LP [144]) has been used as optical source. Once aligned, the IR beam has been first chopped at 667 Hz and then coupled, through an Edmund DIN 20 microscope objective, into a single mode optical fiber whose output facet has been placed at a distance of ~ 1.5 mm from the DUT. A 405 nm laser diode has been used to permit the desired laser spot centering on the DUT. To this purpose, the fiber end has been attached to a micrometric positioner by Suss Microtech. When the measuring system is switched into the optical characterization configuration, the drain bias is applied through a battery-resistance (V_{DD}-R_{DD}) combination. This arrangement allows to reduce the low-frequency AC noise level with respect to the one typically associated to a digital SMU and to develop (through the appropriate choice of R_{DD}) the desired optically-induced AC signal to drive the lock-in amplifier. In particular, a Stanford Research System SR830 dual-phase unit [145] was adopted, with the reference synchronization signal obtained from the optical chopper. The photocurrent can then be calculated as the ratio between the measured photovoltage and the R_{DD} resistance value. A photograph of the complete measurement bench is reported in Fig. 3.10a. In Fig. 3.10b, instead, a detail of the optic fiber placed between the coplanar probe tips is shown. The IR beam spot size has been calculated analytically [146] and a value of 5.3 μm has been found. Then, the beam spot area shining on the sample (0.065 mm^2) has also been estimated by calculating the free space propagation profile of the beam starting from the output facet of the fiber and for a distance equal to the one between the fiber end and the DUT.

A set-up allowing temperature-controlled measurements, in the range [10 °C, 70 °C] has also been developed. This was implemented by making use of a Peltier cell, attached to the wafer probe-station plate, and by putting the DUT on top of it. An optical-fiber thermometer touching the DUT border has been employed to accurately determine the chip temperature. A photograph of the above-mentioned set-up is reported in Fig. 3.10c.

To control in an automated manner all the parameters required for a complete transistor electro/optical characterization (bias voltages/currents, impinging optical power, substrate temperature, etc.), an IEEE-488 bus and a PC-based master unit has been adopted. For its operation, a set of purposely developed HTBasic software programs was implemented. This choice significantly reduces the time required to perform the many setups/acquisitions implied by these extensive DUT characterizations and improves reliability of the great amount of collected data.

Additional auxiliary HTBasic software modules and MATLAB scripts have also been developed to post-process the raw measured data and help the user having global indications on devices performance (evaluation of device global figures of merit, optimal bias regions, etc.). Additional details on the above cited HTBasic bench-automation software modules will be reported in Appendix B while some notes on the preliminary required VNA calibration will be given in Appendix A.

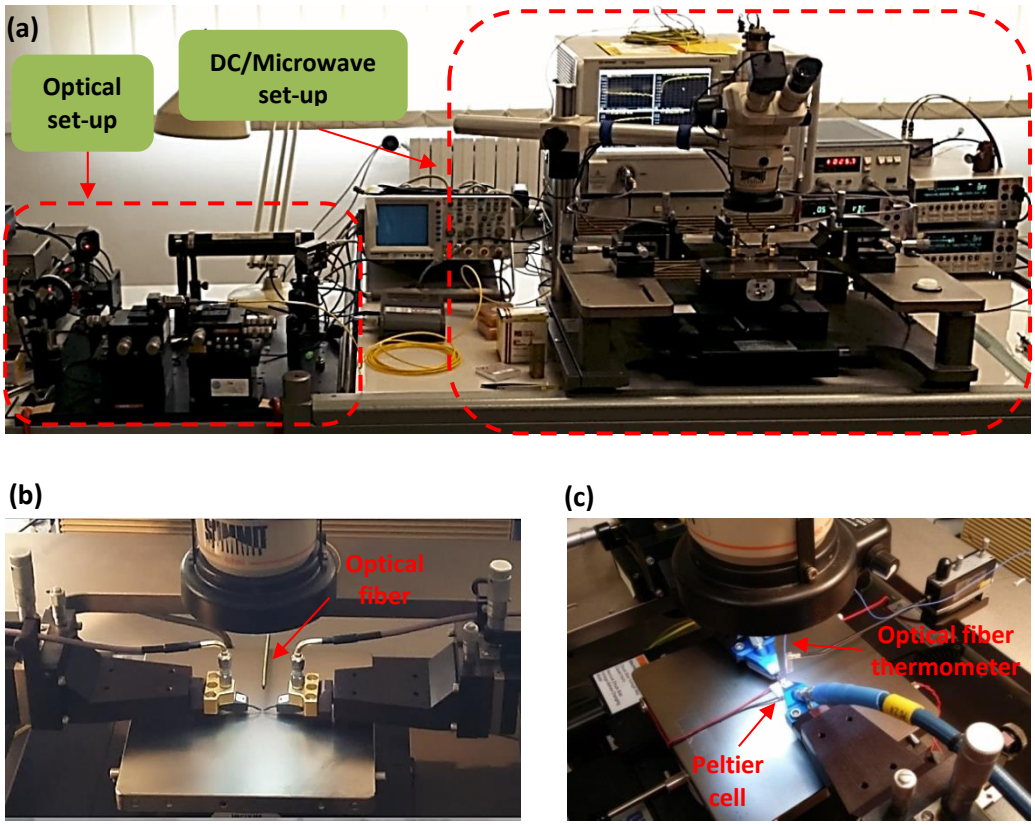


Fig. 3.10 – (a) Photograph of the microwave/optical bench developed at LEM. (b) Detail of the microwave probes employed to contact the transistors and of the optical fiber used to illuminate the sample. (c) Detail of the Peltier Cell and of the optical-fiber thermometer employed for preliminary temperature-controlled measurements.

3.2 - GFETs Fabrication Run #1

3.2.1 - Motivation

During GFETs Fabrication Run #1 (FR #1), the influence of both the substrate material and the layout symmetry/asymmetry have been investigated. It is well known that the substrate choice can strongly affect final devices performance. This is true also for graphene-based devices, in which the interactions graphene-substrate may strongly deteriorate graphene intrinsic characteristics. As already described in the first chapters, Si/SiO_2 has been widely employed as a support material for devices employing graphene (both for high frequency and photonic applications), due to several advantages. First, Si/SiO_2 substrates allow effective modulation of GFETs channel conductivity through the use of simple, low cost, back-gate structures. Silicon substrates also offer enhanced optical contrast, a property that turns out to be useful when dealing with graphene transfer procedures under microscope view. Si/SiO_2 stacks are also slightly affected by negative charge buildup occurring during E-beam lithography steps thus making unnecessary the usage of conductive polymer prior to the exposures. Finally, focusing on graphene photonics, Si allows the fabrication of guiding structures that, in principle, can help improving detectors responsivity, as shown in Chapter 2. Nevertheless, additional aspects need to be taken into account, most of which relates to the intrinsic difficulties of modifying graphene atomic structure as less as possible. From this outlook, Si/SiO_2 substrates may not be the best choice. In addition, as already anticipated in Chapter 1, it has been demonstrated that the interactions between graphene and SiO_2 polar modes can cause significant alterations of graphene properties [27], while additional scattering phenomena caused by the low surface phonon energy and large trap density shown by SiO_2 may deeply deteriorate device performance [147]. In [132], sapphire was proved to be a more valid solution. Its low losses, high dielectric constant and high thermal conductivity [148], in fact, make it an interesting candidate for microwave electronics although its high energy gap suggests that a worse performance is expected for optoelectronic applications. Moreover, its higher surface flatness, compared with Si/SiO_2 substrate, should guarantee a better graphene

uniformity across the chip. Due to our interest in both microwave and photonic properties of graphene, in FR #1 GFETs have been fabricated on both a 330-nm-thick SiO_2 deposited on top of a p-doped 525-μm-thick Si wafer and on a 330-μm-thick sapphire [131] substrate. Both chips have been fabricated simultaneously, thus ensuring constant processing conditions. Moreover, in this fabrication run, a comparison between symmetric and asymmetric GFET layouts has been carried out. In such context, symmetry refers to the gate/source (ΔGS) and gate/drain (ΔGD) distances. In other words, for "asymmetric layout" I denote a layout in which ΔGS and ΔGD are different (details will be given in the next section). In previous works [132], [139], transistors have always been fabricated employing the same values for both spacings, while in non-graphene FET technology a larger width between gate and drain contacts is often used, to reduce the gate drain capacitance and improve the high-frequency performance (see Appendix A for more details on this topic). Nevertheless, due to their peculiar principles of operation, which make graphene-based transistors quite different from conventional devices, the influence of the layout asymmetry in GFETs has been experimentally investigated.

3.2.2 - Chip design

For FR #1, a dual local bottom-gate has been chosen as GFET structure. The fabrication procedure followed the outline previously described while, for electrodes and oxide depositions, the recipes reported in Table 3.1 and Table 3.2 have been employed. With reference to the device layout, the design reported in Fig. 3.11 has been used for gates, drain and sources electrodes. It consists of two separate sections: an extrinsic part, including source (S) metallizations and gate (G) and drain (D) launchers in tapered coplanar wave guide technology (the red dotted region shown in Fig. 3.11), and an intrinsic part, which comprises the transistor active region and G-S-D electrodes (the black dotted region depicted in Fig 3.11). In this way, the extrinsic part design can be kept constant for all the devices fabricated, including the additional passive structures implemented on chip to help with the de-embedding procedure, as it will be discussed later. The gate- and drain-launchers have been dimensioned by employing a combination of both closed-form (compact) models and 3D electromagnetic

simulations. Substrates parameters values employed in simulations have been validated through the use of an additional set of specifically designed test structures (more precisely a pair of ring resonators), as described in Appendix A. As for the contact pads (symmetrical) spacing and size, their value has been chosen equal to the one employed in the Impedance Standard Substrates (ISS) used for the on-wafer VNA calibration, with the 150 μm pitch Cascade probes adopted (see Appendix A for additional details on this topic). This choice allows to deal with the same parasitic elements of the extrinsic device, independently from the specific DUT to be characterized. Device geometries chosen for fabrication are summarized in Table 3.3, in which the values of the different ΔGS and ΔGD spacings are also reported.

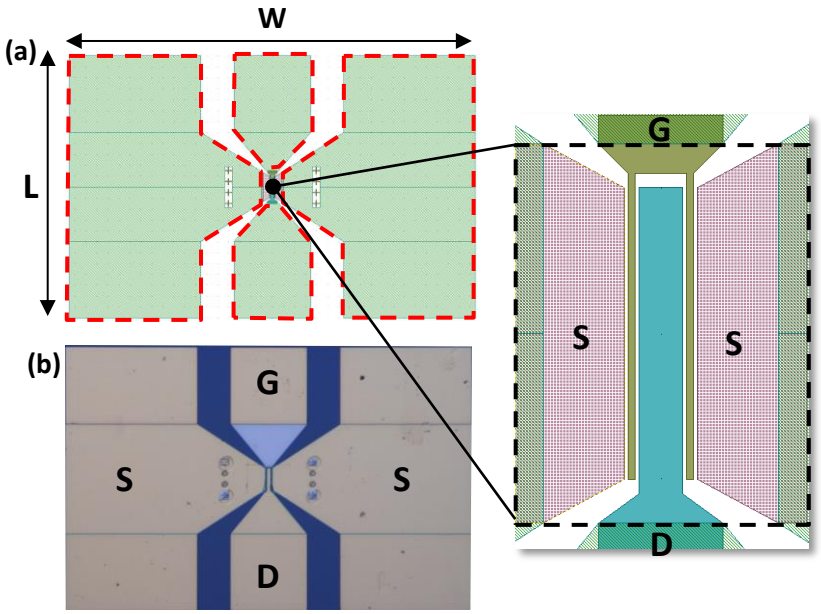


Fig. 3.11 – (a) GFET layout employed during FR #1. The black dotted region depicts a zoom of the intrinsic active device. In (b), a micrograph of the above-mentioned layout is reported. All the transistor dimensions are summarized in Table 3.3.

Eighty devices have been fabricated in each substrate, divided into two main families, according to the gate/source spacing ΔGS (namely, the "A-family", for ΔGS = 0.25 μm and the "B-family", for ΔGS = 0.125 μm). Then, for each family, three groups of different devices have been made, each one showing specific values of the ΔGD width, as summarized in Table 3.3. In addition, a set of test-devices has also been fabricated on the substrate to help with the de-embedding procedures, including: "open", "short" and

"thru" line patterns [149]. Micrographs of the above-mentioned test devices are reported in Fig. 3.12.

Parameter / Group	W	L	Gate Width	Drain Width	Gate Length	ΔGS	ΔGD
A0	370	240	0.25	3	20	0.25	0.25
A2	370	240	0.25	3	20	0.25	0.75
A3	370	240	0.25	3	20	0.25	1
B0	370	240	0.25	3	20	0.125	0.125
B2	370	240	0.25	3	20	0.125	0.5
B3	370	240	0.25	3	20	0.125	0.75

Table 3.3 – Summary of the main transistors physical dimensions (in μm) employed during the FR #1. ΔGS and ΔGD refer to the gate/source and gate/drain spacings, respectively.

Fig. 3.12 – Micrographs of the test-devices fabricated to facilitate the de-embedding procedure, including: (a) "open", (b) "short" and (c) "thru" structures.

3.2.3 - DC/Microwave characterization results

The DC and small-signal AC characterization of the fabricated GFETs have been performed employing the DC/microwave configuration of the integrated measurement bench previously described (Fig. 3.9). Thanks to the purposely-developed control software, both DC and microwave measurements have been carried out at the same time for each bias point in the investigated range of operating conditions. This characteristic turns to be of fundamental importance in order to reduce as much as possible the hysteretic behavior affecting graphene-based devices [39]. Details on the specific time/bias sequences implemented by the control software are reported in Appendix B.

As to the DC characterization, static curves have been collected by sweeping the gate/source voltage (V_{GS}) in the range [-1.25 V, 1.75 V], for the sapphire substrate, and [-0.75 V, 2.25 V] for the Si/SiO_2 substrate, while the range [-1 V, 1.25 V] has been chosen for the drain/source voltage (V_{DS}). These voltage ranges were selected to roughly center the transfer characteristics around each device-specific Dirac point. Simultaneously, S-parameters have also been collected in the frequency range [300 kHz, 20.003 GHz, 401 points log-scaled] and in standard environmental conditions. Figure 3.13 compares both DC and high frequency (in terms of the Short-Circuit Current Gain, |h21|) responses of two representative devices fabricated in sapphire and Si/SiO_2 substrates. In particular, measurements refer to devices belonging to the A2-group although similar relative trend has been found for transistors belonging also to the other groups. Plots shown in Fig. 3.13a depict transfer characteristics, the incremental low-frequency transconductances (g_m) and the output characteristics.

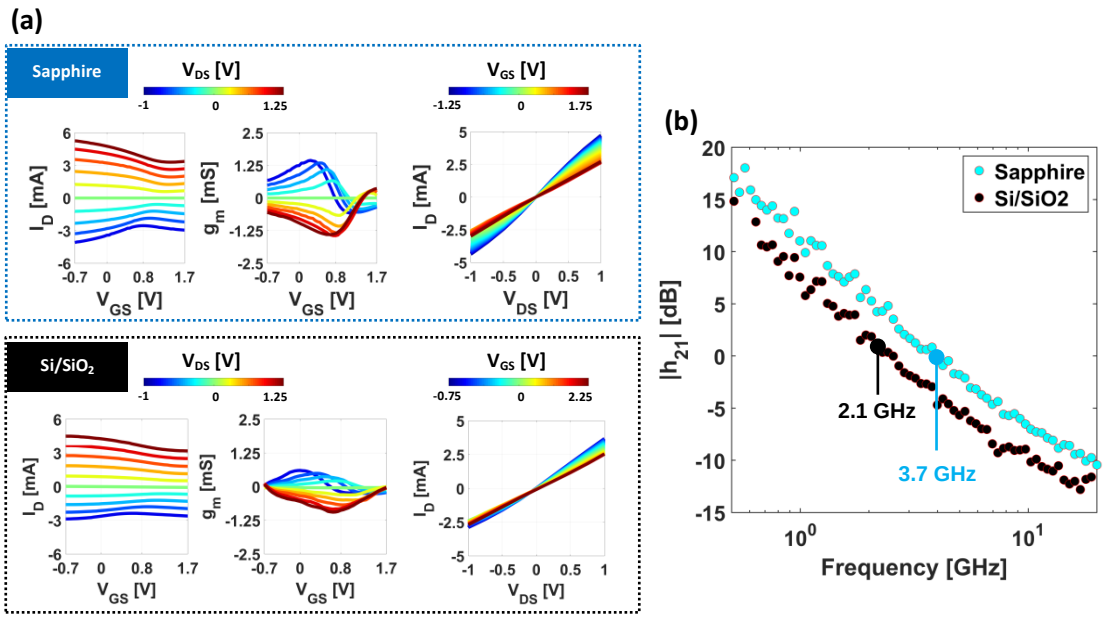


Fig. 3.13 – (a) Transfer characteristics, incremental DC transconductance plots and output characteristics of two representative devices fabricated on sapphire and Si/SiO_2 substrates, respectively. In (b) the related $|h_{21}|$ plots are shown. Graphs refer to de-embedded data.

As it can be noticed, sapphire samples show a more effective drain current modulation through the gate voltage than Si/SiO_2-based devices, as confirmed by the higher g_m (almost double) and the broader fan-spread in the output characteristics. In a subsequent post-processing phase, the Short-Circuit Current Gain ($|h_{21}|$) has also been extracted

from the measured S-parameters and the results, referring to de-embedded data, are reported in Fig. 3.13b. The $|h_{21}|$ plot confirms the better performance of sapphire-based devices which show an average cut-off frequency almost two times higher than GFETs fabricated on Si/SiO_2. The improvement in the high-frequency performance is supposed to be related not only to a higher value of the static transconductance shown by sapphire samples but also to a lower parasitic capacitive contribution offered by the highly insulating sapphire substrate. This can be observed in Fig. 3.14a and b, where s11 and s22 of two representative GFETs, fabricated on both substrates, have been reported, showing an enhanced capacitive behavior of Si/SiO_2 based devices. The same trend is confirmed in Fig. 3.14c, where measurements referring to "open" test structures, fabricated on both substrates, are reported. Notice that, in this case, raw (i.e., not de-embedded) measurements are shown.

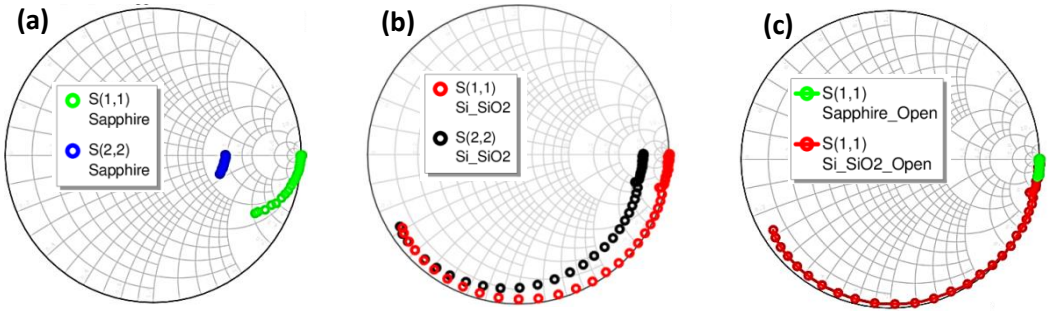


Fig. 3.14 – s11 and s22 parameters of two representative GFETs fabricated on (a) sapphire and (b) Si/SiO_2 substrates, showing the lower capacitive contribution offered by sapphire-based devices. The same trend is confirmed in plot (c), depicting the s11 parameter of "open" test devices made on the above-mentioned substrates. Graphs refer to raw data.

With reference to the investigation of the influence of device asymmetry, measurements refer to devices with different ΔGS and ΔGD spacings, fabricated on sapphire substrates only. Figures 3.15 and 3.16 report DC characterization data for both the A- and the B-families, with depicted measurements referring only to those devices showing the best high-frequency performance for each GFET group. In particular, Fig. 3.15a, b and c show the transfer characteristics, low-frequency transconductance and output characteristics for the A0, A2 and A3 group, respectively. The same measurements, performed for the B0, B2 and B3 groups, instead, have been sorted in Fig. 3.16a, b and c, respectively. A decrease in terms of both the maximum drain current and channel-current modulability through the gate-source voltage is observed, for each GFET

family, when the gate/source, gate/drain asymmetry is increased. This is clear looking at the higher values of g_m and larger spread of the output characteristics of the symmetric structures (Figures 3.15a and 3.16a) with respect to the asymmetric ones (Figures 3.15b,c and 3.16b, c). As reported in Fig. 3.17, cut-off frequencies follow the same trend, with the f_T values decreasing with the increase of the layout asymmetry. This fact confirms that the physics of graphene-based FETs is somehow different from the standard ones, with the gate/drain spacing significantly influencing the device transconductance achievable for a given gate/source spacing.

This phenomenon is observed in both GFETs families, with devices belonging to the B set exhibiting average higher f_T values due to the narrower gate/source spacing.

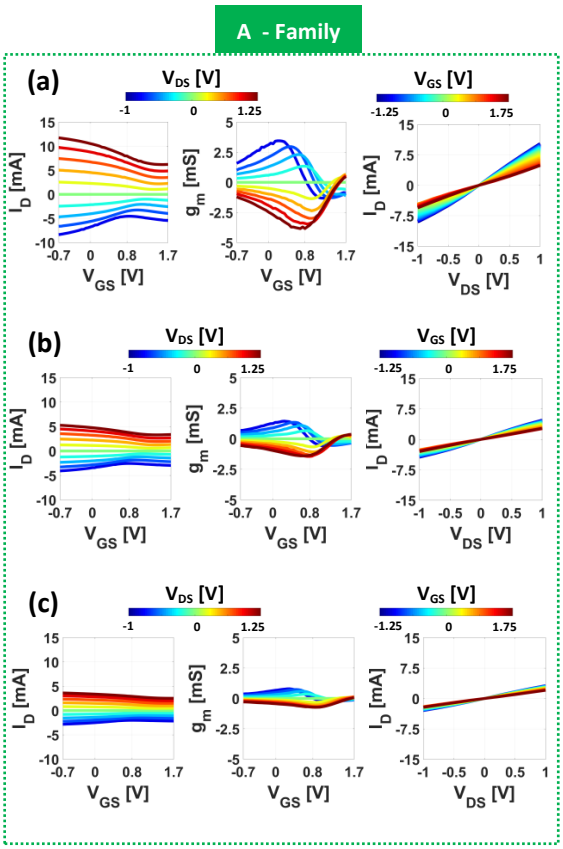


Fig. 3.15 - Transfer characteristics, incremental DC transconductance plots and output characteristics of the best devices belonging to the (a) A0 group, (b) A2 group and (c) A3 group.

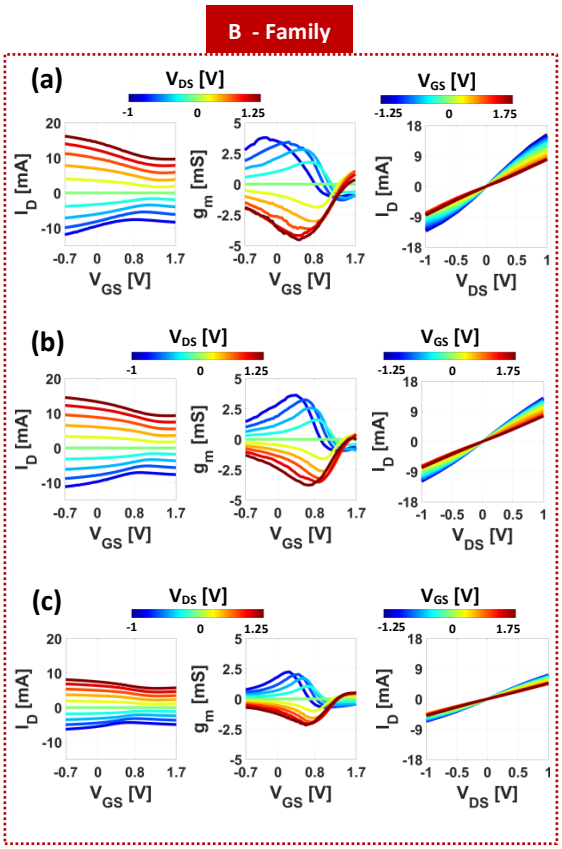


Fig. 3.16 - Transfer characteristics, incremental DC transconductance plots and output characteristics of the best devices belonging to the (a) B0 group, (b) B2 group and (c) B3 group.

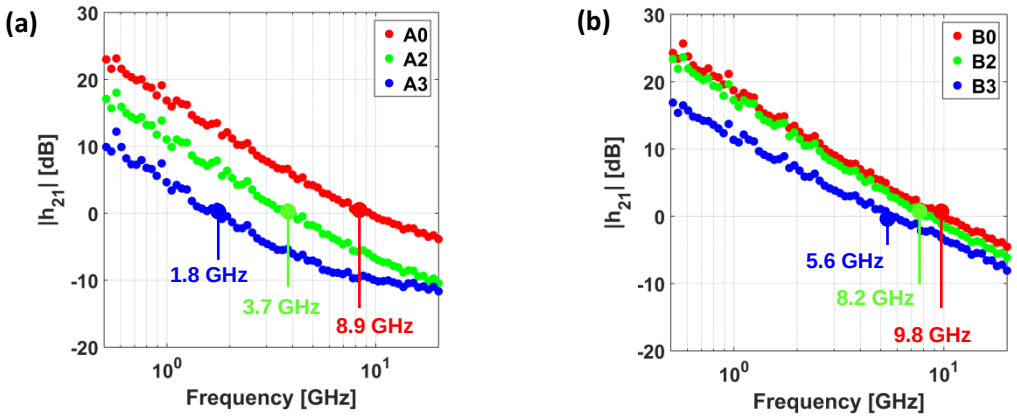


Fig. 3.17 – $|h_{21}|$ plots for the best devices belonging to the (a) A-family and (b) B-family, respectively. Cut-off frequency values are highlighted.

3.3 - GFETs Fabrication Run #2

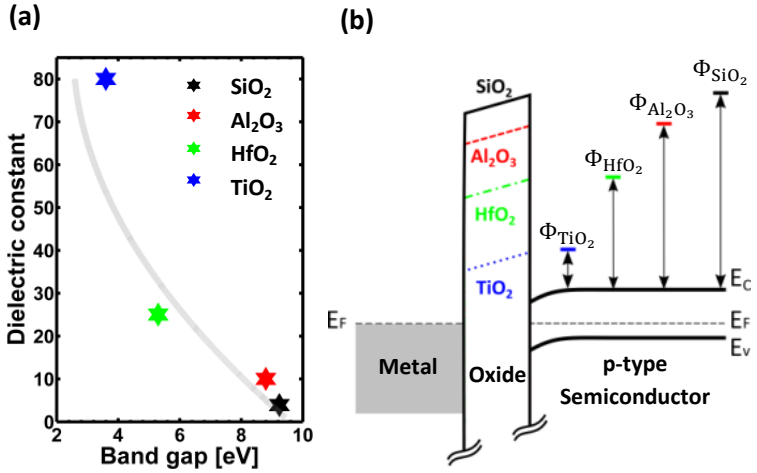
3.3.1 - Motivation

Aim of Fabrication Run #2 (FR #2) is the study of the influence of the gate-isolation dielectric in graphene-based transistors considering both the DC/microwave characteristics and the optical response. It is to be pointed out that all the experimental activity concerning this specific study has been carried out in cooperation with M.A. Giambra, a former PhD student at the University of Palermo, who started working on graphene FETs one year before me [139].

As well-known from theory, the possibility of producing high performance, highly integrated transistors relies on several factors among which the gate dielectric can play a significant role, especially when dealing with high speed devices. In the last years, in fact, the rapid shrinking of transistors dimensions, aimed at improving devices performance, caused both the channel length and the gate dielectric thickness to decrease accordingly [150]. From CMOS technology indeed a reduction of the oxide capacitance (i.e., C_{ox}) is desirable to increase the drive current and, consequently, decrease the average switching time [151]. Also, from conventional MOSFET, it is known that a higher value of the oxide capacitance helps increasing the transconductance and therefore the cut-off frequency too [93]. The most intuitive way of increasing the oxide capacitance is the thickness reduction but this choice is generally

avoided since it leads to an increase of the unwanted leakage current and can decrease devices reliability. For all these reasons, a great interest for the so-called high-κ dielectrics arose during the years, since their use may help designers to increase C_{ox} without acting on the dielectric thickness [151], [152]. Of course additional tradeoffs need to be carefully considered, especially between the dielectric constant and the semiconductor/oxide band offset. A good dielectric, in fact, should guarantee a sufficiently high κ–factor but also a high band offset Φ with the surrounding semiconducting material (to produce low leakage current). Moreover, it should not negatively affect the carrier transport properties of the target substrate and be "friendly" deposited on it. Of course not all these requirements can be met at the same time and a compromise needs to be found (Fig. 3.18a, b). Of course, these arguments can be extended to graphene-based transistors too. More precisely, in this case, additional issues arise from the intrinsic chemical inertness of pristine graphene with respect to the precursors employed for oxides deposition and the difficulties in preserving graphene electronic properties when interacting with other materials.

Accordingly, in this part of the experimental activity, a study of the influence of the gate dielectric material on GFETs DC/microwave performance has been developed. Subsequently, the possible use of our devices as IR detectors has been investigated and the influence of the gate oxide experimentally observed. In particular, three different dielectric materials have been considered, namely: aluminum oxide (Al_2O_3), titanium oxide (TiO_2) and hafnium oxide (HfO_2). This choice relates to the highly different electric and thermal properties shown by the above-mentioned dielectric materials, as reported in Fig. 3.18c, and to the possibility they offer of being easily deposited through ALD systems.



	κ	K_T [$Wm^{-1}K^{-1}$]
Al_2O_3	9	~ 25
TiO_2	80	~ 8
HfO_2	25	~ 1

Fig. 3.18 – (a) Dielectric constant vs. band gap for SiO_2, Al_2O_3, HfO_2 and TiO_2. (b) Energy band diagram for a typical metal/oxide/p-type semiconductor structure showing the different semiconductor/oxide band-offsets (Φ) for the above-mentioned gate dielectrics. (c) Comparison between dielectric constants (κ) and thermal conductivity values (K_T) of Al_2O_3, HfO_2 and TiO_2 (data from [152]–[155]).

3.3.2 - Chip design

For FR #2, dual local bottom-gate GFETs have been fabricated on sapphire substrates [131]. Concerning the single device layout, the design previously described has been used, as reported in Fig. 3.19 for the sake of clarity. Also in this figure, the red-dotted region highlights the extrinsic part (including source metallizations and gate- and drain-launchers) while the black dotted area comprises the intrinsic section with the transistor active region. The contact pads layout has been again chosen coherent with the one implemented in the 150 μm pitch calibration ISS. Devices geometries employed are summarized in Fig. 3.19. Fifty-four active devices, subdivided into three groups according to the employed oxide (Al_2O_3, TiO_2 HfO_2, respectively), have been fabricated on the chip together with a complete set of test-devices, including: “open”, “short” and “thru” line patterns, as described in the previous section (Fig. 3.12). As for the electrodes and dielectrics depositions, the recipes summarized in Table 3.1, 3.2 have been used.

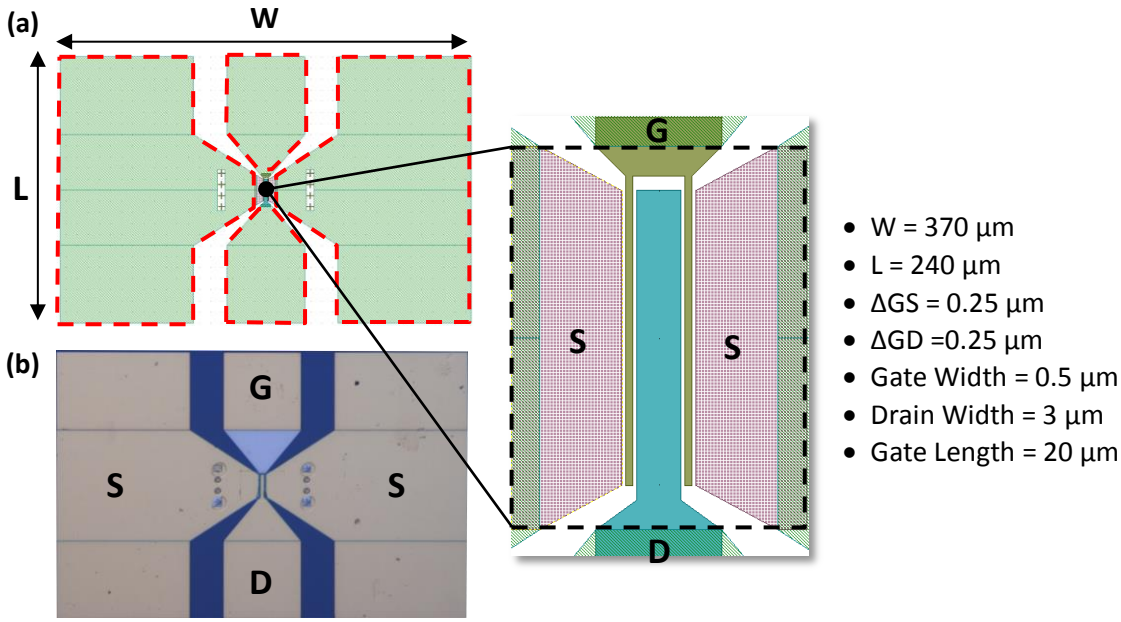


Fig. 3.19 - (a) GFET layout employed during FR #2. The black dotted region depicts a zoom of the intrinsic active device. In (b), a micrograph of the above-mentioned layout is reported. Transistor dimensions are summarized on the right side of the picture. ΔGS and ΔGD refer to the gate/source and gate/drain spacings, respectively.

3.3.3 - DC/Microwave and optical characterizations results

DC and microwave characterization has been performed employing the DC/microwave section of the measurement bench previously described (Fig. 3.9). Also in this case, the static and dynamic characterizations have been executed simultaneously, to guarantee the best possible data coherence and traceability, and reduce influence of hysteresis phenomena. Static curves have been obtained by sweeping the gate/source voltage (V_{GS}) in the range [-1.5 V, 1.5 V] and the drain/source voltage (V_{DS}) in the range [-1.25 V, 1.25 V]. Transfer characteristics of a representative device for each oxide family are reported in Fig. 3.20a-c while the incremental low-frequency transconductance, $g_m = |\partial I_D/\partial V_{GS}|_{V_{DS}=const}$, is reported in Fig. 3.20d-f. As it can be noticed from the position of the Dirac points, all these GFETs show a p-type behavior, while significantly different static characteristics are observed, depending on the gate dielectric employed. In particular, HfO_2-based devices show a wider separation of the curves as a function of V_{DS} as well as a more effective drain current control by V_{GS}.

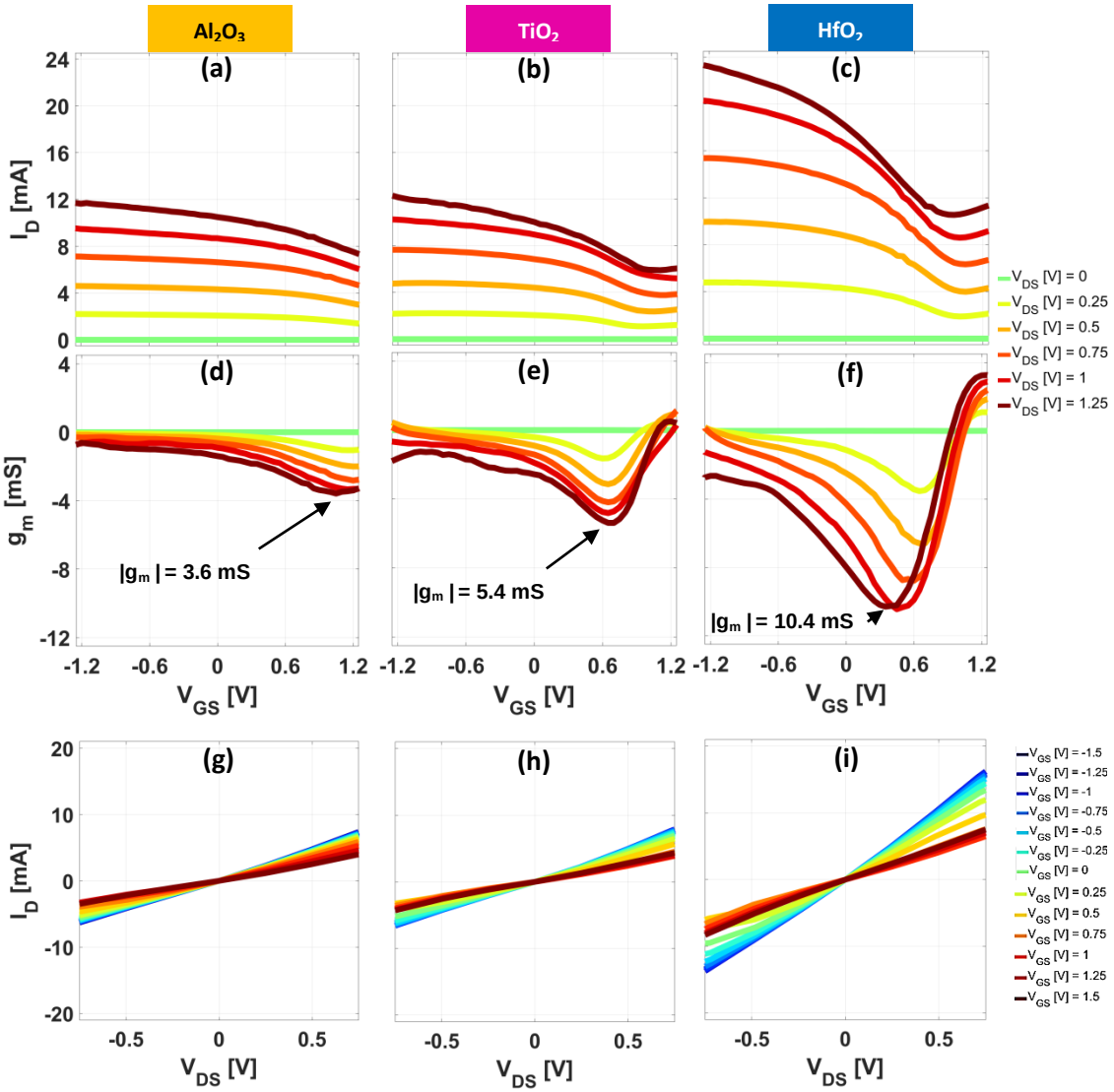
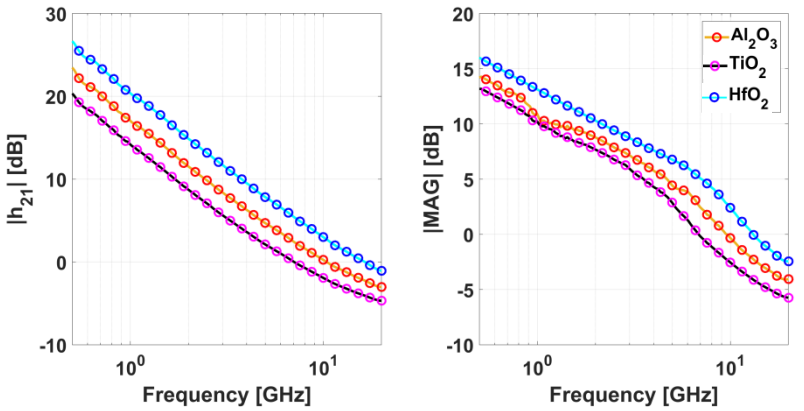


Fig. 3.20 – (a, b, c) Transfer characteristics, (d, e, f) incremental DC transconductance plots and (g, h, i) output characteristics of GFETs employing Al_2O_3, HfO_2 and TiO_2 as gate dielectric.

As a consequence, HfO_2-based transistors exhibit g_m values almost three times higher than Al_2O_3-based devices and two times higher than TiO_2-based devices. On the other hand, no significant improvement in terms of the ON/OFF ratio has been observed, with a maximum value just below 2 obtained in hafnia transistors. GFETs output characteristics are reported in Fig. 3.20g-i, revealing the typical linear behavior of graphene-based FETs for low drain/sources voltages, as discussed in the previous chapter. Again, wider broadening of the output characteristics has been obtained in HfO_2-based devices, as expected from above results. It is to be pointed out that the experimental data obtained confirm that an increase in the gate oxide κ–factor value

alone is not sufficient to guarantee a higher transconductance and, thus, better microwave performance. In fact, the highest values of g_m measured have not been found in TiO_2-based samples. When dealing with graphene, other aspects, mainly related to the quality of the graphene-dielectric material interface, need to be considered, as discussed later in this section. Together with DC measurements, S-parameters have also been collected, exploring the frequency range [300 kHz, 20.003 GHz, 401 points log-scaled] in standard environmental conditions. From them, both the Short-Circuit Current Gain ($|h_{21}|$) and the Maximum Available Gain (MAG) have been extracted for each device and the results compared. The computed average gains (referred to ten identical devices for each oxide group) are depicted in Fig. 3.21. Shown data refer to de-embedded measurements, obtained employing the approach suggested in [149], which makes use of the auxiliary test devices described in the previous section (Fig. 3.12). Gain plots suggest that a significant improvement in terms of microwave performance can be obtained employing HfO_2 as gate dielectric, as demonstrated by the higher values of the low frequency gains and by the higher values of both f_T and f_{max}.



	f_T [GHz]	f_{max} [GHz]
Al_2O_3	10.3	9.4
TiO_2	6.9	6.8
HfO_2	16.5	13.2

Fig. 3.21 – Average short-circuit current gain ($|h_{21}|$) and Maximum Available Gain (MAG) for GFETs employing different gate dielectrics. Maximum values of both the cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) are also reported.

In particular, values of f_T = 16.5 GHz and f_{max} = 13.2 GHz have been obtained for HfO_2-based devices followed by Al_2O_3- and TiO_2-based transistors, as summarized in Fig. 3.21. From DC data, the average contact resistance (R_C) and the field effect mobility (μ) have also been extracted for the devices belonging to the three oxides groups. The results are reported in Fig. 3.22a, b.

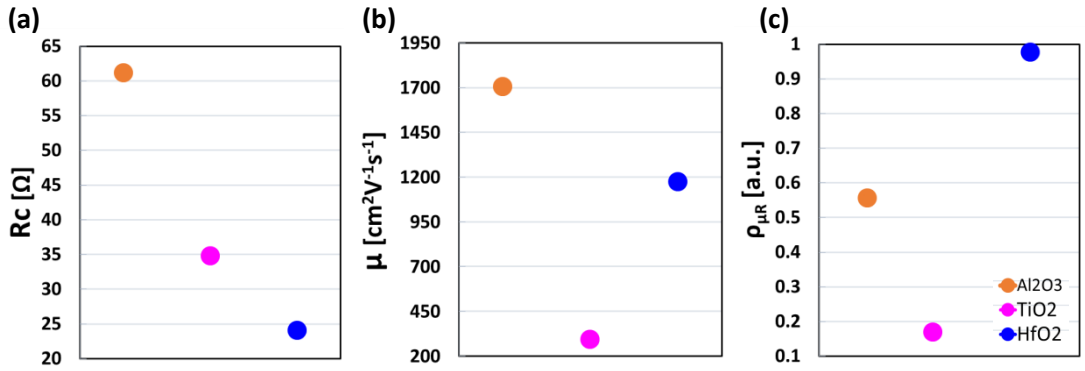


Fig. 3.22 – (a) Average contact resistance and (b) field effect mobility for Al_2O_3, TiO_2, and HfO_2-based devices. In (c), $\rho_{\mu R}$, defined as the ratio between the field effect mobility and the average contact resistance, is depicted, proving the best high frequency performance of HfO_2-based GFETs.

As it can be noticed, Al_2O_3-based devices exhibit the highest contact resistance although showing the highest field effect mobility. The lowest value of contact resistance has been measured, instead, in HfO_2-based transistors together with a mean value of mobility between the three oxides. Conversely, intermediate properties apply for TiO_2-based transistors. Clearly, since both low contact resistance and high field effect mobility are in principle requested, these data suggest that a trade-off needs to be found in the selection of the dielectric material/properties. To this purpose, a specific figure of merit ($\rho_{\mu R}$), defined as the ratio between the field effect mobility and the contact resistance, can be introduced (Fig. 3.22c). Then, by plotting the above defined $\rho_{\mu R}$ as a function of the gate oxide, we can easily come to the conclusion that HfO_2, although having a lower κ–factor than TiO_2, allows the designer to get the best compromise in terms of contact resistance and field effect mobility and, consequently, to obtain the best high-frequency performance.

Together with the study of the microwave response, the possibility of employing GFETs to sense infrared radiation has also been investigated. Although a lower responsivity was expected compared with graphene-based IR detectors described in literature [112], due to the specific microwave-oriented design employed, this approach gave the opportunity to exploit graphene multifunctionality. In particular, the aim of this study was to assess GFETs capabilities of both sensing an incoming 1.55 μm radiation and amplifying the generated electrical signal thus making these devices suitable for

telecom applications. At the same time, a study of the influence of the gate dielectric on the IR photoresponse has been performed.

Photoelectric measurements have been carried out employing the complete set-up previously described (Fig. 3.9), under standard environmental conditions, with the aim of finding the maximum GFETs IR responsivity, as function of both the transistor DC operating point and the gate oxide material. As to the bias ranges adopted for this combined electro-optical characterization, values typical of graphene-based high-frequency transistors have been adopted. In particular, V_{DS} has been varied in the range [0.06 V, 1 V] while V_{GS} in the range [-1.5 V, 1.5 V], roughly bracketing the Dirac point. In a first measurement campaign, the dependence on V_{DS} of the maximum drain/source photocurrent (I_{ph}) generated under laser irradiation, and the one of the mean value of the lock-in current with no laser irradiation (referred as the *noise current*, I_n) has been evaluated. The results referring to Al_2O_3-based devices are reported in Fig. 3.23a. Subsequently, the ratio I_{ph}/I_n has also been calculated, and its trend is reported in Fig. 3.23b. As shown, an initial increase of the photocurrent (blue curve) as a function of V_{DS} is found. Then, starting from $V_{DS} \approx 0.5$ V, a beginning of saturation can be noticed. On the other hand, concerning the noise contribution, an almost linear behavior is shown on the entire voltages interval swept. Consequently, a parabola-like curve is found for the I_{ph}/I_n ratio with a maximum shown at $V_{DS} \approx 0.4$ V.

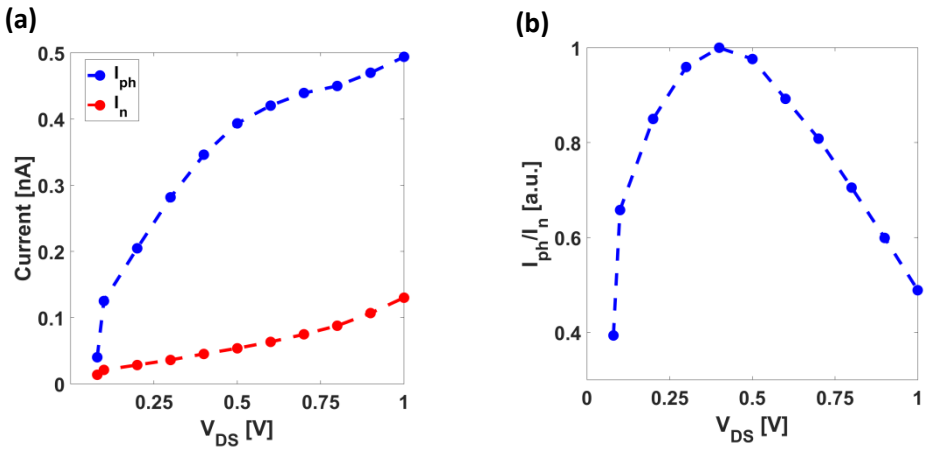


Fig. 3.23 - (a) I_{ph}, I_n and (b) normalized I_{ph}/I_n as function of V_{DS} for Al_2O_3-based devices, at V_{GS} = 0.7 V. An IR laser power of 7 mW was used to shine the sample.

On the basis of this experimental result, the subsequent investigation of the IR response versus the injected laser power (in the range [0 mW, 7.6 mW]), was performed at this

specific drain/source voltage only. Notice that, also in this case, the dedicated bench automation software has permitted to perform simultaneous acquisition of both DC drain current (I_D) and photocurrent (I_{ph}), for each V_{GS} value in the set. The measurement results obtained are reported in Fig. 3.24, where the static transconductance curve (g_m), extracted from the transfer characteristic, is also shown.

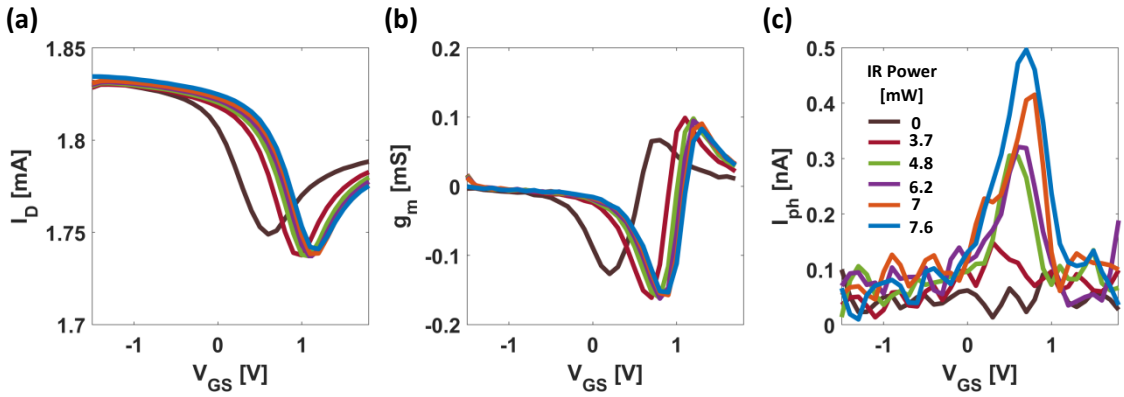


Fig. 3.24 – (a) I_D, (b) g_m and (c) I_{ph} curves as a function of V_{GS} for different values of the IR scan laser power. A drain/source voltage of 0.4 V has been used since the highest value of I_{ph}/I_n is found in this bias conditions.

From Fig. 3.24c, a monotonic increase of GFET photocurrent with the IR laser power shining on the sample is observed, as expected. More in detail, a maximum photocurrent value of ~ 0.5 nA has been measured under 7.6 mW laser irradiation for that bias voltage at which the transistor is found to show the maximum g_m value. A shift of the photocurrent curves is observed (Fig. 3.24c), similarly to the static curves (Fig. 3.24a,b). This behavior can be related to charge injection into the trap sites on the dielectric substrate, charge transfer from neighboring adsorbates and capacitive gating effects, which originate as a result of the alternating forward and backward gate-voltage sweepings [39]–[41], [156]. As for the photo-generation mechanism involved, the effect can be related to a first optical/electrical signal conversion followed by the amplification of the generated signal obtained through GFET transistor effect. No charge carriers are supposed to be provided by the substrate because of the high value of sapphire bandgap (7.3 eV) compared with the 0.8 eV impinging IR laser energy. The maximum photodetector responsivity (R_{max}), defined as the ratio between the maximum photocurrent ($I_{ph,max}$) and the optical power shining on the 40 μm^2 graphene exposed area (*i.e.*, not covered by the drain and source electrodes), has also been estimated.

Taking into account the Gaussian distribution of the beam intensity, R_{max} has been obtained as:

$$R_{max} = \frac{I_{ph,max}}{\text{Optical Power}} = \frac{I_{ph,max}}{\frac{2P}{\pi w^2}\left(\iint_{\substack{\text{Active}\\\text{Area}}} e^{-2\frac{x^2+y^2}{w^2}}\,dx\,dy\right)} \cong 53\ \frac{\mu A}{W}$$

where P is the maximum optical power impinging on the sample (7.6 mW) and w is the 145 μm beam waist ($1/e^2$ radius) on the sample. A value of $R_{max} \cong 53\ \mu A/W$ has been found. As expected, measured responsivity is lower if compared to conventional graphene-based IR detectors due to the microwave-oriented design of our devices which was not optimized for radiation detection.

The same characterization has also been performed on TiO_2- and HfO_2-based devices, finding lower photocurrents and I_{ph}/I_n ratios than those measured for Al_2O_3 samples. In detail, Fig. 3.25 compares the photoresponse of GFETs employing the three different gate dielectrics, together with the corresponding static curves. Drain/source values have been chosen to maximize the I_{ph}/I_n ratios. Optical measurements show that transistors employing Al_2O_3 exhibit the highest photocurrent value when V_{GS} = 0.7 V, followed by TiO_2-based devices. No photoresponse, instead, has been detected in samples with HfO_2, independently on the DC operating point chosen. It has to be noticed that, in case of GFETs used as photo-detectors, a proper choice of the DC bias conditions has to be made to guarantee high sensitivity to the input optical signal. As to the photo-current generation mechanism involved in these photo-detecting devices, we notice a correlation between photocurrent and photo-induced shifts of static drain currents, which we believe to be in favor of photogating effect. The spatial distribution of surface or interfaces trap states, in fact, has been reported to cause the above-mentioned horizontal shifts. Under laser irradiation, trap states can trap photo-generated carriers whose accumulation induces a gate electric field leading to a modulation of the channel conductance [156]. The analysis of both the static drain currents and the photoresponses of our devices allows us to conclude that different interface/trap states configurations are created after transferring graphene on top of the three dielectrics and that the use of Al_2O_3 as gate oxide gives rise to a more effective modulation of the channel conductance under laser irradiation and, consequently, to a higher photocurrent.

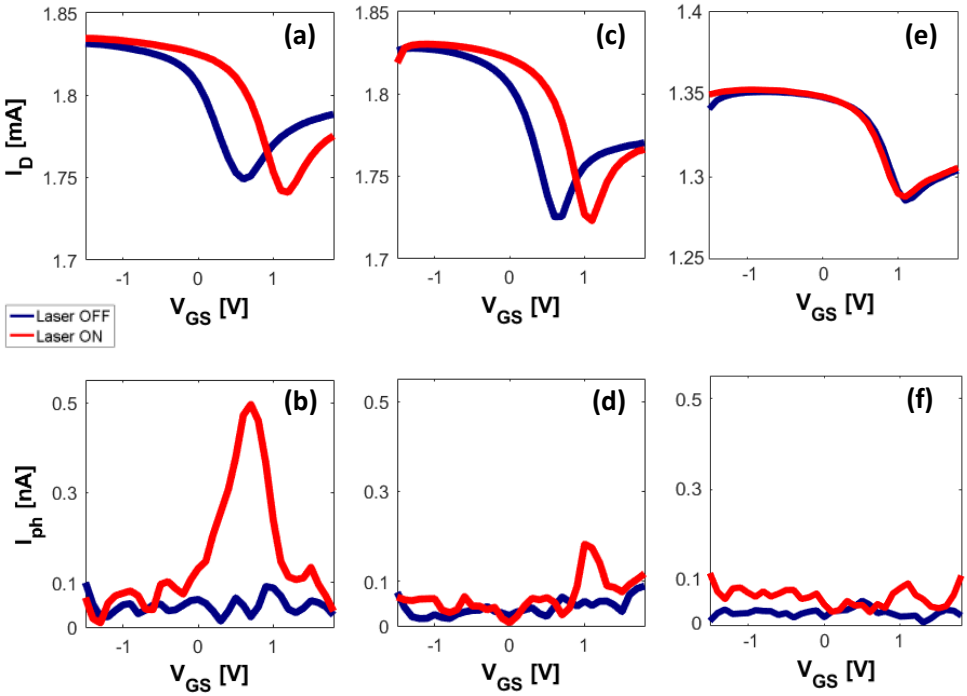


Fig. 3.25 - Static drain current (I_D) and photocurrent (I_{ph}) vs. gate-source voltage (V_{GS}) for GFETs employing (a, b) Al_2O_3 (at V_{DS} = 0.4V), (c, d) TiO_2 (at V_{DS} = 0.1V) and (e, f) HfO_2 (at V_{DS} = 0.2V) as gate oxide, with (red curves) and without (blue curves) laser power impinging on the samples at 7.6 mW.

3.4 - GFETs Fabrication Run #3

3.4.1 - Motivation and chip design

Fabrication Run #3 (FR #3) has been dedicated to the development of a new GFET layout geometry aimed at improving transistors microwave performance. Following this new approach, the "U-shape" dual gate geometry previously employed has been compared with a "T-shape" dual gate layout with reduced access parasitics. In Fig. 3.26a, b and Fig. 3.27a, b both GFET layouts have been reported to point out the differences. Figure 3.26c and Fig. 3.27c, instead, show a detail of the "U-shape" and "T-shape" gate geometry, respectively. As already anticipated previously, the single device layout consists of two separate sections in order to separate the intrinsic part (shown in the black dotted region of Fig. 3.26 and Fig. 3.27) by the extrinsic one (shown in the red dotted region of Fig. 3.26 and Fig. 3.27) which are the same for both the transistors and the test devices. The new layout has been specifically designed to

meet several requirements. From the fabrication point of view, the “T-shape” gate geometry allows to limit more effectively the influence of horizontal alignment errors, likely occurring during the various E-beam writing steps (as previously described), in the definition of gate/source and gate/drain spacings. In fact, by looking at the intrinsic device layout shown in Fig. 3.27a, an unexpected horizontal shift arising during sources and drain exposures would not affect the gate/source and gate/drain spacings, as it could happen, on the other hand, by using the “U-shape” geometry (Fig. 3.26a). The “T-shape” layout allows also to reduce the gate and source parasitic elements, thus decreasing their negative influence on the device performance, and, at the same time, simplifies and makes more accurate the identification of the intrinsic transistor in the subsequent measurements de-embedding phase. For the same reason, the drain geometry has been conceived to mimic a 50 Ω coplanar waveguide structure (up to the very beginning of the transistor intrinsic region) employing a layout identical to the one pertaining the standard substrates used for the VNA calibration. Due to both the new source/drain geometries and the longer gate structure, better microwave performance is expected from GFETs made according to the new design.

Transistors pertaining to both layouts have been fabricated on the same sapphire chip to perform a meaningful comparison of the geometries by employing the same processing conditions. This aspect has proved to be of great importance because of an unexpected failure in the E-beam evaporator during devices fabrication which, being non-recoverable in the allotted time window, prevented the deposition of the source and drain electrodes in Cr/Pd and forced to employ Ti/Al instead. For the same reasons, no deposition of the additional 300 nm Pd films, usually grown on contacting pads to reduce parasitic resistance and improve RF-probing reliability, was possible. This fact significantly influenced the output resistance of devices made during this fabrication run and, consequently, their DC/microwave performance, which is intrinsically inferior to the one obtained in the previous fabrication runs. However, the comparison between the “U-shape” transistors (in the following called “A-family”) and “T-shape” transistors (in the following called “X-family”) is still meaningful, being the two families fabricated simultaneously and on the same chip.

As a matter of fact, two sets of devices for each family (in the following called “Groups”) have been fabricated, each one showing specific values of both the

gate/source (ΔGS) and the gate/drain (ΔGD) distances. A summary of the geometries employed is reported in Table 3.4.

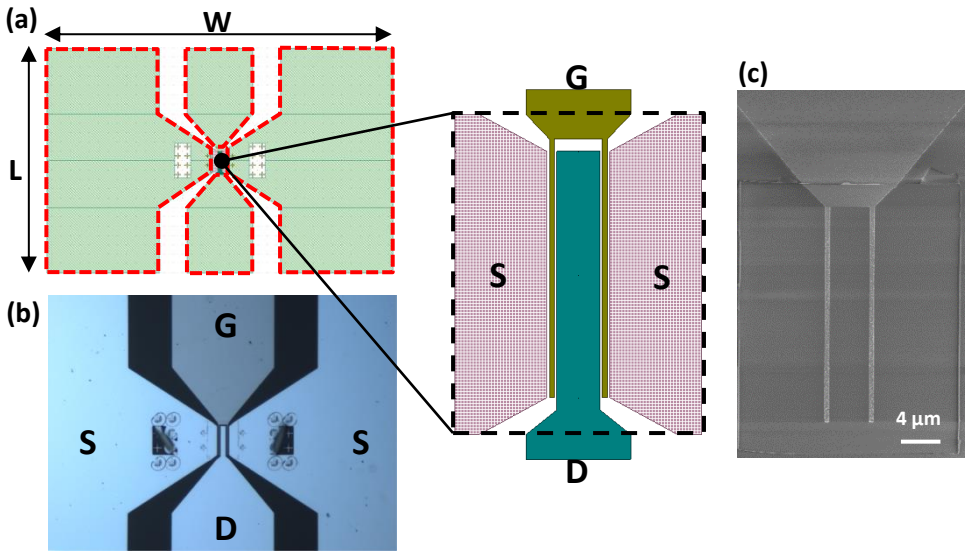


Fig. 3.26 – (a) GFET employing an "U-shape" gate layout fabricated during FR #3. The black dotted region depicts a zoom of the intrinsic active device. In (b), a micrograph of the above-mentioned layout is reported. In (c) a SEM picture shows a detail of the "U-shape" gate. All the transistor dimensions are summarized in Table 3.4.

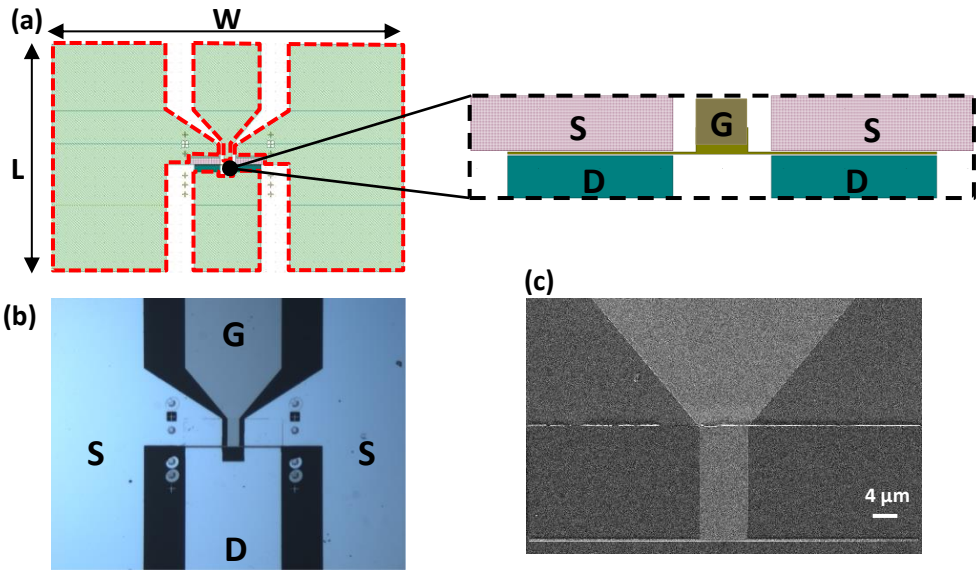


Fig. 3.27 - (a) GFET employing a "T-shape" gate layout fabricated during FR #3. The black dotted region depicts a zoom of the intrinsic active device. In (b), a micrograph of the above-mentioned layout is reported. In (c) a SEM picture shows a detail of the "T-shape" gate. All the transistor dimensions are summarized in Table 3.4.

Parameter / Group	W	L	Gate Width	Drain Width	Gate Length	ΔGS	ΔGD
AB	370	240	0.4	3.5	20	0.2	0.6
AC	370	240	0.4	3.5	20	0.2	1
XB	370	240	0.4	7	70	0.2	0.6
XC	370	240	0.4	7	70	0.2	1

Table 3.4 - Summary of the main transistors physical dimensions (in µm) employed during the FR #3. ΔGS and ΔGD refer to the gate/source and gate/drain spacings, respectively.

In particular, eight transistors have been fabricated for both the AB and the AC group while three devices have been made for the XB and XC group respectively. In the following, all the measurement data refer to the devices showing the best microwave performance for each transistor group. Additional devices belonging to the A-family pertaining to other ΔGS and ΔGD geometries have also been fabricated on the chip but they have not been reported here since they do not evidence better performance. Transistors fabrication has been carried out according to the steps previously reported. In particular, for electrodes and oxide depositions, the recipes reported in Table 3.1 and Table 3.2 have been used. In addition to the transistors, two sets of test-devices have also been made on the substrate to facilitate the de-embedding procedure. For the A-family, the same set of test-devices employed for FR #1 and 2 (Fig. 3.12) has been used. On the other hand, in addition to the old set, a new group of test-devices has been designed specifically for the X-family. In particular, two kinds of "short" structures and an "open-gate" launcher structure have been fabricated, as shown in Fig. 3.28.

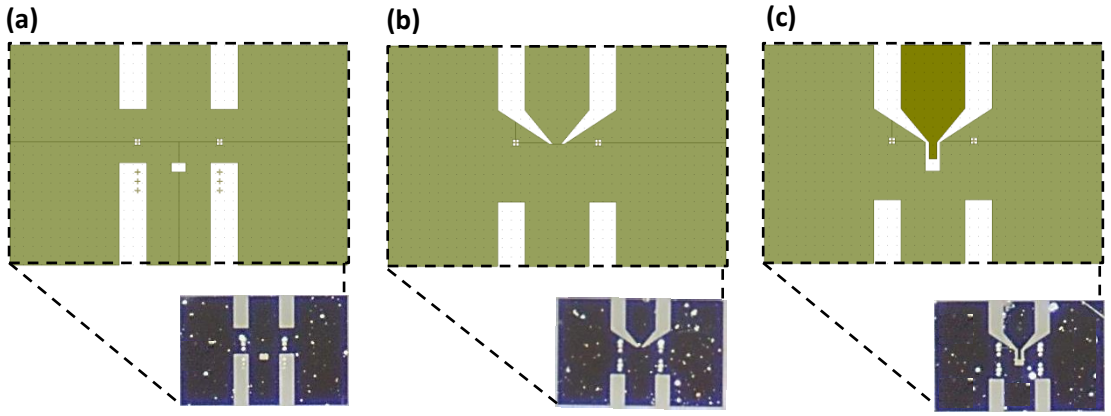
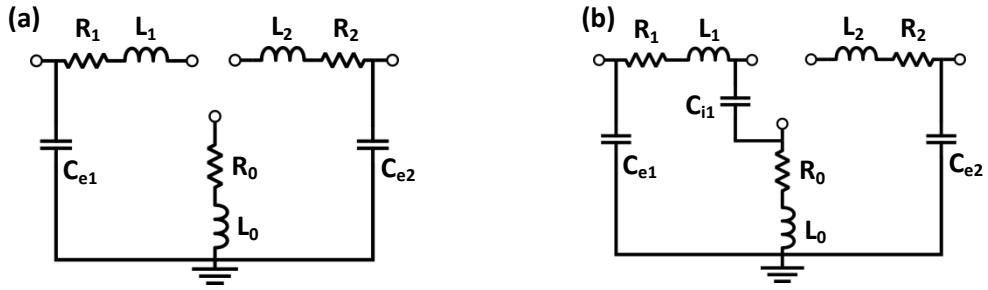


Fig. 3.28 - Additional test devices fabricated during the FR #3 to facilitate the de-embedding procedure, including two "short" structures (a, b) and an "open-gate" launcher structure (c).

The layout of these test-devices has been specifically designed to make the identification of the parasitic components of GFET belonging to the X-family easier. Differently from what made for all the devices fabricated previously, for which de-embedding has been performed according to a standard network [149], for all the transistors belonging to FR #3 an *ad-hoc* embedding network has been synthesized starting from RF measurements performed on the test-devices. In particular, two different embedding equivalent circuits have been extracted for the A- and the X-family, respectively, due to their different layouts. Considering the relatively low microwave frequency range to be investigated, simplified models with lumped elements have been adopted. The schematics of both networks are shown in Fig. 3.29a (for the A-family) and Fig. 3.29b (for the X-family). In Fig. 3.29c a summary of the passive elements employed in each circuit is also reported.



(c)

Parameter / Family	R_1 [Ω]	L_1 [pH]	C_{e1} [fF]	R_2 [Ω]	L_2 [pH]	C_{e2} [fF]	R_0 [Ω]	L_0 [pH]	C_{i1} [fF]
A	3.6	38	10	3.6	38	10	0.7	4	-
X	3.6	38	10	4.3	34	12	0.6	6	25

Fig. 3.29 – Equivalent circuit diagrams used for the de-embedding of transistors belonging to the (a) A-family and to the (b) X-family. In (c), a summary of the passive elements employed in each circuit is also reported.

3.4.2 - DC/Microwave characterization results

DC and microwave measurements have been carried out using the automated microwave bench previously described. In this case, static curves have been obtained first by sweeping V_{GS} in the range [-1.8 V, 0.7 V] and V_{DS} in the range [-2 V, -1.4 V]

and then by changing V_{GS} in the range [-0.2 V, 1.8 V] and V_{DS} in the range [1.4 V, 2 V]. This choice allowed to perform, without increasing too much the measurement time, high-resolution scans (in both inverting and non-inverting gain regions) centered around those V_{GS} and V_{DS} values where a higher incremental DC transconductance (g_m) is expected. The transfer characteristics and the g_m curves of the best device for each transistor group are reported in Fig. 3.30. Simultaneously to DC measurements, the microwave characterization was also performed by collecting the S-parameters in the frequency range [300 kHz, 20.003 GHz, 801 points log-scaled] in standard environmental conditions.

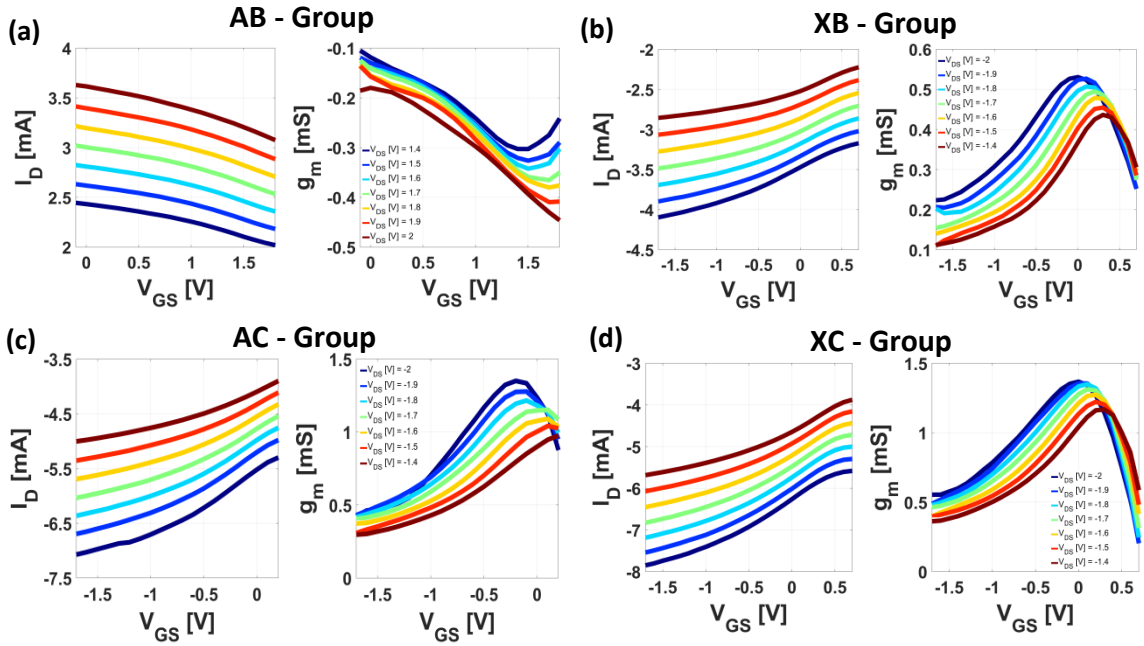


Fig. 3.30 - Transfer characteristics and incremental DC transconductance plots for the devices showing the highest values of transconductance.

To complete the planned GFETs experimental characterization procedure, the small-signal equivalent circuits for each transistor group have also been identified, by employing computer-aided techniques to fit the simulated data and the measurements. Two different circuit topologies have been obtained, due to the different layouts employed for the A- and the X-families. In Fig. 3.31a and 3.31b both small-signal equivalent circuits are shown. Figure 3.31c, instead, reports the measured (blue curves) and the simulated (red curves) S-parameters for each transistor group, confirming the good quality of the fitting achieved. The models parameters values are summarized in

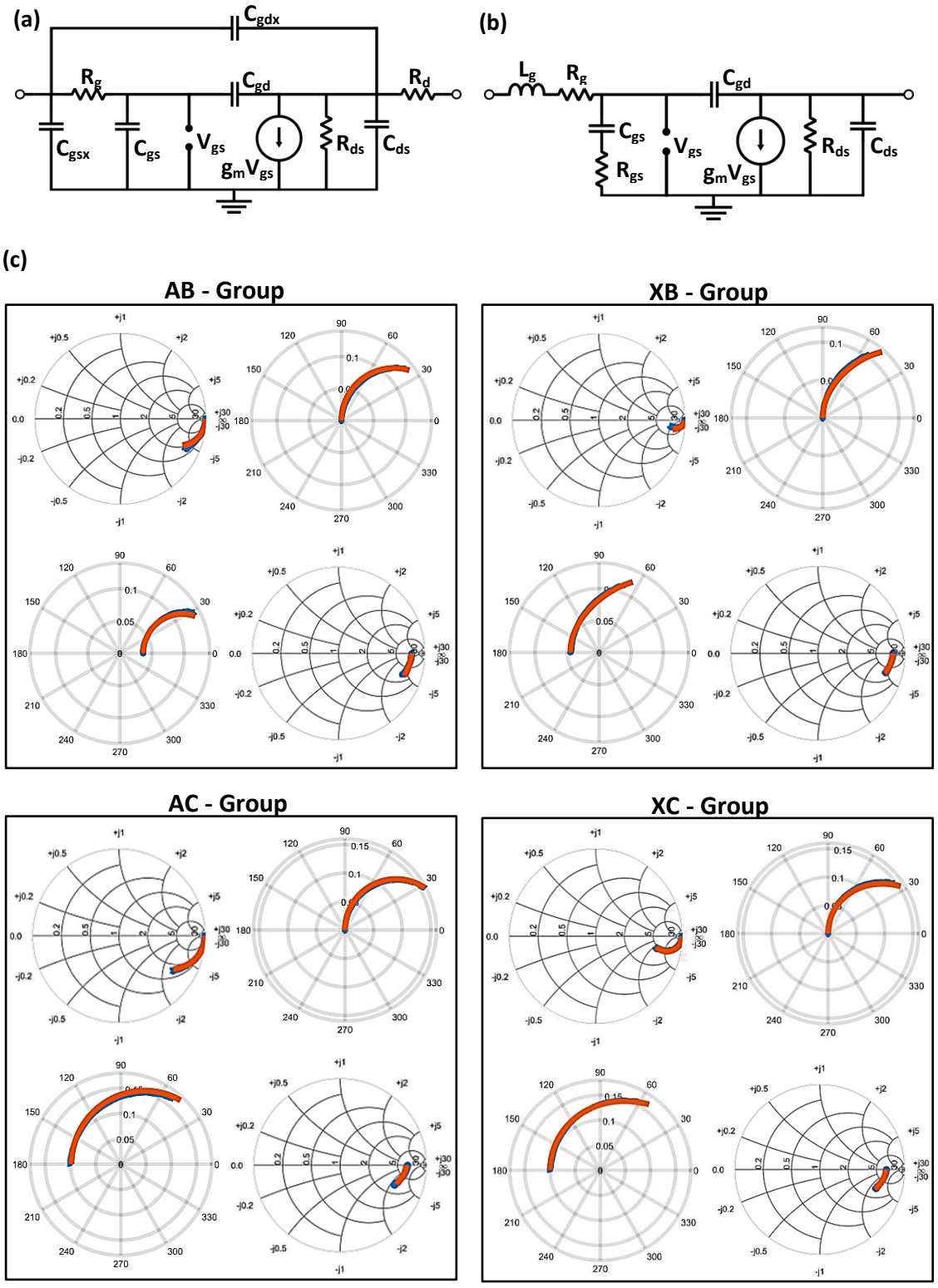


Fig. 3.31 - Small-signal equivalent circuits of GFETs belonging to the A-family (a) and to the B-family (b). In (c), a comparison between simulated (red curves) and measured (blue curves) GFETs S-parameters for the devices belonging to each group and showing the best high-frequency performance is reported. Data show the good fitting achieved and confirm the models validities.

Table 3.5. Then, microwave GFETs performance, in terms of both the short circuit current gain ($|h_{21}|$) and the cut-off frequency (f_T), has been analyzed, by comparing transistors with same ΔGS and ΔGD spacings but pertaining to different layouts (i.e., the best transistor of the AB-group has been compared with the best transistor of the XB-group while the best device belonging to the AC-group has been compared with the best one of the XC-group, respectively).

Param. / Group	R_g [Ω]	R_{gs} [Ω]	R_{ds} [Ω]	R_d [Ω]	C_{gsx} [fF]	C_{gs} [fF]	C_{gd} [fF]	C_{ds} [fF]	C_{gdx} [fF]	L_g [pH]	g_m [mS]
AB	162	-	575	13.7	7.1	24.6	14.8	13.7	2.7	-	0.4
AC	150	-	362	15.6	17.3	25.8	22.9	7.96	2.7	-	1.1
XB	267	1082	665	-	-	11.9	13.1	10.2	-	670	0.5
XC	174	219	403	-	-	25.5	23.8	5.5	-	415	1.1

Table 3.5 – Summary of the circuit models parameters shown in Fig. 3.31.

The results, referred to de-embedded data, are reported in Fig. 3.32. Both gain plots suggest that an improvement in terms of the cut-off frequency has been obtained employing the new layout, as expected due to the use of a longer gate structure and the particular shape employed for the source/drain electrodes.

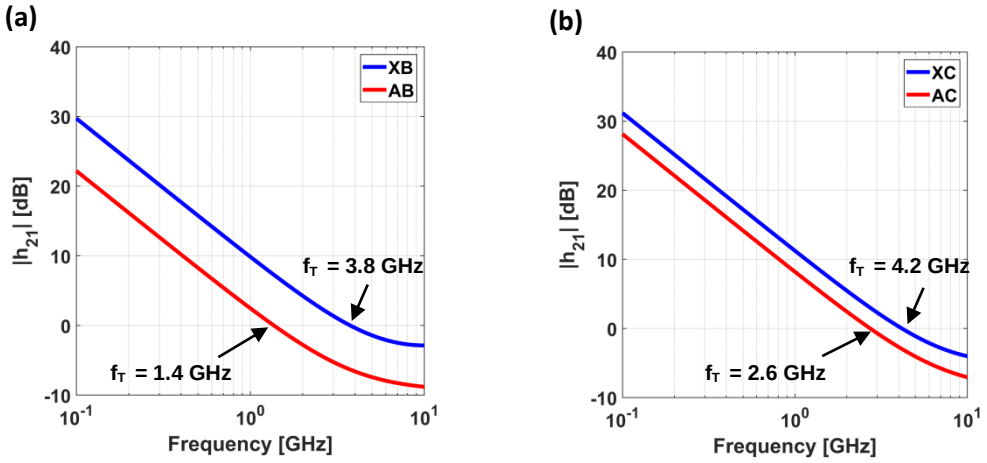


Fig. 3.32 – Comparison of $|h_{21}|$ plots for GFETs belonging to the (a) AB and XB groups and (b) AC and XC groups, respectively. Plots confirm the improvement in terms of cut-off frequency obtained with the new layout. All Data refer to devices showing the best high-frequency performance for each group.

In particular, an average doubling of the f_T values has been obtained (more precisely, an increase of a factor ~ 2.7 has been obtained by the XB-group while an increase of a factor ~ 1.6 has been reached with the XC-group). In terms of low-frequency maximum gain, instead, an increase of ~ 7 dB and ~ 3 dB has been obtained employing the XB-group and the XC-group, respectively.

As a final step, some preliminary temperature-controlled measurements have eventually been performed in the range [10 °C, 70 °C] by adding to the bench a Peltier cell unit, attached to the wafer probe-station chuck (Fig.3.33a) and computer-controlled with the help of a fiber-optic digital thermometer. Several cooling and heating cycles have been performed collecting, for each temperature, the S-parameters. In terms of the short circuit current gain, a worsening in terms of both the low frequency maximum gain and the cut-off frequency has been observed when increasing the substrate temperature from 10 °C to 70 °C. In Fig. 3.33b, a typical variation of both the low frequency maximum short circuit current gain and the cut-off frequency is reported. Additional measurements aimed at a more in-depth investigation of the influence of temperature on GFETs performance are currently underway.

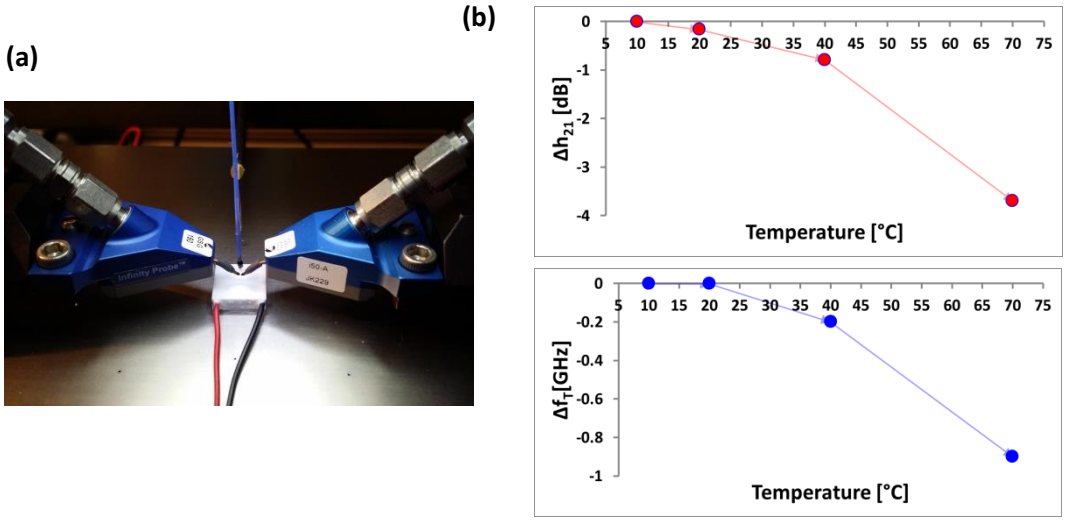


Fig. 3.33 – (a) Detail of the Peltier Cell and of the optical-fiber thermometer employed for preliminary temperature-controlled measurements. (b) Typical variations of the low frequency maximum short circuit current gain (Δh_{21}) and of the cut-off frequency (Δf_T) as a function of the GFET substrate temperature.

3.5 - Diamond X-ray detectors with reduced graphene oxide contacts

As already anticipated in Chapter 2, graphene peculiarities make it an ideal candidate also for transparent conductors fabrication. In this last part of the experimental section, it will be shown how these characteristics have been exploited to develop a novel kind of X-ray detector based on polycrystalline grade diamond substrate and Reduced Graphene Oxide (RGO) contacts [157].

In particular, the main goal of this study was to find a sequence of processing steps that allows the fabrication of X-ray detectors on diamonds without employing expensive noble metals as electrodes material. The well-known low resistivity, high chemical stability and mechanical strength, in fact, suggest the incorporation of graphene as electrode in electronic devices. By exploiting its work function (4.7 – 4.9 eV), which is similar to that of gold (5.1 eV), graphene can potentially lead to ohmic injection also in diamonds substrates. Moreover, thanks not only to their thickness but also to their low atomic number (*Z*), graphene electrodes are basically X-ray transparent, thus introducing an almost negligible perturbation of the incoming beam. These characteristics, together with the high resistivity, high mobility, radiation hardness and high thermal conductivity shown by diamond substrates, make the RGO/diamond detector a very promising solution for *in situ* beam monitoring. Compact linear beam monitors can, in principle, be obtained employing solid-state detectors. Nevertheless, exploiting the low *Z* of carbon of both the sensing material (*i.e.*, diamond) and the electrodes, it is possible to fabricate highly transmissive detectors with several possible geometries directly in the beam path. Such detectors are particularly suitable for X-ray beam monitors where the intensity and the position of the photon beam need to be measured with minimal effect on the beam itself. Moreover, electrical characteristics of both graphene and diamond have been shown to be mostly unaffected by X-ray beam exposure [158], [159], thus suggesting the permanent use of the RGO/diamond detector into an X-ray beam (i.e., as a solid-state, position-sensitive "ionization chamber"). It is important to point out here that RGO has been chosen as electrode material, rather than pristine graphene, due to its lower cost and easiness to be

deposited even on large substrates, being the starting material (i.e., the Graphene Oxide, GO) in the form of aqueous solution. Clearly, in this contest, the reduction methods play a role of primary importance, since they can lead to a final product that resemble pristine graphene very closely in terms of electrical, thermal and mechanical properties. As widely discussed in Chapter 1, most of the reduction methods are based on chemicals or thermal treatments (in furnaces or by using alternative eating sources like flash light, e-beam, laser, etc.). However, they generally require very long and controlled cycles and, among them, a good compromise in terms of safety of the process, film quality and reduction time is hardly found (see Chapter 1 for additional details on this topic). For these reasons, the possibility of employing Rapid Thermal Annealing (RTA) systems to reduce GO and obtain patterned electrodes on polycrystalline diamond substrates has been investigated. RTA systems allow, in fact, to combine the good properties typical of all thermal treatments (*e.g.*, no need of toxic agents and the possibility of performing the reduction reaction parallel on more GO-coated substrates) with an unequalled reduction speed and without worsening the film quality.

3.5.1 - Outline of detector fabrication

CVD polycrystalline diamond substrates employed for detectors fabrication have been supplied by Element Six, world-leader company in synthetic diamond research and production [160]. They belong to the *thermal grade* diamond group, which identifies the plates specifically designed to exploit the excellent thermal properties of diamond. Such substrates are not the most suitable for radiation detection, due to their worse performance in terms of electronic properties and defects concentration, if compared with single crystal plates. Nevertheless, their low cost suggests their use, at least as case study, in the outlook of a simple and economical X-ray detectors fabrication. In particular, TM180 diamond plates have been used; a complete list of their specifications can be found in [161]. The outline of detectors fabrication is described below. I specify that detectors preparation has been performed at the Stanford Nanofabrication Facility (SNF) and at the Stanford Nano Center (SNC), part of the Stanford Nano Shared Facilities, while first X-ray tests have been carried out at the SLAC National

Accelerator Laboratory. Detectors fabrication starts with a first substrate cleaning procedure (Fig. 3.34a). It has been proved that this step can play a fundamental role in defining the behavior of the final sample, since it can strongly influence diamond substrate termination. In fact, almost every step of the post-processing phases of CVD diamond growth introduces some surface contaminants like oxygen species and hydrocarbons [162] or graphitic phases (caused by the laser cutting of the plates). Sometimes diamond surfaces are also exposed to hydrogen plasma after the growth process to etch the damaged layers and remove the polishing-induced defects [163]. These treatments, together with the predominance of H-species during the CVD growth [164], [165], cause diamond surface to be hydrogen terminated, that is known to be p-type conductive in ambient condition [166]. Both the graphitic phases and the H-termination are responsible of a decrease of diamond surface resistivity, which is highly undesired causing surface leakage currents. Conversely, if an oxygen-termination is induced, a desired high insulating behavior can be obtained [167], thus helping particle detectors operation, in which low values of current (nA) are normally involved.

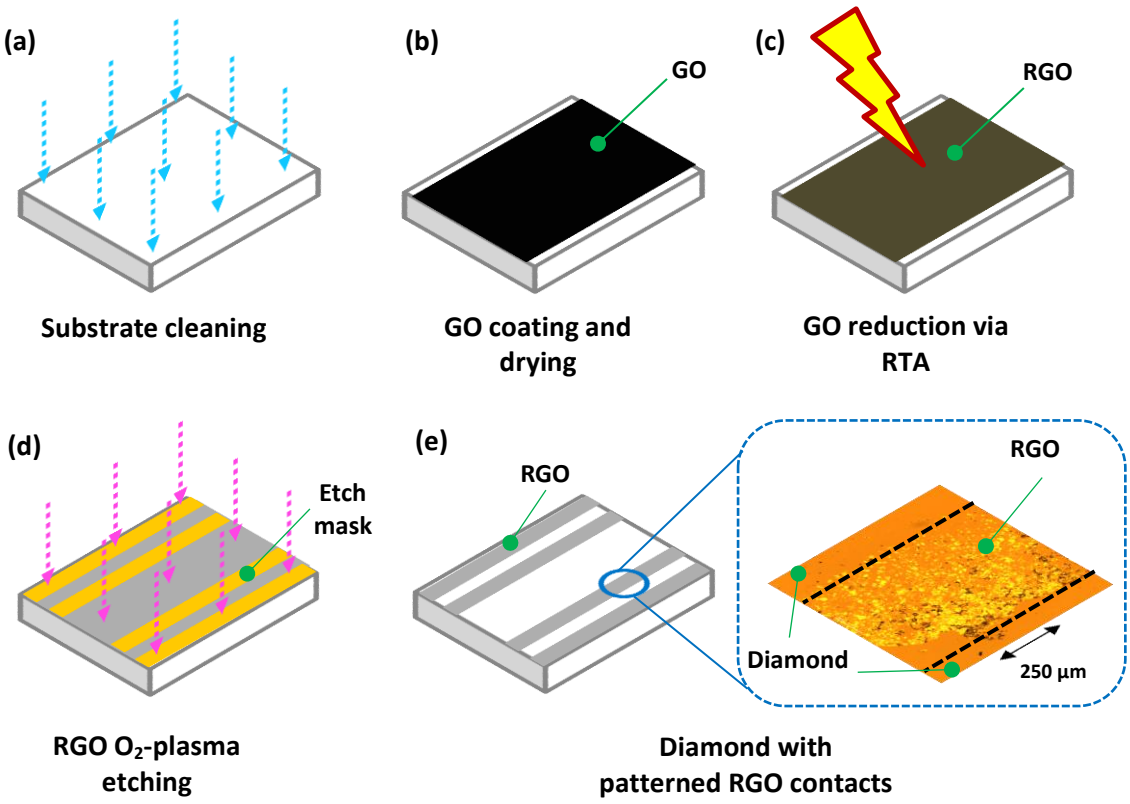


Fig. 3.34 – Outline of X-ray detector fabrication. The detail in (e) shows a micrograph of a RGO contact.

Therefore, a combination of both dry and wet cleaning procedures has been chosen before GO coating to remove surface contaminants and oxidize the substrates. In particular, the following recipe has been used:

- 5 H_2O + 1 H_2O_2 + 1 NH_4OH at 50 °C for 10 min. (to remove organic impurities and perform a first mild oxidation);
- Rinse in deionized water;
- 5 H_2O + 1 H_2O_2 + 1 HCl at 70 °C for 10 min. (to remove the metallic impurities and perform a second mild oxidation);
- Rinse in deionized water;
- 9 H_2SO_4 + 1 H_2O_2 at 120 °C for 20 min. (to strongly oxidize the substrate);
- Rinse in deionized water;
- Drying with N_2 gas;
- Oxygen plasma at 100 sccm, 700 mTorr and 500 W for 10 min (immediately before GO deposition to remove residual impurities and give a final surface oxidation).

Although more aggressive chemical oxidizing solutions can be found in literature, the above-mentioned choice has been made as a compromise between having a sufficient oxidizing action and the respect of SNF safety standards.

Storage of cleaned substrates has been performed inside the cleanroom in polystyrene plastic boxes with polyurethane membranes. In order to limit surface contaminations, metal deposition was never performed more than 24 hours after cleaning.

After the substrate cleaning, GO film has been deposited (Fig. 3.34b) by using a manual spin coater and a commercial high concentration solution [168]. Then, the film has been dried in N_2 inert atmosphere at 130 °C for 4 hours employing the thermal cycle reported in Fig. 3.35, panel A. As discussed in Chapter 1, this temperature is not sufficient to start a reduction reaction, but helps to improve the film adhesion and uniformity. Then, the reduction process by RTA follows (Fig. 3.34c). Two different cycles in Ar atmosphere, the first one at 550 °C for two minutes and the second one at 650 °C for two minutes, have been performed. Details on the thermal and Ar-flow

cycles employed are summarized in Fig. 3.35, panel B. In Fig. 3.35, panel C, micrographs of the deposited film immediately after the coating (I), after the first drying cycle (II) and after the reduction process via RTA (III) are also depicted.

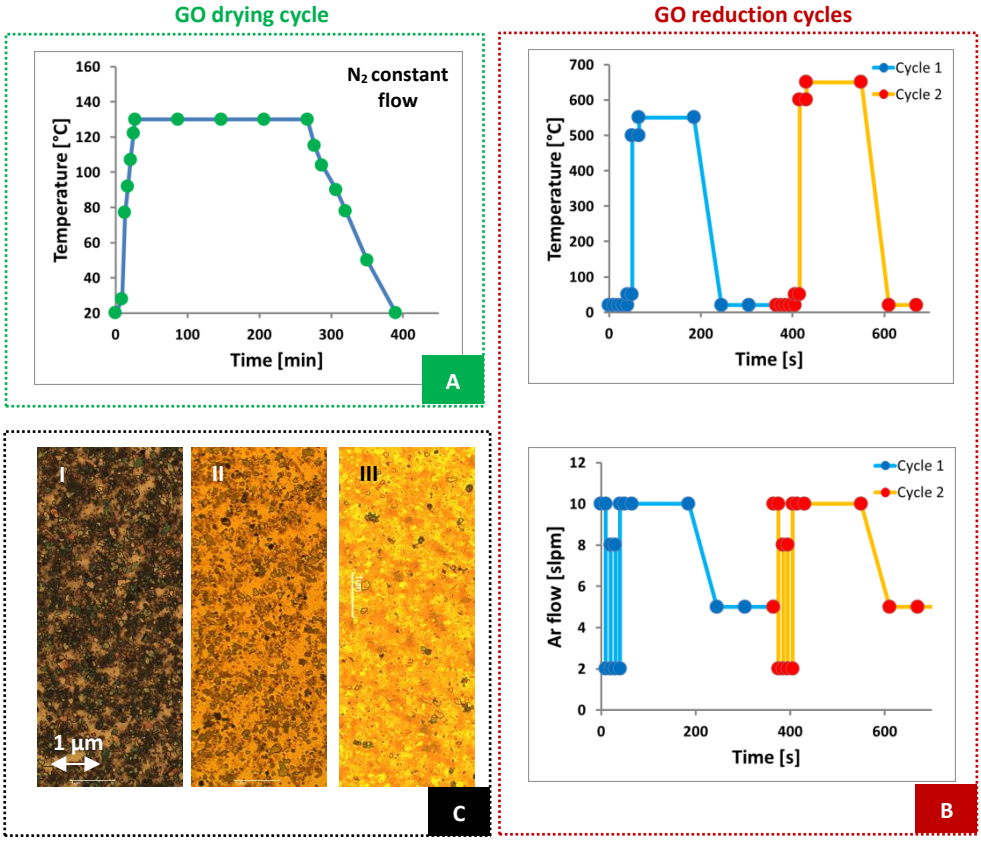


Fig. 3.35 – Panel A shows the GO drying cycle employed. In panel B, the RTA reduction recipe, in terms of both the chamber temperature and the gas flow, is reported. Panel C depicts three micrographs of the deposited GO film immediately after the coating (I), after the first drying cycle (II) and after the reduction process via RTA (III).

Once reduced, the RGO electrodes can be patterned using O_2 plasma etching and a shadow mask (Fig. 3.34d). In Fig. 3.34e, a micrograph showing a detail of the RGO film electrode patterned on the diamond substrate is also reported.

3.5.2 - RGO film characterization and preliminary X-ray tests

Preliminary investigation of the reduction process of GO through RTA has been performed by conductivity measurements employing a standard four-point-probe approach, through a Prometrix OmniMap RS35c. A sheet resistance of ~ 2.3 kΩ/□ has

been obtained for a ~ 90 nm thickness film, which is comparable with typical sheet resistances of films reduced by applying different thermal processes [70], [79]. Then, additional analysis concerning film quality have been performed via X-ray Photoelectron Spectroscopy (XPS). In fact, both optical and electrical properties of carbon–based materials are strongly related to π-electrons. This causes the sp^2 carbon fraction to represent one of the most important parameters to characterize the degree of oxidation in graphene films [169]. In Fig. 3.36a-d, an example of the evolution of the C1s spectra of GO film after 20, 90 and 260 minutes of thermal reduction is reported [170]. As it can be noticed, as the reduction reaction proceeds, a decrease in the C-O, C=O and C(O)OH lines is observed. In Fig. 3.36e, instead, the C1s spectrum of the RGO film obtained via RTA is reported, showing a well-defined C-C sp2 bonding line at 284.5 eV and a significant removal of oxygenated groups. This confirms the quality of the developed reduction reaction, despite having considerably decreased the duration of the reduction procedure (few minutes vs. hours).

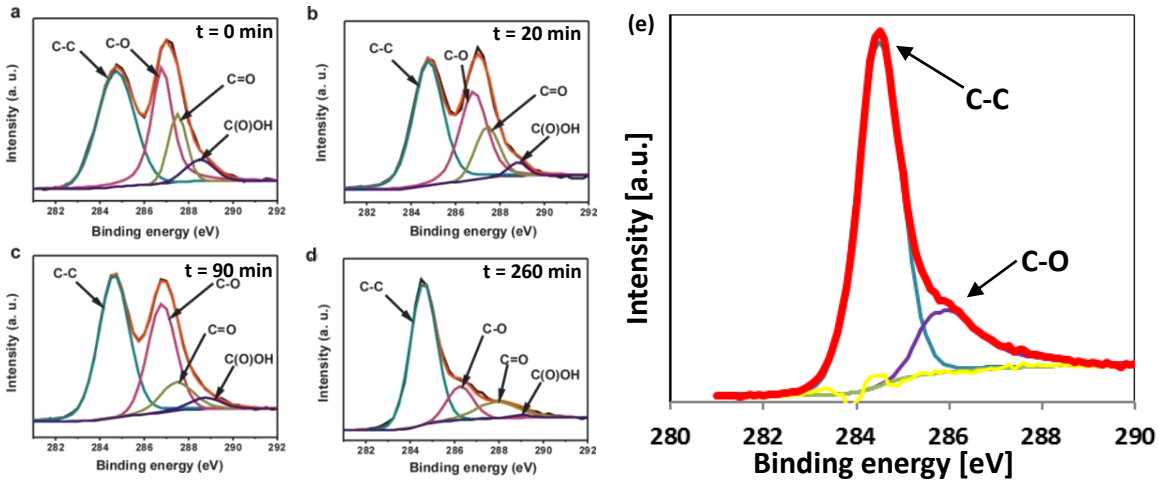


Fig. 3.36 – (a, d) Example of the evolution of the C1s spectra of a GO film after 20, 90 and 260 minutes of thermal reduction [170]. In (e), the C1s spectrum of RGO obtained with RTA is reported, showing the effectiveness of the developed reduction procedure despite the decreased reaction duration.

Preliminary X-ray tests have also been performed employing a sealed radioactive source (^{241}Am) and a Keithley 4200 SCS probe station, as shown in Fig. 3.37a. In Fig. 3.37b, a detail of the patterned RGO contacts on diamond substrate is also depicted. The X-ray source could be mechanically moved towards (at a distance of ~ 2 cm) and away from

the detector, biased at 100 V, and the values of current have been measured as a function of time. A schematic of the set-up employed is shown in Fig. 3.37b. X-ray tests show a change of detector photocurrent of ~ 17 pA (for Event 1) and 11 pA (for Event 2) when the source is "turned on" (i.e., put closer to the detector), thus showing X-ray detection capability of the device.

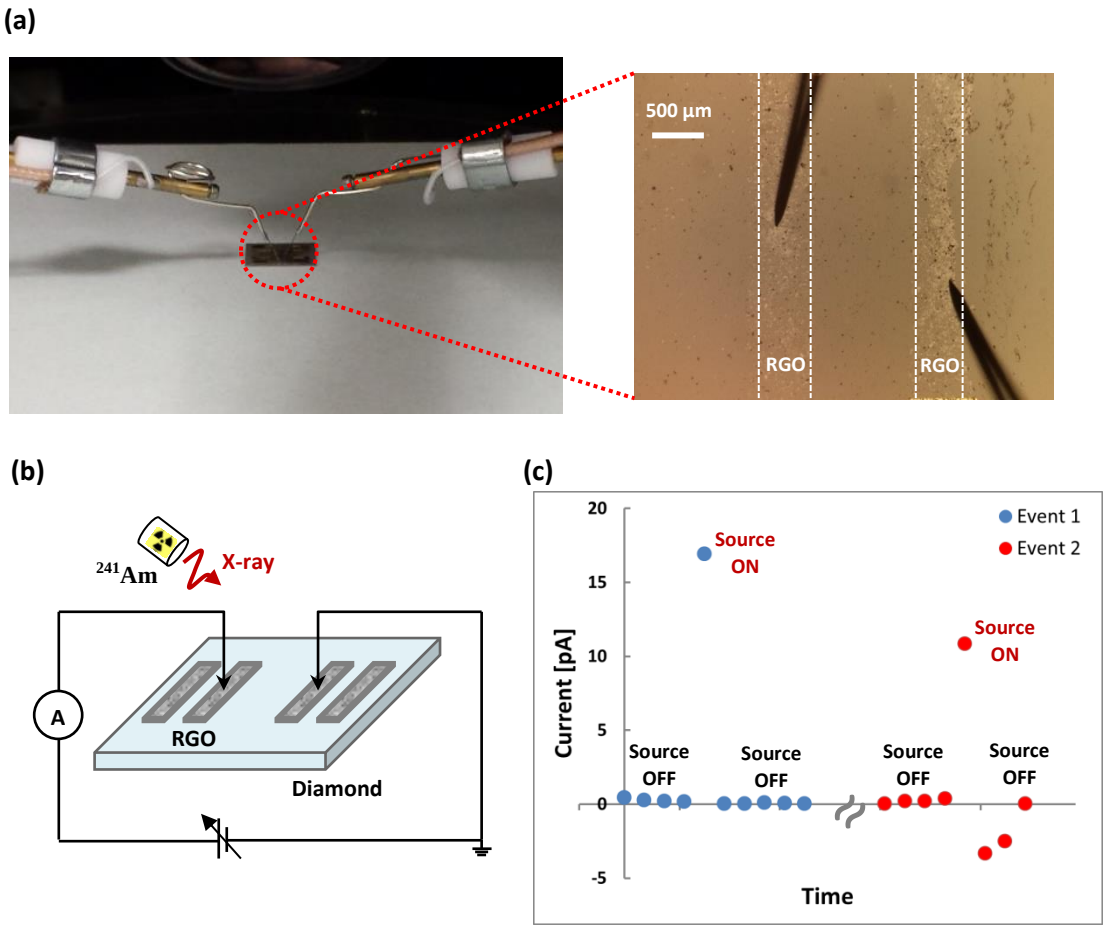


Fig. 3.37 – (a) Diamond detector connected to the probe station and detail of the patterned RGO contacts. (b) X-ray measurement setup and (c) first tests using ^{241}Am.

Appendix A
Additional notes of Microwave Electronics

A1 - Scattering parameters and microwave figures of merit

Most of the experimental activity carried out in this work has been dedicated to fabrication and characterization of graphene-based microwave transistors through Scattering parameters (S-parameters) measurements. Then, GFETs amplification characteristics have been described in terms of current and power gains. For these reasons, in this section, an overview on the above-mentioned parameters will be given.

S-parameters are a parameters set that relates to the travelling waves scattered or reflected when an n-port is inserted into a transmission line [171], [172]. From a physical point of view, among all the network parameters set, the S-parameters are the most suitable to describe the operation of a microwave circuit, in which voltages and currents are not directly measurable. Conversely, it is always possible to measure amplitude and phase of the waves travelling to and from the microwave circuit. S-parameters derivation is related to a new set of variables (a_i, b_i) which are defined as the normalized complex voltage waves incident on and reflected from the ith port of the network, respectively. In particular, considering a 2-ports network, the S-parameters can be written as [172]:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0}; S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}; S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}; S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \quad \text{(A1)}$$

where:

$$a_i = \frac{V_i + Z_i I_i}{2\sqrt{|ReZ_i|}}; \qquad b_i = \frac{V_i - Z_i^* I_i}{2\sqrt{|ReZ_i|}} \quad \text{(A2)}$$

and V_i and I_i refer to the terminal voltage and current of the ith port of the network, while Z_i is an arbitrary reference impedance.

Then, transistor gains can also be defined [93]. Among them, the short-circuit current gain (h_{21}) and the available power gain (G_A) are widely employed to describe and compare transistors microwave performance. Their expressions, in terms of the S-parameters, are reported below:

- $h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} = -\frac{2s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}s_{21}}$ (A3)
- $G_A = \frac{Power\ available\ from\ network}{Power\ available\ from\ source} = \frac{|s_{21}|^2(1-|\Gamma_s|^2)}{(1-|s_{22}|^2) + |\Gamma_s|^2(|s_{11}|^2-|D|^2) - 2Re(\Gamma_s M)}$ (A4)

where Γ_s is the source reflection coefficient, $D = s_{11}s_{22} - s_{12}s_{21}$ and $M = s_{11} - Ds_{22}^*$.
Another useful parameter used to evaluate the high frequency performance of transistors is the Maximum Available power Gain (MAG or $G_{A,max}$), whose expression, under simultaneous conjugate match conditions, can be written as:

$$G_{A,max} = \frac{|s_{21}|}{|s_{12}|}(K - \sqrt{K^2 - 1}) \qquad \text{(A5)}$$

where $K = \frac{1+|D|^2-|s_{11}|^2-|s_{22}|^2}{2|s_{12}s_{21}|}$ is the network *stability factor*, whose value needs to be greater than 1 in order to properly define $G_{A,max}$ (*i.e.*, to guarantee that the $G_{A,max}$ value remains finite). Closely related to the above-mentioned current and power gains are the two most widely used figures of merit of RF transistors, namely the cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}). In particular, f_T is defined as the frequency at which the magnitude of h_{21} approximates unity (*i.e.*, 0 dB) while f_{max} corresponds to that particular frequency at which $G_{A,max}$ is equal to 1 [93]. Their importance relates to the observation that they actually represent the upper frequency limits beyond which transistors lose their ability to amplify. Considering a typical small-signal equivalent circuit of a FET (Fig. A1), the cut-off frequency and the maximum frequency of oscillation for both the intrinsic and the extrinsic model of the transistor are found to be [22]:

- $f_{T-int} = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$ (A6)
- $f_{max-int} = \frac{g_m}{4\pi C_{gs}} \cdot \frac{1}{\sqrt{g_{ds}R_i}}$ (A7)

- $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \cdot \frac{1}{1+g_{ds}(R_S+R_D)+\frac{C_{gd}g_m(R_S+R_D)}{C_{gs}+C_{gd}}}$ (A8)

- $f_{max} = \frac{g_m}{4\pi C_{gs}} \cdot \frac{1}{\left[g_{ds}(R_i+R_S+R_G)+g_m R_G \frac{C_{gd}}{C_{gs}}\right]^{1/2}}$ (A9)

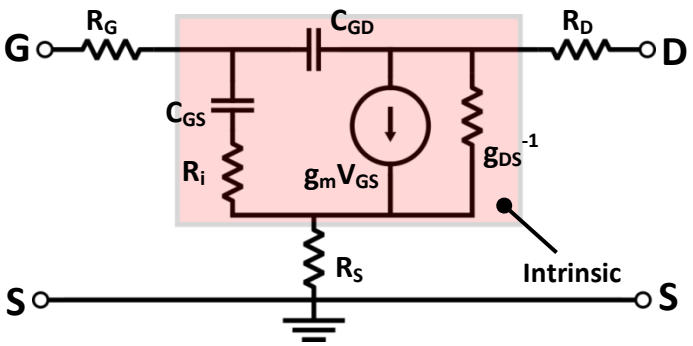


Fig. A1 – Typical small-signal equivalent circuit of analog/RF FETs (adapted from [22]).

From the previous frequency expressions, we can infer that high f_T and f_{max} values can be obtained by trying to increase transistor transconductance and limiting as much as possible all other elements of the equivalent circuit. Furthermore, both f_T and f_{max} are quite sensitive to DC bias conditions. In fact, from (A8) and (A9), we can conclude that, at low V_{DS} (that is, when transistors operate in the so called linear regime) the small g_m value and large g_{ds} lead to small gain and limit the cut-off frequency and, even more, the maximum frequency of oscillation. This observation suggests the importance of driving transistors into saturation to improve RF performance, a condition that is not easy reachable when dealing with graphene-based transistors due to their typical weak saturation regime, as already discussed in Chapter 1 [22].

A2 - Vector Network Analyzer calibration

High measurement accuracy is a generic target required for every kind of device characterization. Nevertheless, when dealing with RF and microwave measurements, achieving this goal can become even more critical due to the additional difficulties

arising with high frequencies. As widely described in the experimental section, the most common task in microwave characterization concerns the analysis of a device through the use of S-parameters, performed via a Vector Network Analyzer (VNA). This means that high VNA accuracy is required to obtain reliable results and this can be obtained only by calibrating the test system using a mathematical technique called vector error correction [173]. Through this technique, a set of error terms can be identified using known standard (e.g., open, short, load/match, thru, line, reflect, etc. [174]) and, then, removed from actual measurements [174]. In other words, a VNA calibration allows the final user to mathematically remove systematic errors from the system caused by a not perfect test and VNA hardware. In Fig. A2 a typical eight-terms error model is reported in which the systematic errors associated to the VNA are modeled by error port adapters (X and Y, respectively) while the VNA itself is assumed to be ideal (error-free) [175].

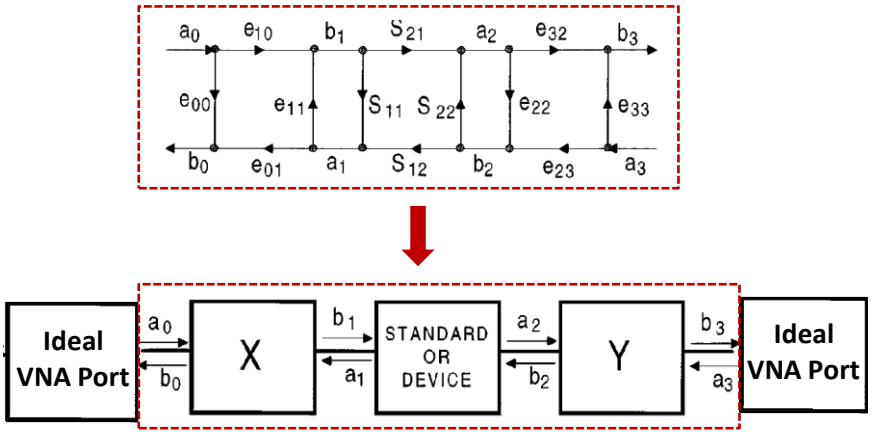


Fig. A.2 – The widely used eight-terms error model for a VNA and the associated block diagram. The systematic errors associated to the VNA are modeled by error port adapters (X and Y, respectively), each one connected to the device under test and to the VNA, which is assumed to be error-free (adapted from [175]).

During the years, different calibration types (that is, which ports are connected and to which level) and algorithms (that is, how the correction is performed) have been proposed and their choice is generally made on the basis of the available calibration standards and the required trade-off between time consumption and accuracy [176]. An overview of the various calibration types and algorithms is reported in Table A1 and A2 respectively.

Type	Parameters calibrated	Uses
Full 2-port	s_{11}, s_{12}, s_{21} and s_{22}	Most complete calibration
Full 1-port	s_{11} or s_{22} or s_{11} and s_{22}	Reflection only
1-path 2-port	s_{11} and s_{21} or s_{22} and s_{12}	1-port reflection and simple transmission (fast, low transmission accuracy unless DUT loss)
Frequency response	Any parameter (or pairs of symmetric parameters)	Normalization only (fast, low accuracy)

Table A1 - Main VNA calibration types [176].

Algorithm	Description	Advantages	Disadvantages
SOLT (Short-Open-Load-Thru)	Coaxial	Simple, redundant standards. Not band limited	Very well-defined standards required, poor on-wafer, lower accuracy at high frequency
SSLT (Short-Short-Load-Thru) shorts with different offset lengths	Waveguide	Same as SOLT	Same as SOLT and band limited
SSST (Short-Short-Short-Thru) all shorts with different offset lengths	Waveguide or high freq. coaxial	Same as SOLT but better accuracy at high frequency	Very well-defined standards required, poor on-wafer, band limited
SOLR/SSLR/SSSR, like the previous ones but with 'reciprocal' instead of 'thru'	Like the previous ones but when a good thru is not available	Well-defined thru not required	Some accuracy degradation, but slightly less definition, other disadvantages of parent calibration
LRL (Line-Reflect-Line) or **TRL** (Thru-Reflect-Line)	High performance coaxial, waveguide or on-wafer	Highest accuracy, minimal standard definition	Requires very good transmission lines, less redundancy, band-limited
LRM (Line-Reflect-Match) or **TRM** (Thru-Reflect-Match)	Relatively high performance	High accuracy, only one line length (easier to fixture and on-wafer). Usually not band-limited	Requires load definition. Reflect standard setup may require care depending on load model used
LRRM (Line-Reflect-Reflect-Match)	High performance	Same as LRM but only one match standard (partially unknown) required	Requires load definition.

Table A2 - Main VNA calibration algorithms (adapted from [176]).

Several vendors provide different calibration kits for every specific algorithm (e.g., SOLT kits, LRL kits, microstrip and coplanar waveguide kits, etc.). Among them, several calibration-standard substrates or Impedance-Standard Substrates (ISS), containing opens, shorts, loads, transmission lines, are also available for on-wafer calibrations. In this work, a Full 2-port, on-wafer, eight-terms, Line-Reflect-Reflect-Match (LRRM) calibration algorithm has been employed [175], [177], achieved using a Cascade 101-190 ISS [178]. Some pictures showing the four standards employed during the VNA calibration procedure are reported in Fig. A3. For the purpose of the high-frequency characterizations performed in this work, the reference planes have been chosen at the probe tips.

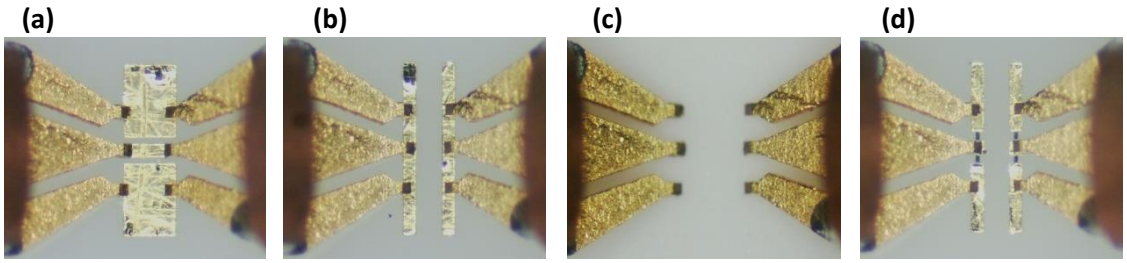


Fig. A.3 – The four standards employed in this work to perform the LRRM VNA calibration, including: (a) "Thru" (i.e., "line"), (b) "short" (i.e., first "reflect"), (c) "open" (i.e., second "reflect"), (d) 50 Ω load (i.e., "match").

A3 - De-embedding

As already concisely described in the previous section, the first step before performing high-frequency measurements is the VNA calibration. In the case of on-wafer characterizations, this is done by defining a reference plane for the S-parameters measurements at the probe tips and by employing a standard calibration technique. Then, additional on-chip parasitics (*e.g.*, contacting pads, coplanar waveguides connecting the probes to the DUT, etc.) need also to be characterized in order to remove them from the measurements and obtain the actual (intrinsic) transistor two-port parameters. This is the so-called *de-embedding* procedure. As it happened for the calibration procedures, several approaches have been developed in the past years to tackle the de-embedding problem [149], [179], [180]. In the case of on-wafer de-embedding, two main techniques can be found in literature, namely the equivalent

circuit model-based de-embedding and the direct use of "in-situ" standard elements, which is basically an extension of the S-parameters probe-tip calibration technique applied to the intrinsic device planes [180]. In the first approach, the DUT is modeled by an equivalent circuit model (representing the extrinsic parasitic components) surrounding (i.e., "embedding") the active device. Hence, the intrinsic transistor S-parameters are extracted from raw measurements on the DUT simply by removing (numerically, in a computer-aided post-processing phase) the network parameters of the embedding circuit, once available. In particular, their identification task can be accomplished employing additional measurements on auxiliary test devices, whose number, in general, relates to the complexity of the parasitic circuit model adopted [180]. A widely employed simplified approach to this task, owing to its sufficient accuracy below 30 GHz, makes use of two shells to model the parasitic network surrounding the transistor (see Fig. A.4a). The identification of the six one-ports there appearing can be carried out by a two-step systematic error-correction approach with the help of only two auxiliary test devices, namely, a "short" and an "open", theoretically ideal [149]. Their real world implementation, if appropriately made, usually introduces only additional uncertainty in the low-microwave range.

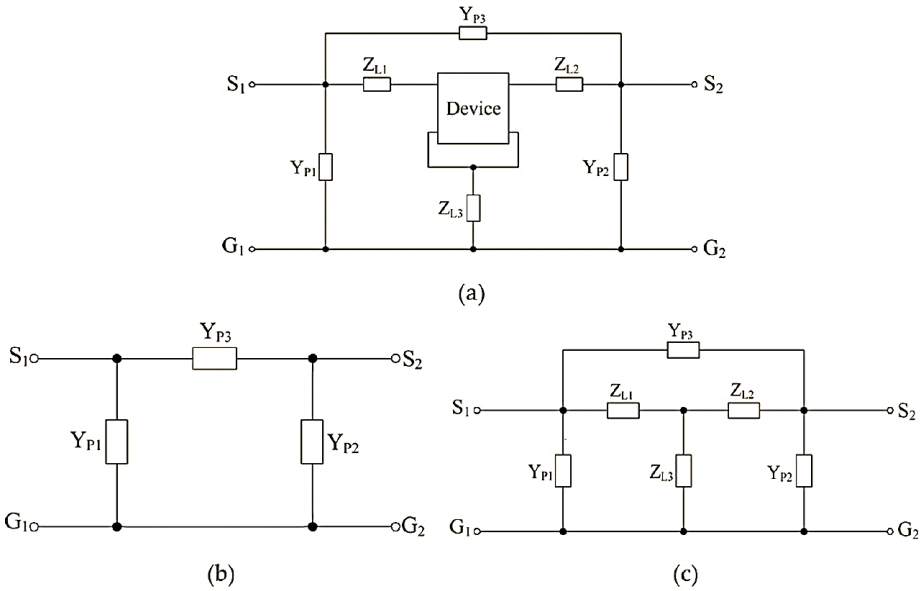


Fig. A.4 – (a) Equivalent circuit diagram employed for the two-steps correction method reported in [149]. (b) and (c) show the equivalent circuit diagram of the open and short patterns needed in the above-mentioned de-embedding algorithm (pictures from [180]).

Figure A.4b, c, show the equivalent circuit diagrams of the open and short patterns used to identify (separately) the "parallel" and the "series" parasitics, respectively. As it can be noticed from the previous picture, parasitic components are represented in terms of their impedance (Z_{ij}) and admittance (Y_{ij}) parameters, without assuming any specific circuit-topology form them. In the schematic of Fig. A.4a, the different circuit elements have the following roles [149], [180]: Y_{p3} takes into account the cross talk between the input and output network ports due to substrate coupling and fringing capacitance, Y_{p1} and Y_{p2} model the parasitic capacitances between bond pads and ground, Z_{L1} and Z_{L2} measure the series parasitic of metal lines while Z_{L3} models the dangling ground lead parasitic. Once the raw measurements on the DUT (i.e., Y_{DUT}) and on the test devices have been obtained (i.e., Y_{OPEN} and Y_{SHORT}, respectively), the intrinsic device admittance matrix can be extracted according to the following:

$$Y_{DEV} = [(Y_{DUT} - Y_{OPEN})^{-1} - (Y_{SHORT} - Y_{OPEN})^{-1}]^{-1} \quad \text{(A10)}$$

Then, S-parameters can be obtained through mathematical manipulation of the Y_{DEV} matrix [93].

In alternative to the above two-tier de-embedding approach, more complex parasitic network topologies can be adopted even at low-microwave frequencies, either made of explicit (lumped or distributed) elements or Z/Y numerically characterized n-ports. For their identification, additional test-device are in this case needed, e.g., a "thru", matched, transmission line.

On the other hand, when much higher frequency (or high-precision) characterizations are required, the general (five-ports) parasitic embedding network identification demands for an actual in-situ calibration at the intrinsic device reference planes, and then the on-chip implementation of a complete set of metrology-grade standards.

In the de-embedding procedures carried out on the fabricated GFETs, the above-mentioned in-situ calibration approach could not be applied due to the lack of a load standard fabricated on chip. On the other hand, available "open", "short" and "thru" structures, have been differently used, depending on the specific fabrication run.

In particular, for both FR #1 and FR #2, the "open" and "short" test devices have been employed to perform the two step de-embedding approach proposed by [149] while the 50 Ω "thru" transmission line has been used to carry out a subsequent check of the de-embedding quality. In FR #3, instead, a multi-measure approach has been adopted in which "open", "short" and "thru" test devices, together with an additional set of auxiliary passive elements specifically designed for the "T-shape transistors" (see Chapter 3 for additional details), have been employed to synthesize two *ad hoc* embedding networks, each one for a specific transistors family. Then, de-embedding procedure has been performed by numerically "subtracting", in a computer-aided post-processing phase, the network parameters of the embedding circuits to the raw measurements. This choice allowed to carry out a higher-precision characterization, if compared with the approach previously adopted, and to perform, at the same time, a more meaningful comparison of the two transistor families.

A4 - Ring resonators

The ring resonator method, originally proposed by [181], is one of the most successful experimental procedures developed for the evaluation of the effective permittivity of a transmission line (e.g., microstrip line, coplanar lines, coupled lines, etc.) in a wide range of frequencies, from low RF to high millimeter-waves [182]. In this work, a set of ring resonators has been purposely fabricated in order to validate, in the frequency range of interest, the value of the substrate dielectric constant (ε_R) provided by the vendor and subsequently employed in the circuit/electromagnetic simulations performed to appropriately size all active and passive devices electrodes. In particular, to extract such ε_R values, two differently sized ring resonators have been fabricated on the same sapphire substrate used for GFETs and characterized in microwave regime. Then, a 3D electromagnetic (EM) model has been developed and simulated (Fig. A5a), by employing the Analyst^{TM} 3D finite element method EM software included in the NI-AWR Design Environment [183]. After a proper setting of the 3D EM simulator parameters for the specific layout at hand, the microwave response of the ring resonators has been simulated for different values of the substrate dielectric constant

until a good matching of the resonance frequencies between the fabricated and the EM-simulated resonators was reached (Fig. A5b). Such best fitting has been found at ε_R = 9.7, slightly different from ε_R = 9.39 provided by the vendor [148].

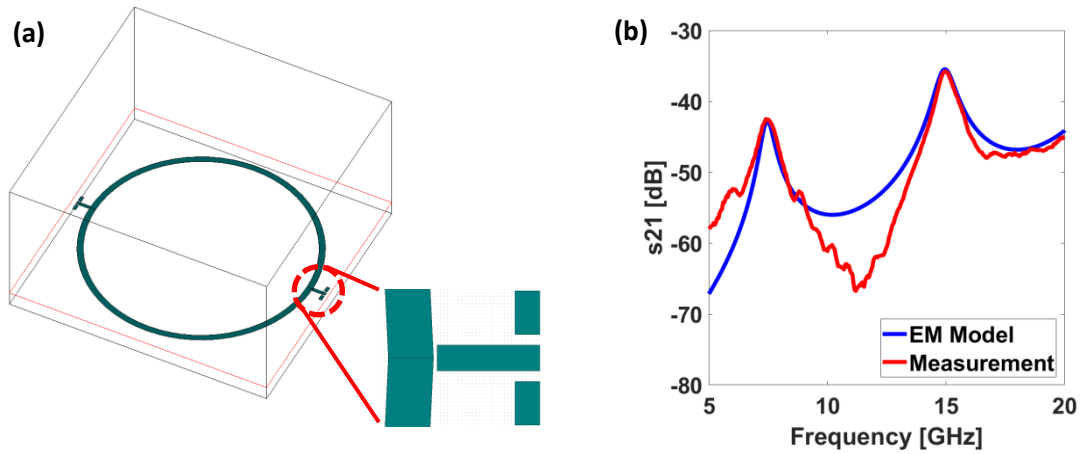


Fig. A.5 – (a) Layout of the ring resonator employed to experimentally evaluate the substrate dielectric constant. A detail of the input/output transmission lines is also reported. (b) Comparison between simulated and measured ring resonator data. A good matching of resonance frequencies has been obtained for ε_R = 9.7.

Appendix B
Bench automation software

During the experimental activity carried out in this work, great attention has been paid to the development of a reliable and "user friendly" bench automation software. As described in Chapter 3, several different types of GFETs characterizations have been performed, including DC/microwave, optical and thermoelectric ones, all requiring many parameters to be set and producing large amount of measurement data. In order to automate the characterization procedure and facilitate the system configuration required before the beginning of each measurement campaign, an IEEE-488 bus controlled by a PC-based master station unit has been adopted and a complete set of HTBasic software modules implemented [184]. As said, this choice helps to reduce significantly the time required for the system configuration and the subsequent measures acquisition, improving also data reliability. All these aspects, of course generally desirable, turn out to be of fundamental importance when dealing with GFETs due to the additional difficulties (hysteresis, great sensitivity to DC bias conditions, rapid degradation, etc.) which specifically affect prototype (e.g., non-passivated) graphene-based devices and that can make the measurement process quite tricky. In the next pages, a brief overview of the main HTBasic software programs, specifically developed for GFETs characterizations, will be given together with the pertaining "high-level" flowcharts, thus helping the reader in understanding the main target of each software module.

B1 - Software Module #1

Software Module #1 (SM #1) has been specifically implemented to provide the user with a versatile tool to perform DC resistance measurements of two-port resistive networks of the general type illustrated in the red dashed rectangle shown in Fig. B.1. In particular, the program has been specifically adopted to measure, first, the parasitic resistances associated to the bias-tee nets and the coaxial cable/probe assemblies (for each VNA port) and, then, to perform an error-corrected resistance measurement of the

"Thru" and "Shunt" (i.e., "short-short", "open-open", "load-load") type of devices employed for both the calibration and the on-chip verification/de-embedding. A simplified circuit schematic of the measurement bench when considering only the DC characterization mode handled by SM #1 is depicted in Fig. B.1.

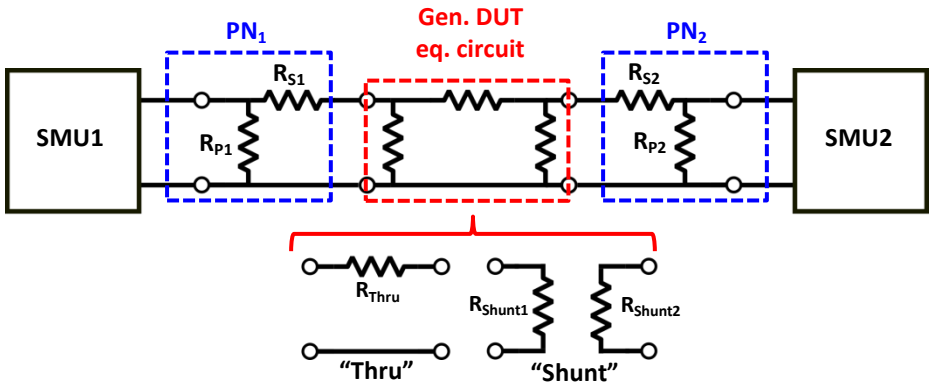


Fig. B.1 – Simplified diagram of the measurement bench when considering only the DC characterization mode handled by SM #1. R_{Si} and R_{Pi} refer to the parasitic resistances associated to the bias-tee networks and the coaxial cable/probe system connected to the i^{th} VNA port. The "Thru" and "Shunt" networks illustrate the simplification of the general resistive DUT equivalent circuit applied when dealing with the measurement of the Cascade ISS calibration elements or the on-chip auxiliary test circuits.

In Fig. B.1, the set of resistors $\{R_{Pi}, R_{Si}\}$ models the parasitic resistances associated to the bias-tee and the coaxial cable/probe system connected to the i^{th} VNA port while the "Thru" and "Shunt" networks sketch the two simplified circuit topologies that we usually deal with. The flowchart associated with SM #1 is reported in Fig. B.2. Once initialized the instruments and entered the main measurement parameters, the user has the possibility of performing a preliminary parasitic resistances measurement (i.e., identifying the $\{R_{Pi}, R_{Si}\}$ set) or loading the - previously measured - values from memory, or entering them manually. Then, he can select the specific test circuit to be characterized ("Thru" or "Shunt" network type, in our case) and start the characterization procedure. All the resistance measurement cycles are performed in the same way: once the voltage is set, a control loop is executed until the desired regime (stable steady state, after instrumentation/thermal transients are died) is reached. Then, a number of simultaneous voltage and current acquisitions (equal to the preset N_{acq} value) are performed and, on this basis, each DUT equivalent model resistance value is eventually computed as the average of the set of acquisitions performed in the various measurement cycles.

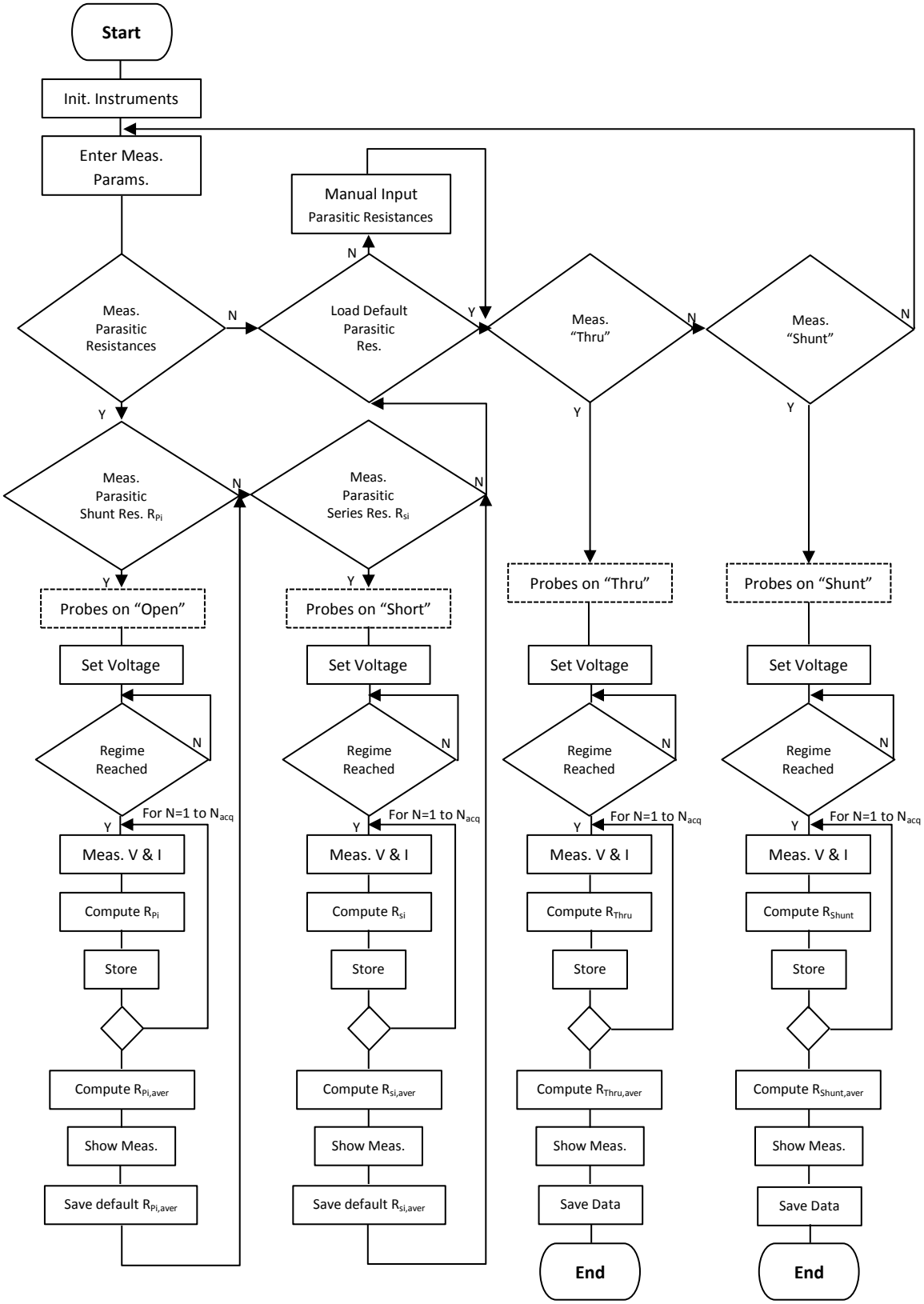


Fig. B.2 – Flowchart describing SM #1 operating mode.

B2 - Software Module #2

Software Module #2 (SM #2) manages the DC characterization of GFETs, including also the control of the laser source employed for the electro/optical tests. A simplified block diagram of the measurement bench illustrating the operation mode pertaining to SM #2 is depicted in Fig. B.3, where PN_1 and PN_2 refer to the parasitic resistive networks (bias-tees/coaxial cables/probes) described in the previous section.

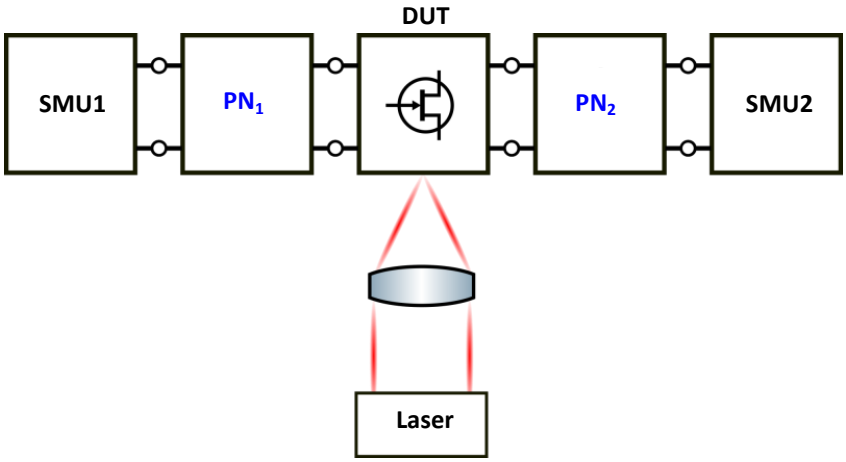


Fig. B.3 - Simplified diagram of the measurement bench referring to the operation mode handled by SM #2. PN_1 and PN_2 refer to the parasitic resistive networks (bias-tees/coaxial cables/probes) described in Fig. B.1.

The simplified flowchart of SM #2 is reported in Fig. B.4. The software program allows the user to choose between three different DC-characterization operating modes, namely: *single point*; *sweep* V_G */ step* V_D (i.e., sweep gate voltage / step drain voltage) and *sweep* V_D */ step* V_G (i.e., sweep drain voltage / step gate voltage). In the *single point* operating mode, the user provides the system with the gate and drain voltages (V_{GG} and V_{DD}, respectively) required for the desired GFET bias, as well as the nominal laser power to shine on the chip, if applicable. Then, the system sets the SMUs at the desired voltages and, after the regime check, simultaneously acquires the gate and drain voltages (V_G and V_D, respectively) and the associated currents (I_G and I_D, respectively). A so-called "Time domain" operation is also available. In this operating mode the user can acquire DC data for a predefined time interval (t_x in Fig. B.4) and at specific time steps (t_{step} in Fig. B.4) and observe GFETs bias transients (measurement- or thermal-

related). The *sweep/step* represents the main operating mode, employed for the GFETs combined DC/microwave characterization, as it will be described later.

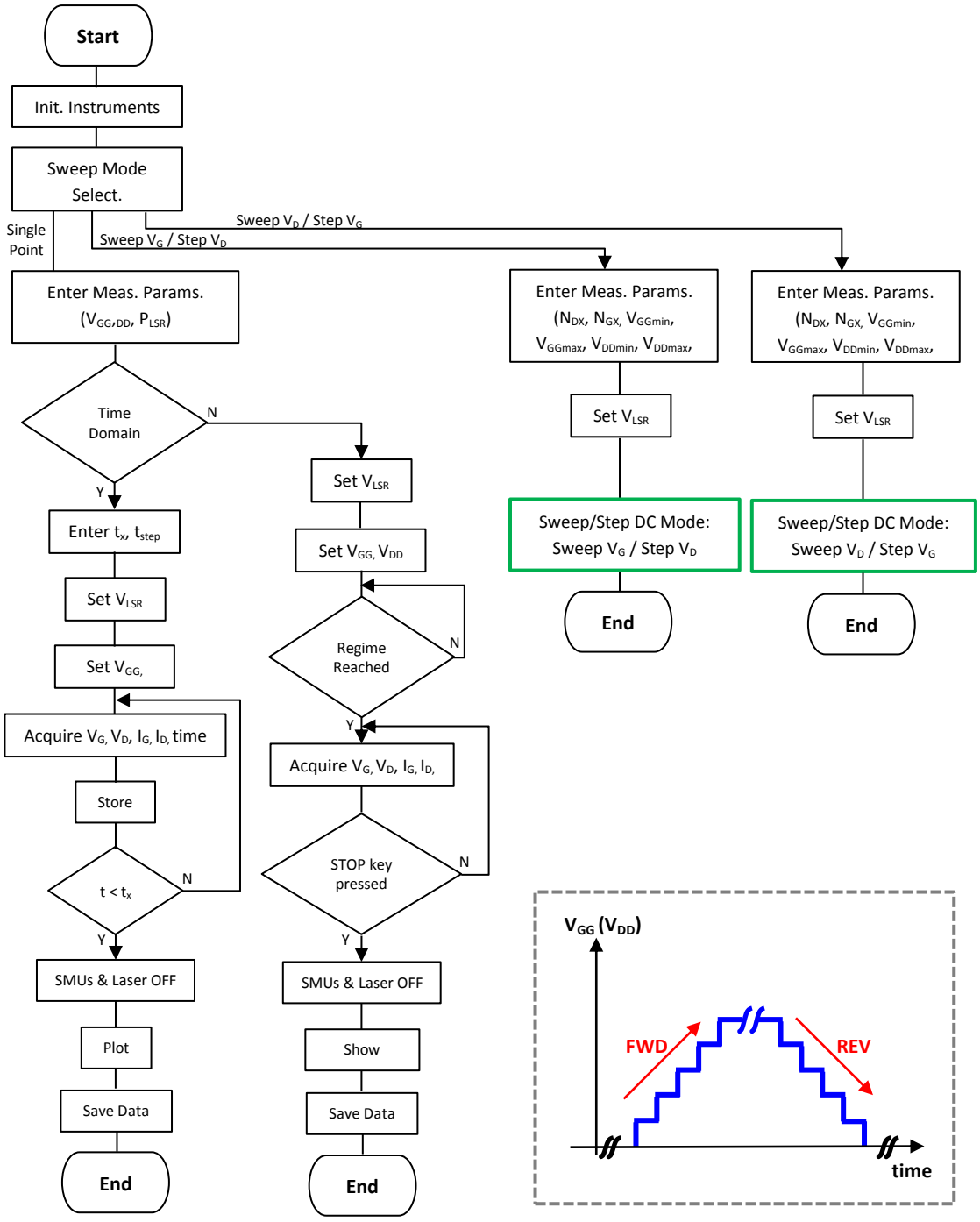


Fig. B.4 - Flowchart describing SM #2 operating mode. The inset sketches the *forward* (FWD) and *reverse* (REV) directions of the sweeping voltage (V_{GG} or V_{DD}, depending on the specific mode selected) performed for each measurement cycle.

In this case, the user is required to provide the system with the minimum and maximum values of both the gate and drain voltages ($V_{GGmin,\ max}$ and $V_{DDmin,\ max}$, respectively) and the number of points for each voltage (N_{DX} and N_{GX}, respectively). In addition, the laser power to be applied in each cycle can also be chosen together with the number of repeated (subsequent) measurement cycles (N_{cx}) to be executed for each step. A more detailed flowchart referring to the above-mentioned operating modes can be found in the green dotted region of Fig. B.5. If the *sweep* V_G */ step* V_D mode is selected, the system, for each V_D value, performs a gate-voltage sweep with a voltage step computed on the basis of the $V_{GGmin,\ max}$ and N_{GX} values set by the user. In particular, each gate-voltage sweep consists of two single measurement runs: the first one, is executed from V_{GGmin} to V_{GGmax}, i.e., in the *forward* (FWD) direction, while the second one is performed from V_{GGmax} to V_{GGmin}, i.e., in the *reverse* (REV) direction, as schematically depicted in the inset of Fig. B.4. This choice has been made to provide the user with a flexible operating mode allowing a more in-depth investigation of the hysteresis phenomena affecting graphene-based devices. As previously described, a checking of the regime condition of the swept variable is always performed as well as an averaging of the DC data acquired. As for the *sweep* V_D */ step* V_G option, measurements are executed following the same approach but, in this case, the voltage sweepings pertain the drain voltage, each one performed for a specific gate voltage.

B3 - Software Modules #3 and #4

Software Module #3 (SM #3) is the program specifically implemented to perform DC and microwave characterizations simultaneously. The corresponding flowchart is depicted in Fig. B.5 for the *sweep* V_G */ step* V_D mode that operates as described in the previous section. In addition, specific software routines handle the VNA settings and the RF data acquisition.

Software Module #4 (SM #4), on the other hand, manages photoelectric measurements required for the electro/optical GFETs characterization. As evident from the associated flowchart, reported in Fig. B.6, the main loop follows the same acquisition logic pertaining both SM #2 and SM #3. In addition, specific routines have been implemented to perform photovoltage measurements, in terms of both “in-phase”

(*X* in Fig. B.6) and "quadrature" (*Y* in Fig. B.6) voltage components, from the dual-phase lock-in amplifier employed.

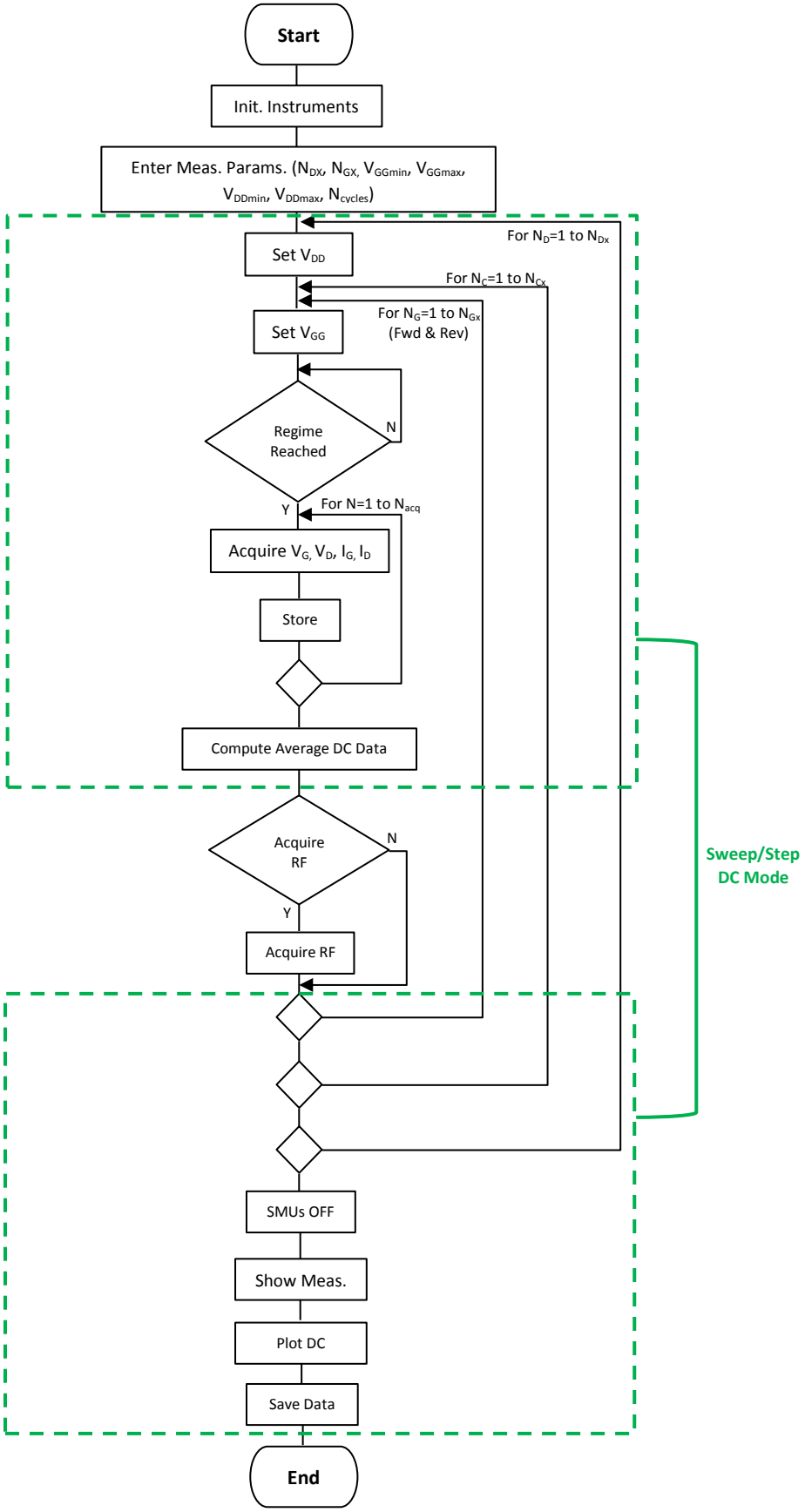


Fig. B.5 - Flowchart describing SM #3 operating mode.

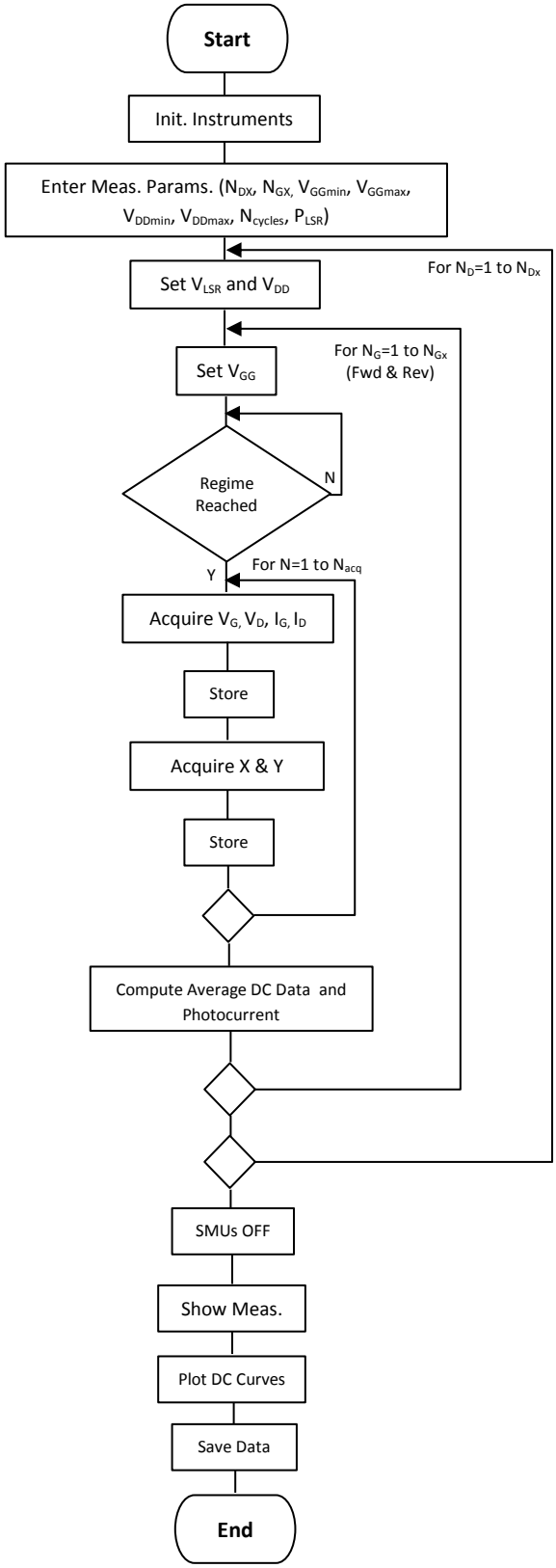


Fig. B.6 - Flowchart describing SM #4 operating mode.

References

[1] A. K. Geim and K. S. Novoselov, "The rise of graphene.," *Nat. Mater.*, vol. 6, no. 3, pp. 183–91, 2007.

[2] R. Peierls, "Quelques propriétés typiques des corps solides," *Ann. l'institut Henri Poincaré*, vol. 5, no. 3, pp. 177–222, 1935.

[3] L. D. Landau, "Zur Theorie der phasenumwandlungen II," *Phys. Zeitschrift der Sowjetunion*, vol. 11, pp. 26–35, 1937.

[4] J. A. Venables, G. D. T. Spiller, and M. Hanbucken, "Nucleation and growth of thin films," *Reports Prog. Phys.*, vol. 47, no. 4, pp. 399–459, Apr. 1984.

[5] M. Evans, James & Thiel, Patricia & C. Bartelt, "Morphological evolution during epitaxial thin film growth: Formation of 2D islands and 3D moundsle," *Surf. Sci. Rep.*, vol. 61, pp. 1–128, 2006.

[6] K. S. Novoselov *et al.*, "Electric field effect in atomically thin carbon films.," *Science*, vol. 306, no. 5696, pp. 666–9, 2004.

[7] K. S. Novoselov *et al.*, "Two-dimensional atomic crystals," *Proc. Natl. Acad. Sci.*, vol. 102, no. 30, pp. 10451–10453, 2005.

[8] J. C. Meyer, A. K. Geim, M. I. Katsnelson, K. S. Novoselov, T. J. Booth, and S. Roth, "The structure of suspended graphene sheets," *Nature*, vol. 446, no. 7131, pp. 60–63, 2007.

[9] S. Stankovich *et al.*, "Graphene-based composite materials," *Nature*, vol. 442, no. 7100, pp. 282–286, 2006.

[10] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. Mod. Phys.*, vol. 81, no. 1, pp. 109–162, 2009.

[11] P. R. Wallace, "The band theory of graphite," *Phys. Rev.*, vol. 71, no. 9, pp. 622–634, 1947.

[12] S. D. Sarma, S. Adam, E. H. Hwang, and E. Rossi, "Electronic transport in two dimensional graphene," *arXiv Prepr. arXiv1003.4731*, pp. 1–85, 2010.

[13] S. Reich, J. Maultzsch, C. Thomsen, and P. Ordejón, "Tight-binding description

of graphene," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 66, no. 3, pp. 354121–354125, 2002.

[14] C. Bena and S. A. Kivelson, "Quasiparticle scattering and local density of states in graphite," *Phys. Rev. B*, vol. 72, no. 12, 2005.

[15] K. S. Novoselov *et al.*, "Two-dimensional gas of massless Dirac fermions in graphene," *Nature*, vol. 438, no. November, pp. 197–200, 2005.

[16] K. I. Bolotin *et al.*, "Ultrahigh electron mobility in suspended graphene," *Solid State Commun.*, vol. 146, no. 9–10, pp. 351–355, 2008.

[17] Eduardo Fradkin, "Critical behavior of disordered degenerate semiconductors. II. Spectrum and transport properties in mean-field theory," *Phys. Rev. B*, vol. 33, no. 5, pp. 3263–3268, 1986.

[18] K. Nomura and a. H. MacDonald, "Quantum transport of massless Dirac fermions in graphene," *Phys. Rev. Lett.*, vol. 98, no. 7, 2007.

[19] P. M. Ostrovsky, I. V. Gornyi, and a. D. Mirlin, "Electron transport in disordered graphene," *Phys. Rev. B*, vol. 74, no. 23, p. 21, 2006.

[20] M. I. Katsnelson, "Zitterbewegung, chirality, and minimal conductivity in graphene," *Eur. Phys. J. B*, vol. 51, no. 2, pp. 157–160, 2006.

[21] J. Tworzydlo, B. Trauzettel, M. Titov, A. Rycerz, and C. W. J. Beenakker, "Quantum-limited shot noise in graphene," *Phys. Rev. Lett.*, vol. 96, pp. 1–6, 2006.

[22] F. Schwierz, "Graphene Transistors: Status, Prospects, and Problems," in *Proceedings of the Ieee*, 2013, vol. 101, no. 7, pp. 1567–1584.

[23] J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, and M. S. Fuhrer, "Intrinsic and extrinsic performance limits of graphene devices on SiO2," *Nat Nano*, vol. 3, no. 4, pp. 206–209, Apr. 2008.

[24] A. Geim, "Graphene Update," *Session J21: Focus Session: Graphene Transport I*, 2010. Available: http://meetings.aps.org/Meeting/MAR10/Event/118963.

[25] F. Schwierz, "Graphene transistors," *Nat. Nano.*, vol. 5, pp. 487–496, 2010.

[26] J. H. Chen, C. Jang, M. S. Fuhrer, E. D. Williams, and M. Ishigami, "Charged Impurity Scattering in Graphene," *Nat. Phys.*, vol. 4, pp. 377–381, Aug. 2008.

[27] J. Sabio, C. Seoánez, S. Fratini, F. Guinea, A. H. C. Neto, and F. Sols, "Electrostatic interactions between graphene layers and their environment," *Phys.*

Rev. B, vol. 77, no. 19, p. 195409, May 2008.

[28] Z. H. Ni, T. Yu, Y. H. Lu, Y. Y. Wang, Y. P. Feng, and Z. X. Shen, "Uniaxial Strain on Graphene : Raman Spectroscopy Study and Band Gap Opening," *ACS Nano*, vol. 2, no. 11, pp. 2301–2305, 2008.

[29] S.-M. Choi, S.-H. Jhi, and Y.-W. Son, "Effects of strain on electronic properties of graphene," *Phys. Rev. B*, vol. 81, no. 8, p. 81407, 2010.

[30] Y. W. Tan *et al.*, "Measurement of scattering rate and minimum conductivity in graphene," *Phys. Rev. Lett.*, vol. 99, no. 24, pp. 1–4, 2007.

[31] J. Yang, K. Jia, Y. Su, Y. Chen, and C. Zhao, "Hysteresis analysis of graphene transistor under repeated test and gate voltage stress," *J. Semicond.*, vol. 35, no. 9, p. 94003, 2014.

[32] O. Leenaerts, B. Partoens, and F. M. Peeters, "Adsorption of H2O, NH3, CO, NO2, and NO on graphene: A first-principles study," *Phys. Rev. B*, vol. 77, no. 12, p. 125416, 2008.

[33] Y. Yang, K. Brenner, and R. Murali, "The influence of atmosphere on electrical transport in graphene," *Carbon N. Y.*, vol. 50, no. 5, pp. 1727–1733, 2012.

[34] F. Guinea, M. I. Katsnelson, and M. A. H. Vozmediano, "Midgap states and charge inhomogeneities in corrugated graphene," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 77, no. 7, pp. 1–8, 2008.

[35] C. L. Li, "New position of Dirac points in the strained graphene reciprocal lattice," *AIP Adv.*, vol. 4, no. 8, 2014.

[36] E. H. Hwang, S. Adam, and S. Das Sarma, "Carrier transport in 2D graphene layers," *Phys. Rev. Lett.*, vol. 98, no. 18, 2007.

[37] J. H. Chen, W. G. Cullen, C. Jang, M. S. Fuhrer, and E. D. Williams, "Defect scattering in graphene," *Phys. Rev. Lett.*, vol. 102, no. 23, 2009.

[38] J. Martin *et al.*, "Observation of electron–hole puddles in graphene using a scanning single-electron transistor," *Nat. Phys.*, vol. 4, pp. 144–148, Nov. 2008.

[39] H. Wang, Y. Wu, C. Cong, J. Shang, and T. Yu, "Hysteresis of Electronic Transport in Graphene Transistors," *ACS Nano*, vol. 4, no. 12, p. 13, 2010.

[40] M. Lafkioti *et al.*, "Graphene on a hydrophobic substrate: Doping reduction and hysteresis suppression under ambient conditions," *Nano Lett.*, vol. 10, no. 4, pp. 1149–1153, 2010.

[41] C. M. Aguirre *et al.*, "The role of the oxygen/water redox couple in suppressing electron conduction in field-effect transistors," *Adv. Mater.*, vol. 21, no. 30, pp. 3087–3091, 2009.

[42] J. Moser, A. Barreiro, and A. Bachtold, "Current-induced cleaning of graphene," *Appl. Phys. Lett.*, vol. 91, no. 16, pp. 3–6, 2007.

[43] A. C. Ferrari *et al.*, "Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems," *Nanoscale*, vol. 7, no. 11, pp. 4598–4810, 2014.

[44] K. S. Novoselov, V. I. Fal'ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, "A roadmap for graphene," *Nature*, vol. 490, no. 7419, pp. 192–200, 2012.

[45] T. Moldt *et al.*, "High-yield production and transfer of graphene flakes obtained by anodic bonding," *ACS Nano*, vol. 5, no. 10, pp. 7700–7706, 2011.

[46] S. Dhar *et al.*, "A new route to graphene layers by selective laser ablation," *AIP Adv.*, vol. 1, no. 2, 2011.

[47] D. C. Elias *et al.*, "Dirac cones reshaped by interaction effects in suspended graphene," *Nat. Phys.*, vol. 8, p. 172, Feb. 2012.

[48] M. Lotya, P. J. King, U. Khan, S. De, and J. N. Coleman, "High-Concentration, Surfactant- Stabilized Graphene Dispersions," *ACS Nano*, vol. 4, no. 6, pp. 3155–3162, 2010.

[49] Y. Hernandez *et al.*, "High yield production of graphene by liquid phase exfoliation of graphite," *Nat. Nanotechnol.*, vol. 3, no. 9, pp. 563–8, 2008.

[50] S. Wang, Y. Zhang, N. Abidi, and L. Cabrales, "Wettability and surface free energy of graphene films," *Langmuir*, vol. 25, no. 18, pp. 11078–11081, 2009.

[51] A. O'Neill, U. Khan, P. N. Nirmalraj, J. Boland, and J. N. Coleman, "Graphene dispersion and exfoliation in low boiling point solvents," *J. Phys. Chem. C*, vol. 115, no. 13, pp. 5422–5428, 2011.

[52] M. Lotya *et al.*, "Liquid Phase Production of Graphene by Exfoliation of Graphite in Surfactant / Water Solutions," *J. Am. Chem. Soc.*, vol. 131, no. 10, pp. 3611–3620, 2009.

[53] T. Hasan *et al.*, "Solution-phase exfoliation of graphite for ultrafast photonics," *Phys. Status Solidi Basic Res.*, vol. 247, no. 11–12, pp. 2953–2957, 2010.

[54] A. V. T. A.J. Van Bommel, J.E. Crombeen, "LEED and Auger electron

observations of the SiC(0001) surface," *Surf. Sci.*, vol. 48, no. 2, pp. 463–472, Mar. 1975.

[55] A. Charrier *et al.*, "Solid-state decomposition of silicon carbide for growing ultra-thin heteroepitaxial graphite films," *J. Appl. Phys.*, vol. 92, no. 5, pp. 2479–2484, 2002.

[56] I. Forbeaux, J. M. Themlin, A. Charrier, F. Thibaudau, and J. M. Debever, "Solid-state graphitization mechanisms of silicon carbide 6H-SiC polar faces," *Appl. Surf. Sci.*, vol. 162, pp. 406–412, 2000.

[57] C. Virojanadara, M. Syväjarvi, R. Yakimova, L. I. Johansson, A. A. Zakharov, and T. Balasubramanian, "Homogeneous large-area graphene layer growth on 6H-SiC(0001)," *Phys. Rev. B*, vol. 78, no. 24, p. 245403, Dec. 2008.

[58] N. Mishra, J. Boeckl, N. Motta, and F. Iacopi, "Graphene growth on silicon carbide: A review," *Phys. Status Solidi*, vol. 213, no. 9, pp. 2277–2289, 2016.

[59] S. N. Yannopoulos, A. Siokou, N. K. Nasikas, V. Dracopoulos, F. Ravani, and G. N. Papatheodorou, "CO2-Laser-Induced Growth of Epitaxial Graphene on 6H-SiC(0001)," *Adv. Funct. Mater.*, vol. 22, no. 1, pp. 113–120, 2012.

[60] D. Perrone *et al.*, "Study on the possibility of graphene growth on 4H-silicon carbide\nsurfaces via laser processing," in *Proceedings of the Fifth International WLT-Conference on Lasers in Manufacturing 2009*, 2009, no. June, pp. 1–6.

[61] N. A. Kholin, E. Rut'kov, and A. Tontegode, "The nature of the adsorption bond between graphite islands and iridium surface," *Surf. Sci.*, vol. 139, no. 1, pp. 155–172, Apr. 1984.

[62] X. Li *et al.*, "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," *Science (80-.).*, vol. 324, no. 5932, pp. 1312–1314, 2009.

[63] S. Bae *et al.*, "Roll-to-roll production of 30-inch graphene films for transparent electrodes," *Nat Nano*, vol. 5, no. 8, pp. 574–578, Aug. 2010.

[64] D. Yoon, Y. W. Son, and H. Cheong, "Negative thermal expansion coefficient of graphene measured by raman spectroscopy," *Nano Lett.*, vol. 11, no. 8, pp. 3227–3231, 2011.

[65] X. Li, W. Cai, L. Colombo, and R. Ruoff, "Evolution of graphene growth on Ni and Cu by carbon isotope labeling," *Nano Lett.*, vol. 12, no. Cvd, pp. 1–15, 2009.

[66] Y. Kim *et al.*, "Low-temperature synthesis of graphene on nickel foil by

microwave plasma chemical vapor deposition," *Appl. Phys. Lett.*, vol. 98, no. 26, pp. 2–4, 2011.

[67] T. Terasawa and K. Saiki, "Growth of graphene on Cu by plasma enhanced chemical vapor deposition," *Carbon N. Y.*, vol. 50, no. 3, pp. 869–874, 2012.

[68] J. Lee *et al.*, "RF performance of pre-patterned locally-embedded-back-gate graphene device," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2, no. c, pp. 568–571, 2010.

[69] W. S. Hummers and R. E. Offeman, "Preparation of Graphitic Oxide," *J. Am. Chem. Soc.*, vol. 80, no. 6, p. 1339, 1958.

[70] S. Mao, H. Pu, and J. Chen, "Graphene oxide and its reduction: modeling and experimental progress," *RSC Adv.*, vol. 2, no. 7, p. 2643, 2012.

[71] H. He, J. Klinowski, M. Forster, and A. Lerf, "A new structural model for graphite oxide," *Chem. Phys. Lett.*, vol. 287, no. 1–2, pp. 53–56, 1998.

[72] A. Lerf, H. He, M. Forster, and J. Klinowski, "Structure of Graphite Oxide Revisited," *J. Phys. Chem. B*, vol. 102, no. 23, pp. 4477–4482, 1998.

[73] I. K. Moon, J. Lee, R. S. Ruoff, and H. Lee, "Reduced graphene oxide by chemical graphitization," *Nat. Commun.*, vol. 1, p. 73, Sep. 2010.

[74] T. Szabó *et al.*, "Evolution of Surface Functional Groups in a Series of Progressively Oxidized Graphite Oxides," *Chem. Mater.*, vol. 18, no. 11, pp. 2740–2749, 2006.

[75] W. Gao, L. B. Alemany, L. Ci, and P. M. Ajayan, "New insights into the structure and reduction of graphite oxide," *Nat. Chem.*, vol. 1, no. 5, pp. 403–408, 2009.

[76] Z. Fan *et al.*, "Facile synthesis of graphene nanosheets via fe reduction of exfoliated graphite oxide," *ACS Nano*, vol. 5, no. 1, pp. 191–198, 2011.

[77] I. Jung *et al.*, "Reduction Kinetics of Graphene Oxide Determined by Electrical Transport Measurements and Temperature Programmed Desorption," *J. Phys. Chem. C*, vol. 113, no. 43, pp. 18480–18486, 2009.

[78] C. Mattevi *et al.*, "Evolution of electrical, chemical, and structural properties of transparent and conducting chemically derived graphene thin films," *Adv. Funct. Mater.*, vol. 19, no. 16, pp. 2577–2583, 2009.

[79] A. B. Héctor, M. Jie, L. Zunfeng, B. Randall, M. Stoltenberg Zhenan, and C.

Yongsheng, “Evaluation of Solution-Processed Reduced Graphene Oxide Films as as Transparent Conductors,” *ACS Nano*, vol. 2, no. 3, pp. 463–470, 2008.

[80] D. Yang *et al.*, “Chemical analysis of graphene oxide films after heat and chemical treatments by X-ray photoelectron and Micro-Raman spectroscopy,” *Carbon N. Y.*, vol. 47, no. 1, pp. 145–152, 2009.

[81] L. J. Cote, R. Cruz-Silva, and J. Huang, “Flash Reduction and Patterning of Graphite Oxide and Its Polymer Composite,” *J. Am. Chem. Soc.*, vol. 131, no. 31, pp. 11027–11032, Aug. 2009.

[82] E. Kymakis, C. Petridis, T. D. Anthopoulos, and E. Stratakis, “Laser-assisted reduction of graphene oxide for flexible, large-area optoelectronics,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 20, no. 1, 2014.

[83] Y. Zhang *et al.*, “Direct imprinting of microcircuits on graphene oxides film by femtosecond laser reduction,” *Nano Today*, vol. 5, no. 1, pp. 15–20, 2010.

[84] R. Trusovas *et al.*, “Reduction of graphite oxide to graphene with laser irradiation,” *Carbon N. Y.*, vol. 52, no. Supplement C, pp. 574–582, 2013.

[85] P. Kumar, K. S. Subrahmanyam, and C. N. R. Rao, “Graphene Patterning and Lithography Employing Laser/Electron-Beam Reduced Graphene Oxide and Hydrogenated Graphene,” *Mater. Express*, vol. 1, no. 3, pp. 252–256, 2011.

[86] A. Benfante, “Diamond-based X-ray detectors: physics and technology,” University of Palermo, 2014.

[87] E. V Castro *et al.*, “Biased Bilayer Graphene: Semiconductor with a Gap Tunable by the Electric Field Effect,” *Phys. Rev. Lett.*, vol. 99, no. 21, p. 216802, Nov. 2007.

[88] P. Gava, M. Lazzeri, A. M. Saitta, and F. Mauri, “Ab initio study of gap opening and screening effects in gated bilayer graphene,” *Phys. Rev. B*, vol. 79, no. 16, p. 165431, Apr. 2009.

[89] M. Y. Han, B. Özyilmaz, Y. Zhang, and P. Kim, “Energy Band-Gap Engineering of Graphene Nanoribbons,” *Phys. Rev. Lett.*, vol. 98, no. 20, p. 206805, May 2007.

[90] P. Kim, M. Y. Han, A. F. Young, I. Meric, and K. L. Shepard, “Graphene nanoribbon devices and quantum heterojunction devices,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 241–244, 2009.

[91] T. Fang, A. Konar, H. Xing, and D. Jena, “Mobility in semiconducting graphene nanoribbons: Phonon, impurity, and edge roughness scattering,” *Phys. Rev. B*, vol. 78, no. 20, p. 205403, Nov. 2008.

[92] B. Obradovic *et al.*, “Analysis of graphene nanoribbons as a channel material for field-effect transistors,” *Appl. Phys. Lett.*, vol. 88, no. 14, 2006.

[93] G. Gonzalez, *Microwave Transistors Amplifiers. Analysis and Design*. Prentice-Hall, Inc., 1997.

[94] A. Balandin *et al.*, “Superior Thermal Conductivity of Single Layer Graphene,” *Nano Lett*, vol. 8, pp. 902–907, 2008.

[95] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, “Metal/graphene contact as a performance Killer of ultra-high mobility graphene - Analysis of intrinsic mobility and contact resistance,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 565–568, 2009.

[96] J. J. L. Frank Schwiers, *Modern Microwave Transistors: Theory, Design, and Performance*. Wiley, 2002.

[97] E. Watanabe, A. Conwill, D. Tsuya, and Y. Koide, “Low contact resistance metals for graphene based devices,” *Diam. Relat. Mater.*, vol. 24, pp. 171–174, 2012.

[98] J. T. Smith, A. D. Franklin, D. B. Farmer, and C. D. Dimitrakopoulos, “Reducing contact resistance in graphene devices through contact area patterning,” *ACS Nano*, vol. 7, no. 4, pp. 3661–3667, 2013.

[99] J. Kedzierski *et al.*, “Epitaxial Graphene Transistors on SiC Substrates,” *Electron Devices, IEEE Trans.*, vol. 55, no. 8, pp. 2078–2085, 2008.

[100] M. C. Lemme, T. J. Echtermeyer, M. Baus, and K. Heinrich, “A graphene field-effect device,” *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, 2007.

[101] I. Meric, N. Baklitskaya, P. Kim, and K. L. Shepard, “RF performance of top-gated, zero-bandgap graphene field-effect transistors,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, no. c, pp. 2–5, 2008.

[102] Y. M. Lin *et al.*, “Development of graphene FETs for high frequency electronics,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 237–240, 2009.

[103] Y.-M. Lin *et al.*, “100-GHz Transistors from Wafer-Scale Epitaxial Graphene,” *Science (80-.).*, vol. 327, no. 5966, pp. 662–662, 2010.

[104] Y. Wu *et al.*, "State-of-the-Art Graphene High-Frequency Electronics," *Nano Lett.*, vol. 12, no. 6, pp. 3062–3067, 2012.

[105] R. Cheng *et al.*, "High-frequency self-aligned graphene transistors with transferred gate stacks," *Proc. Natl. Acad. Sci.*, vol. 109, no. 29, pp. 11588–11592, 2012.

[106] C. Yu *et al.*, "Improvement of the Frequency Characteristics of Graphene Field-Effect Transistors on SiC Substrate," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1339–1342, 2017.

[107] R. R. Nair *et al.*, "Fine Structure Constant Defines Visual Transperency of Graphene," *Science (80-.).*, vol. 320, no. June, p. 2008, 2008.

[108] F. Bonaccorso, Z. Sun, T. Hasan, and A. C. Ferrari, "Graphene Photonics and Optoelectronics," *Nat. Photonics*, vol. 4, no. 9, pp. 611–622, 2010.

[109] P. Avouris, "Graphene: Electronic and Photonic Properties and Devices," *Nano Lett.*, vol. 10, pp. 4285–4294, 2010.

[110] F. Xia, T. Mueller, Y. Lin, A. Valdes-Garcia, and P. Avouris, "Ultrafast graphene photodetector," *Nat. Nanotechnol.*, vol. 4, no. 12, pp. 839–843, 2009.

[111] H. Zimmermann, *Integrated Silicon Optoelectronics*, 2010.

[112] Z. Sun and H. Chang, "Graphene and graphene-like two-dimensional materials in photodetection: Mechanisms and methodology," *ACS Nano*, vol. 8, no. 5, pp. 4133–4156, 2014.

[113] F. H. Koppens, T. Mueller, P. Avouris, a C. Ferrari, M. S. Vitiello, and M. Polini, "Photodetectors based on graphene, other two-dimensional materials and hybrid systems," *Nat. Nanotechnol.*, vol. 9, no. 10, pp. 780–793, 2014.

[114] T. Mueller, F. Xia, M. Freitag, J. Tsang, and P. Avouris, "Role of contacts in graphene transistors: A scanning photocurrent study," *Phys. Rev. B*, vol. 79, no. 24, p. 245430, Jun. 2009.

[115] E. C. Peters, E. J. H. Lee, M. Burghard, and K. Kern, "Gate dependent photocurrents at a graphene p-n junction," *Appl. Phys. Lett.*, vol. 97, no. 19, pp. 2010–2013, 2010.

[116] D. Farmer and R. Golizadeh-Mojarad, "Chemical doping and electron−hole conduction asymmetry in graphene devices," *Nano Lett.*, vol. 9, pp. 388–392, 2008.

[117] M. C. Lemme *et al.*, "Gate-activated photoresponse in a graphene p-n junction," *Nano Lett.*, vol. 11, no. 10, pp. 4134–4137, 2011.

[118] G. Giovannetti, P. A. Khomyakov, G. Brocks, V. M. Karpan, J. Van Den Brink, and P. J. Kelly, "Doping graphene with metal contacts," *Phys. Rev. Lett.*, vol. 101, no. 2, pp. 4–7, 2008.

[119] M. Freitag, T. Low, F. Xia, and P. Avouris, "Photoconductivity of biased graphene," *Nat. Photonics*, vol. 7, no. January 2013, pp. 53–59, 2012.

[120] V. N. Kotov, B. Uchoa, V. M. Pereira, F. Guinea, and A. H. Castro Neto, "Electron-Electron Interactions in Graphene: Current Status and Perspectives," *Rev. Mod. Phys.*, vol. 84, no. 3, pp. 1067–1125, Jul. 2012.

[121] S. Piscanec, M. Lazzeri, F. Mauri, A. C. Ferrari, and J. Robertson, "Kohn Anomalies and Electron-Phonon Interactions in Graphite," *Phys. Rev. Lett.*, vol. 93, no. 18, p. 185503, Oct. 2004.

[122] J. C. W. Song, M. S. Rudner, C. M. Marcus, and L. S. Levitov, "Hot Carrier Transport and Photocurrent Response in Graphene," *Nano Lett.*, vol. 11, no. d, pp. 4688–4692, 2011.

[123] V. Ryzhii, V. Mitin, M. Ryzhii, N. Ryabova, and T. Otsuji, "Device Model for Graphene Nanoribbon Phototransistor," *Appl. Phys. Express*, vol. 1, no. 6, p. 63002, 2008.

[124] T. Mueller, F. Xia, and P. Avouris, "Graphene photodetectors for high-speed optical communications," *Nat. Photonics*, vol. 4, no. 5, pp. 297–301, 2010.

[125] M. Freitag, T. Low, and P. Avouris, "Increased responsivity of suspended graphene photodetectors," *Nano Lett.*, vol. 13, no. 4, pp. 1644–1648, 2013.

[126] X. Gan *et al.*, "Chip-integrated ultrafast graphene photodetector with high responsivity," *Nat. Photonics*, vol. 7, no. 11, pp. 883–887, 2013.

[127] M. Furchi *et al.*, "Microcavity-integrated graphene photodetector," *Nano Lett.*, vol. 12, no. 6, pp. 2773–2777, 2012.

[128] Z. Fang *et al.*, "Plasmon-induced doping of graphene," *ACS Nano*, vol. 6, no. 11, pp. 10222–10228, 2012.

[129] X. Wang, L. Zhi, and K. Müllen, "Transparent, conductive graphene electrodes for dye-sensitized solar cells," *Nano Lett.*, vol. 8, no. 1, pp. 323–327, 2008.

[130] L. Vicarelli *et al.*, "Graphene field-effect transistors as room-temperature

terahertz detectors.," *Nat. Mater.*, vol. 11, no. 10, pp. 865–71, 2012.

[131] "Roditi - Sapphire Wafers C-Plane." [Online]. Available: http://www.roditi.com/SingleCrystal/Sapphire/C-Plane.html.

[132] E. Pallecchi, C. Benz, a. C. Betz, H. V. Löhneysen, B. Plaçais, and R. Danneau, "Graphene microwave transistors on sapphire substrates," *Appl. Phys. Lett.*, vol. 99, no. 11, p. 113502, 2011.

[133] "Raith - eLine Plus." [Online]. Available: https://www.raith.com/products/eline-plus.html.

[134] "Showa Denko K.K. - Espacer." [Online]. Available: http://www.showadenko.us/products/espacer/.

[135] "Picosun - R-200 Advanced." [Online]. Available: http://www.picosun.com/product/r-200-advanced/.

[136] "Cambridge Nanotech - Savannah." [Online]. Available: http://www.cambridgenanotechald.com/products/Savannah-ald-system.shtml.

[137] X. Wang, J. Li, Q. Zhong, Y. Zhong, and M. Zhao, "Wafer-scale synthesis and transfer of monolayer graphene," *Proc. IEEE Conf. Nanotechnol.*, pp. 652–655, 2013.

[138] A. C. Ferrari, "Raman spectrum of graphene and graphene layers," *Phys. Rev. Lett.*, vol. 97, p. 187401, 2006.

[139] M. A. Giambra, "Electrical and optical properties of Graphene Field-Effect Transistors (GFETs) fabricated on sapphire," University of Palermo, 2017.

[140] "Keysight Technologies - N5232A PNA-L Microwave Network Analyzer." [Online]. Available: http://www.keysight.com/en/pdx-x201915-pn-N5232A/pna-l-microwave-network-analyzer-20-ghz?cc=US&lc=eng.

[141] "Cascade Microtech, Inc. - RF Microwave Probes." [Online]. Available: https://www.cascademicrotech.com/products/probes/rf-microwave.

[142] "Keithley - 2400 Source Meter Unit." [Online]. Available: https://www.tek.com/keithley-source-measure-units/keithley-smu-2400-series-sourcemeter.

[143] "Pulsar Microwave Corporation - BT-50-400D Bias Tee." [Online]. Available: https://www.pulsarmicrowave.com/product/bias_tee/BT-50-400D.

[144] "IPG Photonics - ELT Series Erbium Fiber Lasers." [Online]. Available:

http://www.ipgphotonicskorea.com/Collateral/Documents/English-US/ELTSeries.pdf.

[145] “Stanford Research Systems - SR830 Lock-In Amplifier.” [Online]. Available: http://www.thinksrs.com/products/SR810830.htm.

[146] G. P. Agrawal, *Fiber-Optic Communications Systems*. John Wiley & Sons, Inc., 2002.

[147] Y. Wu *et al.*, “High-frequency, scaled graphene transistors on diamond-like carbon.,” *Nature*, vol. 472, no. 7341, pp. 74–8, 2011.

[148] “Roditi - Sapphire.” [Online]. Available: http://www.roditi.com/SingleCrystal/Sapphire/sapphire.html.

[149] M. C. a. M. Koolen, J. a. M. Geelen, and M. P. J. G. Versleijen, “An improved de-embedding technique for on-wafer high-frequency characterization,” *Proc. 1991 Bipolar Circuits Technol. Meet.*, pp. 188–191, 1991.

[150] Y. Taur, “CMOS design near the limit of scaling,” *IBM J. Res. Dev.*, vol. 46, no. 2.3, pp. 213–222, 2002.

[151] G. D. Wilk, R. M. Wallace, and J. M. Anthony, “High-K gate dielectrics: Current status and materials properties considerations,” *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, 2001.

[152] J. Robertson, “High dielectric constant gate oxides for metal oxide Si transistors,” *Reports Prog. Phys.*, vol. 69, no. 2, pp. 327–396, 2005.

[153] “AZO Materials - Al2O3.” [Online]. Available: https://www.azom.com/properties.aspx?ArticleID=52.

[154] “AZO Materials - TiO2.” [Online]. Available: https://www.azom.com/properties.aspx?ArticleID=1179.

[155] “American elements - HfO2.” [Online]. Available: https://www.americanelements.com/hafnium-oxide-12055-23-1.

[156] H. Fang and W. Hu, “Photogating in Low Dimensional Photodetectors,” *Adv. Sci.*, vol. 4, no. 12, 2017.

[157] A. Benfante, A. Tomada, and G. A. Carini, “Novel diamond X - ray detectors with patterned reduced graphene oxide contacts,” in *IEEE NSS-MIC-RTSD*, 2015, pp. 1–3.

[158] J. Morse, B. Solar, and H. Graafsma, “Diamond X-ray beam-position monitoring

using signal readout at the synchrotron radiofrequency," *J. Synchrotron Radiat.*, vol. 17, no. 4, pp. 456–464, 2010.

[159] J. Hicks *et al.*, "X-ray radiation effects in multilayer epitaxial graphene," *Appl. Phys. Lett.*, vol. 99, p. 232102, 2011.

[160] "elementsix." [Online]. Available: http://e6cvd.com/.

[161] "elementsix - TM180." [Online]. Available: http://e6cvd.com/us/material/polycrystalline/tm180-10-0x10-0mm-0-30mm-thick-pl.html.

[162] S. Michaelson and A. Hoffman, "Ambient contamination of poly-crystalline diamond surfaces studied by high-resolution electron energy loss spectroscopy and X-ray photoelectron spectroscopy," *Diam. Relat. Mater.*, vol. 17, no. 6, pp. 920–924, 2008.

[163] T. Teraji, "Chemical vapor deposition of homoepitaxial diamond films," *Phys. Status Solidi*, vol. 203, no. 13, pp. 3324–3357, 2006.

[164] P. W. May, "Diamond Thin Films: A 21st-Century Material," *Philos. Trans. Math. Phys. Eng. Sci.*, vol. 358, no. 1766, pp. 473–495, 2014.

[165] J. Lettington, A.H., Steeds, *Thin Film Diamond*. Springer, 1994.

[166] J. Ristein, F. Maier, M. Riedel, M. Stammer, and L. Ley, "Diamond surface conductivity experiments and photoelectron spectroscopy," *Diam. Relat. Mater.*, vol. 10, no. 3, pp. 416–422, 2001.

[167] J. Shirafuji and T. Sugino, "Electrical properties of diamond surfaces," *Diam. Relat. Mater.*, vol. 5, no. 6, pp. 706–713, 1996.

[168] "Graphene Supermarket - Ultra Highly Concentrated Single-Layer Graphene Oxide." [Online]. Available: https://graphene-supermarket.com/Ultra-Highly-Concentrated-Graphene-Oxide-60ml.html.

[169] "Thermo Scientific - XPS." [Online]. Available: https://xpssimplified.com/elements/carbon.php.

[170] H. Chang *et al.*, "Regulating Infrared Photoresponses in Reduced Graphene Oxide Phototransistors by Defect and Atomic Structure Control," *ACS Nano*, no. 7, pp. 6310–6320, 2013.

[171] K. Kurokawa, "Power Waves and the Scattering Matrix," *IEEE Trans. Microw. Theory Tech.*, vol. 13, no. 2, pp. 194–202, 1965.

[172] D. Anderson, L. Smith, and J. Gruszynski, “Test & Measurement Application Note 95-1 S-Parameter Techniques,” 1997.

[173] M. Hiebel, *Fundamentals of Vector Network Analysis*. Rohde & Schwarz, 2008.

[174] M. Hiebel, “Vector Network Analyzer (VNA) Calibration: The Basics,” 2008.

[175] F. Purroy and L. Pradell, “New theoretical analysis for the LRRM calibration technique for vector network analyzers,” *IEEE Trans. Instrum. Meas.*, vol. 50, no. 5, pp. 1307–1314, 2001.

[176] Anritsu Company, “Understanding VNA Calibration,” p. 36, 2012.

[177] A. Davidson, K. Jones, and E. Strid, “LRM and LRRM Calibrations with Automatic Determination of Load Inductance,” *36th ARFTG Conf. Dig.*, vol. 18, no. 503, pp. 57–63, 1990.

[178] “Cascade Microtech, Inc. - Impedance Standard Substrates.” [Online]. Available: https://www.cascademicrotech.com/products/calibration-tools/impedance-substrate.

[179] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, “A New Method for Determining the FET Small-Signal Equivalent Circuit,” *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 7, pp. 1151–1159, 1988.

[180] S. Goudos, “On-Wafer Microwave De-Embedding Techniques,” in *Microwave Systems and Applications*, InTech, 2017.

[181] P. Troughton, “Measurement Techniques in Microstrip,” *Electron. Lett.*, vol. 5, no. 2, pp. 1968–1969, 1969.

[182] S. A. Ivanov and V. N. Peshlov, “Ring-resonator method - Effective procedure for investigation of microstrip line,” *IEEE Microw. Wirel. Components Lett.*, vol. 13, no. 6, pp. 244–246, 2003.

[183] “NI AWR Design Environment - Analyst.” [Online]. Available: http://www.awrcorp.com/products/ni-awr-design-environment/analyst.

[184] “Trans Era - HTBasic.” [Online]. Available: http://transera.com/htbasic/.

Ringraziamenti

Desidero ringraziare, in primo luogo, i miei tutor, prof. Alessandro Busacca, prof. Enrico Calandra e dr. Salvatore Stivala, per avermi concretamente "accompagnato" durante i tre anni e per avermi dato l'opportunità di svolgere questo lavoro.
Grazie al prof. Busacca, per i suoi consigli e per l'impegno costante che mostra nel supportare gli studenti tutti.
Ringrazio Salvatore, per avermi confermato, con il suo esempio, come gentilezza, disponibilità e preparazione tecnica non siano fattori incompatibili.
Un grazie particolare al prof. Calandra, per il suo aiuto e per la sua disponibilità durante tutte le fasi che hanno condotto alla stesura di questo manoscritto e per essermi stato accanto molto più di quanto, normalmente, competa ad un tutor.
Un sentito ringraziamento anche alla sig.ra Calandra per la sua sincera gentilezza.
Ringrazio, inoltre, il collega Marco Angelo Giambra, con il quale ho condiviso una parte di questo lavoro, il dr. Riccardo Pernice e il dr. Antonino Parisi.

Passando dall'Italia alla Germania, desidero ringraziare il dr. Romain Danneau e il prof. Ralph Krupke per avermi accolto presso il loro istituto e Simone Dehm per il suo importante supporto tecnico.
Grazie anche ai colleghi Pranauv Balaji Selvasundaram, Preeti Pandey e Rainer Kraft per il loro aiuto all'interno dei laboratori dell'INT.
Un ringraziamento speciale va alla mia amica Hui Yu Liu, per aver condiviso con me momenti divertenti e non durante la mia permanenza in Germania.

Con riferimento alla mia esperienza negli Stati Uniti, voglio ringraziare lo staff di SLAC, SNF e SNC ed in particolare: Gabriella Carini, Astrid Tomada, Maurice Stevens, Uli Thumser, Sven Herrmann e Traci Kawakami.
Ringrazio, in particolare, Gabriella e il prof. Claudio Arnone per avermi dato la possibilità di tornare a SLAC una seconda volta.
Grazie anche a Stefan Zappe, per essere stato molto più di un semplice coinquilino.

Ringrazio, inoltre, Giulia per aver sopportato i miei sbalzi d'umore.

Il ringraziamento più importante, infine, ancora una volta, ai miei genitori, per avermi fatto sentire a casa anche quando non lo ero.