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ELECTRICAL AND OPTICAL PROPERTIES OF GRAPHENE FIELD-EFFECT TRANSISTORS (GFETs) FABRICATED ON SAPPHIRE

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Electrical and optical properties of graphene field-effect transistors (GFETs) fabricated on sapphire

Ph.D. thesis

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Abstract

Graphene, a monolayer of carbon atoms arranged in a honeycomb lattice, is still one of the most investigated fields of research in condensed matter physics since its discovery in 2004 [1], [2]. The reasons for its amazing success are the unique electronic, optical, mechanical and thermal properties such as its extremely high charge carrier motility, the quantum Hall effect observed at room temperature and its flexibility, as well as mechanical strength. Among the various potential application fields, high frequency electronics and photodetection represent two of the most promising ones. Graphene field effect transistors (GFETs) for high frequency applications have been already fabricated [3] exploiting the electronic transport properties of the graphene. GFETs have rapidly developed and are now considered for post-silicon Electronics. However, different techniques have been developed to grow graphene to large scale production, such as CVD graphene or graphitization of silicon carbide. Promising results exploiting such techniques have been reached inducing the research to deeply invest on this field, although the quality of the obtained graphene is not equal to that obtained by mechanical exfoliation in terms of mobility [4]. Fabrication of high-performances GFETs is an important challenge, since a conventional device-fabrication process can damage the graphene lattice, or introduce excessive parasitic capacitance

or series resistance, thus resulting in degraded electronic performances [5]. The high graphene carriers mobility is not the only important feature in graphene-based devices, in fact, concerning high frequency transistors, the possibility to fabricate devices with extremely short channels is highly desired, since this could allow GFETs to be scaled to shorter channel lengths and higher speeds without encountering short-channel effects which restrict the performance of existing devices [3].

On the other hand, graphene absorbs visible in a wide frequency range with an almost constant absorption rate of 2.3% [6]. Photodetectors made of graphene operating at 10 Gbps have already been realized [7]. Combining electronic and optical signal processing is highly desirable, since higher processing speed at less power consumption is possible. A strong nonlinear electromagnetic response of graphene due to the linear dispersion relation has been proposed [8], [9] and experimentally verified [10]. This paves the way to a new field of potential applications for graphene: nonlinear signal operations such as modulators, demodulators or frequency converters (mixers). These components are needed, for instance, in telecommunication engineering.

Aim of my PhD work has been the design, fabrication and characterization of GFETs for both high frequency applications and photodetection. The limits of GFETs performances are due to several effects, such as contact resistance, degradation of the mobility and hysteresis. In the work described in this thesis, great effort has been made to minimize these effects in order fully exploit graphene properties. The work has been carried out within the *Laboratorio di Elettronica delle Microonde* (LEM) of the University of Palermo (Italy) and the *Institute of Technology* (INT) of *Karlsruher Institut für Technologie* (KIT, Germany). Devices manufacturing have been carried out at the INT with the aim to fabricate different families of transistors with several device structures. The influence of the layout on microwave performances of Graphene Field Effect Transistors has been investigated finding an important role of the device structure. This work has been associated with a preliminary optical characterization of the devices under test. Finally, a subsequent device family has been fabricated with the aim to analyze the role of the gate dielectric on RF/Opto fields. A supplementary work has been made on GFETs trying to exploit a novel geometry to improve their high frequency performances and on phase change material employed for mixed mode in nanophotonic circuits aimed to non-volatile memory application.

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Germany for me was not just the PhD ... indeed, I remember when I arrived there and I did not know a German word ... all new, the scents, the flavors, the climate ... but above all, the people ... I was there before the beginning of this Doctoral course, in order to make experience, to test myself. If I managed to "survive," I have to thank special people. I refer to my colleagues at "La Pizza". They welcomed me, they made me feel at home. They helped me, they made me understand that I could make it; Tighten your teeth, wash dishes, tables and bake pizzas. The jokes and affection of Gino Pinto and Sino Pendola, the sweetness of Herman, the mythical Ciccio Meli who also gave me a bed and a room to sleep, like Gino who I thank so much. If I was able to stay, there is also thanks to you and I am grateful to you.
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CHAPTER 1

1. Graphene properties

The properties of graphene derive from its crystallographic structure and its 2D nature. It is a single two-dimensional layer of sp^2 hybridized carbon atoms bound in a hexagonal lattice structure (Fig. 1.1(a)). Concerning the orbital planes [11], in the xy-direction (in-plane) the carbon atoms form σ-bonds, responsible for the mechanical strength of graphene, with an orbital angle of 120°. In the z-direction (out-of-plane) orbitals form weaker and completely delocalized bonds (i.e. π-bonds), responsible for the electronic transport properties of graphene (Fig. 1.1(b)). The honeycomb lattice can be considered as interpenetrations of two triangular sublattices [12], [13] (red and green triangles with dotted lines in Fig. 1.1(c)) where each center is defined by the **A** (red dots) and **B** (green dots) with carbon-carbon distance of ≈1.42 Å. Great interest has been paid to understand the electronic properties of such material since it is the building block of the different allotropes

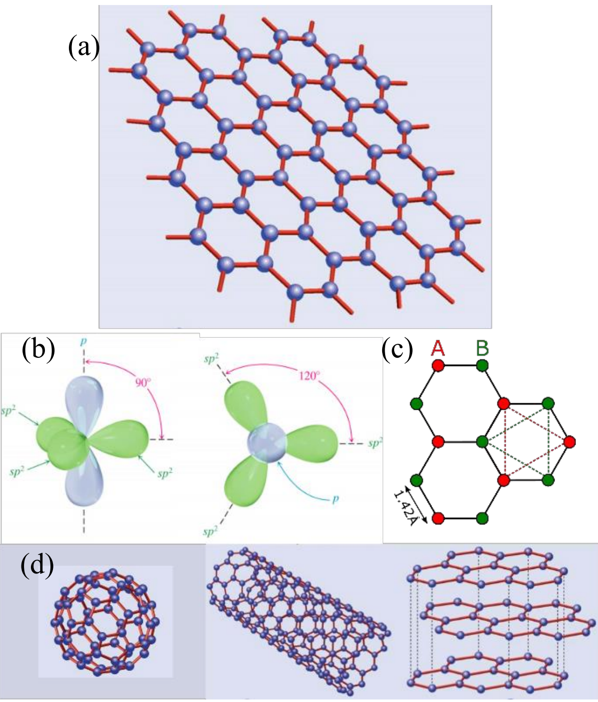


Fig. 1.1: *a) Graphene, a honeycomb lattice of carbon atoms, b) side view and top view of the sp^2 hybridized carbon, c) lattice structure of graphene obtained by the two interpenetrating triangular lattices, d) graphene allotropes. Sources: adapted from* [11]–[13]

[12] shown in Fig. 1.1(d): fullerenes, the 0D allotrope, where some hexagons in the graphene sheet, are replaced by pentagons[14], carbon nanotubes, the 1D allotrope, rolled up graphene sheets[15], and graphite, the 3D allotrope, a stacking of graphene sheets[2] by weak van-der-Waals bonds.

1.1 Band structure

As preliminary described, graphene can be studied as a particular triangular Bravais lattice with a basis of two atoms per unit cell [12], [13] and a tight-binding approximation has been used to describe graphene energy dispersion [12], [16]. Graphene honeycomb lattice and its Brillouin zone are depicted in Fig. 1.2. By looking at Fig. 1.2(a), a real and a reciprocal lattice can be considered with the following lattice vectors:

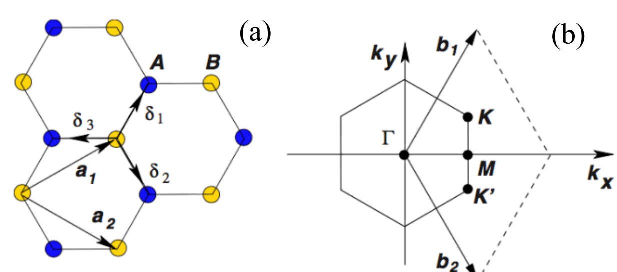


Fig. 1.2: *a) Graphene honeycomb lattice as an interpenetration of two triangular sublattices, b) related Brillouin zone. Source: adopted by* [12].

$$\dot{a}_1 = \frac{a}{2}(3, \sqrt{3}),\ \ \dot{a}_2 = \frac{a}{2}(3, -\sqrt{3}) \tag{1}$$

$$\dot{b}_1 = \frac{2\pi}{3a}(1, \sqrt{3}),\ \ \dot{b}_2 = \frac{2\pi}{3a}(1, -\sqrt{3}) \tag{2}$$

where $\boldsymbol{a}$ is the carbon-carbon distance. From the associated Brillouin zone depicted in Fig. 1.2(b), it is possible to introduce the two important points $\boldsymbol{K}$ and $\boldsymbol{K'}$ named Dirac points, placed at the corners of the graphene Brillouin zone. The graphene band structure obtained by solving its associated Hamiltonian [17], [18] is depicted in Fig. 1.3. Thanks to the similarity of its associated Hamiltonian, the particles are quantum mechanically described by the massless Dirac equation [12]. The Dirac cones are located at the $\boldsymbol{K}$ and $\boldsymbol{K'}$ points. In this particular case, the Fermi velocity used in the calculations does not depend on the energy or momentum [12], [13]. In addition, by looking at the energy dispersion plot, the conduction and valence band touch in the Dirac points (at the six corners of the Brillouin zone) (Fig. 1.3(a)). For low energy ($|E| < 1eV$) the electron energy is linearly dependent on the wave vector, thus assuming the shape of a cone (Fig. 1.3(b)) [12].

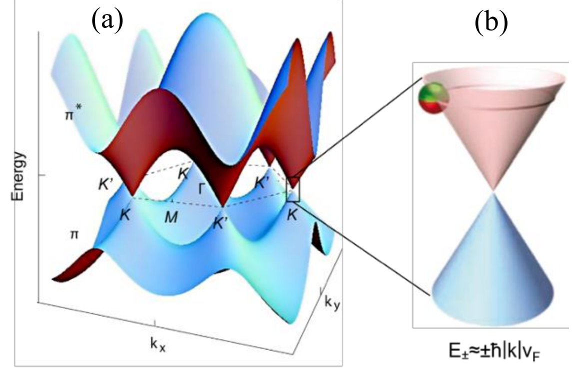


Fig. 1.3: *a) Energy dispersion plot of graphene. The conduction and valance bands touch at the six Dirac points (K, K'). For low energy, the dispersion diagram can be considered as linear (b).Source: adopted from*[12]

1.2 Graphene electronic properties

The ability to modify the electronic properties of a material by varying the carrier concentrations, by means of an external electric field, is the key task in electronics. Great interest has been paid concerning electronic transport in graphene, thanks to its very high carrier concentration and mobility [2]. Ambipolar field effect has been already proved in graphene [1], [2], [19]. In particular, it has been demonstrated that charge carriers can be tuned between electrons and holes in concentrations n as high as $10^{13}\ \mathrm{cm}^{-2}$ with mobilities μ up to $15{,}000\ \mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ under ambient conditions [2]. The extremely high mobility values are always related to large-area gapless graphene, which can be compared by the conventional semiconductor where the electron mobility decreases as the bandgap increase [3]. Charge carriers can be both electrons or holes and additionally, by applying an external electric field, it is possible to tune the Fermi energy level [1], [2] (Fig. 1.4). Ideally, suspended graphene exhibits no doping, so the resistivity (ρ) presents its maximum value at 0 gate voltage ("V_g"). Depending on the applied positive or negative gate voltage, it is possible to tune the Fermi level to the conduction band or valence band, respectively. A positive gate voltage provokes a n-doping in the graphene and vice versa. Another aspect which pushes the research towards graphene technology is given by the results obtained in terms of carrier velocity with respect to the applied electric field (Fig. 1.5). In particular, higher values have been predicated and reached [20] showing a no drop compared to the III-V semiconductors [3] (Fig. 1.5). As a drawback due to the graphene zero bandgap and its semimetal behavior is its application for logic switching devices [21], even if several efforts have been devoted to open a gap and to overcome this issue [22]–[24].

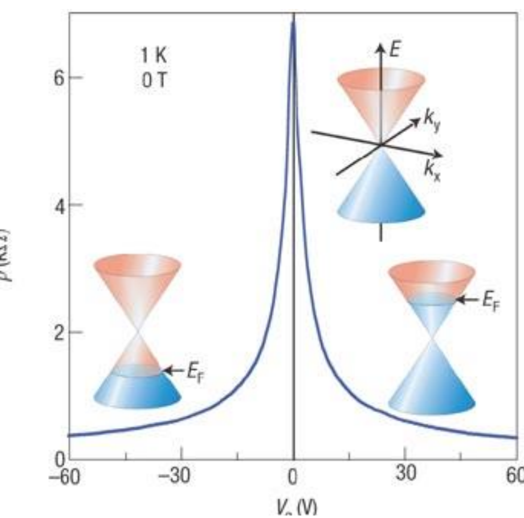


Fig. 1.4: *Resistivity in graphene by applying an external electric field. A positive gate voltage provokes a n-doping of the material and vice versa by moving the Fermi energy level (*$\boldsymbol{E_F}$*) as shown in the inset. Source: adopted from* [2].

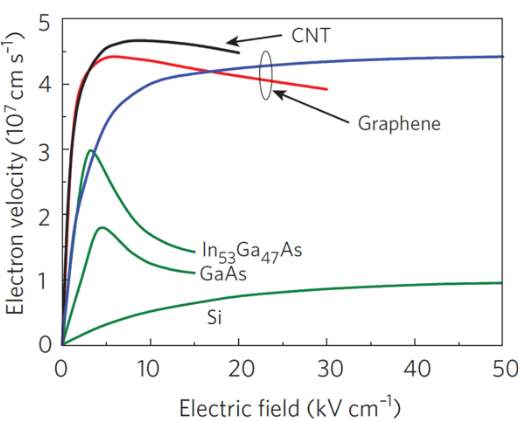


Fig. 1.5: *Comparison of electron velocity versus electric field between graphene, CNT and conventional semiconductors. Source: adopted from* [3].

1.3 Graphene optical properties

Thanks to graphene remarkable properties, it has been widely employed even for photodetection [25], [26]. Graphene "limit" due to its semimetal nature becomes a peculiar point, in the optoelectronics field, since it could potentially break the "long wavelength limit" of the convectional semiconductors which are transparent to the light with photon energy smaller than their bandgap. Its gapless nature in addition to its ultrafast carrier dynamics [26], [27], wavelength-independent absorption [26], [28], from the X-rays to the Terahertz frequencies [29], [30], with a flat optical absorption of 2.3% in the range from 300 to 2500 nm [6], [25], [31], tunable optical properties via electrostatic doping [26], [29], are the main characteristics which lead the success of such material in optoelectronics. As a drawback, pure graphene-based devices show poor photodetection performances, mainly due to both the small optical absorption [6] and the short charge recombination lifetime [7]. Photovoltaic, photo-thermoelectric, bolometric and photogating effects are the main mechanisms responsible of light detection in graphene-based devices [26], as it will be described in the following sections.

3.1.1 Photodetection mechanisms

The above-mentioned photodetection mechanisms are shown in Fig. 1.6 and described in the following.

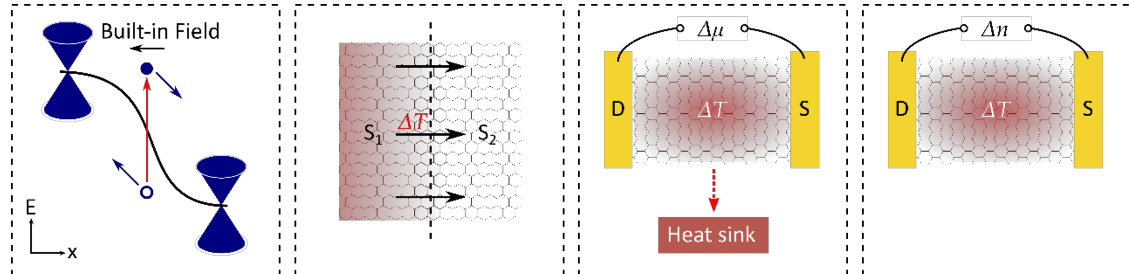


***Fig. 1.6:** From left to right: Photovoltaic effect, Photo-thermoelectric Effect, Bolometric Effect and photogating effect* [26].

1.3.1.1 Photovoltaic effect

Thanks to its 2D structure, graphene can be easily employed as photodetector, merely, by placing it longitudinally in between two contact electrodes (Source and Drain). By applying an incident light, electron-holes pairs photogenerated are separated by a built in electric field which occurs in between n-doped and p-doped graphene or between to different doped region [26], [32]. The involved built-in field could be induced exploiting the difference between graphene and contacting metal work function [33], or by a local chemical doping [34] or by using split gates [32]. The electric field could be also externally applied, but since the semimetal nature of

graphene, it is avoided, due to large dark current generation. Experimental results have been obtained on a device governed by this effect [35]. A picture of a scanning photocurrent measurement is shown in Fig. 1.7(b) where the device has been measured at zero source-drain and bias. As can be seen, the most part of photogenerated current occurs at the two metal contacts compared to the negligible current along the sheet where the small yellow dots are due to the presence of local built-in electric fields. The photogenerated current provokes a shift of $I_d \; vs \; V_{ds}$ curve at the contacts when irradiated (Fig. 1.7(c)). Such a behavior reveals that metal electrodes play a fundamental role in the photoresponse in graphene-based devices [35].

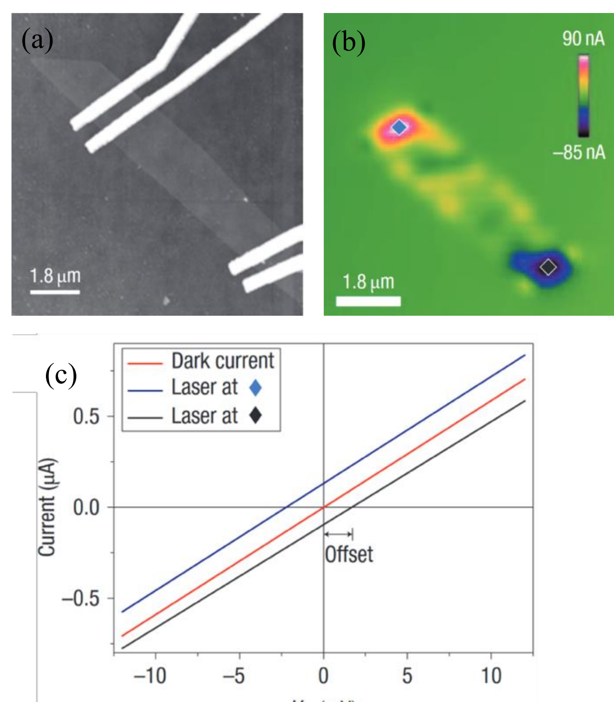


Fig. 1.7: *a) AFM micrograph of monolayer graphene flake connected by gold source-drain contacts, b) Scanning photocurrent measurements, c) $I_d \; vs \; V_{ds}$ characteristics measured in dark condition with the laser beam located on the drain/source contacts. Source: adopted by* [35].

1.3.1.2 Photo-thermoelectric effect

Photo-thermoelectric effect (PTE) is another mechanism which involves carrier generation in graphene. When graphene is exposed to an electromagnetic irradiation, the photogenerated electron-hole pairs provoke an ultrafast ($\sim fs$) carriers heating (Hot carriers) [36]. The photogenerated hot carriers remain at the same temperature thanks to graphene high phonon energy [37]. Such temperature, higher than the lattice, remains for picosecond, so the equilibrium is restored via scattering between acoustic phonons and charge carriers ($\sim ns$) [38]. Such hot electrons produce a photovoltage which depends on the Seedback coefficients of the two graphene doped regions and on their temperature gradient ($V_{PTE} = (S_1 - S_2)\Delta T_e$). PTE graphene detectors can achieve high bandwidths compared to PV detectors [26].

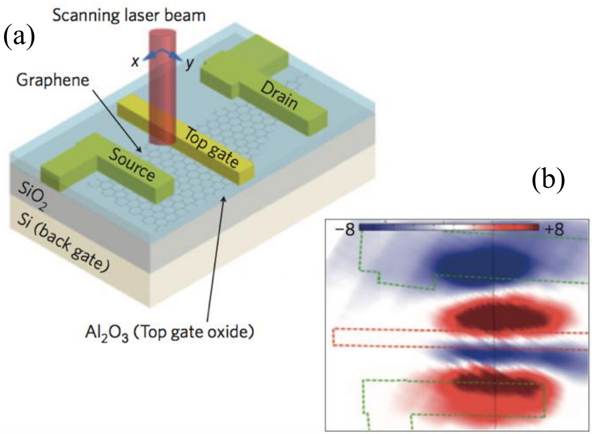


Fig. 1.8: *a) Schematic of the device used to evaluate the PTE effect, b) Scanning photocurrent of the device. Source: adopted from* [39].

Graphene-based photodetectors based on such mechanism have been already exploited [39]. A schematic of the double gate used to evaluate the PTE effect and a scanning photocurrent are shown in Fig. 1.8(a). The photocurrent response has been measured by applying a laser beam with a wavelength λ = 600 nm, without source-drain bias and zero back gate voltage applied. Both positive and negative photocurrents have been measured closer the drain contacts and at the edge of the top gate contact due to electron and hole photocurrent (see Fig. 1.8(b)). Due to the high temperature at the generated p-n junction thermoelectric current has been induced through the junction.

1.3.1.3 Bolometric effect

A bolometer consists in a device which measures the heating of a material having a temperature-dependent electrical resistance [40]. In particular, by applying an electromagnetic irradiation with a specific incident power, an increment of the temperature can be converted by an absorption layer which converts the light into heat. The most important parameter associated to a bolometer is the thermal resistance $R_h = {}^{dT}/_{dP}$, where C_h is the specific heat of the bolometer and dP the absorbed power. Such parameters permit to calculate the response time $\tau = R_h C_h$ [41]. Graphene is an appealing material if used as bolometer since presents low C_h thanks to the small volume for a given area and, in addition, the inefficiency of electron cooling by acoustic phonons, which means that R_h is high, thus the bolometric sensitivity results high as well [26]. Based on the change of the conductivity of the material due to the heat, an external bias is required and it does not need a p-n junction. This mechanism can be induced by a change of the carrier mobility due to the heat or by the change of the number of carriers [26]. Experimental measurements on graphene-based photodetectors exploiting this mechanism are reported in the following[42] and shown in Fig. 1.10. On such experiments both bolometric and photovoltaic effects are identified, but it has been demonstrated that the operating conditions are the cause of the photogeneration mechanism involved. Particularly, without applied bias, the

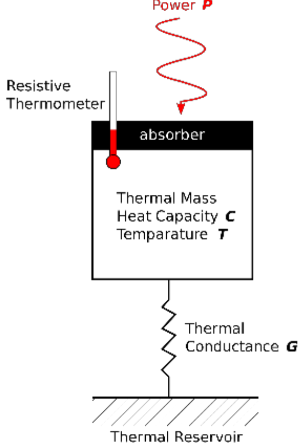


Fig. 1.9: *Conceptual schematic of a bolometer.*

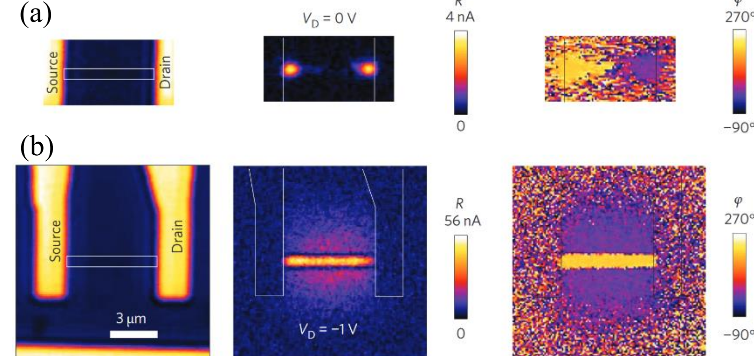


Fig. 1.10: *a) Measured photocurrent (magnitude and phase) at V_D=0 V drain bias and Vg=5V gate bias (n-type regime). (b) Photocurrent magnitude and phase at V_D=-1 V drain bias and Vg=5V gate bias (n-type regime).*

contribution of the photocurrent is due to the PV effect as can be seen from the vicinity of the photogenerated current with the metal contacts (Fig. 1.10(a)). Instead, by applying an external electric field, the photogeneration arise almost uniform in the whole graphene sheet (Fig. 1.10(b)).

1.3.1.4 Photogating effect

Photogating effect is a photogeneration mechanism based on the change of the material conductance as a consequence modification of the carrier density induced by the light [26]. In this mechanism, the electron-hole pair can be generated in graphene and then one carrier type can be trapped in charge traps, or photogenerated in charge traps or nanoparticles closer to the graphene sheet. For this photodetection mechanism a gain is provided which is dependent on the mobility of the material: therefore, for this reason, graphene is an optimum candidate. As a drawback, high dark current values can be reached since an external electric field has to be applied. Hence, not very high responsivity values can be reached. To overtake this issue, regarding IR photodetection, graphene functionalization has been exploited, in particular by using quantum dots [43], which can absorb IR light more efficiently. In particular, NIR photodetectors has been exploited by achieving 10^7 A/W as photodetector responsivity [43].

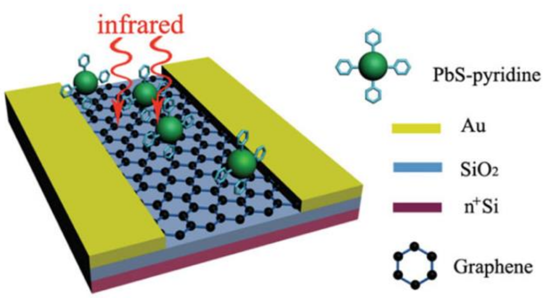


Fig. 1.11: *Schematic of the grpahene-based photodetector expliting the photogating effect. Source: adopted by* [43]

1.4 Graphene growth techniques

The production of graphene with specific properties for each application is the key issue for the diffusion of graphene-based devices. Different growth techniques have been developed since graphene discovery [4]. The common ones are depicted in Fig. 1.12 and the most used are subsequently described [44]–[46].

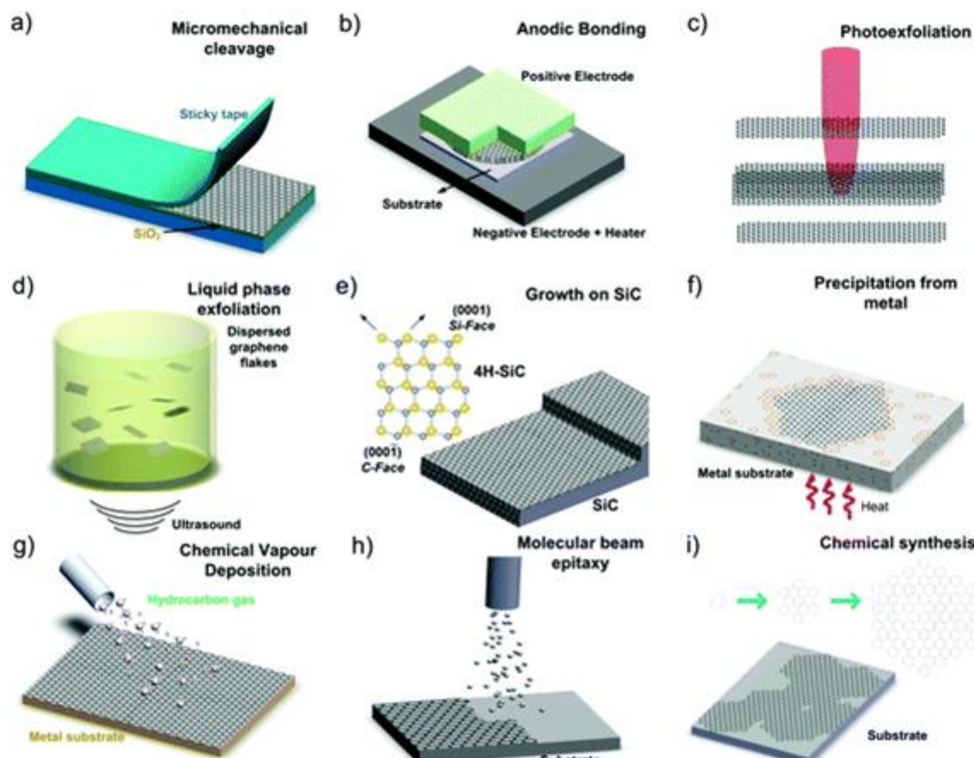


Fig. 1.12: *Graphene growth techniques*. *Source: adopted by* [46].

Micromechanical cleavage (MC), also known as micromechanical exfoliation, has been widely employed by crystal growers and crystallographers. Single Layer Graphene (SLG) can be achieved, thanks to MC procedures, by cleaving the graphene layers from the bulk graphite surface using an adhesive tape [1], [47]. Most of the prototypes are usually obtained using mechanical cleavage, since the quality of the obtained flakes is very high, in terms of mobility. As a drawback, such technique cannot be used for large scale applications. Nevertheless, MC remains ideal to investigate new physics and new device concepts.

Chemical Vapor Deposition (CVD), is nowadays a promising way to produce large scale polycrystalline graphene films on copper foil [48]. Due to the importance to the wafer scale integration [49], many efforts have been made to growth as much graphene with the compromise to obtain both high carrier mobility and uniformity of the film. A drawback of such technique is that a subsequent transfer of the graphene film from the copper foil to the achieved substrate is required [50]. Such post-treatment often affects the final quality of the graphene film [51] since it requires the use of PMMA mask, water intercalation methods, introduction of metallic impurities [52] and so on.

Synthesis on SiC. Graphitic layers can be grown on the silicon or carbon faces of a SiC wafer by sublimating Si atoms, obtaining a graphitized surface. The C-terminated face of SiC is used to

grow a stack of randomly oriented polycrystalline layers [53]. The graphene quality obtained employing this technique can be very high, but the drawbacks consist in the very high cost of the SiC wafer and the high temperature needed [44].

Liquid-phase exfoliation of graphite. Such a technique is based on the graphite exfoliation in a solvent by using ultrasounds to separate single and multilayer graphene. The solvents could be both aqueous [54] and non-aqueous [55]. A subsequent purification of the flakes is needed in order to separate the exfoliated to the un-exfoliated ones through centrifugation [45].

Laser ablation and photo-exfoliation is a technique which employs a laser pulse to ablate/exfoliate graphite flakes [45]. Such technique has been used for direct laser irradiation of graphene oxide (GO) obtaining promising results [56] for further improvements.

Depending on the fabrication methods, it is possible to obtain a compromise in terms of quality and costs as reported in Fig. 1.13 [44]. MC continues to be widely employed for the production of prototypes due to high quality graphene achieved, although the high cost prevents its use for mass production. CVD technique, instead, allows large area monolayer graphene growth. The "high-yield" and the relative cheapness of CVD graphene make this technique the primary candidate for large-scale electronics[49]. Graphene growth on SiC allows also high quality, large areas, films production. However, the high cost of the SiC wafers, the high temperatures (above 1000°C) used during the process and the incompatibility with silicon electronics technology make this technique not very feasible yet. In this work thesis, CVD monolayer polycrystalline graphene has been employed.

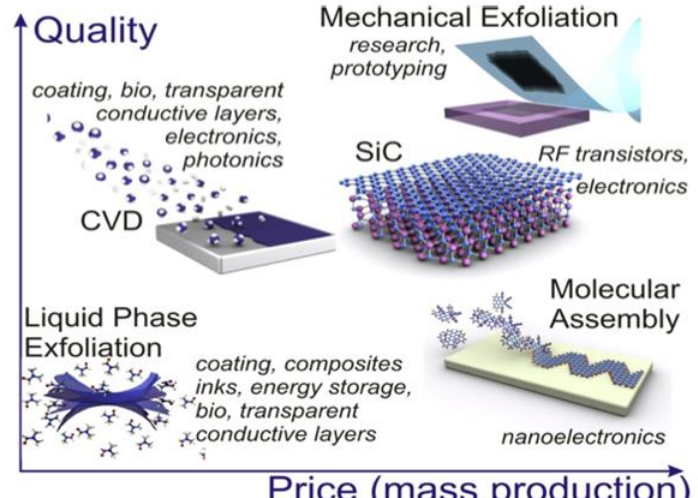


Fig. 1.13: *Map of graphene quality versus mass production. Source: adopted from* [44]

2. Graphene-based devices

Thanks to its electrical and optical properties, already described in the previous chapter, graphene represents an ideal candidate not only to overcome actual well-established technologies but also, given its 2D nature, to be integrated within them. Since the large development of Silicon technology, its replacement by a novel material would not be a completely smart idea [3]. Therefore, many efforts have been made and to exploit novel technologies which could improve significantly the performances of existing technologies in electronics and optoelectronics fields. Unfortunately, the high cost, the low efficiency and, somehow, the low quality of graphene growth and patterning techniques are the limit of such material [45]. However, the excellent graphene properties inspired great interest to make use of such material on the realization of high frequency electronics and ultra-fast photodetectors. In this chapter, the adoption of graphene in such fields is reported. A short review on the-start-of art of graphene field effect transistors (GFETs) and graphene-based photodetectors will be presented in order to compare the obtained experimental results with the ones in the literature. Concerning high frequency application, before talking about novel transistor geometries it is fundamental to start with the introduction of the classical Metal–oxide–semiconductor field-effect transistors (MOSFETs) in order to let understand their limit and try to explain why the adoption of a novel material is needed. Its success is due to performance improvement thanks to the continuous scaling of its geometry [57]–[59]. MOSFET consists of a channel region connecting source and drain electrodes, and a barrier separating the gate from the channel [60]. The channel conductivity is controlled by a voltage applied between the gate and the source, i.e. V_{GS}. To speed up the operation of such devices, a quick response to variations of V_{GS} is needed, so the most important requirements are fast carriers in even shorter channel. The scaling down of the MOSFET geometry leads to the well-known "short-channel effects", i.e. threshold-voltage roll-off, drain-induced barrier lowering, and impaired drain-current saturation [61]–[63]. Nowadays, Si MOSFETs with 20-nm gates are already in mass production, but the further scaling and the simultaneous achievement of better device performance become more and more difficult. Nevertheless, different efforts have been made on the development of non-classical MOSFET architectures [59], [64] and meanwhile, this leads research to introduce devices based on a fundamentally different physics or on materials different than silicon. In this scenario, graphene obtained a great success, since its peculiar electrical properties [2], [3]. Graphene-based transistors can be employed in both digital and radiofrequency electronics. Due to the graphene nature and its zero band-gap, a low on–off ratio has been demonstrated in GFETs and this makes them unusable ("up to now") in the field of logic applications [3] even if recently, ON-OFF ratios around 100 and 2000 at room temperature and

20K have been obtained [24], revealing the great potential of bilayer graphene in digital electronics. Regarding radio-frequency (RF) electronics, materials with high carrier mobility are needed [3] even if their ON-OFF ratio is poor. Graphene properties make it the ideal candidate to improve ultrafast high-performance transistors. The most important figures of merit (FOM) describing the high-frequency performance of a FET are the transit frequency f_T and the maximum oscillation frequency f_{max}. f_T is the frequency where the circuit current gain $|h_{21}|$ approximates unity, f_{max} instead is the frequency where the maximum oscillation power gain G_{MAX} is equal to 1 [65]. These FOM specify up to which frequencies the transistor offers current and power gain, respectively. In Fig. 2.1 the promising results already obtained are shown.

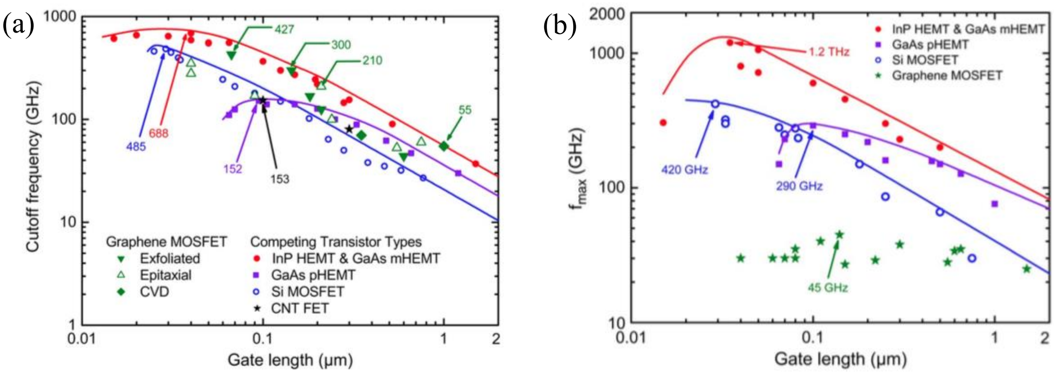


Fig. 2.1: *Comparison of f_T (a) and f_{max} (b) of graphene MOSFETs versus gate length and f_T performance of CNT FET, InP HEMTs, GaAs mHEMTs, GaAs pHEMTs; and SiMOSFETs. Source: adapted from*[3]

With regard to the optoelectronic field, instead, as reported in paragraph 3.1.1, different photoresponse mechanisms can be exploited to fabricate graphene-based photodetectors aimed to collect and convert photons to an electrical signal [26], [44], [66]. To evaluate the quality of photodetection, several FOM are commonly used, such as the external quantum efficiency (EQE), which is given by:

$$\boldsymbol{EQE = \frac{I_{ph}}{q\phi_{in}}} \tag{2.1}$$

where I_{ph} is the measured photocurrent, ϕ_{in} is the photon flux and q the electron charge. EQE represents the quantity of e-h pairs detected per incident photon [67]. To evaluate the photodetection efficiency the internal quantum efficiency (IQE) is used:

$$\boldsymbol{IQE = \frac{I_{ph}}{q\phi_{abs}} = \frac{EQE}{A_{abs}}} \tag{2.2}$$

where $\phi_{abs} = A_{abs}\phi_{in}$ is the absorbed photon flux and A_{abs} is the absorbed fraction. This FOM gives the photodetector ability to transduce the absorbed photons to an electrical signal. The sensitivity, instead, is described by its responsivity R which is given by the ratio of the photocurrent to the incident power:

$$R = \frac{I_{ph}}{P} = EQE\frac{q}{h\nu} \tag{2.3}$$

2.1 Graphene field effect transistors (GFETs)

Graphene field effect transistors (GFETs) is the name given to the novel devices exploiting graphene as channel layer. Several GFET layouts have been designed, fabricated and characterized in order to reach better performances compared to well-known ones, exploiting graphene properties [3], [68]–[70]. Herein, a comparison of standard Si-MOSFETs and different GFETs geometries is reported. In Fig. 2.2 cross sections of a standard Si-MOSFET and three different types of GFETs are shown. A distinction between GFETs with local and non-local gate structure is also reported. Fig. 2.2(b) refers to a non-local gate structure, also called back gate GFET while (c) and (d) refer to a local, top and bottom gate, respectively.

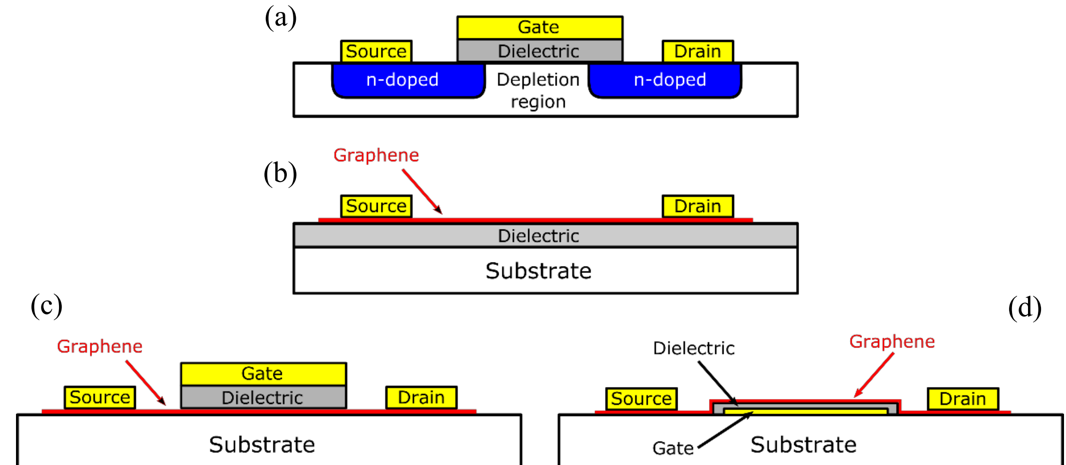


Fig. 2.2: *a) Schematic of a n-type semiconductor-based FET. (b) GFET with back gate structure, (c)GFET with local top gate and (d) local bottom gate.*

Back-gate devices have been very useful for research purposes, but since the presence of 300nm silicon oxide layer and doped silicon as back gate, large parasitic capacitances are reached [1]. Additionally, poor gate efficiency and the impossibility of integration makes this configuration vain for further performance improvements [3]. GFETs with local top gate structure, instead, can exploit the flatness of the deposited graphene sheet but the subsequent oxide layer deposition usual degrades graphene mobility [71]. Local bottom gate structures, instead, could exploit higher values of graphene mobility, even if large flat areas are more difficult to obtain. In order to characterize such devices, since graphene-based transistors are affected by hysteretic behavior simultaneous DC and RF characterizations have to be performed. By starting from the typical

transfer characteristics obtained in [72], [73], as it can be seen in Fig. 2.3, by applying an external bias i.e. drain-source voltage "V_{DS}" and by sweeping the gate-source voltage "V_{GS}", it is possible to tune the graphene Fermi level, and thus to dope the channel depending on the applied V_{GS}. Large positive gate voltage causes channel electron accumulation (n-doping) and vice versa. In particular, it has to be noticed that, after graphene transfer process on the desired substrate to fabricate transistors, it usually reaches an intrinsic doping [34], [74]. As can be seen in Fig. 2.3, the two estimated Dirac points are not located at $V_{GS} = 0$, but they are slightly shifted in one direction (p-doping in this case). As a consequence of the increment of V_{DS} values, the Dirac point continues to shift as it can be seen in the following chapter based on the experimental work. The transcharacteristic curves are also fundamental for the further RF measurements, since their slope determinates an important FOM for RF characterization, which is named transconductance (g_m). Such a value describes how effective the gate voltage modulates the drain current. It is defined as the partial derivative of I_{ds} with respect to V_{GS} at given operating point V_{DS}:

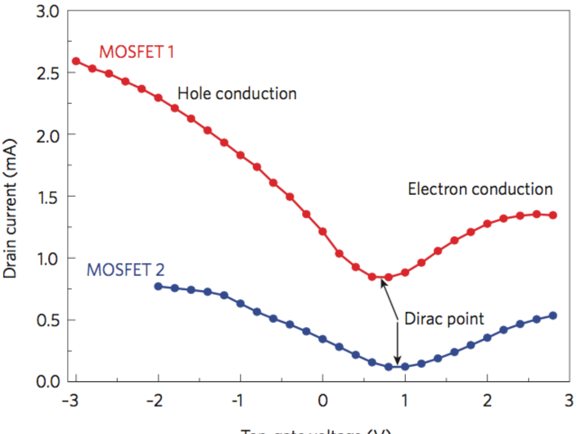


Fig. 2.3: *transfer characteristic for two characterized GFETs. Source: adopted by* [3]

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{GS}}\right|_{V_{DS=const}} \tag{2.4}$$

By looking at the transcharacteristic curves, their highest slope determinates the highest transconductance values, so further RF characterization based on the S-parameters measurements has to be carried out in the particular range of V_{GS} and V_{DS} around this value in order to reach the best device performances in terms of gain, f_T and f_{MAX}. The same behavior, of course, occurs by looking the I-V device curves (output characteristics) (see Fig. 2.4). No saturation [75] or only weak saturation [69], [76] can be seen. Three different region can be considered, the first where the curves have a linear shape, for small values of V_{DS} and the channel is n-type (region I). By increasing the V_{DS} values, a principle of saturation can be seen (Dirac point) until the inflection point at V_{DS} =

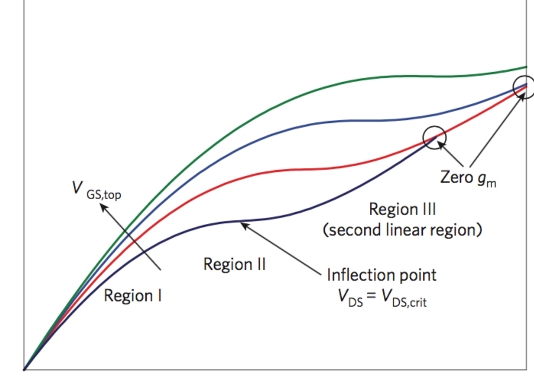


Fig. 2.4: *qualitative shape of the GFETs output characteristics. Source: adopted by* [3]

$V_{DS,crit}$ is reached (region II). By further increasing the V_{DS} value over the $V_{DS,crit}$, the channel switches from n-type to p-type [77], [78] and the curves show again a linear behavior (region III). All the DC curves shown have been reached without emphasizing a well-known problem of the hysteresis in graphene-based devices[79]. Another very important drawback which crucially affects graphene-based devices performances is the contact resistance between graphene and the metal electrodes. In the following paragraphs both issues will be shortly explained, in order to understand the limitation induced on such devices and the methods used to overtake them.

2.2 Hysteresis in graphene-based devices

As preliminary discussed, hysteresis represents an important issue in graphene-based devices, since it leads to an instability of the operating point and thus in their practical usage [79]. Both the transfer characteristics and the drain conductance, being related, exhibit shifts depending on the gate/drain sweep measurement procedure leading to a not univocal operating point of the device under study. A typical hysteretic behavior in graphene-based devices is shown in Fig. 2.6. As reported in [79], there are two main mechanisms involved in the phenomena (see Fig. 2.5). First, the charge transfer (holes/electrons) from graphene to charge traps in the oxide and second, the capacitive gating. In the first mechanism, by looking the forward sweep, due to the initial graphene p-doping, holes transfer from graphene to the charge traps in the oxide. This increases the gate effective potential if compared with the applied external voltage, and thus, the Dirac point is reached by applying a lower V_{GS} value, vice versa for n-doping. Instead, capacitive gating occurs when the charged ions alter the local electrostatic potential around the graphene, which pulls more opposite charges onto graphene from the contacts.

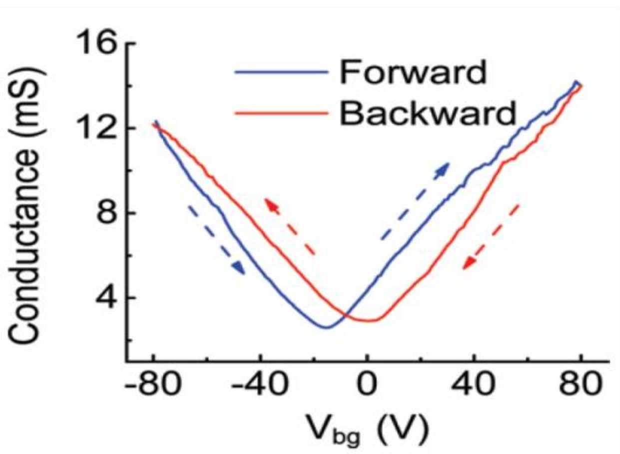


Fig. 2.6: *Conductance vs gate voltage curves measured in ambient condition. A hysteresis behavior is observed when backward V_{GS} sweep is performed. Source: adopted by* [79].

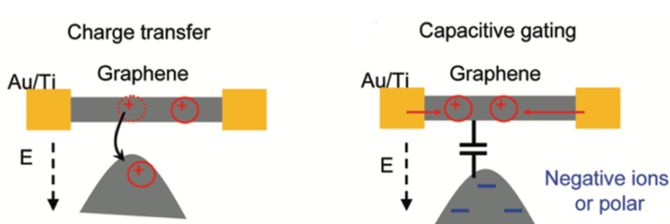


Fig. 2.5: *Schematic of the two mechanisms involved in the hysteretic behavior of graphene-based devices*

2.3 Contact resistance

Graphene/metal connections are necessary and at the same time fundamental for the fabrication of performing devices. In particular, not only choice of the right metal [80], but even the way to connect it to graphene [81], [82] significantly influence device contact resistance "R_c"[83] which is a performance killer for the high performance graphene-based transistors [84]–[86]. The use of metal contacts leads to an induced graphene doping [87] depending on the difference between work function between metal and graphene [80]. It has been studied that the adoption of copper, nickel and palladium alter by chemisorption graphene electronic transport, while aluminum, silver and gold only cause small alterations in the band structure due to the weak bonding [80]. Moreover, high work function difference has effect on the contact resistance reduction [23], [83], [84], [88], [89]. As a drawback, it leads to formation of a p-n junction in the channel region [84]. Different efforts have been made to reduce contact resistance values, such as post annealing procedures or contacting graphene from both sides [90] by using Ti/Pd contacts. "End-contacting" graphene at the edges has been demonstrated as a promising exploit in order to reduce graphene contact resistances [81], [91].

2.4 State of art of GFETs

Several works have been published concerning the evolution of GFET device performance and they are summarized in the following. In 2009, IBM published the first work on GFET representing a significant step toward the realization of graphene-based electronics for high-frequency applications [75]. Top-gated graphene transistors have been fabricated and their characteristics analyzed at microwave frequencies. This work highlights that measured intrinsic GFET current gain shows an ideal 1/f frequency dependence, indicating a FET-like behavior for graphene transistors. They claimed that f_T increases reducing the gate length, and a

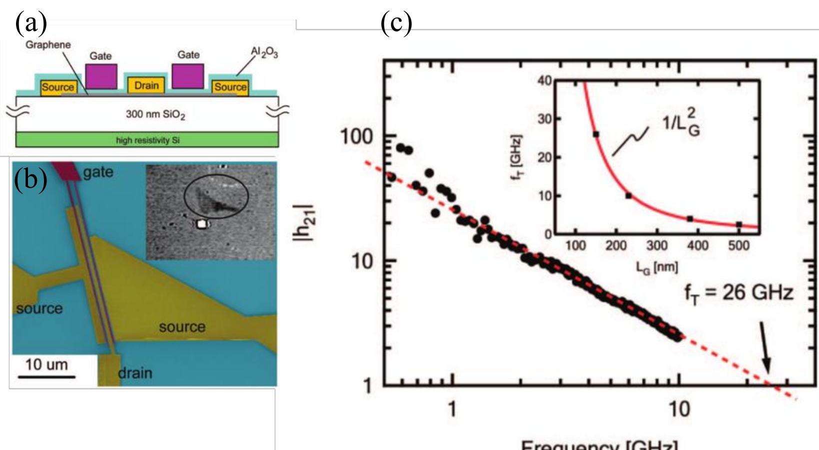


Fig. 2.7: *(a) Schematic cross section of the graphene transistor (b) scanning electron microscopy image of the graphene channel and contacts. (c) Measured current gain h_{21} as a function of frequency of a GFET with L_G = 150 nm, showing a cut-off frequency at 26 GHz.* [75].

value of 26 GHz has been measured for a graphene transistor with a gate length of 150 nm and

carrier mobility of $2000\ cm^2/Vs$. Due to the chemically inert behavior of graphene surfaces to atomic layer deposition precursors, NO_2 functionalization has been employed for the subsequent Al_2O_3 deposition. The limitation in the frequency response of the fabricated devices has been attributed to charged impurity scattering associated with the functionalization layer and interface phonon scattering in the oxide which leads to current and mobility degradation.

In 2010, a dual-gate graphene field-effect transistor with higher mobility values ($2700\ cm^2/Vs$) has been obtained [92]. A cut-off frequency of 50 GHz has been demonstrated in a 350-nm-gate-length device by reducing the access resistance using electrostatic doping and 2-nm of Al (first deposited and then oxidized) to serve as nucleation layer for the subsequent ALD-deposited film. The poor high frequency performances are essentially due to the high capacitance induced by the conductive substrate used.

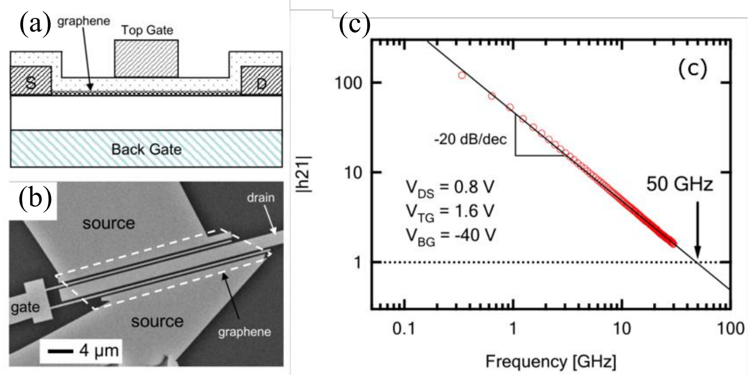


Fig. 2.8: *(a) Device schematic of the dual-gate graphene transistor. (b) SEM image of a dual-channel graphene transistor. (c) RF performance shows a current gain at -20dB/dec and a cut-off frequency f_T of 50GHz* [92].

Both the above-mentioned examples refer to GFET employing exfoliated monolayer graphene. As reported before, large scale devices are not feasible employing this technique. In 2010 IBM group reported the performances of a matrix of GFETs on SiC wafer exhibiting 100GHz cut-off frequency [93]. Epitaxial graphene growth on SiC with thermal annealing at 1450℃ has been used. The reported estimated mobility was in the range $1000 \div 1500\ cm^2/Vs$. Arrays of top-gated FETs were fabricated with various gate lengths (L_G), with the shortest being 240 nm. In order to form the top gate stack, an interfacial polymer layer made of a derivative of poly-hydroxystyrene was spin-coated on the graphene before the atomic layer deposition of a 10-nm-thick HfO_2 insulating layer [94].

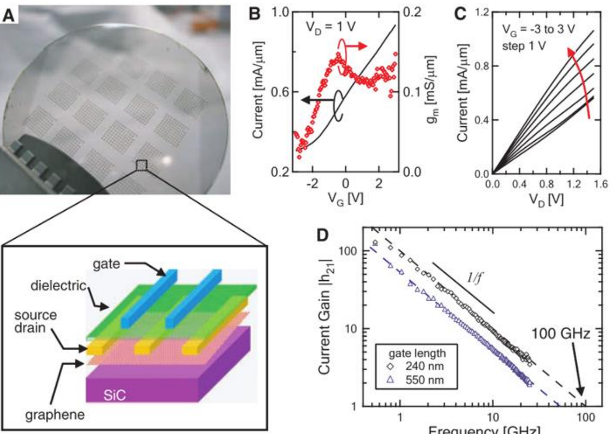


Fig. 2.9: *(a) Image of devices fabricated on a 2-inch graphene wafer and schematic cross-sectional view of a top-gated graphene FET. (B) Drain current versus gate voltage at drain bias of 1 V and (C) Drain current as a function of V_D for various gate voltages of a GFET with L_G = 240 nm. (D) Measured small-signal current gain $|h_{21}|$ versus frequency for a 240-nm-gate and a 550-nm-gate GFET at V_D = 2.5 V showing 100 and 53 GHz, respectively. Source: adopted by* [93].

Finally, in 2012 Wu *et al*. [70] focused their work on an optimized GFET architecture with an intrinsic cut-off frequency of 300 GHz, obtained employing wafer-scale CVD grown graphene on diamond-like carbon (DLC), and of 350 GHz for epitaxial graphene on SiC. For CVD graphene on DLC, the top-gate dielectric stack includes an electron-beam evaporated and oxidized Al layer followed by an atomic layer deposited (ALD) film of Al_2O_3 [95]. For epitaxial graphene, 15 nm silicon nitride was grown by plasma-enhanced CVD (PECVD) at 400 °C [96].

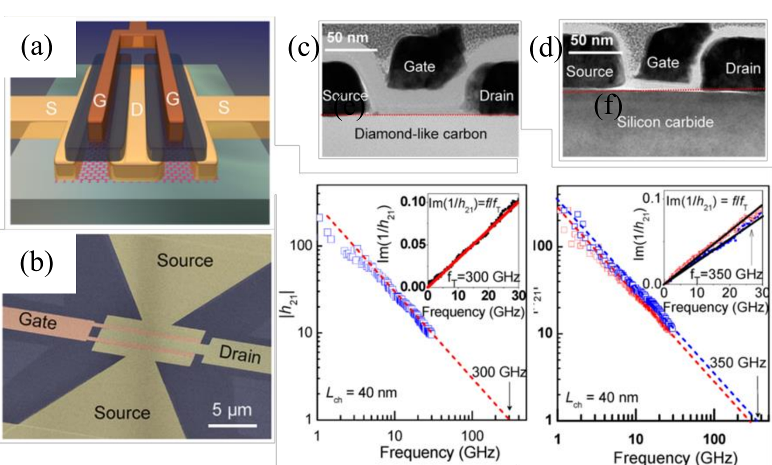


Fig. 2.10: *(a) Schematic view of a top-gated graphene RF transistor on a DLC substrate. (b) SEM image of top-gated dual-channel RF device. Cross-section TEM images of a transistor based on CVD graphene on DLC(c) and on epitaxial graphene on SiC (d); |h21| versus frequency for the 40 nm device with* f_T *= 300 GHz for GFET on DLC (e). (f) and for two 40 nm GFETs on SiC with* f_T *= 300 and 350 GHz* [70].

2.5 State of art graphene-based photodetectors

As preliminary discussed in par. 1.3, by exploiting both graphene ultra-high carrier mobility and short carrier lifetime, a metal-graphene-metal photodetector has been fabricated and characterized [7]. Since the built-in electric fields take place in a small region close to metal/graphene interfaces [97], interdigitated metal finger has been designed above the graphene sheet to enhance the PV effect by increasing the detection area (see Fig. 2.11). Such device has been employed in a $10\,Gbit\,s^{-1}$ optical datalink, reaching a maximum external responsivity of R = 6.1 mA/W at $1.55\,\mu m$. In order to enhance the PV effect, the difference between graphene and metal source work function has been chosen higher than graphene and metal drain work function. 16 GHz as 3-dB bandwidth has been evaluated limited by the RC

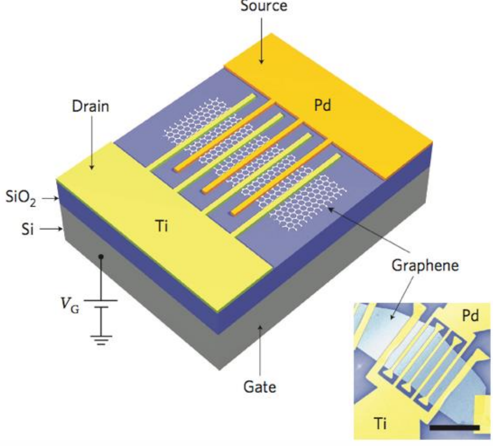


Fig. 2.11: *Schematic of the interdigitated metal-graphene-metal photodetector. Source: adopted by* [7].

constant of the device. Such experiment led graphene photodetector to be a promise candidate for telecommunication application. As preliminary discussed, graphene absorbs 2% of incident light [6] which is a large value if compared to its atomically thickness but still not enough to reach high photoresponse values. Different configurations have been proposed in order to enhance the detection capability of such devices. Exploiting graphene-light interaction length, it has been integrated in an optical microcavity [98]. In Fig. 2.12 both the schematic of the fabricated device and the photoresponse achieved by using a bilayer device are shown. As it is possible to notice, when exploiting multiple light absorption in graphene by using the microcavity, an enhancement of the photocurrent is reached if compared to the detector without cavity. A maximum external responsivity of 21mA/W has been achieved [98]. The limit due to integration in such cavity is to restrict photodetection to narrow bandwidth. In order to overcome this issue, a proposed way to enhance graphene-based photodetector response has been to integrate graphene on a photonics waveguide [99], [100]. In particular, by coupling the evanescent field out of the waveguide in the graphene, a photoresponsivity of 0.1 A/W has been reached in a broad spectral bandwidth [99] as shown in Fig. 2.13. It has been demonstrated that another way to enhance graphene-based photodetectors sensitivity is to exploit the excitation of surface plasmon by placing the plasmonic nanostructures close to the contacts [101]. When low intensity has to be detected, hybrid phototransistors can be employed which exploit the PV effect in efficient absorbing synthetized centers with the subsequent charge transfer in a conductor [26], [102].

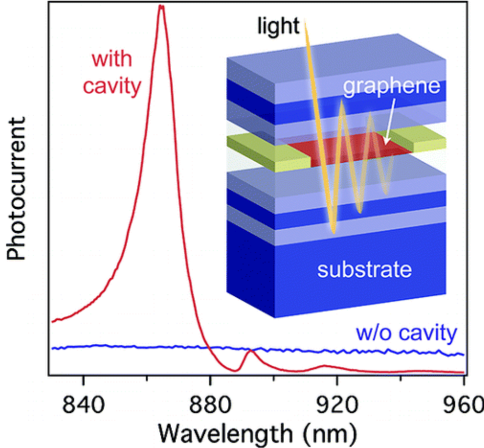


Fig. 2.12 : Schematic of the graphene microcavity photodetector. Photocurrent results for bilayer graphene. Source: adopted by [98].

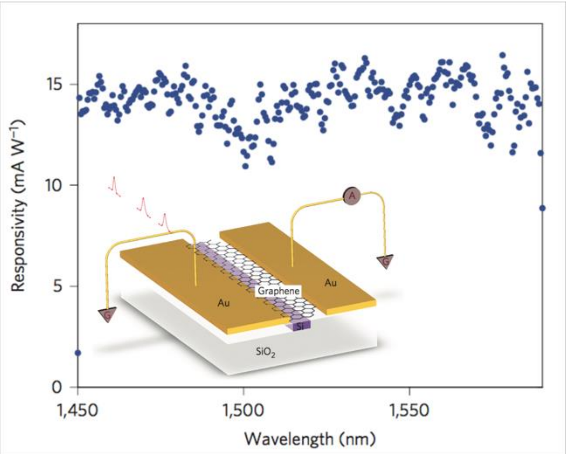


Fig. 2.13: Responsivity of graphene integrated on photonics waveguide as photodetector. Source: adopted from [99]

3. Experimental activities

In this chapter, GFETs fabrication steps and the results of electrical (RF/Microwave) and optical characterization are reported. Starting from the choice of the most suitable substrate, first a statistical study on the layout influence on microwave performance has been made. Then, taking into account the role of the gate dielectric, a comparison of different thin oxide layers has also been performed. Finally, an optical characterization has been carried out aimed at exploiting GFETs use as visible and infrared photodetectors, with a wideband intrinsic gain capability.

3.1 Substrate

The choice of the substrate plays a key role to enhance graphene-based devices performance, since graphene charge mobility is strictly connected to the scattering induced by the substrate [103]. High mobility values are needed in order to improve GFETs gains and cut–off frequency values in the MW regime and fast modulation in the photonics field. The first graphene devices have been fabricated on Si/SiO_2 substrates [1], [104], [105], exploiting the possibility to tune graphene Fermi level by using the highly doped Si as back gate and to use the stack (300nm of SiO_2 on the p-doped Si) to enhance the optical contrast under microscope view. However, it has been demonstrated that its use limits the graphene potential due to several issues, such as flatness, charge traps in SiO_2 forming “charge puddles” [106] , which lead scattering, a low dielectric constant ($\varepsilon_r \sim 4$), even though it offers high break-down voltage. Additionally, the low energy SiO_2 phonons enhance scattering phenomena [107]. Such substrate is also not suitable for high frequency electronics, as confirmed also by experiments/simulations already done. In fact, its physical properties imply high values of parasitic capacitances and losses. For this kind of applications, the optimal substrate should be flat, insulating, and free of charge traps. As reported in 2.4, GFETs showing the best performance have been fabricated on insulating or semi-insulating substrates [108]. In this framework, sapphire can be considered a good candidate[109], [110]. It exhibits low dielectric losses and good heat conduction in addition to high dielectric constants ($\varepsilon_r = 9.39$ (E perpendicular to the C-axis) and $\varepsilon_r = 11.58$ (E parallel to the C-axis)[111]). Sapphire resistivity is orders of magnitude larger than the one of high resistive Si [111], which leads to a reduction of the parasitic capacitances between the pads and the device launchers. Also, its high thermal conductivity [111] enables fast cooling and thus high current densities. In the optoelectronics field and, particularly, for telecom applications, sapphire does not represent a good substrate candidate due to its high band gap (it cannot provide carriers). Nevertheless, its use can help keeping graphene flatness after the transfer procedures. Due to the above-mentioned characteristics and for continuity with the experimental activity performed by

Dr. C. Benz, a former PhD student at KIT [112], in this work sapphire has been chosen as the substrate for graphene-based devices fabrication.

3.2 Gate dielectric

Once the substrate has been chosen, a good gate dielectric needs to be found to allow the development of competitive ultrafast transistors. Graphene surface is chemically inert to atomic layer deposition (ALD) precursors making the integration of high-dielectric constant materials a tricky process [71]. Fig. 3.1 shows the band gap versus the dielectric constant of some materials commonly used as gate dielectric [113]. As well known, in MOSFET technology, a thinner oxide - i.e., a higher oxide capacitance (C_{OX}) - is desired to maximize the device RF-performances since it leads to a higher value of the transconductance and, consequently, of the cut-off frequency. Unfortunately, a thin gate oxide causes two main drawbacks: high leakage current due to tunneling phenomena and poor long-time reliability [114]. As a possible solution, high

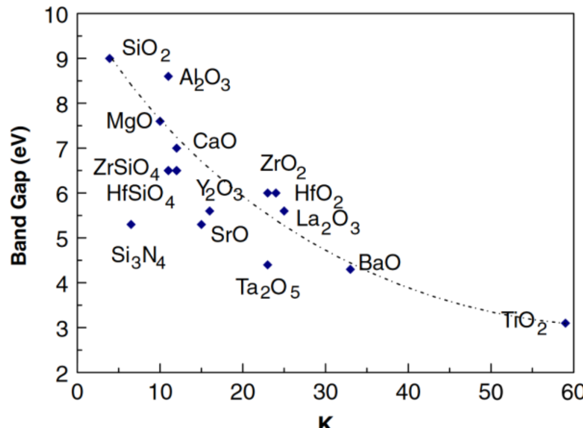


Fig. 3.1: *Bandgap vs. dielectric constant of some common gate dielectrics. Source: adapted from* [114]

κ-oxide materials have been widely employed [115], [116]. Additionally, leakage current significantly depends on the conduction bands offset between the oxide and the semiconductor employed [114]. For these reasons, a trade-off should be found between oxide thickness and band offset. Traditionally, hafnium has been the most exploited oxide thanks to its high κ factor ($\kappa \approx 25$). Titanium oxide exhibits a higher κ-value ($\kappa \approx 80$), but it is thermally unstable when deposited over silicon. Aluminum oxide exhibits a too low κ value ($\kappa \approx 9$), but shows a very high breakdown voltage [19]. In graphene, all the above mentioned oxides can potentially be used as gate oxide layers for field effect transistors fabrication. Atomic Layer Deposition (ALD) is a common way to grow dielectrics with an exact control on the thickness. Nevertheless, it cannot be used directly on graphene due to its inertness. However, by exploiting graphene small imperfections as nucleation centers, the growth could be possible [117]. In this work, for the fabrication of top gate devices, air oxidation of a thin layer of aluminum [95] deposited by Molecular beam epitaxy (MBE) has been exploited, which acts as seed layer for the further nucleation of the oxide film.

3.3 Fabrication techniques

In the following, the techniques used for fabrication steps of the samples are reported.

Substrate cutting and cleaning: 2 inches sapphire has been provided by Roditi [111]. Before starting the fabrication process, it has been cut into small pieces by a diamond pen. Then, the substrate has been soaked in acetone and put in the sonication for 20s. Afterwards, it has been cleaned again with acetone and isopropanol and placed in reactive ion etching (RIE) with oxygen plasma for 2 min in 0.2 mbar conditions. Subsequently, it has been backed in the hot plate at 200°C for 15 min.

Fig. 3.2: *Substrate cutting and cleaning by using RIE*

Spin-coating of PMMA resist: Poly (methyl methacrylate) (PMMA 4.5wt%) masks have been used for all the technological steps. PMMA has been spin-coated at 6000 rpm for 90s, resulting in an average thickness of 200nm. A subsequent backing on hot plate at 180°C for 1min has been made.

Fig. 3.3: *Spin-coating of the PMMA as mask for all the technological steps*

Spin-coating of E-spacer: Since sapphire is insulator, beam deflections occurs on the surface when PMMA masks are exposed by electron beam lithography. For this reason, E-spacer 300Z,

a conductive polymer from Showa Denko K.K., has been used as charge dissipation layer. In order to reach a good thickness homogeneity, it has been spin-coated at a speed of 3000 rpm for 60s with subsequent baking at 100°C for 45 s on the hot plate.

Development of PMMA resist: In order to develop the exposed PMMA masks, the E-spacer has to be removed by soaking the sample in distilled water. Subsequently, the resist has been developed in 1:3 MIBK:IPA for 15 s, soaked in isopropanol and then let it dry using a nitrogen gun.

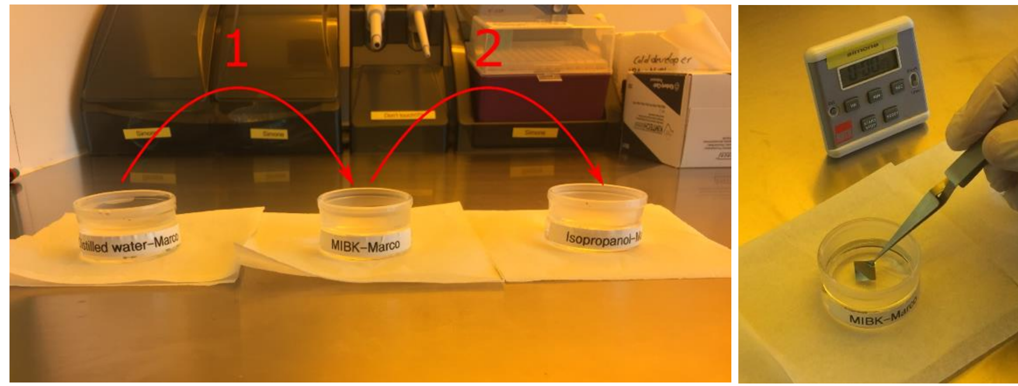
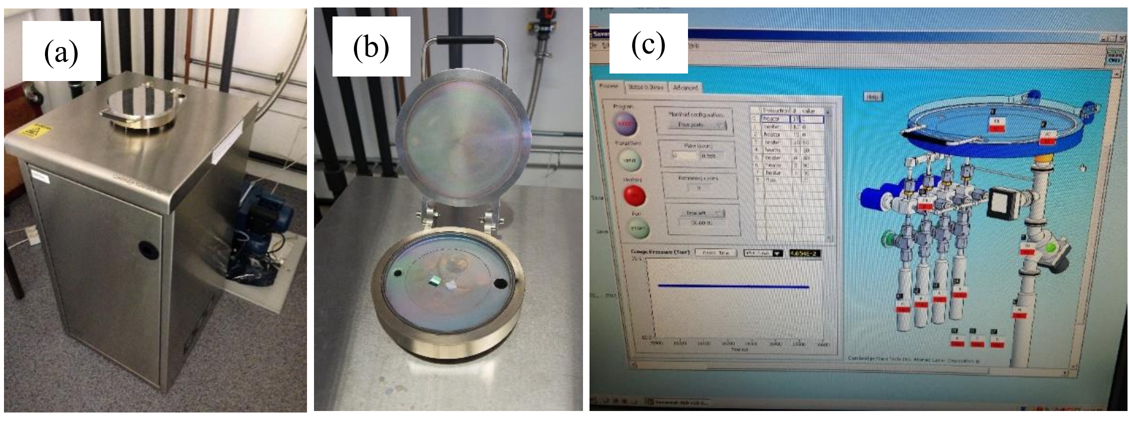


Fig. 3.4: *PMMA development procedure*

Electron beam lithography (EBL): During sample fabrication, several consecutive steps of EBL have been performed in order to expose the PMMA masks for subsequent metal/oxide deposition or for graphene etching. Raith eLine EBL system has been used to write the patterns into the PMMA (Fig. 3.5). It operates at a maximum acceleration voltage of 30 keV with a gun pressure of 6×10^{-10} mbar and a chamber pressure $< 2 \cdot 10^{-6}$mbar. High accuracy in the xy-movement (~2nm) is reached thanks to the interferometric stage. Depending on the aimed resolution, due the pattern dimensions, two different beam apertures have been used. The first consists of 20 µm aperture and a step size of 8nm used for the exposition of the inner part of drain, source, gate electrodes and graphene mask. The second, instead, consists of 120 µm aperture and a step size of 69nm for the exposition of the source, drain and gates coplanar waveguides and for the contacting pads.

Fig. 3.5: *Raith "eLine" electron beam lithography system*

Atomic layer deposition (ALD): Atomic layer deposition has been used for the gate oxide deposition. This is a critical step, since the thickness, the uniformity and the quality of the deposited oxide have effect on the device performances, in terms of graphene mobility and gate capacitance. For my purpose, Cambridge Nanotech Savannah ALD (Fig. 3.6(a-c)) and R-200 Advanced system from Picosun (Fig. 3.6(d)) have been used.



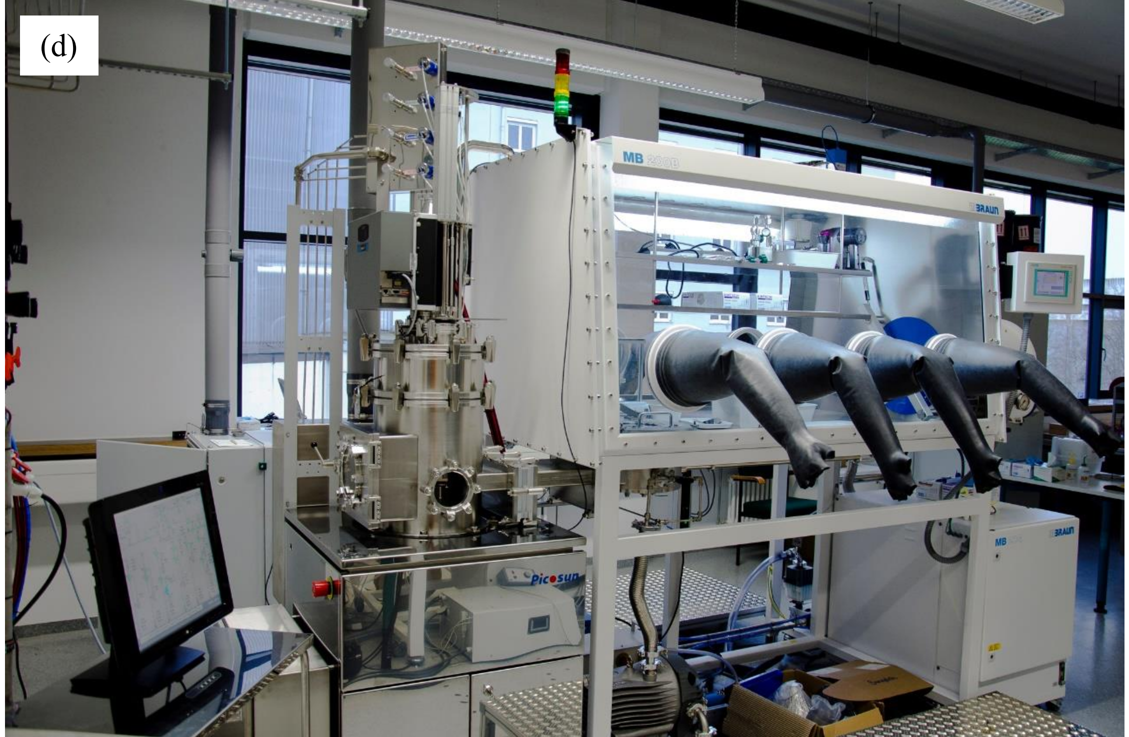


Fig. 3.6: *a-c) Cambridge Nanotech Savannah ALD, d) R-200 Advanced system from Picosun*

CVD Graphene transfer: Monolayer CVD graphene used in my work has been provided by Prof. M.H. Jang and Prof. J.-H. Ahn from the School of Electrical and Electronic Engineering, Yonsei University, Seoul, South Korea. It has been initially grown on copper foil and then transferred onto a SiO_2/Si substrate using standard methods [118]. Since graphene has to be transferred again from such support to the aimed substrate (sapphire), all the steps used are illustrated in the Fig. 3.7

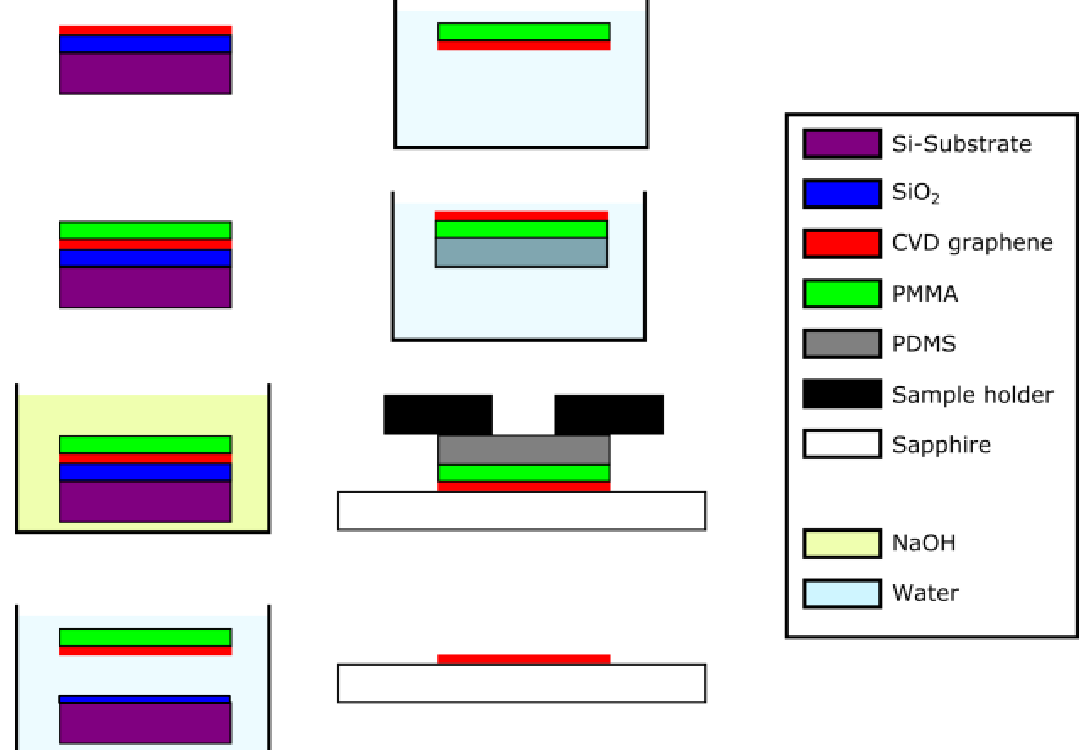


***Fig. 3.7:** Graphene transfer process sketch*

Around 800 nm of PMMA, (8wt%) has been spin coated onto the graphene layer. Such PMMA thickness guarantees at the same time a good elasticity and mechanical resistance. A PDMS adhesion layer has been used as a mechanical support to help the imprinting of the PMMA-graphene sheet (*i.e.* the assembly) on the target substrate. In order to help the detachment of the assembly from the substrate, the edges have been scratched and then the stack has been soaked first in a 1 mol NaOH solution to dissolve the thin SiO_2 layer (*Fig. 3.8*(a-b)) and then cleaned by soaking it in pure distilled water (*Fig. 3.8*(c)).

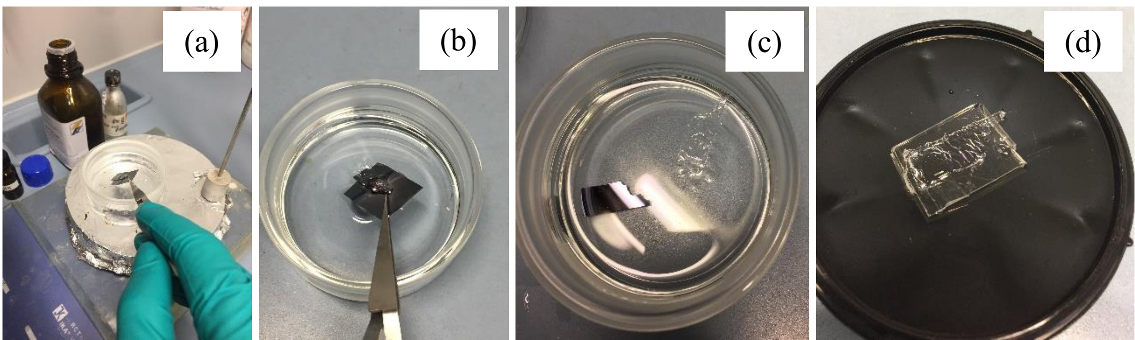


***Fig. 3.8:** Detaching of the assembly from the silicon substrate*

Afterwards, the assembly has been placed on a microscope glass to let it dry and then mounted on ad-hoc sample holder with a hole in the metal made to watch through and help for the further

alignment in the microscope (Fig. 3.9). Below the sample holder, the sample is placed on a hot plate at 60°C.

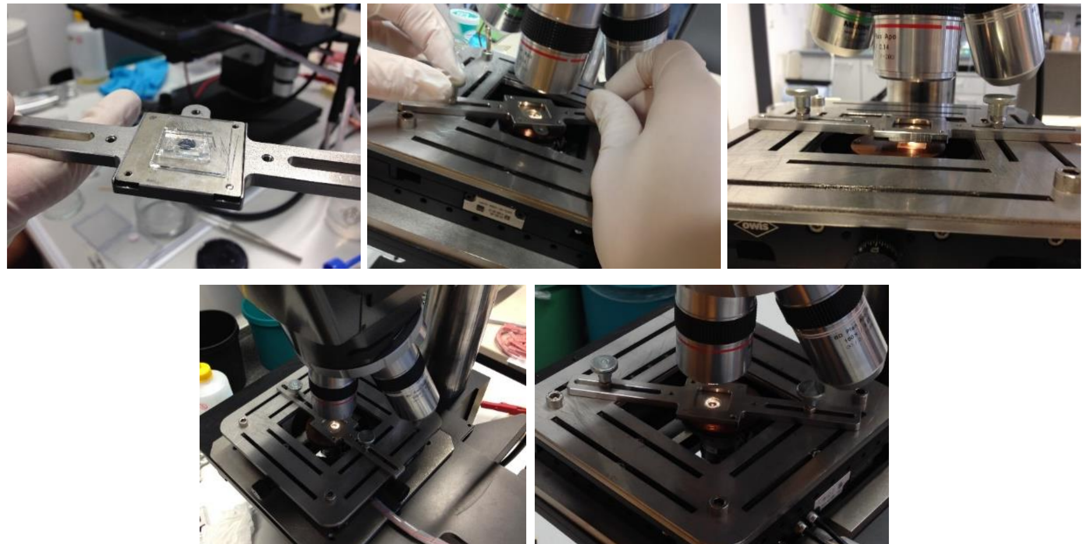


Fig. 3.9: *Assembly placed on the ad-hoc sample holder for the transfer process on the arbitrary substrate*

When the assembly touches the substrate, the temperature has been increased up to 120°C and it starts to adhere as shown in Fig. 3.10. The alignment has been controlled through the sample holder mounted on the optical microscope. Finally, after waiting for 5 min, the sample holder has been lifted up and both the PMMA and the graphene remains. A subsequent soaking in acetone and isopropanol has been performed to remove the PMMA residue.

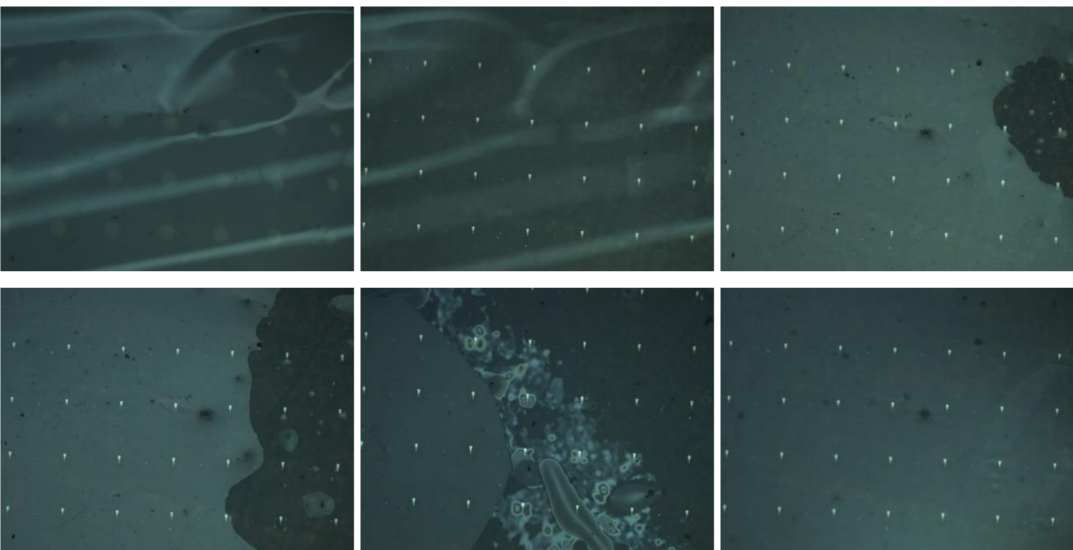


Fig. 3.10: *Graphene-PMMA-PDMS adhesion on the sample*

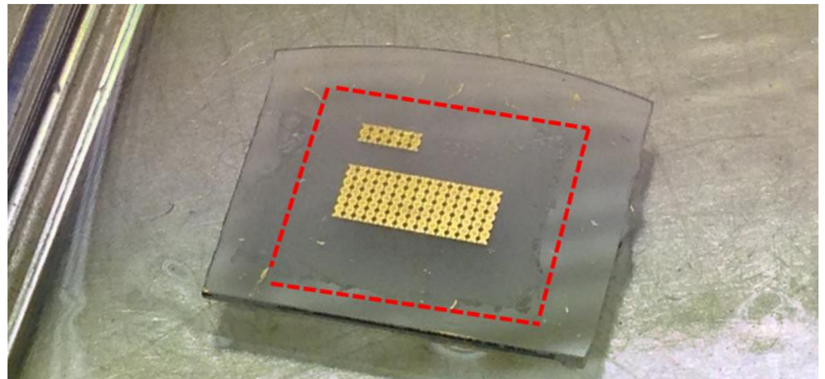


Fig. 3.11: PMMA-graphene transferred on the sample

HV metal evaporation: For metal evaporation the system in Fig. 3.12a has been used. Different metals such as palladium, copper, chromium, titanium and gold can be evaporated (Fig. 3.12b).

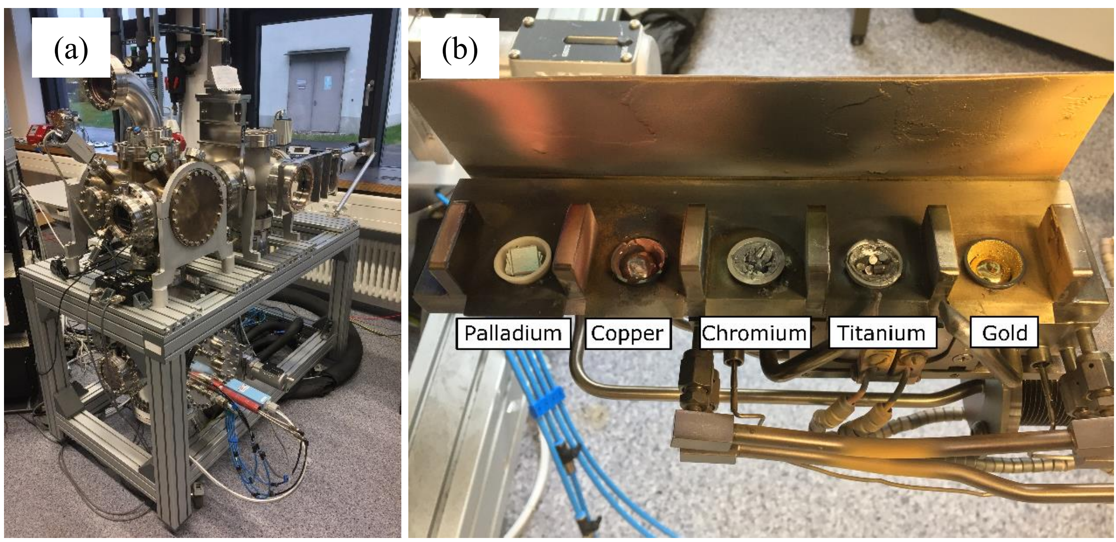


Fig. 3.12: (a) HV metal evaporator (Schimmel group), (b) crucibles.

A high voltage (3 kV) electron beam is used to melt the targets, deflected by magnetic fields (xy-deflection). The system is equipped by a load-lock chamber in order to keep the very low pressure of the main chamber. Both the main and the pre-chamber, when both evacuated by turbomolecular pumps, reach a pressure of around 10^{-7}mbar.

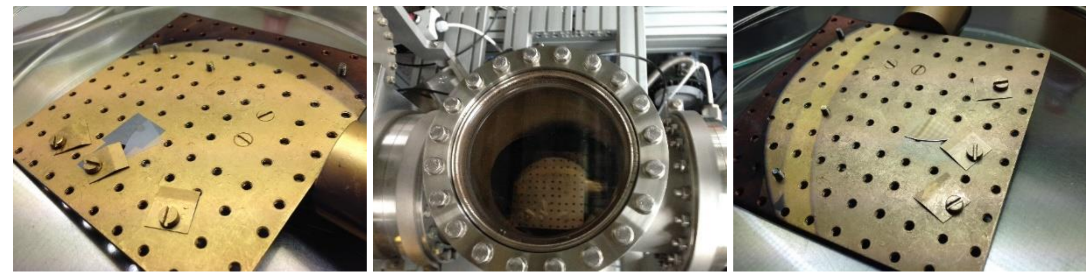


Fig. 3.13: HV Metal evaporation

UHV metal evaporation*:* Due to graphene inertness to atomic layer deposition precursors, a deposition of ~3nm of aluminum by the molecular beam epitaxy (Fig. 3.14) has been made in order to let it naturally oxides. This process has been necessary for the subsequent ALD oxide deposition.

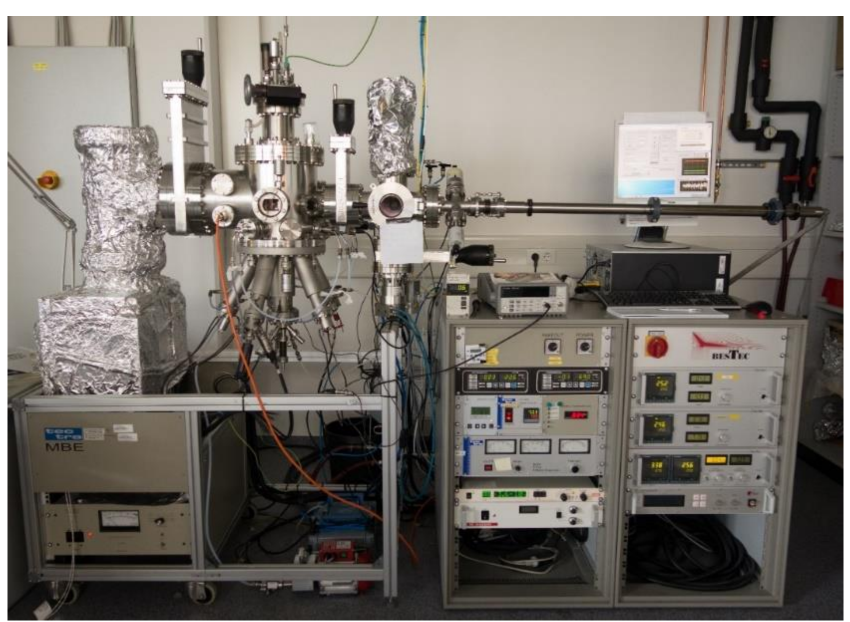


Fig. 3.14: *UHV metal evaporator (Beckmann group)*

Lift-off*:* In order to remove the PMMA mask after the metal/dielectric deposition a lift-off procedure has been performed. Both acetone and dimethyl sulfoxide (DMSO) have been used. In particular, after ALD deposition, since the material is deposited isotropically, even at the edge of the structure, soaking the sample in acetone is inefficient. Therefore, the sample, after applying scratches far away from the structures (in order to let the solvent, go through), has been soaked in DMSO at 70°C. For metal lift-off, instead acetone has been used. If graphene has not been transferred on the surface, sonication could help the lift-off but it is avoided after its transfer.

Fig. 3.15: *lift off procedure*

3.4 M4 Device

3.1.2 Design

After choosing Sapphire as a good and promising substrate for graphene high-frequency electronics, a design of GFETs has been made selecting, at first, aluminum oxide for the gate dielectric. A top dual gate structure with coplanar waveguide has been used. The new design is composed of the extrinsic part (see orange in Fig. 3.16) and the intrinsic part (see yellow in Fig. 3.16). Thanks to this configuration, the extrinsic part (drain/gate tapered CPW launchers) remains the same for all the devices, including test-devices for the de-embedding procedure (A.4). Additionally, the vertical spacing between the input/output contact pads (Fig. 3.16(a)) has been chosen equal to that of the Impedance Standard Substrates (ISS) of the on-wafer calibration Kit (A.2.3). This aspect allows the design to keep always the same coupling capacitance.

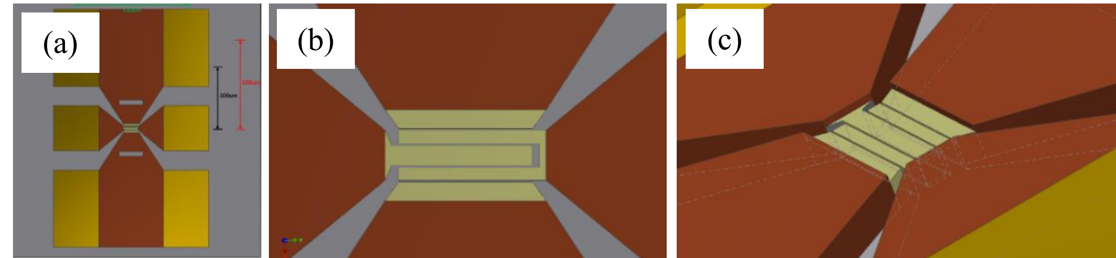


Fig. 3.16: *Sketch of the design of device M4*

The cross section of this family devices, called M4, is shown in the following sketch, Fig. 3.17:

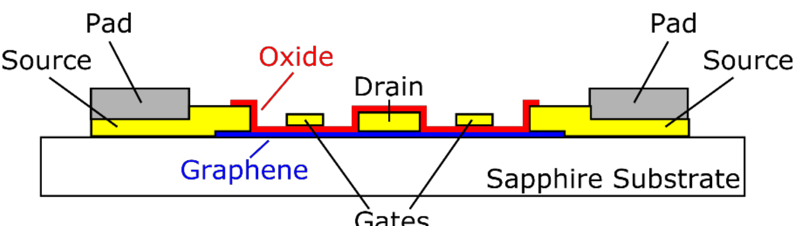


Fig. 3.17: *Cross section of M4 family devices*

3.1.3 Layout influence on GFETs microwave performances

A statistical and parametrical investigation aimed at experimentally evaluating the microwave parameters dependence on GFETs dimensions has been made. In detail, the analysis has been carried out on samples with different geometries (i.e., varying both the gate-drain/source distance and the gate length) to study the layout influence on the device performances. The cross section of the devices is depicted in Fig. 3.18(a)

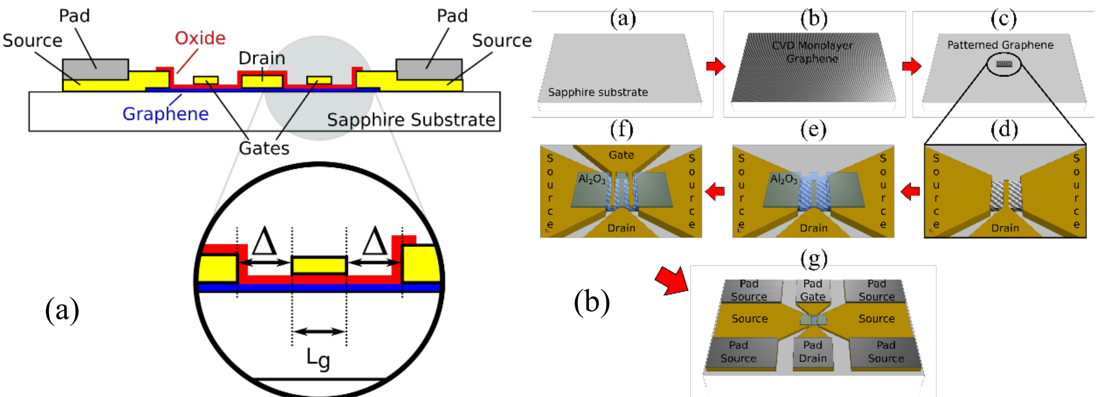


Fig. 3.18: *a) Cross-section diagram of the GFET, b) Sketch of the fabrication process of GFETs*

All the fabrication techniques have been already described in par. 3.3. All the steps aimed at the construction of the devices are shown in Fig. 3.18(b). The samples were built on a sapphire substrate. A single-layer of Chemical Vapor Deposition (CVD) graphene has been first transferred onto the substrate. Reactive Ion Etching has been used to pattern the graphene channel. Source/drain electrodes have been patterned onto a graphene sheet using E-beam lithography followed by a Ti / Au (~ 5 / 150 nm) deposition and lift-off in acetone. Around 2 nm of aluminum have been evaporated by molecular beam epitaxy as seed layer for the subsequent step. Around 10-nm thick Al_2O_3 film has been directly grown via Atomic Layer Deposition at 90°C as dielectric layer on the active device area. Finally, gate fingers geometries have been patterned by E-beam lithography on the oxide layer and then Ti / Au (~ 5 / 150 nm) contacts have been deposited. A sketch and a micrograph of a typical fabricated GFET are shown in Fig. 3.19.

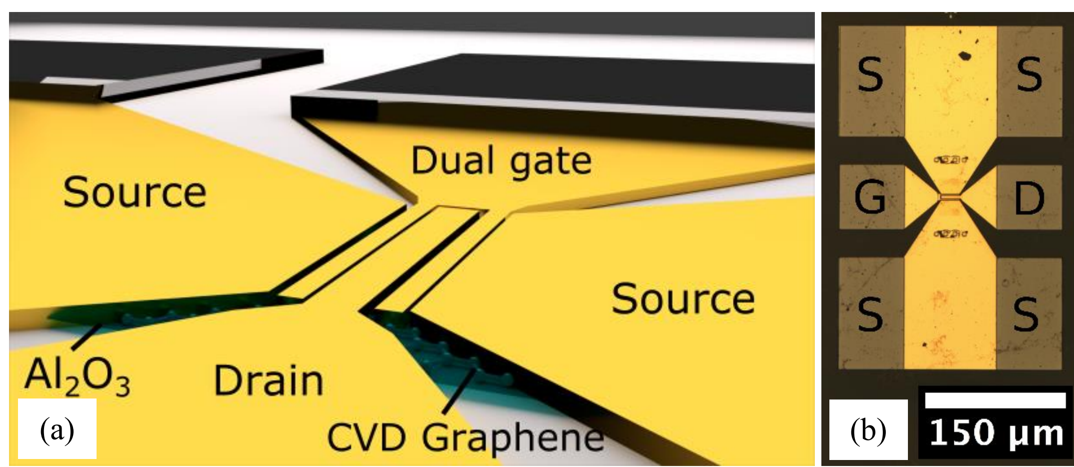


Fig. 3.19: *(a) Sketch of the device; (b) Micrograph of a fabricated sample.*

Twenty-four GFET families, differing from each other only for the gate-drain/source distance (Δ) and the gate length (L_g), have been fabricated on a single chip. Each family includes 10 nominally identical devices. GFETs dimensions (Δ and L_g) have been chosen in the range [0.125 ÷ 0.175]

μm and [0.125 ÷ 2.000] μm, respectively, while the drain length and the channel width have been kept constant at 3 μm and 20 μm, respectively. Moreover, in order to perform the de-embedding procedure, auxiliary test structures (open, short and thru-line) have been fabricated on the same chip.

3.1.3.1 Chip description

The map of the fabricated devices is shown in Fig. 3.20. The devices are divided into four groups which will be described below:

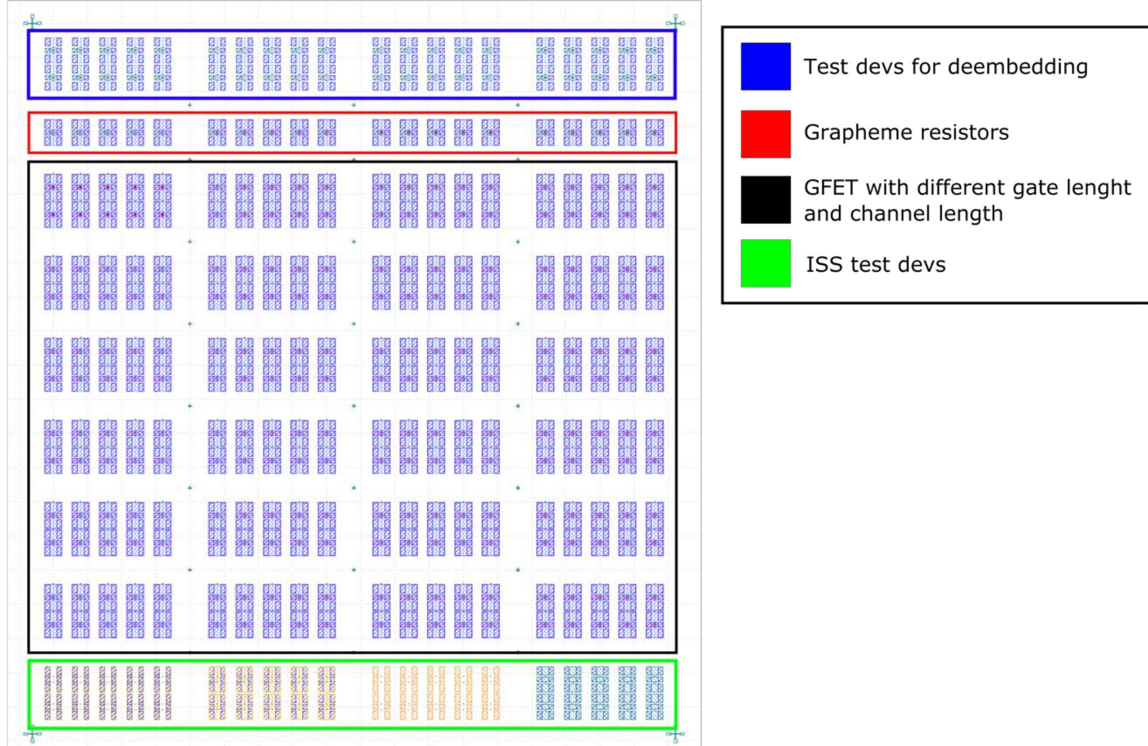


Fig. 3.20: *Map of M4 fabricated devices*

First (see Fig. 3.20), the blue block is composed of the test devices fabricated to help the de-embedding procedure. In detail, such devices are two groups of open circuit devices (Open) (Fig. 3.21 (a-c)), one group of the short circuit devices (Short) (Fig. 3.21(b)), and one group of thru line devices (Thru) (Fig. 3.21(d)). In particular, the latter are test elements designed to make a verification of the passive devices electromagnetic simulation.

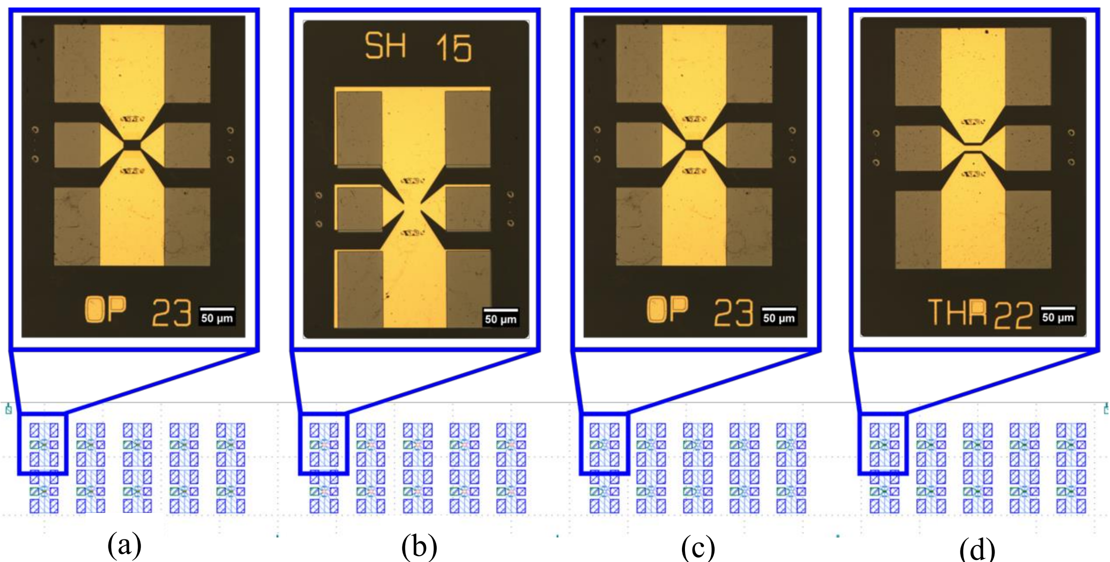


Fig. 3.21: *Map of the test devices for de-embedding*

The second block (see Fig. 3.22) consists of a group of graphene resistors fabricated to evaluate the graphene resistivity after the transfer procedure.

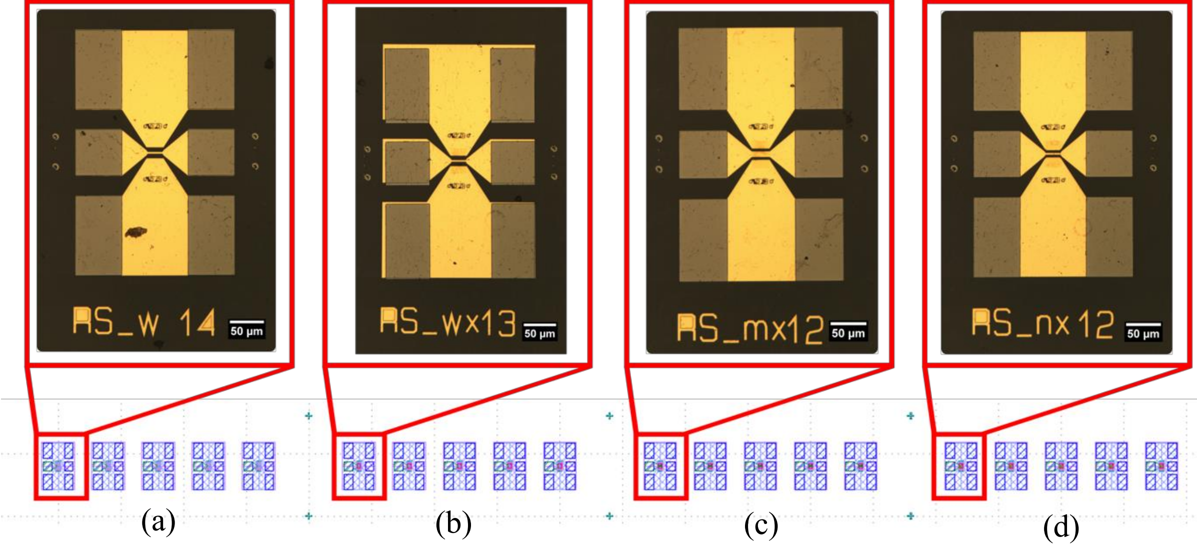


Fig. 3.22: *Map of the Graphene-resistors*

Graphene resistors have been fabricated with different intrinsic contacts dimensions. All the resistors exhibit the same extrinsic geometry of the GFET. The resistor in Fig. 3.22(a) has a width of 3µm of the center contact equal to the fabricated GFET. The contact area is the same of the GFET drain. This kind of device has not oxide on top, so this means that is not encapsulated. The same geometry has been used for the Resistors shown in Fig. 3.22(b). In these devices, additional 10nm of Al_2O_3 have been deposited onto it. The aim of the fabrication of these resistors is to compare the measurements results with the previous ones without oxide.

Then, resistors shown in Fig. 3.22(c) exhibit a larger center contact (8.5µm), so a smaller area of graphene exposed and, moreover, it is encapsulated means devices with 10nm of Al_2O_3 deposited onto them.

Lastly, in Fig. 3.22(d) the resistors have 3 um width center contact but the upper and lower launchers are closer compared to the usual ones.

The center of the chip is composed of 24 families of GFETs having different gate length and channel length. All the dimensions are chosen in order to make a comparison of the layout influence on microwave performances. Fig. 3.23 summarizes the denomination of each family and the corresponding Δ and L_g values.

		Δ=0.125um	Δ=0.250um	Δ=0.500um	Δ=0.750um
		A	B	C	D
Lg=0.125um	A				
Lg=0.250um	B				
Lg=0.500um	C				
Lg=1.000um	D				
Lg=1.500um	E				
Lg=2.000um	F				

Fig. 3.23: *Map and photos with labels of the devices M4*

The last block consists (see Fig. 3.24) of test elements designed to make a verification of the electromagnetic simulation on the passive devices.

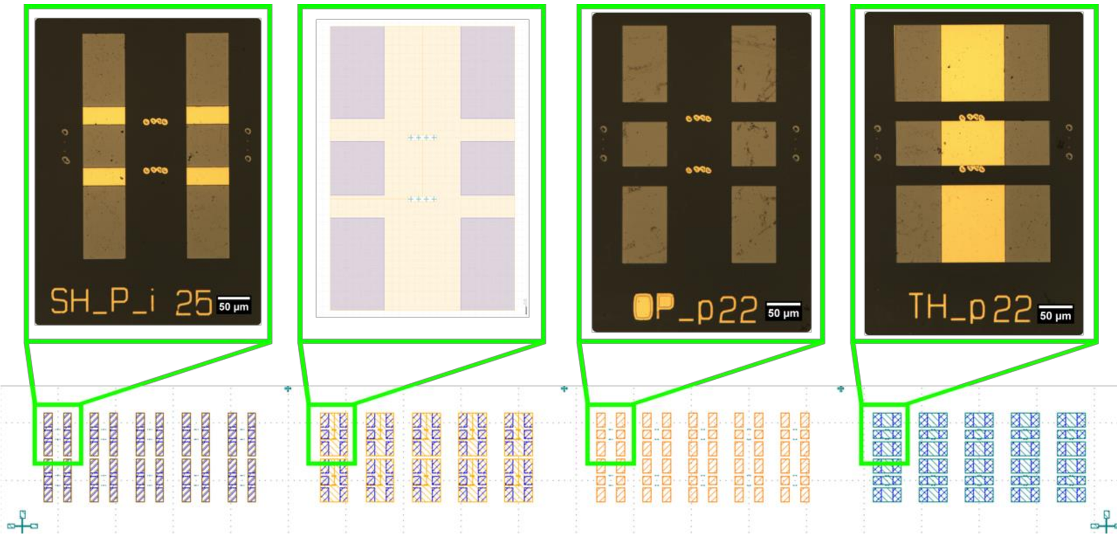


Fig. 3.24: Map of the test element

3.1.4 DC and RF characterization

DC and RF measurements have been performed by using the set-up described in A.2.1. Typical DC curves of the characterized devices are shown in Fig. 3.25. In particular, Fig. 3.25(a) and Fig. 3.25(b) show I_D and gm vs V_{GS} as a function of V_{DS}, respectively. The fabricated transistors exhibit a n-type behavior, as inferred from the shift of the Dirac point on the left of $V_{GS} = 0$. Subsequent RF/microwave measurements have been performed in the region where g_m exhibits its highest value. The scattering parameters have been than measured using a HP8510C Vector Network Analyzer and a Cascade Summit 9000 wafer-probe station in the frequency range [50 MHz ÷ 20.05 GHz] in standard environmental conditions. The de-embedding of the devices has been carried out through a combined use of electromagnetic simulations and experimental measurements on auxiliary test structures implemented on the same chip (Open, Short, ecc.) (A.4.2). The short-Circuit Current Gain ($|h_{21}|$) and the Maximum Available Gain (MAG) of both intrinsic and extrinsic device, as calculated from the measured S-parameters, are depicted in Fig. 3.25(c) and Fig. 3.25(d), respectively.

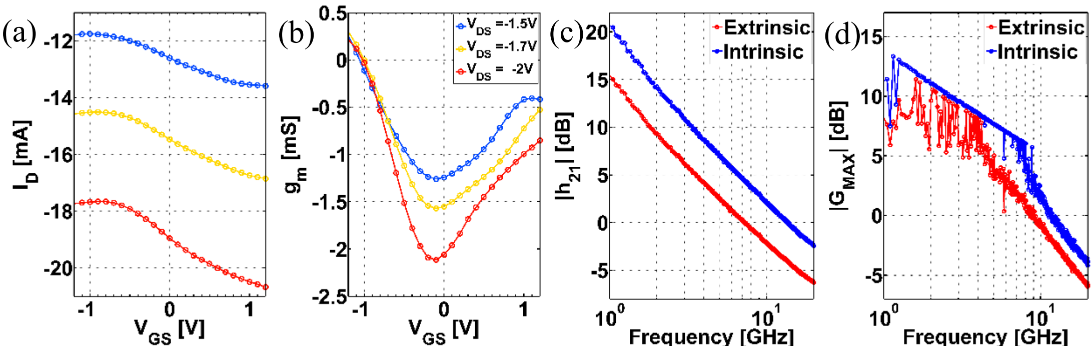


Fig. 3.25: *I_D (a) and g_m (b) vs V_{GS} curves as a function of V_{DS} values for a GFET with Δ = 0.125 µm and Lg = 0.250 µm. (c) Intrinsic and extrinsic values of |h21| and (d) MAG as function of frequency for a GFET with Δ = 0.125 µm and Lg = 0.250 µm*

Once verified the transistor effect in our fabricated devices, an in-depth investigation of geometry dependence in particular on the influence of both gate-length and gate-drain/source spacing has been carried out, aimed at optimizing high frequency performances. To achieve this goal, a parametric analysis on the twenty-four fabricated GFET families has been performed by means of a statistical average on 10 nominally identical devices. Fig. 3.23 summarizes the denomination of each family and the corresponding Δ and L_g values. Fig. 3.26(a-b) depicts f_T and f_{max} values of the parametrical analysis, as a function of Δ and L_g. Each histogram has been obtained as the average of the measured f_T and f_{max} on 10 devices of the same family. Additionally, an interpolation of these data has been performed and the results are shown in the two 2D maps, Fig. 3.26(c-d)). All the values are referred to the de-embedded data. As shown in the maps, the trends of f_T and f_{max} look similar. In detail, when keeping constant L_g and decreasing Δ, an increase of both figures of merits is observed. Moreover, when keeping constant Δ, both f_T and f_{max} do not increase monotonically. These results allow to infer that f_T and f_{max} are both Δ and L_g dependent

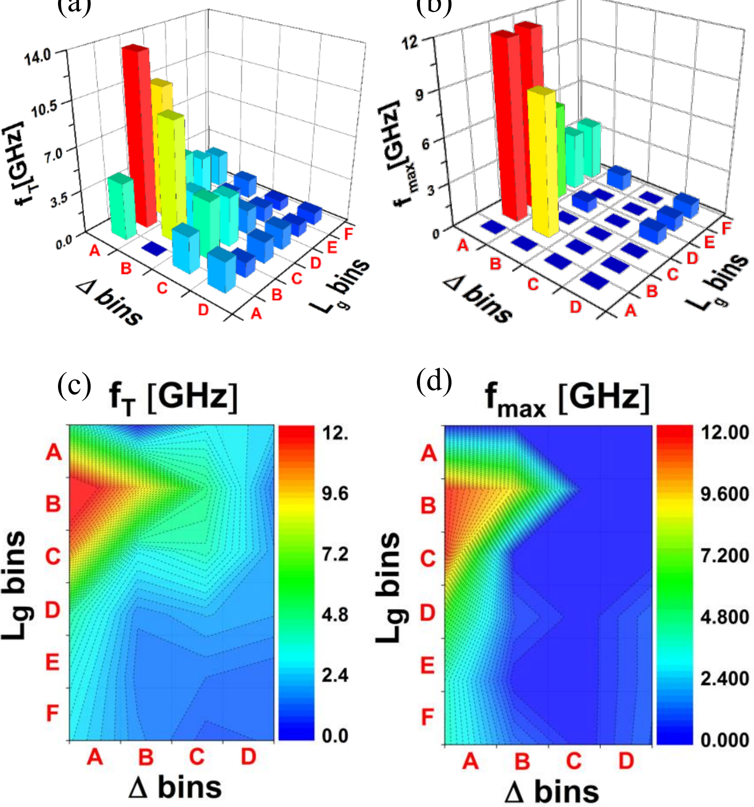


Fig. 3.26: *Results of the statistical and parametrical analysis: 3D histograms and 3D map of (a-c) cut-off frequency f_T and (b-d) maximum frequency of oscillation. f_{max},;*

and an optimum region exists where both the figures of merit are maximized. The best values reached for f_T and f_{max} are 13.68 GHz and 12.3 GHz, respectively. These values are obtained for devices belonging to BA bin (Δ = 0.250 μm; L_g = 0.125 μm) and are more than ten times higher than those ones reached with the devices having the largest channel length (i.e., FD bin: Δ = 2.000 μm; L_g = 0.750 μm), but also higher than ones pertaining to smaller channel length devices, contrarily to what could be expected from similarity with non-graphene-based FETs.

3.1.5 Optical measurements

On the same devices, a study of the optical response has been performed by using the optical set-up described in (A.2.4.1). Four devices with different dimensions have been tested:

- Device BA24 (Δ = 0.125 μm; L_g = 0.125 μm);
- Device BC15 (Δ = 0.25 μm; L_g = 0.125 μm);
- Device EA24 (Δ = 0.125 μm; L_g = 1.500 μm);
- Device EC24 (Δ = 0.5 μm; L_g = 0.125 μm).

Photovoltage measurements have been performed without applying an external bias to evaluate the photovoltaic effect. Optical measurements as a function of both the incident laser power and the gate-source voltage of the transistors have been carried out employing an automated bench controlled via dedicated software, and the results are shown in Fig. 3.27.

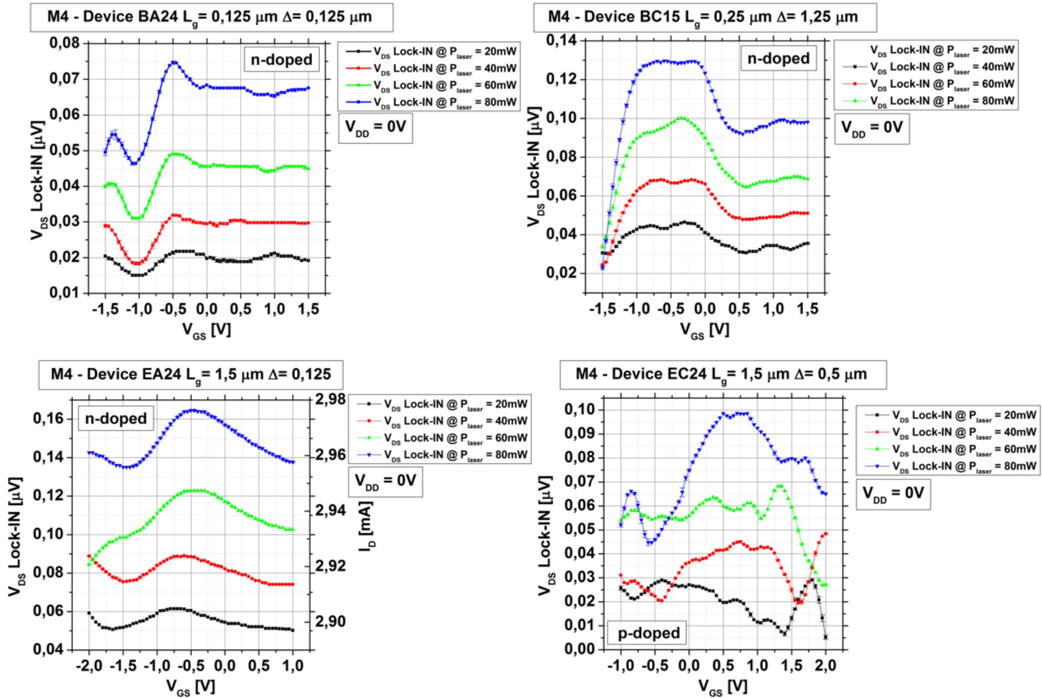


Fig. 3.27: *Comparison between optical response of all the devices under test at 0 V bias voltage.*

It is possible to assume that in the devices with smaller channel (BA24 - BC15) the gating effect is stronger due to probable built-in field through the channel. Instead, in the other two devices the effect is less evident but a photovoltage can be measured.

3.5 M7 Device

3.1.6 Design

Fabrication of competitive Graphene Field-Effect Transistors (GFETs) is surely a key and challenging task due to the need of avoiding the damage of graphene lattice and reducing unwanted parasitic components [70] that would drastically worsen devices performances. As discussed in Par. 3.2, in graphene all the above mentioned oxides can potentially be used as gate oxide layers for field effect transistors fabrication. In particular high-k dielectrics have been studied to enhance the transistor performances [116]. Device family called M7 consists of back gated graphene field effect transistors employing Al_2O_3, TiO_2 and HfO_2 as oxide layers.

3.5.1.1 Chip description

The map of the fabricated devices is shown in Fig. 3.28. The devices are divided into four groups which will be described below.

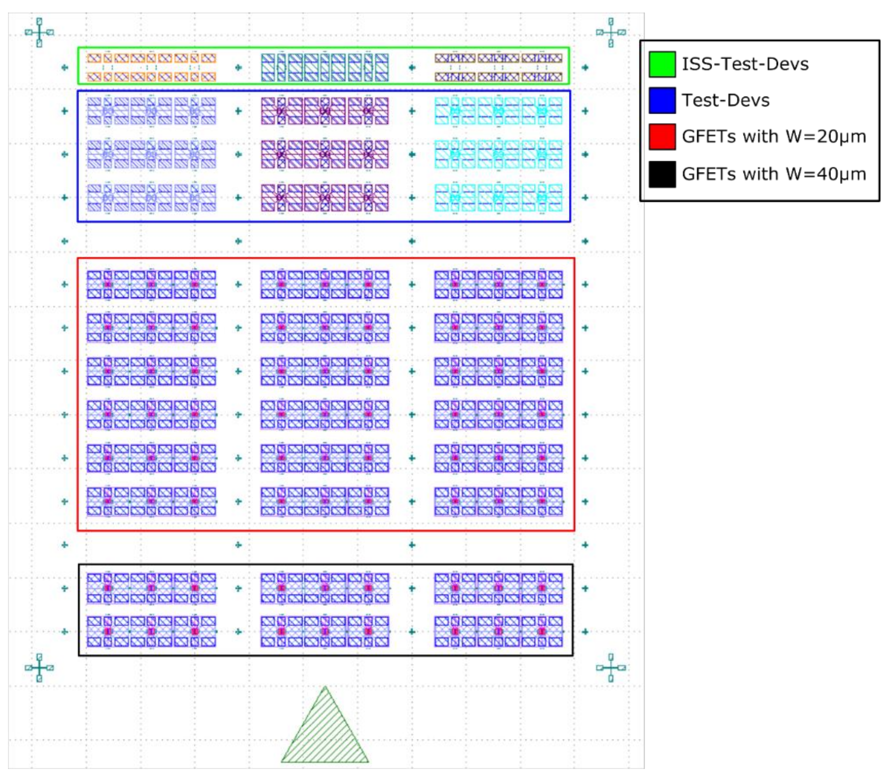


Fig. 3.28: *Map of the devices M7*

The red block is composed of GFETs having the same gate length and gate width (0.5µm and 20 µm respectively). The block can be divided into three different groups. In the first one on the left there are GFETs with Al_2O_3 as dielectric layer, in the second one TiO_2 and in the third one HfO_2. The black block instead consists of three families of GFETs having the three different oxides, however in this case the gate width of the devices is 40 µm.

In the blue block, all the devices used for the de-embedding procedures have been fabricated such as Open, Short and Thru structures as shown in the figures below (Fig. 3.29).

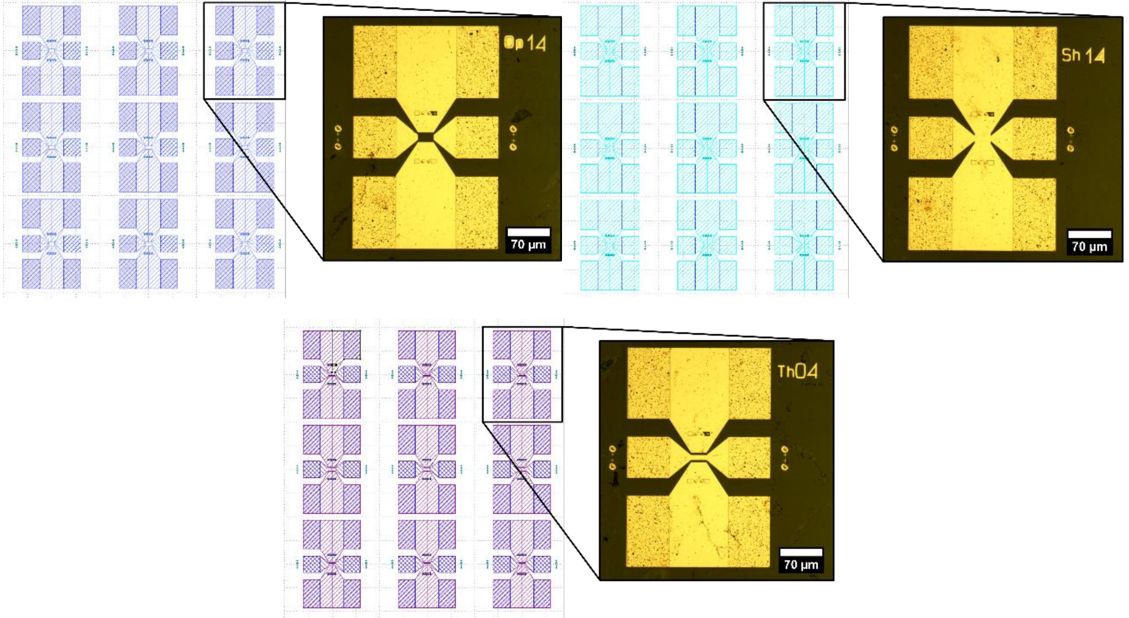


Fig. 3.29: *Map and micrographs of Open, short and thru devices*

Lastly, the green block presents all the devices called ISS fabricated to support the simulations of the more complex structures.

3.1.7 A comparison of different thin oxide films in GFETs performances

A comparison among different dielectrics employed as gate layers in Graphene field effect transistors (GFETs) has been performed in order to evaluate their Microwave response. In particular, aluminum oxide (Al_2O_3), titanium oxide (TiO_2) and hafnium oxide (HfO_2) have been tested. The devices have been fabricated on a single chip and a statistical analysis has been performed on an average of ten devices for each type of oxide in order to evaluate the dependence of high-frequency performances on the oxide material. Short Circuit Current gain and Maximum Available Gain have been chosen as quality factors to evaluate Microwave performances.

3.5.1.2 Fabrication technique

Herein, it is possible to refer to a "devices group" as a set of ten nominally identical devices fabricated on the same chip and employing the same gate oxide (i.e., Al_2O_3, TiO_2 or HfO_2). The fabrication steps used for the devices are herein summarised and depicted in Fig. 3.30(a). First, the dual-finger back-gate was patterned on a sapphire substrate by e-beam lithography followed by the evaporation of a thin Ti/Au bilayer (~ 5/40nm) and lift-off in acetone.

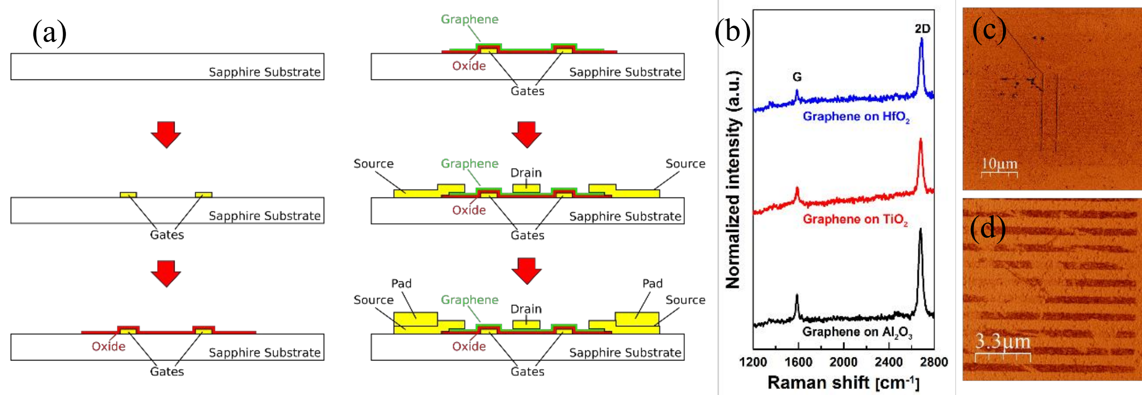


Fig. 3.30: *a) Schematic representation of GFETs fabrication steps, (b) Comparison among Raman spectra of transferred graphene on Al2O3, TiO2, and HfO2. (c) Results of an AFM phase measurement; (d) Zoom of the meandered structure of the devices.*

The oxides employed in the three different devices groups were deposited via Atomic Layer Deposition (ALD) by using the R-200 Advanced system from Picosun (par.3.3), by using the following recipes:

- TiO_2 deposition:
  - 220 cycles 100 °C
  - 0.1s Pulse $TiCl_4$ 4s purge
  - 0.1s Pulse H_2O 6s purge
  - Thickness ~ 13 nm
- HfO_2 deposition:
  - 107 cycles 120 °C
  - 0.5s Pulse tetrakis dimethylamino hafnium (TEMAH) 10s purge
  - 0.1s Pulse H_2O 12s purge
  - Thickness ~ 11 nm
- Al_2O_3 deposition:
  - 160 cycles 100 °C
  - 0.1s Pulse trimethylaluminium (TMA) 4s purge
  - 0.1s Pulse H_2O 4s purge
  - Thickness ~ 11 nm

A CVD-grown graphene film has been transferred onto the different oxides. Raman spectroscopy has been employed to assess the high quality of the transferred monolayer graphene onto all three oxides employed as gate dielectrics, as shown by the distinctive G (1580 cm^{-1}) and 2D (2680 cm^{-1}) peaks reported in Fig. 3.30(b). Afterwards, a meandered structure has been used to minimize contact resistance [82]. The meander is composed of a fingered structure with 500-nm-wide fingers, patterned by Reactive Ion etching (RIE). Atomic Force Microscopy (AFM) measurements were performed to evaluate the quality of the transfer process and of the etching (Fig. 3.30(c-d)). Subsequently, source/drain electrodes were patterned onto a graphene sheet using E-beam lithography followed by a Ti / Au (~ 5 / 100 nm) deposition and lift-off in acetone. All the fabricated devices exhibit the same geometry. In particular, the gate-drain/source distance (Δ) is 0.25 μm and the gate length (L_g) is 0.5 μm.

3.5.1.3 DC and RF characterization

After fabrication, all the samples were characterized under both DC and Microwave regimes by using the set-up described in A.2.2. DC measurements performed in the ranges V_{GS} = -1 V ÷ 1 V and V_{DS} = -1 V ÷ 1 V allowed to obtain the static transconductance curves (I_D vs V_{GS}) and, hence, to evaluate the incremental low-frequency transconductance ($g_m = \partial I_D / \partial V_{GS}|_{V_{DS}=cost}$), whose value deeply influences all the device performances. The results of the three samples employing Al_2O_3, TiO_2 and HfO_2 respectively, showing the best performances in terms of ON/OFF ratio and maximum g_m, are presented in Fig. 3.31. In particular, this figure shows I_D and g_m as functions of V_{GS} for all the oxides employed. All the curves are parameterized in V_{DS}. The transistors exhibit a p-type behavior as inferred from the shift of the Dirac point on the right of V_{GS} = 0. As a consequence of the different gate oxides employed, each DC curves group shows a different broadening. This aspect is of great interest, since it leads to different ON-OFF ratios and static g_m values. Table 3.1 reports the ON-OFF ratio and the static transconductance for the devices belonging to each oxide group. As it can be seen, the use of HfO_2 as oxide layer leads to a sharp improvement in terms of the static transconductance with the DC output currents showing higher values and slopes. A moderate increase on the ON/OFF ratio, instead, has been found.

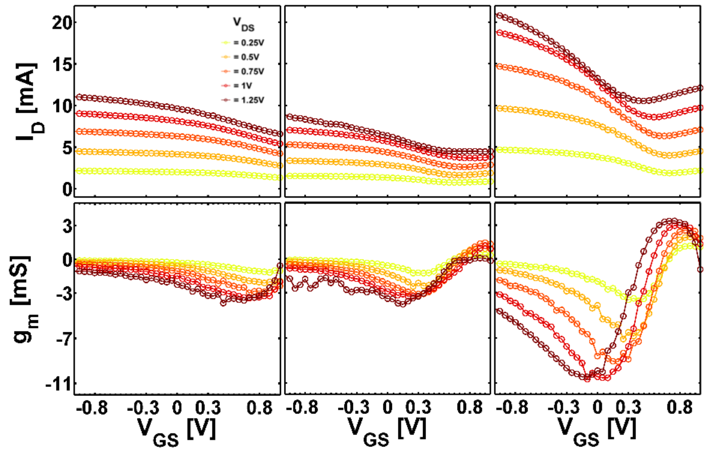


TABLE 3.1
ON/OFF RATIO AND MAXIMUM STATIC TRANSCONDUCTANCE OF THE DEVICES FOR EACH OXIDE GROUP

Device Oxide	ON/OFF Ratio	g_m [mS]
Al_2O_3	1.67	-3.86
TiO_2	1.93	-4.03
HfO_2	1.97	-10.66

Fig. 3.31: *I_D and gm vs V_{GS} curves as a function of V_{DS} for GFETs employing Al_2O_3, TiO_2 and HfO_2 as gate oxide.*

To avoid the shift of the static curves due to the well-known hysteresis in graphene-based devices [79], DC and RF/microwave [300kHz - 20GHz] measurements have been simultaneously performed for each operating point (A.2.2) following an appropriate pre-determined, computer controlled, voltage sequence/timing. Short-Circuit Current Gain ($|h_{21}|$) and Maximum Available Gain (MAG) (and, from these, f_T and f_{MAX}) have been calculated for each device from the S-parameters and chosen as quality indexes for high-frequency analysis. To extrapolate the intrinsic device gain values, a de-embedding has been performed through experimental measurements on auxiliary test structures implemented on the same chip (A.4). The results are depicted in Fig. 3.32. The data refer to a statistical average of ten identical devices for each oxide family.

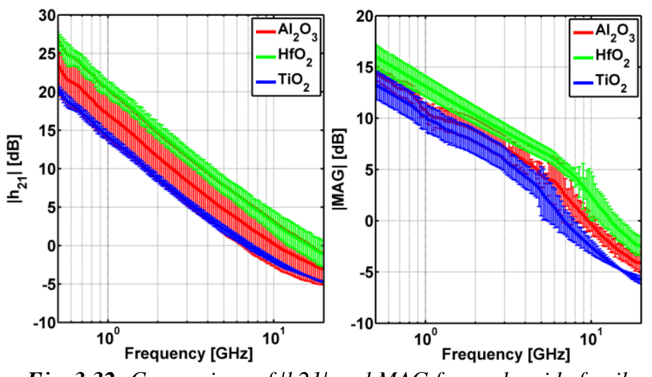


TABLE 3.2
CUT-OFF FREQUENCY AND MAXIMUM FREQUENCY OF OSCILLATION OF THE DEVICES FOR EACH OXIDE GROUP

Device Oxide	f_T [GHz]	f_{max} [GHz]
Al_2O_3	10.56	9.72
TiO_2	7.15	6.96
HfO_2	16.46	13.19

Fig. 3.32: *Comparison of |h21| and MAG for each oxide family*

The error bars in the figure represent the standard deviation of the performances for each analyzed family. As shown in Fig. 3.32, the behavior of the $|h_{21}|$ is 20 dB/dec and the trends of the three curves are well defined. In other words, by looking at the standard deviation of the curves, each oxide group exhibits a performance curve which is well confined in a specific region, without any noteworthy overlap with other device types. As expected from the DC analysis, the devices with

hafnium oxide show the best performances in terms of gains (magnitude), with a f_T = 16.46 GHz and a f_{max} = 13.19 GHz. Instead, alumina and titania devices show lower f_T and f_{max} values as reported in Table 3.2. From these results, it is possible to infer that, even in graphene-based transistors, the κ-factor is not the only key to improve microwave performance since, in this case, the best results would be obtained using titanium oxide. In fact, a lower energy gap, which is typical of high-κ dielectrics, and thus a smaller conduction band offset, facilitates the transport of the charge carriers through the potential barrier increasing the gate leakage and thus decreasing the transistors performances. Hence, a compromise between both the band offset and the κ-factor should be found and hafnium oxide represents the best choice in this sense.

3.1.8 Photodetection in graphene-based transistors for telecom applications

M7 devices have been employed also as 1.55 μm infrared photodetectors for telecom applications. A combination of both bolometric and phototransistor effects has been shown as the photogeneration and amplification mechanism in the fabricated devices. For the first time, an experimental campaign aimed at evaluating the signal-to-noise ratio dependence on the transistor operating point has been accomplished. Photoresponse measurements have been carried out varying both the incident optical power and the transistor operating point. Optical measurements as a function of both the incident laser power and the DC biasing of the transistors have been carried out employing an automated bench controlled via dedicated software.

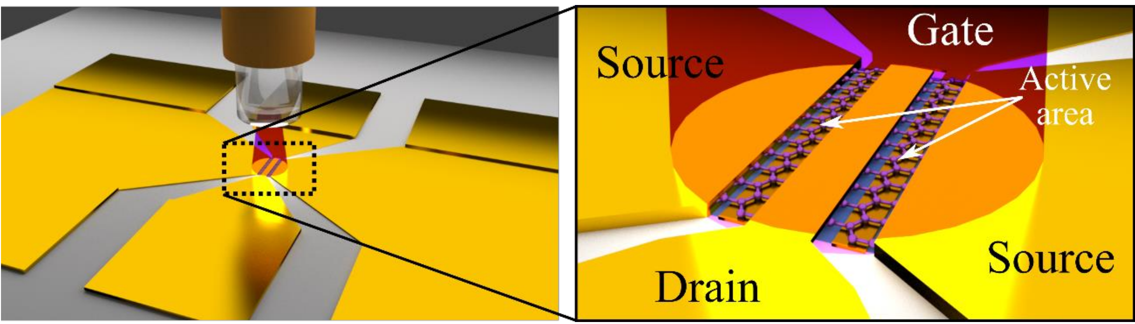


Fig. 3.33: *Rendered image of the GFET under laser illumination.*

The drain-source photocurrent (I_{ph}) has been calculated as the ratio between the voltage read from the lock-in and R_{DD} (Fig. 3.34(a)). It has been noticed that a wrong choice of the operating point can vanish the photodetector performance, being the output current independent on the laser power or noisy. Conversely, by appropriately changing the bias condition, it is possible to obtain a sharp variation of the output photocurrent as a function of the input optical signal. For this reason, optical measurements have been performed with and without laser irradiation and at different DC bias conditions (i.e., V_{GS} = -1.5 V ÷ 1.5 V and V_{DS} = 0.06 V ÷ 1 V). In what follows,

it is referred to *signal* as the maximum photocurrent (I_{ph}) generated under laser irradiation and to *noise* as the mean value of the lock-in current with no laser excitation. Therefore, it is defined the Signal-to-Noise Ratio (SNR) as the ration between the two above mentioned currents. Fig. 3.34 shows the dependence of signal (Fig. 3.34(a)), noise (Fig. 3.34(b)) and SNR (Fig. 3.34(c)) on the drain-source voltage.

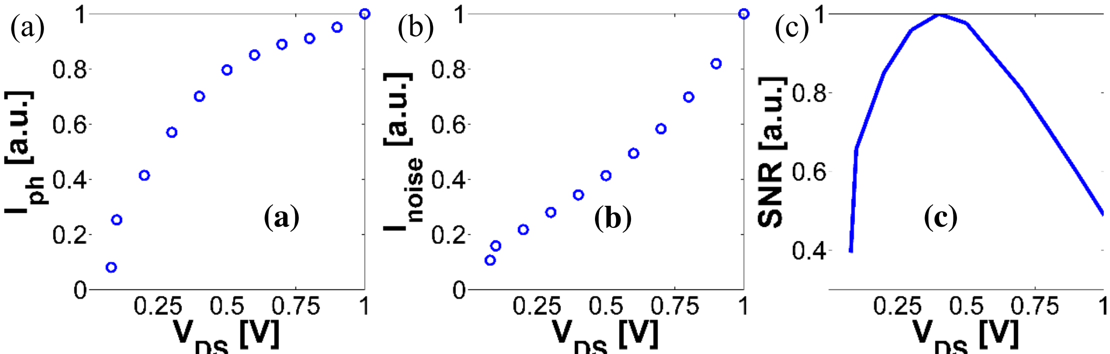


Fig. 3.34: *(a) Photocurrent, (b) average noise and (c) SNR as function of V_{DS}. The laser power on the sample was set to 7 mW.*

By looking at Fig. 3.34(a), it is possible to notice an initial increase of the photocurrent with the V_{DS} value, followed by a saturation starting at $V_{DS} \sim 0.5$ V. The average noise Fig. 3.34(b) instead, rises with V_{DS}, with an approximately linear trend on the entire explored bias range, leading to a SNR maximum value at V_{DS} = 0.4 V Fig. 3.34(c). The subsequent analysis of GFETs photoelectrical response as a function of the laser power impinging on the GFET, in the range [0 ÷ 7.6] mW, has been performed at this voltage. More precisely, static drain-source current (I_D, measured from the SMU) (Fig. 3.35(a)), static transconductance ($g_m = \partial I_D / \partial V_{GS}|_{V_{DS}=cost}$, Fig. 3.35(b)) and photocurrent (I_{ph}) (Fig. 3.35(c)) were measured simultaneously, in order to limit the typical hysteretic behavior [79], [119], [120] of graphene-based devices.

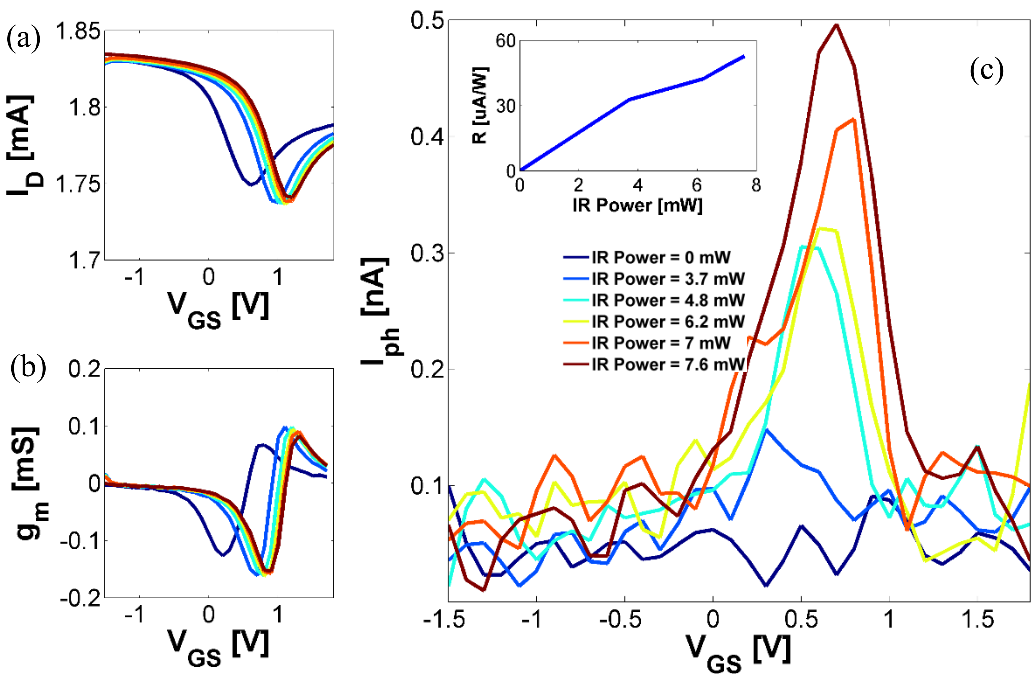


Fig. 3.35: *(a) Static drain current, (b) static transconductance and (c) photocurrent vs. gate source voltage (V_{GS}) under different IR power irradiation. Inset: Responsivity versus IR laser power for V_{DS} = 0.4 V.*

The photocurrent (Fig. 3.35(c)) increases with the laser power, reaching its highest value (I_{ph} = 0.49 nA) when the I_D-V_{GS} curve has its maximum slope, i.e. when the magnitude of the static transconductance is maximum (gm = -0.15 mS) (Fig. 3.35(b)). Photocurrent curves shift in V_{DS} Fig. 3.35(c)) according to the shift of the static curves, due to the well-known hysteresis in graphene-based transistors (Fig. 3.35(a)) [25-27].

The mechanisms of photogeneration involved in our GFETs are herein briefly explained. The optical signal is first down-converted to an electrical signal and then amplified exploiting the transistor effect of our device. More in deep, due to the higher energy bandgap of sapphire (7.3 eV) compared to the incident laser energy (0.8 eV), carriers cannot be provided by the substrate. For this reason, a combination of bolometric effect and phototransistor effect has been assumed as the responsible mechanism of both photocarrier generation and photocurrent amplification. The photodetector responsivity (R) has also been calculated as the ratio between the photocurrent and the optical power imping the 40-μm^2 graphene active area. A value of $R \cong 53 \frac{[\mu A]}{[W]}$ has been found. As depicted in the inset of Fig. 3.35(c), the responsivity as a function of the IR laser power at V_{DS} = 0.4 V shows an upward trend. This result relates with the monotonic increase of the I_{ph} versus the IR laser power.

3.6 Supplementary works

3.1.9 GFETs exploiting double-clamped geometry

Device geometry scaling has been the key task in the performance improvement of Si-MOSFET technology [59]. However, this aspect gave rise to different serious drawbacks, all known as short channel effects [121]. A technique employed in Si-MOSFET technology to avoid this important issue has been the adoption of a double gate device structure with promising results [122]–[124]. In par. 3.1.7 a comparison between different oxides has been done. Herein, instead, GFET exploiting the double-, clamped-gate structure has been designed, fabricated and characterized. A double clamped structure has been designed to improve the MOGFETs performances by increasing the device transconductance (g_m) without significantly influencing gate leakage, output conductance and reactive parasitic elements. An investigation has been made between single-bottom gate and double bottom/top gate geometries. Two different geometries were used with the same gate-length and channel-length (500nm/850nm respectively).

The first one (Fig. 3.36(a)) consists of a GFET with a single back gate, while the second one shows a clamped-gate (Fig. 3.36(b)). To reach better DC and RF performance, both structures were fabricated using double source/drain contacts [90]. Moreover, with the aim of reducing parasitic resistances [83], [86], meandered graphene contacts [82] devices were fabricated and compared with the standard ones.

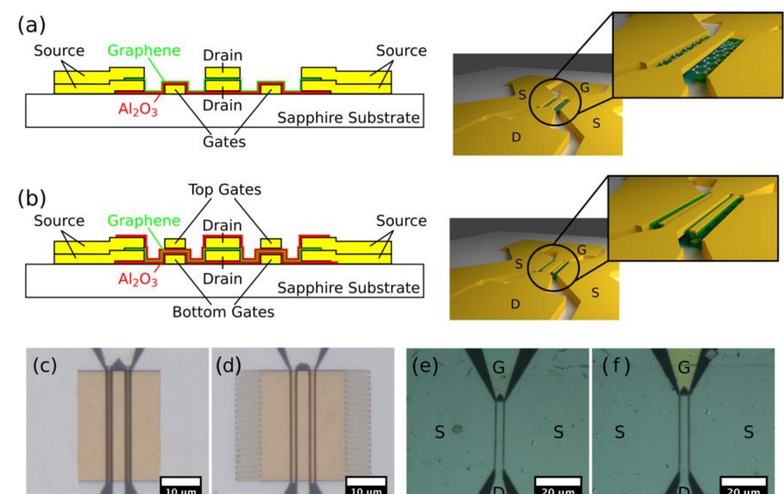


Fig. 3.36: Cross-section and tridimensional sketch of single-gate (a) and clamped-gate GFET (b), optical micrographs of the PMMA mask for the not meandered graphene (c) and for the meandered one (d), single-gate (e) and clamped-gate (f) fabricated devices.

3.6.1.1 Fabrication technique

For the fabrication of the devices, the following technological steps have been performed. First, the dual-finger back-gate has been patterned on a sapphire substrate by e-beam lithography followed by the evaporation of Ti/Au bilayer (~ 5/20nm) and lift-off in acetone. A ~ 8nm thick Al_2O_3 film has been directly grown via atomic layer deposition at 90° as dielectric layer. After

the deposition of bottom contacts (Ti/Au ~ 5/20nm), a CVD-grown graphene film has been transferred and etched into rectangular (Fig. 3.36(c)) or meandered pattern (Fig. 3.36(d)) by Reactive Ion etching (RIE). Source/drain top electrodes have been patterned onto Graphene sheet via e-beam lithography step followed by a Ti/Au (~ 5/25nm) deposition. Subsequently, the devices have been covered locally by a second layer of Al_2O_3 (~ 8nm) (Fig. 3.36(e)). In order to fabricate the clamped-gate samples, the dual-finger top-gate has been patterned on Al_2O_3 by e-beam lithography, followed by the evaporation of a Ti/Au bilayer (~ 5/20nm) and lift-off in acetone (Fig. 3.36(f)).

3.6.1.2 DC and RF characterization

After fabrication, GFETs have been characterized in the DC regime (Fig. 3.37). Fig. 3.37(a-d) shows a comparison of the drain current (I_D) versus the gate voltage (V_{GS}) by varying the drain voltage values (V_{DS}) for the four different kinds of devices. Fig. 3.37(e-h) instead, depicts the DC transconductances ($g_m = |\partial I_D / \partial V_{gs}|_{V_{DS}=const}$). From the comparison of the four measurement sets, it is possible to claim that in devices with the same gate length and channel length, both the ON-OFF ratio and the static gm increase for meandered graphene devices (Fig. 3.37(b,f), (d,h)). As expected, this trend is even more evident in clamped-gate structures (Fig. 3.37(d, h)). Measurements of I_D versus V_{DS} by varying V_{GS} (Fig. 3.37(i-n)) have also been performed. As can be observed, clamped-gate devices present a broader spread in the I_D-V_{DS} curves at in- creasing V_{GS} (Fig. 3.37(b, d)) if compared to single-gate ones (Fig. 3.37(a, c)). Meandered devices also present a larger I_D, for the same bias voltage, (Fig. 3.37(c, d)) than the not meandered ones (Fig. 3.37(a, b)), probably due to the lower contact resistance between

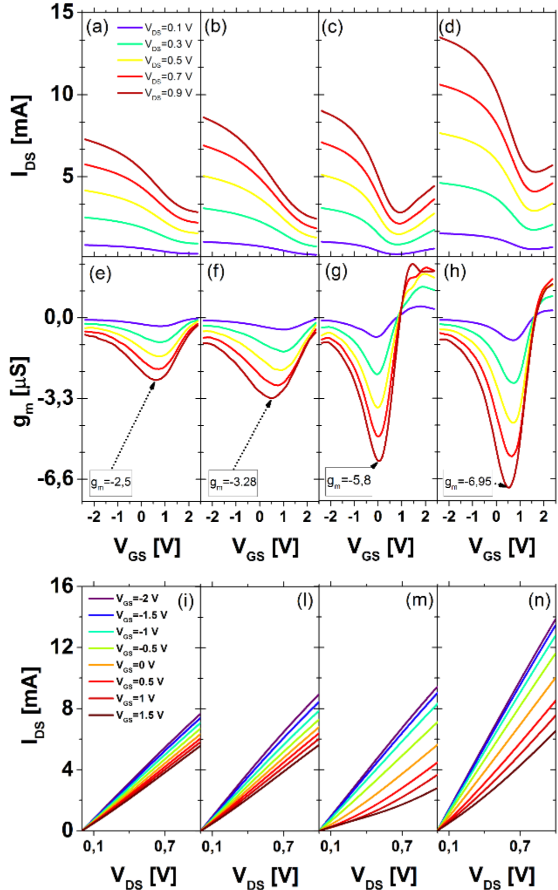


Fig. 3.37: *Graphs of I_D vs V_{GS}, g_m vs V_{GS} as a function of V_{DS} and I_D vs V_{DS} with V_{GS} as a parameter for: : (a, e, i) single-gate device with not meandered graphene source contacts, (b, f, l) clamped-gate device with not meandered graphene source contacts, (c, g, m) single-gate device with meandered graphene source contacts, (d, h, n) clamped-gate device with meandered graphene source contacts*

source and channel. Once verified that devices with meandered graphene exhibit better properties in terms of static g_m, we focused only on the meandered devices for the subsequent RF/microwave characterization and modeling, herein reported. More precisely, once identified the intervals of V_{GS} and V_{DS} with the highest value of gm for each device, scattering parameters have been measured in the 50 MHz - 20 GHz frequency range using the set-up reported in A.2.1. In order to extract the intrinsic transit frequency of the transistor, a standard de-embedding procedure has been applied[125](A.4.1). De-embedded S-parameters, short circuit current gain and maximum available gain have been calculated biasing the transistors at the operating points in which they exhibit the maximum transconductance (i.e., V_{GS}= 2V, V_{DS} = 1.5V for a single gate device; V_{GS} = 1.4V, V_{DS} = 1.5V for the double clamped gate device) and shown in Fig. 3.38. The extensive characterization campaign performed on the various fabricated devices permits us to claim that MOGFETs with clamped-gate exhibit better performances in terms of gain, cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}). In this connection, notice that f_T increased by a factor of 1.22 (from 4.83 GHz to 5.92 GHz) and f_{MAX}, one of the most significant quality indexes of a transistor intended for RF/Microwave use, increased by a factor of 2.19 (from 2.03 GHz to 4.65 GHz) respectively. To more deeply investigate the differences between the fabricated single-gate and clamped-gate GFETs, the small-signal equivalent circuits of the intrinsic devices have been identified using computer-aided techniques to fit measured data. In Fig. 3.39, the equivalent circuit topology adopted for the intrinsic GFET modeling is illustrated. The table reports the equivalent circuit parameter values identified for the same two devices whose S-parameters and gains have been depicted in Fig. 3.38(a-b). It is worth noticing that the equivalent circuit model includes, in addition to the main transconductance (g_m) and output resistance (R_{ds}) parameters,

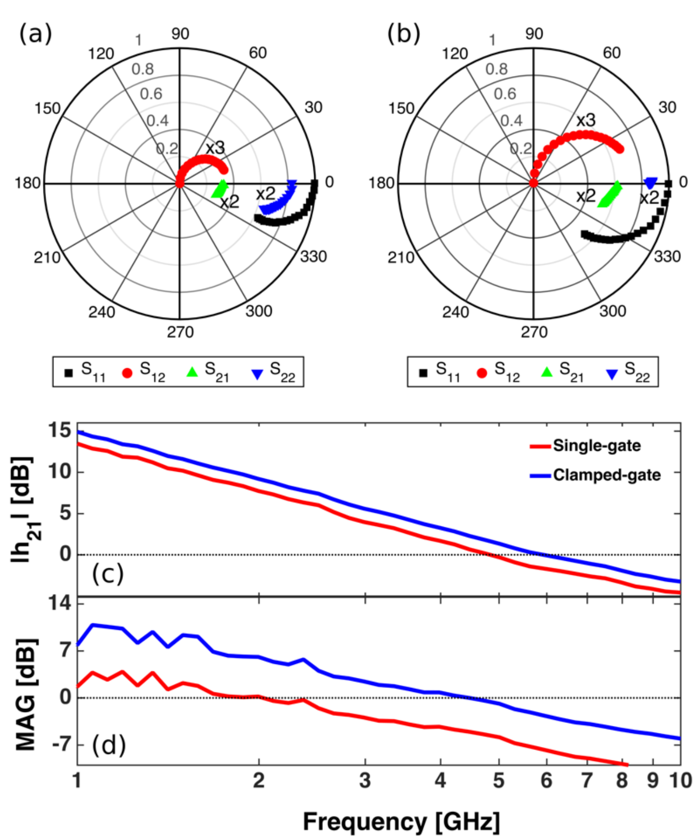
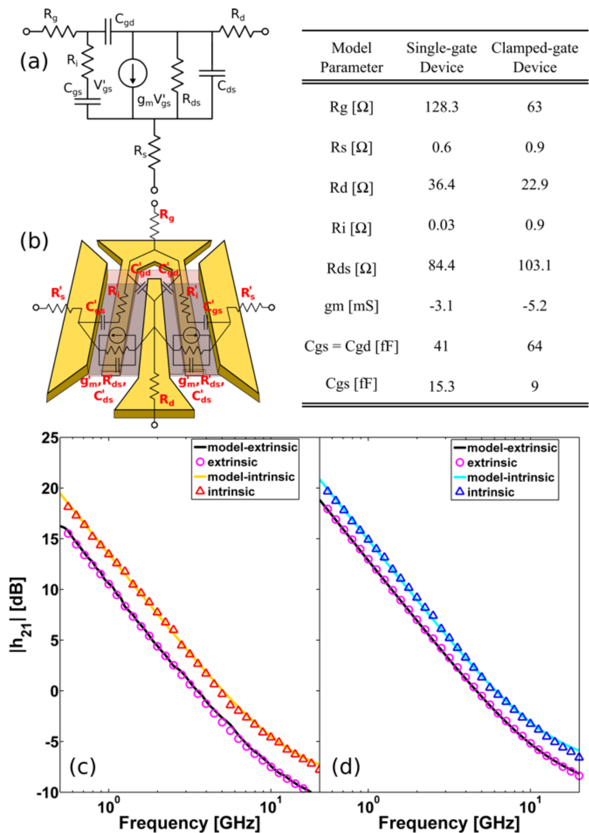


Fig. 3.38: *Polar plot of the S-parameters of single-gate de vice (a) and clamped-gate device (b). The frequency range is from 50 MHz to 20 GHz. Comparison of measured $|h_{21}|_{dB}$, $|MAG|_{dB}$, as a function of frequency for a single-gate device (red curves) and clamped-gate one (blue curves).*

also the parasitic access resistances (gate, R_g, source, R_s , and drain R_d) as well as the coupling capacitances between gate-source (C_{gs}) and gate-drain (C_{dg}). Fig. 3.39(c-d) illustrates the good quality of the fitting achieved. The measured vs simulated values of |h21|dB are compared for both the intrinsic and extrinsic devices of single-gate and clamped-gate types. From the model parameter values reported, it can be observed that the main variation between single-gate and clamped-gate devices is associated to the increase of the transconductance magnitude (from 3.1 to 5.2 mS) and to the decrease of the gate resistance (from 128.3 to 63Ω), as expected by virtue of the improved gating mechanism and of the double metal-layer structure of the clamped-gate configuration. The former result is consistent also with the DC characterization above reported. Since the other circuit parameters exhibit only small variations, the model confirms the improvement in the gain and frequency response expected from the new design and verified by the measurements.



Model Parameter	Single-gate Device	Clamped-gate Device
Rg [Ω]	128.3	63
Rs [Ω]	0.6	0.9
Rd [Ω]	36.4	22.9
Ri [Ω]	0.03	0.9
Rds [Ω]	84.4	103.1
gm [mS]	-3.1	-5.2
Cgs = Cgd [fF]	41	64
Cgs [fF]	15.3	9

Fig. 3.39: *Small-signal equivalent circuits (a, b), Measured and simulated curves of* $|h_{21}|dB$ *for both the intrinsic and extrinsic devices of single-gate (c) and clamped-gate (d) GFETs. The table shows the model parameter values for both single- and clamped-gate devices.*

3.1.10 Mixed-mode operation of hybrid phase change nanophotonic circuits

Reversible ultrafast phase transition and scalability are the main features of phase change materials (PCMs). The ability to store information in their amorphous and crystalline phases could be fundamental in nonvolatile and all-optical memory application. For such reason, in this supplementary work PCM nanowires have been embedded in nanophotonic circuits with the aim to exploit their phase transition when excited by the evanescent field of an optical waveguide.

My contribution to this research activity has been focused on the fabrication of the devices, in particular on the GeTe nanowire transfer. A 330 nm Si_3N_4 optical waveguide on 3300 nm buried SiO_2 layer on top of silicon substrate has been fabricated [126], with the aim to integrate single-crystalline GeTe nanowires which have been synthesized using metal catalyst mediated vapor-liquid-solid (VLS) process [127], [128]. GeTe nanowires have been transferred mechanically onto the fabricated photonic chip using the transfer process schematically depicted in Fig. 3.41(a). Contact printing method has been employed to assemble GeTe nanowires on a bare layer of polydimethylsiloxane (PDMS) [129]. A PDMS stamp has been brought into contact with the sample with deposited GeTe nanowires, and consequently some sparse GeTe nanowires have been transferred onto the surface of the PDMS due to surface adhesion. The PDMS stamp has been affixed to a transfer plate with a hole in the middle, such that the GeTe nanowire can be observed through the hole. With nanowires on the downside, the transfer plate has been placed movably on a 2D-stage under an optical microscope. The prefabricated nanophotonic chip has been fixed on the microscope 1D-stage below the sample. In this way the transfer plate, through its hole the GeTe nanowire, and the chip could be observed via a microscope objective above the 2D-stage. Prior to performing the nanowire transfer, the nanophotonic chip has been covered with PMMA and exposed via EBL to pattern opening windows across waveguide and electrodes. The selected GeTe nanowire has been aligned to the electrode in the window of the PMMA layer, and then the chip has been raised slowly until it touched the GeTe nanowire above. After heating to 120 °C for 30 min, the chip has been lowered down to lift off the PDMS on the transfer plate from the chip. The nanowire remains in contact with the electrodes because of van der Waals adhesion [130]. Subsequently, the chip has been annealed at 150°C for 10 min in order to enhance the contact between GeTe nanowire and electrodes. Finally, the chip has been immersed upside down in the acetone in order to remove the PMMA, as well as the unwanted GeTe nanowires out of the PMMA window. In Fig. 3.41(b) an optical microscope image of the final device is shown. In order to improve the electrical contact between the Au electrodes and GeTe nanowire, additional Pt has been selectively deposited on both ends of the nanowire, as can be seen in Fig. 3.41(c), by using focused ion beam (FIB) deposition.

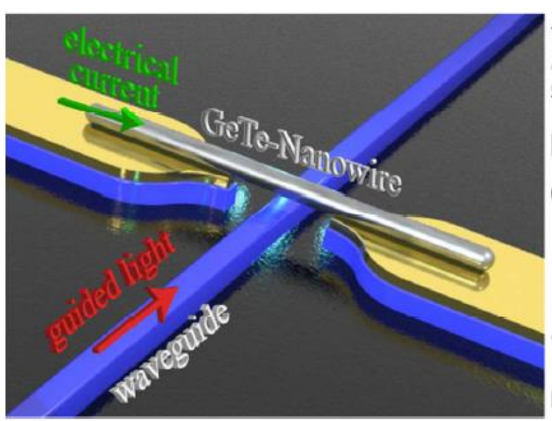


Fig. 3.40: *Sketch of the on-chip mixed-mode device. Source: adopted from* [131].

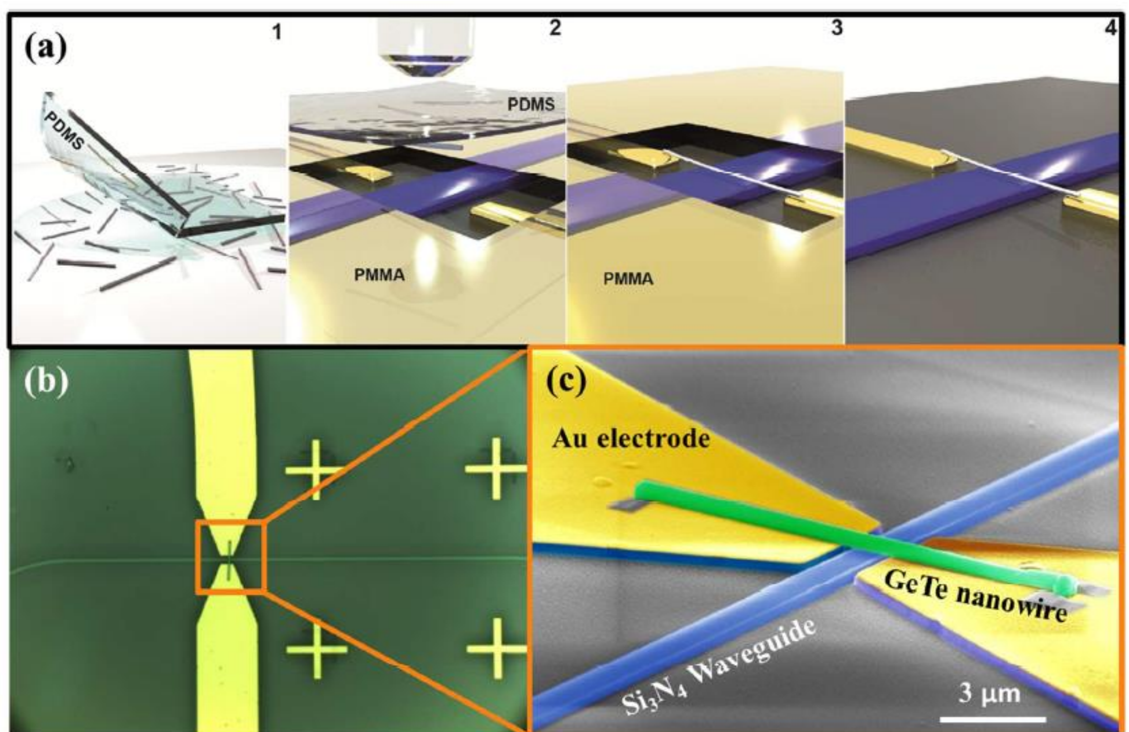


Fig. 3.41: *(a) Schematic of the GeTe nanowire transfer process, (b) Optical microscope image and (c) tilted view false-color SEM image of the device. The GeTe nanowire is in electrical contact with the Au electrodes with the aid of Pt deposition at both ends of the nanowire. Source: adopted from*[131]

4 Conclusions

As conclusion of this PhD thesis, herein are summarized all the main results of the work that has been carried out.

First, in order to investigate on the influence of the device geometry to exploit graphene properties for Microwave application, 24 families of GFETs, fabricated on a single chip and differing for the gate-drain/source distance (Δ) and the gate length (L_g), have been characterized in both DC and RF/microwave regimes. A parametrical and statistical analysis has been performed, and the dependence of the main RF parameters on both Δ and L_g evaluated. This study allowed to demonstrate the existence of an optimal region where the cut-off frequency and the maximum frequency of oscillation are maximized. The obtained results are very interesting since for the first time f_T and f_{MAX} dependence in GFETs of both geometrical parameters Δ and L_g has been evaluated. Moreover, taking into account the importance of the environments (substrate, oxides) in graphene technology, a comparison between aluminum oxide, titanium oxide and hafnium oxide employed as gate dielectrics in GFETs has been performed. Ten identical devices for each oxide material have been fabricated and their microwave response evaluated. It has been found that graphene transistors employing hafnia as the oxide layer show the best performances in terms of both the cut-off frequency and the maximum frequency of oscillation. This confirms that, even for Graphene-based transistors, the choice of hafnia as the gate dielectric allows to obtain the best compromise in terms of the conduction band offset and the κ-factor.

Another important part of my work consists in employing graphene-based phototransistor for telecom applications for IR detection. Due to the importance of the operating point in the photoresponse of the GFETs, optical measurements have been carried out as a function of both the incident laser power and the DC biasing. For the best of our knowledge, for the first time, an in-depth analysis of GFETs IR response in terms of the Signal to Noise Ratio has been accomplished to find the best detector operating point. The best performances have been found at V_{DS} = 0.4 V and a maximum photoresponsivity of ~ 53 μA/W at room temperature has been obtained.

Future activities of my work could consist in realizing a novel generation of GFETs for high frequency application employing different substrate adopting an asymmetrical gate-drain/source spacing structure in order to improve the device performances on the same sapphire substrate.

A. Appendix

A.1 Scattering and admittance parameters

Two-port scattering (S) and admittance (Y) parameters have been used to describe GFETs electrical characteristics in the small-signal regime at microwave frequencies. In particular, the S-parameters have been measured by using Vector Network Analyzers - VNA (see details in A.2 and A.3), and Y-parameters derived from them using mathematical transformations. The latter parameter set has been adopted as helper for both the de-embedding (A.4) and the circuit modeling phases. The main figures of merit used to characterize the high-frequency device gain performances, such as f_{MAX} and f_T, have been also numerically derived from S-parameters.

As well known, for a linear two ports network (the Device Under Test – DUT, as usually indicated in a characterization/measurement framework), the scattering-parameter representation relates incident ($\mathbf{a}_1$ and $\mathbf{a}_2$) reflected ($\mathbf{b}_1$ and $\mathbf{b}_2$) wave vectors (square root of power waves), as depicted in Fig. A.1.

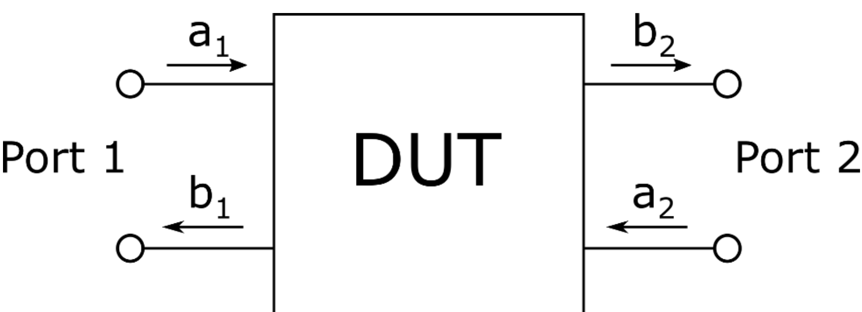


Fig. A.1: *Waves representation of a linear two-port network.*

The corresponding S-parameter matrix [**S**] is given by:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \qquad (A.1)$$

where, $\mathbf{S}_{11}$ and $\mathbf{S}_{22}$ are the input and output voltage reflection coefficients, while $\mathbf{S}_{12}$ and $\mathbf{S}_{21}$ are the reverse voltage and forward voltage gains. It has to be noticed that scattering parameters are defined and measured using "matched" loads, or – more precisely – terminated into a reference load of impedance $\mathbf{Z}_0$, which usually is set as real and equal to 50 Ohm. This fact, not only simplifies the VNA test-set hardware, but also minimizes the risk of oscillations onset during the S-parameters measurement phase. With the help of the modern systematic-errors correction routines, executed by the VNA firmware after a preliminary “calibration” phase, reliable and highly accurate S-parameter characterizations can thus be achieved. This is especially true if appropriate attention is paid, as here done, also to ancillary and practical aspects of the procedure.

Among these, one can evidence the care and the proper positioning and contact pressure/skate of the CPW microwave probes adopted to connect the VNA to the DUT (see Fig. A.2(c)) as well as the due attention to the mechanical and thermal aspects of the measurement (e.g.: limited cable flexure after calibration, adequate warm-up time for instruments, and control of ambient/device temperature, etc.). Once the “raw” (but error-corrected) measurements of DUT scattering parameters have been collected and transferred from VNA to the controlling PC (and the associated [**Y**] matrix calculated/saved “on the fly”), subsequent DUT characterization and diagnostic phases can be carried out numerically via a combination of purposely developed software routines and commercial software, including advanced ECAD tools (e.g., the NI/AWR Design Environment in our case). To convert the S-parameters to Y-parameters, the standard equations have been adopted:

$$\boldsymbol{Y_{11}} = \frac{\boldsymbol{1}}{\boldsymbol{Z_0}} \frac{(\boldsymbol{1} - \boldsymbol{S_{11}})(\boldsymbol{1} + \boldsymbol{S_{22}}) + \boldsymbol{S_{12}S_{21}}}{\boldsymbol{\Delta s}} \qquad (\boldsymbol{A.2})$$

$$\boldsymbol{Y_{12}} = \frac{\boldsymbol{1}}{\boldsymbol{Z_0}} \frac{-\boldsymbol{2S_{12}}}{\boldsymbol{\Delta s}} \qquad (\boldsymbol{A.3})$$

$$\boldsymbol{Y_{21}} = \frac{\boldsymbol{1}}{\boldsymbol{Z_0}} \frac{-\boldsymbol{2S_{21}}}{\boldsymbol{\Delta s}} \qquad (\boldsymbol{A.4})$$

$$\boldsymbol{Y_{22}} = \frac{\boldsymbol{1}}{\boldsymbol{Z_0}} \frac{(\boldsymbol{1} + \boldsymbol{S_{11}})(\boldsymbol{1} - \boldsymbol{S_{22}}) + \boldsymbol{S_{12}S_{21}}}{\boldsymbol{\Delta s}} \qquad (\boldsymbol{A.5})$$

where $\Delta s = (1 + S_{11})(1 + S_{22}) - S_{12}S_{21}$ and $\mathbf{Z}_0$ = 50 Ohm. As already described, the most important figures of merit (FOM) describing the high-frequency performance of a FET are the transit frequency f_T and the maximum oscillation frequency f_{max}:

- f_T is the frequency where the circuit current gain $|h_{21}|$ approximates unity[65];
- f_{max} instead is the frequency where the maximum oscillation power gain G_{MAX} is equal to 1 [65].

A.2 Setup at LEM

Two different workbenches have been setup and used at the Laboratorio di Elettronica delle Microonde (LEM) of the University of Palermo for the DC /RF GFETs characterization and they are herein described.

A.2.1 DC/RF set-up #1

In the first set-up, RF measurements have been performed by using a Cascade Summit 9000 wafer-probe station and a Hewlett-Packard 8510C Vector Automated Network Analyzer (VANA). In particular, scattering parameters measurements have been carried out in the 50 MHz

÷ 20 GHz frequency range. The DC biasing of the devices, as well as their static characterization, has been made through the addition to the setup of two remotely controlled Stimulus-Measure Units (SMU). For each selected test bias point, the GFETs RF characterization has been performed adopting a sinusoidal input signal of appropriately low amplitude, so to guarantee that the device under test (DUT) is working linearly. When a too high signal level is used, in fact, active circuits start to work nonlinearly, whereas with a too small RF drive, the consequent low signal to noise ratio (SNR) impairs the measurement quality. To connect the VANA cables to the pads of the DUT, ACP40 G-S-G coplanar-waveguide (CPW) micro-probes by Cascade have been used (see Fig.A.2c). Gate-source and drain-source voltages are applied by two SMU Keithley 2400. A simplified sketch and a photograph of the implemented workbench are shown in Fig. A.2a and A.2b, respectively. Several software tools have been developed, using the HTBasic programming language (by Transera), for the computer-controlled biasing of the devices and to make proper preliminary measurements, aimed to remove the systematic errors from the test bench (e.g., cable and contact resistances). The main measurements automation software has been organized in various interacting modules, each one implementing different elementary tasks, in order to measure trans-characteristic curves, I-V curves and single point measurements with appropriate timings, error corrections, and so on.

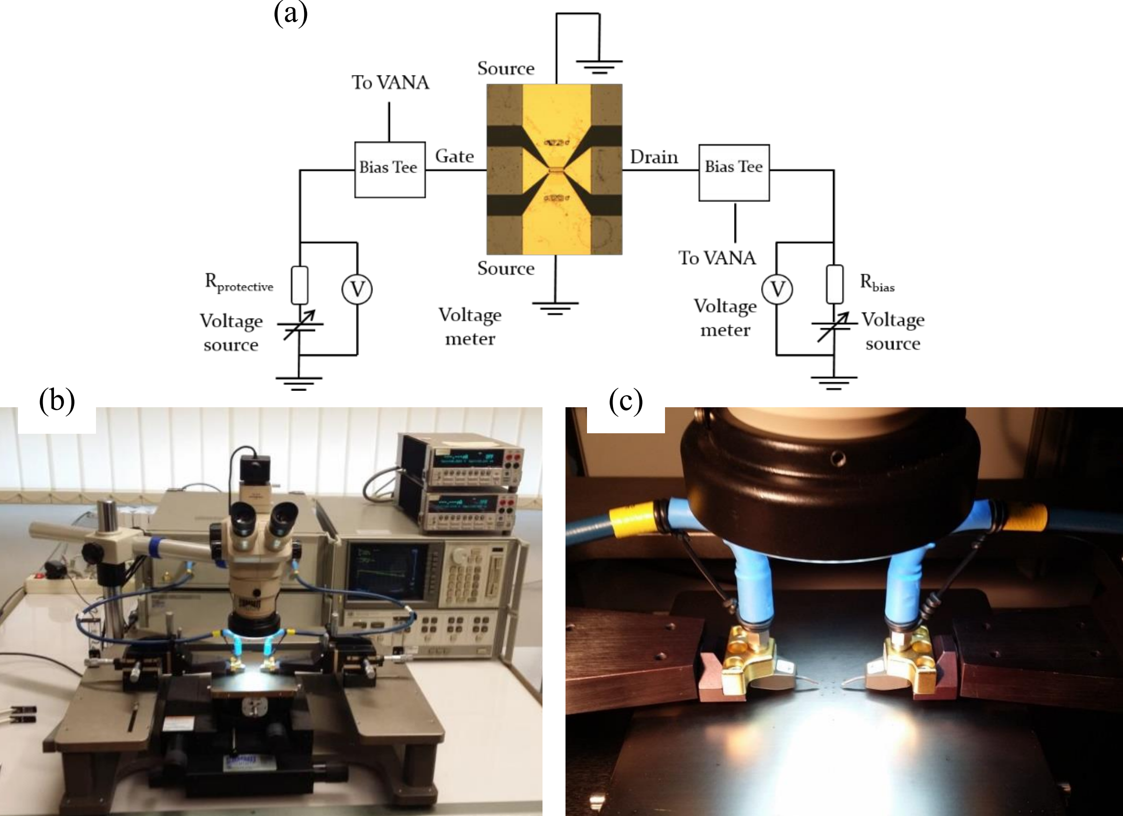


Fig. A.2: *(a) Schematic and (b-c) photographs of the RF/DC set-up 1.0.*

A.2.2 DC/RF set-up #2

In the second setup used for DC/RF characterization at LEM, a Keysight N5232A Precision Vector Network Analyzer (PNA) has been coupled to the Cascade Summit 9000 wafer-probe station, in order to widen the measurement's range toward lower frequencies [300 KHz ÷ 20.003 GHz] and increase accuracy. ACP40 probes have been employed to connect the PNA to the pads of the DUT, making use of high-stability coaxial cables in between by Cascade Microtech. Gate-source and drain-source voltages are applied by two SMU Keithley 2400 and two auxiliary Agilent 34401A DMMs added to the setup. A sketch and a photograph of the developed workbench are shown in Fig. A.3. This bench has been completely automated by several HTBasic software modules used for the biasing of the DUT and to acquire the measurements of the scattering parameters. In particular, exploiting the speed of the modern PNA, it has been possible to program the acquisition software so to perform simultaneously DC and RF/Microwave measurements for each test operating condition (bias point, etc.). In analogy to the operation of the previous bench (A.2.1), a set of auxiliary measurements have been preliminary performed by using other software modules, in order to remove systematic errors. The acquired measured data have been subsequently post-processed by other custom HTBasic software modules to get the global indications on device performances, e.g., identify the bias points corresponding to the maximum transconductance or current gain. This permitted to focus subsequent device-performance analyses on a smaller subset of the very large amount of data collected (thousands of files).

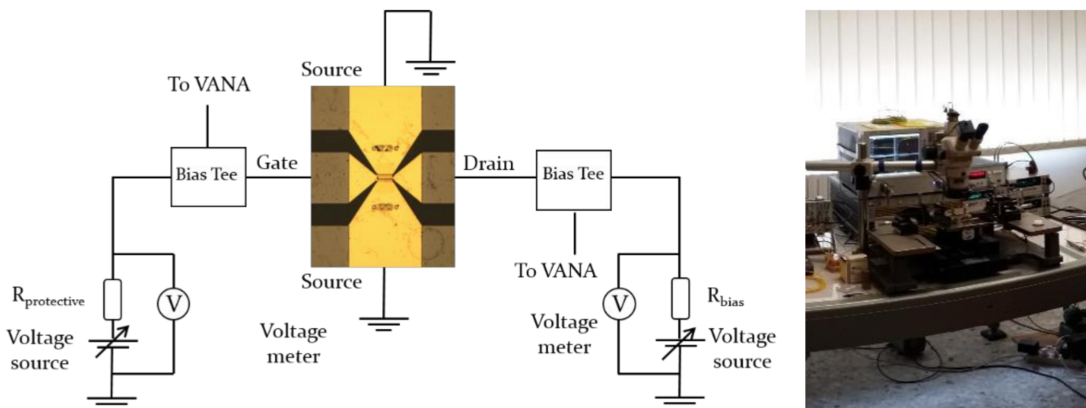


Fig. A.3: *Schematic and photograph of the RF/DC set-up 2.0.*

A.2.3 VANA calibration

Real world VANA-based S-parameters measurements are unavoidably affected by both random and systematic errors. Calibration procedures permit to remove these systematic errors during (online) or after the measurement cycle (offline). The typical error sources causing systematic errors are due to non-ideality of the directional couplers, cable losses and phase-shifts, MW tips and contact imperfections, and so on. Such systematic errors can be represented by an error network (comprising 8, 10 or 12 terms) put in between of the virtual ports of an ideal (errorless) network analyzer [132], [133] for the simplest 8-term error model. Calibration procedure identifies the error networks parameters (terms) by measuring known calibration standards, which allows to obtain the real S-parameters of the DUT by numerical data-processing of the imperfect (raw) measured data. Calibration standards are passive, high-quality (traceable and stable) components. The calibration standards typically used are the following:

- Thru, T: transmission line (typically 50 Ω and zero-length). For on-wafer measurements a true Thru standard does not exist, since the probes cannot be connected directly to each other and thus a short transmission line is used as a Thru standard.
- Line, L: short transmission line (typically 50 Ω), which defines the normalization impedance.
- Delay, D: the same as Line, typically the length of the Delay is 20° - 160° different than Thru.
- Reflect, R: an unknown reflective termination; the reflection coefficient does not need to be known, but needs to be the same in both measurement ports. Usually used in self-calibration methods. Typically, Short or Open termination.
- Open, O: Open circuit; the reflection coefficient needs to be known.
- Short, S: Short circuit; the reflection coefficient needs to be known.
- Match, M: matched load, which defines the normalization impedance.
- Load, L: resistive termination (typically 50 Ω). Thus the same as Match.

The calibration of VNAs is based on error models that include error terms characterized by complex S-parameters values at each calibration frequency. Different error models and calibration methods to define the error network have been studied [131]. In my PhD work an 8-term, Line-Reflect-Reflect-Match (LRRM) calibration has been used [132]. The reference plane is set at the probe tips. In Fig.A.4, micrographs of the Cascade ISS calibration standards are shown, when contacted by the ACP40 coplanar probes.

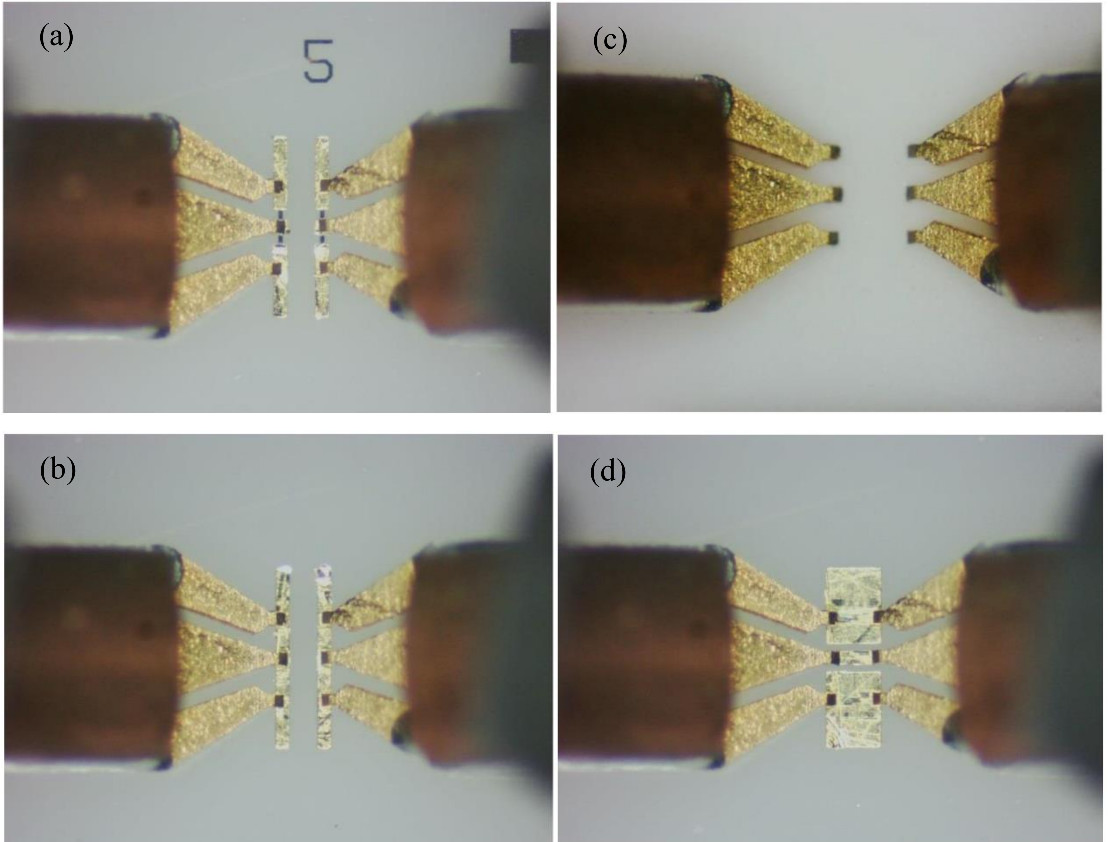


Fig. A.4: *a) Match, b) Open, c) Short, d) Line*

A.2.4 Optical set-ups

Two optical set-ups have been developed to perform the optical characterization of the GFETs under test. The first one has been made for the visible range, while the second focuses more towards telecom applications.

A.2.4.1 Optical set-up 1.0 (for visible wavelength)

A fist set-up has been made to inject the optical signal into the GFETs through a trinocular microscope focusing head, perpendicularly mounted. An amplitude-modulated optical signal in the visible range has been used, whose intensity/modulation can be monitored via beam-splitting for calibration/reference purposes. More precisely, a 405nm PHR-805T (Blue Ray Laser Diode) was used as source, and a FPD510-FV broadband photodetector (by Thorlabs/MenloSystems) was used to characterize the resulting optical carrier and its AM modulation. A lock-in amplifier has been employed (SR830 DSP Lock-In Amplifier by Stanford Research Systems) to read out the AM electrical signal. A digital camera has been applied at one ocular of the microscope, in

order to visually track the fine adjustment of the position of the beam on the devices. This spot centering is possible since provision was made to move the laser diode within its ("ad-hoc" built) mount/heatsink, by means of an incorporated XY micro-metric stage, as illustrated in Fig. A.5.

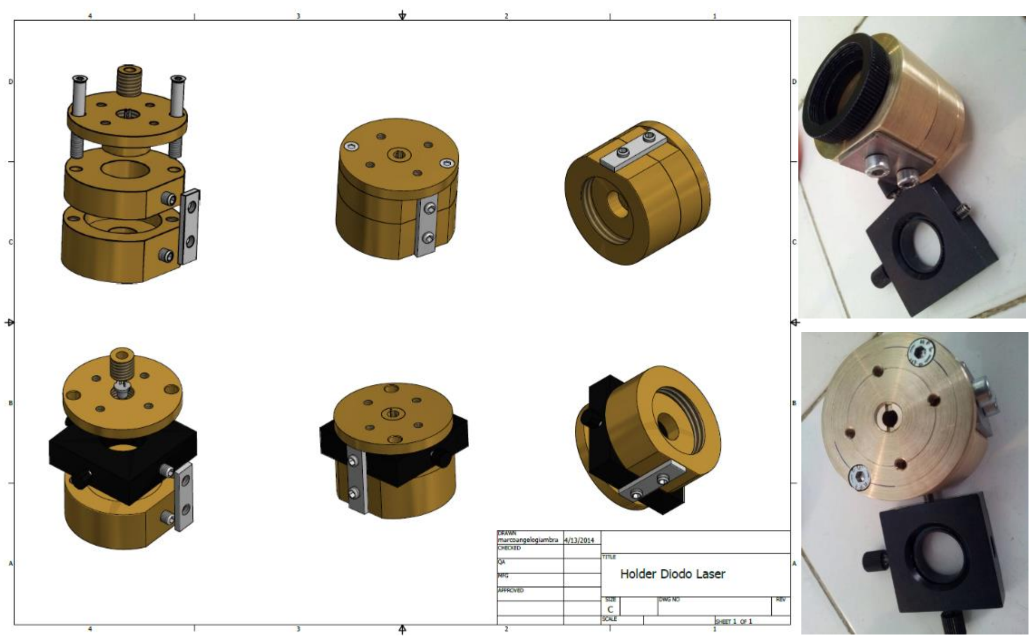


Fig. A.5: *Design of the ad-hoc laser sample holder*

Additionally, custom software was written to permit an automatic characterization of the optical response. A simplified sketch of the optical work bench assembly, the laser diode datasheet, and a photo of the overall measurement setup are reported in Fig. A.6.

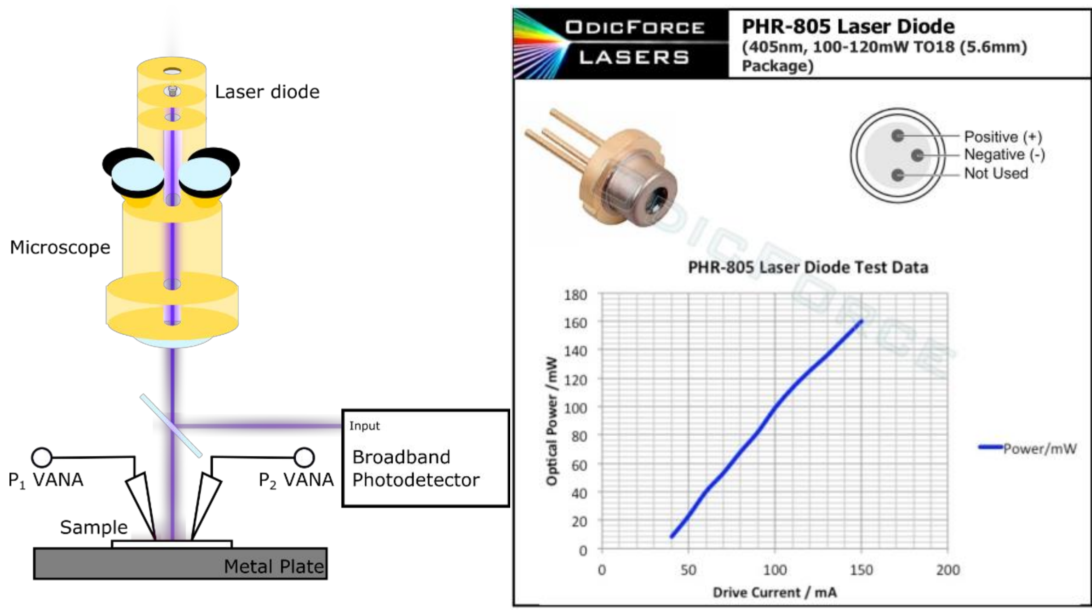


Fig. A.6: Sketch of the optical set-up 1.0, blue laser datasheet, and photograph of the optical set-up

A characterization of the laser beam out of the optical microscope has been preliminarily performed (Fig. A.7). The beam spot was measured at the microscope's focal distance, as function of the operating current of the laser and the magnification (zoom setting) of the optical microscope. A knife-edges technique by using the "Beam'R2 XY Scanning Slit System" has been employed. The measured spots size are reported in Table A.1.

Mgnification $[X]$	Beam Spot $[um^2]$
1.5	438746.88
2	212487
2.5	97933
3	46860
4	9139.35
5	784
6.3	61.56

Table A.1: *Laser spot sizes at different microscope magnifications*

A minimum size beam spot of $61.56\mu m^2$ has been reached using the maximum magnification of the microscope, but, since a constant optical power density over all area of the graphene channel is the goal, spot measurement the same distance from the microscope lens have been performed.

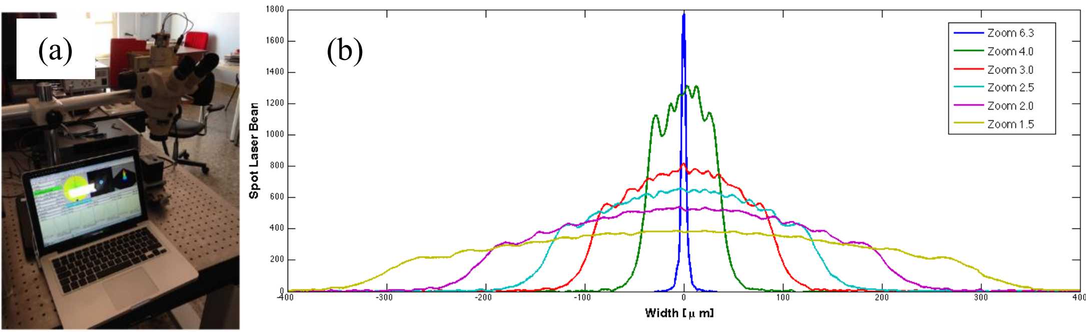


Fig. A.7: (a) Set-up for knife-edges technique used for laser beam characterization, (b) section of different laser beam spot by changing the microscope magnification.

Taking into account these measurements, a 3X microscope magnification has been selected, obtaining a quasi-constant laser power over all the GFET active area.

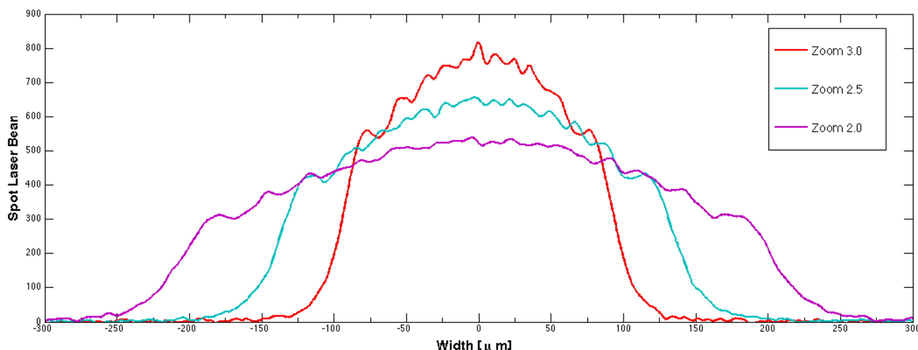


Fig. A.8: *Section of different laser beam spot by changing the zoom of the optical microscope*

Additionally, a characterization of the broadband photodetector has been made. To this purpose, the fabricated sample holder has been mounted on an optical table. Preliminarily, in order to align the laser source on the optical table, a He-Ne laser has been used. DC and chopped measurements have then been performed. These measurements have been made to verify the responsivity of the photodetector at different loads ($V_{OUT}/1M\Omega$ vs P_{opt} - $V_{OUT}/50\Omega$ vs P_{opt}). The source beam has been previously conditioned and focused on the active area of the photodetector ($400\mu m \times 400\mu m$).

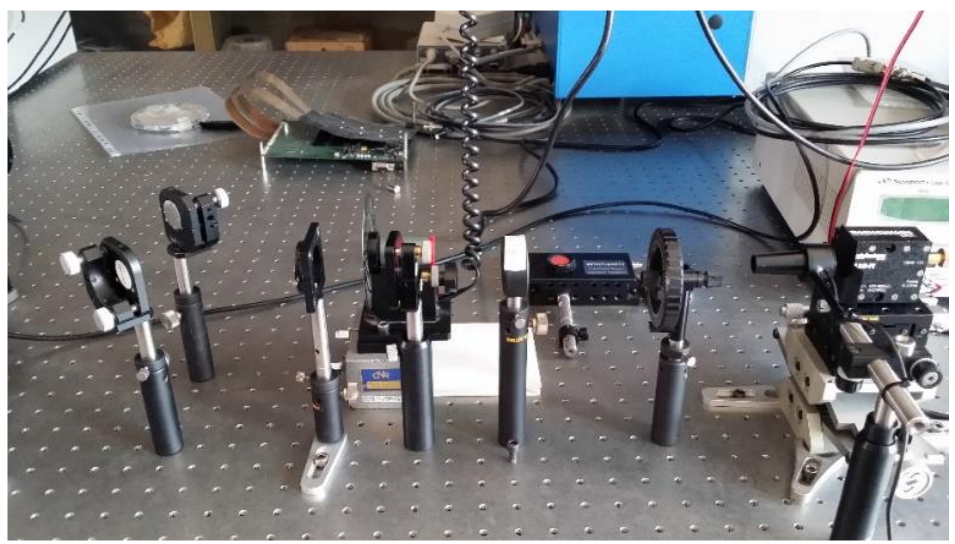


Fig. A.9: *He-Ne laser, mirrors, lenses, power meter, broadband photodetector, chopper for DC, chopped measurements*

A.2.4.2 Optical set-up 2.0 (for infrared wavelengths)

With the second test-bench photoelectrical characterization of the GFETs has been performed (at room temperature) using a 1.55 μm erbium fiber laser (*IPG Photonics ELT-1-CL-SF-LP*) with the

output beam chopped at 667 Hz and coupled into a single mode optical fiber through a microscope objective (*Edmund DIN 20*). The electrical signal (output voltage of the GFETs mounted in a common-source amplifier configuration) was measured using a lock-in amplifier (*Stanford Research Systems SR510*) synchronized to the chopper frequency. A sketch of the experimental set-up is depicted in Fig. A.10(a). An auxiliary visible laser (405 nm laser diode) has been employed for alignment purpose, while two DC Source-Meter Units (SMUs) have been used for the DC device biasing. The spot size of the IR beam at the output face of the single mode fiber has been analytically evaluated (w = 5.3 µm, Fig. A.10(b))[134]. Then, the laser spot area on the sample (0.065 mm^2) has been calculated by simulating the free space propagation of the beam exiting the fiber for a distance of ~ 1.5 mm (i.e. the distance between the fiber end and the sample) and irradiating the 40-μm^2 graphene active area (Fig. A.10(b)) A photo of the set-up employed is depicted in Fig. A.10(c).

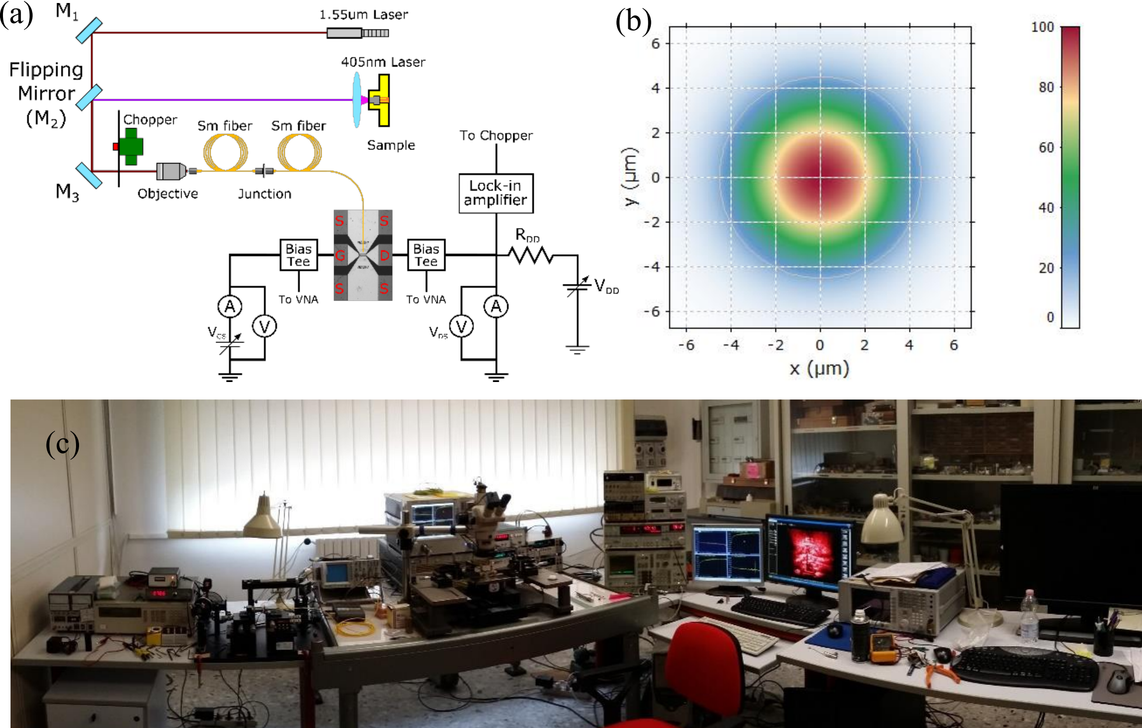


Fig. A.10: *a) Sketch of the experimental setup for optical measurements, b) Intensity plot of the simulated beam, after exiting the fiber, c) photo of the workbench used for DC/optical measurements.*

A.3 Set up at KIT

A number of initial (DC/RF) verification measurements has been made, soon after GFETs construction, directly at the Laboratory of the Institute of Nanotechnology (INT) of the Karlsruher Institut für Technologie (KIT). In particular, a Rhode & Schwarz ZVA40 Vector Network

Analyzer with |Z|PROBE probes in the range [10 MHz – 40 GHz]. BTN- 0040 ultra-broadband bias tees from Marki Microwave have been used. Gate-source and drain-source voltages are applied by a Yokogawa 7651 programmable DC voltage source. DC measurements have been performed by using Agilent 34410A 6^{1}/2 digit multimeters. This setup is illustrated in Fig. A.11.

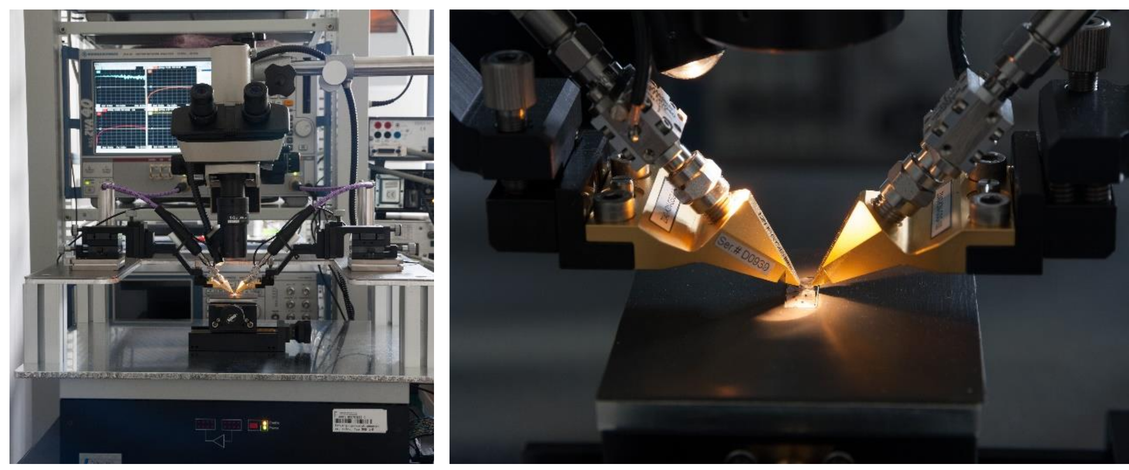


Fig. A.11: P*robe station with RF probes attached to the VNA used at the KIT*

A.4 De-embedding techniques

To be able to measure and characterize the intrinsic properties of the fabricated graphene transistors, two correction procedures have to be applied to the VNA raw measurements, correcting for external parasitic effects originating from the cables and coplanar probes, outside the chip, and the launching structures inside the individual devices. The first procedure is the VNA calibration which shifts the reference planes to the tips of the probes and correct for systematic errors (A.2.3). However, RF measurements after proper calibration still include parasitic effects of the contacting pads and the on-chip tapered CPW lines connecting the probes to the intrinsic GFET. To correct for and extract these parasitic effects, it is a common practice to use the so called "de-embedding" procedure. De-embedding procedure at microwave frequencies is an important and critical step, especially in a situation such as this one, in which a certified on-chip set of standards is not available for a direct device plane calibration. For this reason, two complementary de-embedding procedures have been investigated and applied.

A.4.1 Y-parameters based de-embedding approach

Historically, zero bias has been used to extract the series parasitic elements from transistors thanks to the simplicity of the small signal equivalent circuit [135]. In order to improve the precision of the results of the de-embedding technique, a method has been proposed [125] which consists in the measurements of the S-parameters of the DUT and its open structure (device composed by the pads and the interconnection lines) (Fig. A.12). This approximation method corrects the data only form the parallel parasitics, assuming the series parasitics negligible [125]. By using the conversion from S-parameters to Y-parameters (A.1), it is possible to calculate the approximated de-embedded Y-parameters of transistor under test by following the equation:

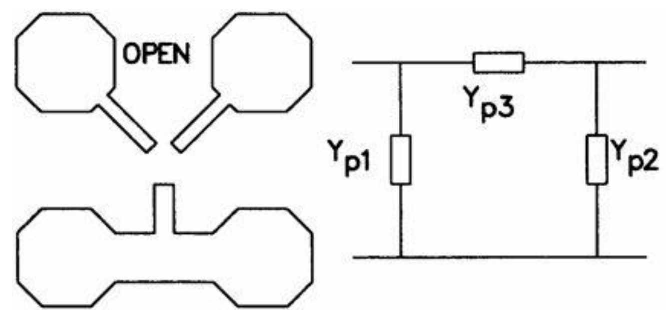


Fig. A.12: *Open pattern on wafer in order to determinate parallel parasitics for the de-embedding procedure. Source: adopted from* [125].

$$\boldsymbol{Y_{transistor-simple} = Y_{DUT} - Y_{Open}} \qquad (\boldsymbol{A}.1)$$

However, this approximation cannot be sufficient in novel on-chip fabricated devices since the series parasitics could be larger [125]. For such reason, an upgrade of the method has to be taken into account in order to determine losses and phase rotation in the interconnect lines. For such reason, short pattern has to be included in the de-embedding process [125]. In order to do it, first, all the parallel parasitics, associated to the open pattern, have to be removed from the short pattern. A simpler subtraction of the Y-parameters between short and open has to be performed:

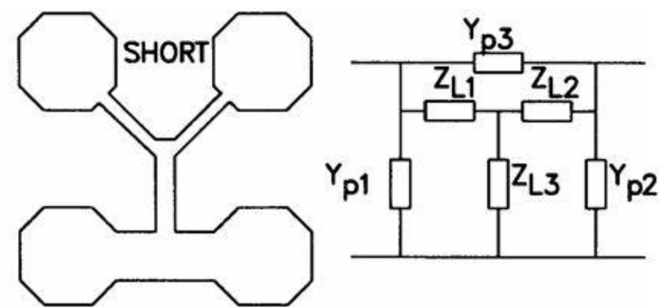


Fig. A.13: *Open and short pattern on wafer in order to determinate parallel and series parasitics. Source: adopted from* [125].

$$\boldsymbol{Y_{series\,parasitics} = Y_{short} - Y_{Open}} \qquad (\boldsymbol{A.7})$$

Then, in order to extrapolate the Y-parameters of the DUT after the “two steps” de-embedding procedure, $Y_{series\ parasitics}$ matrix (A.7) has to be subtracted to the $Y_{transistor\text{-}simple}$ matrix obtained by (A.6):

$$\boldsymbol{Y^{-1}_{transistor} = Y^{-1}_{transistor-simple} - Y^{-1}_{series\,parasitics}} \qquad (\boldsymbol{A.8})$$

$$Y_{transistor} = \left(\left(Y_{DUT} - Y_{Open}\right)^{-1} - \left(Y_{short} - Y_{Open}\right)^{-1}\right)^{-1} \qquad (A.9)$$

Practically, in order to perform the de-embedding procedures on the fabricated devices, test-devs (Short-open-thru patterns) have been fabricated on the same chip of the transistors by using the same fabrication steps (exposed masks, thickness of the metals). The small signal model used to extract the GFET parameters is depicted in Fig. A.14.

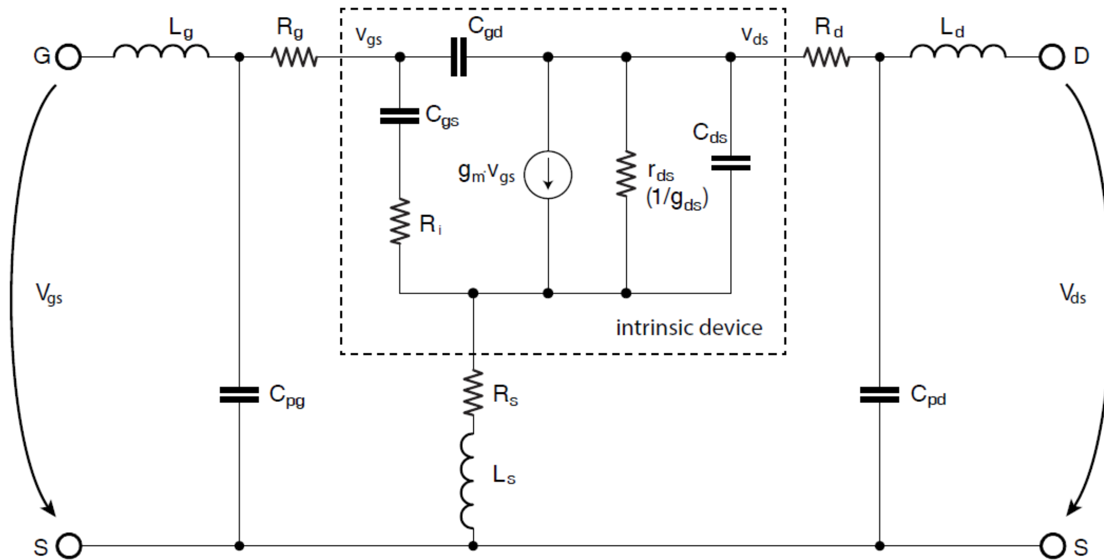


Fig. A.14: *Small-signal equivalent circuit of the GFETs used for the extraction of GFETs parameters*

A.4.2 Electromagnetic De-embedding

The aim is to make an Electro-Magnetic (EM) simulation of the launchers which are used to connect the probe tips to the intrinsic device, directly calculating their 2-port scattering parameters. Such matrices can be thus directly adopted for the de-embedding, according to the following scheme:

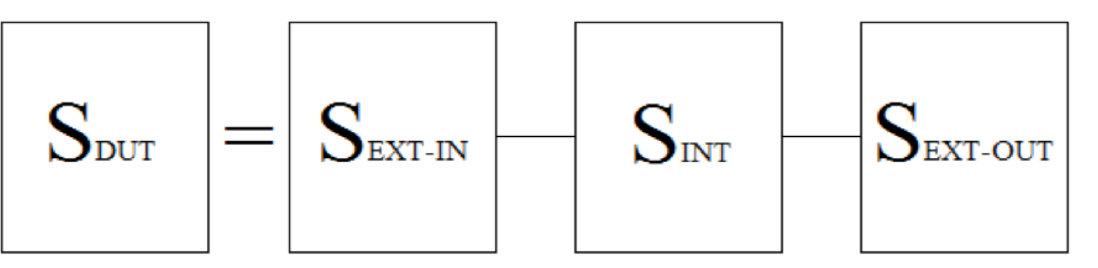


Fig. A.15: *DUT schematic in terms of scattering parameters*

The blocks S_{EXT-IN} and $S_{EXT-OUT}$ represent the effects introduced by IN/OUT extrinsic structures, while S_{INT} is the intrinsic device, all expressed in terms of their EM-simulated S-parameters. Notice that, in this case, there is not a predetermined equivalent circuit for the extrinsic structures. By knowing the measured raw data of the overall device (S_{DUT}), through a proper manipulation of transfer parameters (T) it is possible to obtain the following:

$$[\boldsymbol{T_{DUT}}] = [\boldsymbol{T_{EXT_INT}}][\boldsymbol{T_{INT}}][\boldsymbol{T_{EXT_OUT}}] \qquad (\boldsymbol{A}.2)$$

$$[\boldsymbol{T_{INT}}] = [\boldsymbol{T_{EXT_INT}}]^{-1}[\boldsymbol{T_{DUT}}][\boldsymbol{T_{EXT_OUT}}]^{-1} \qquad (\boldsymbol{A}.3)$$

One can, therefore, easily determine the parameters of the intrinsic device (S_{INT}). Open-Short-Thru structures available on the chips are not a sufficient set for complete calibration (i.e., a closed form correction of the measurements). However, they are useful to verify the de-embedding procedure correctness, taking also into account that the probe-plane ISS calibration kit has different substrate material as well as a different gold thickness, which introduces (small) variations in the contact resistance and EM environment. To perform the 3D-EM simulation of the launching structures the Analyst module of NI-AWR Design Environment has been used. A comparison with the fabricated/measured passive devices has been done in order to experimentally validate the simulations performed, thus realizing a reliable and robust technique for the de-embedding procedure for all the devices under study.

A.4.2.1 Experimental de-embedding (M4 devices)

In order to achieve meaningful results from the comparison between the measurements on these verification devices with associated electromagnetic simulation, extreme care has been taken in their design and fabrication process. For the launching structures, only one step has been used in writing the layout on the PMMA, so that only one step to evaporate them has been involved, thus avoiding the presence of metal overlaps. In the following, a comparison between EM simulations and measurements of the fabricated OPEN, SHORT and THRU structures is reported:

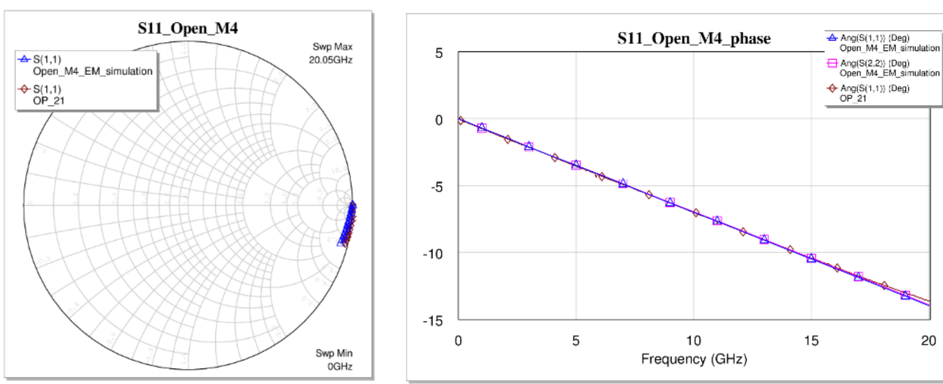


Fig. A.16: *Results of the comparison between measured and EM simulations on open device*

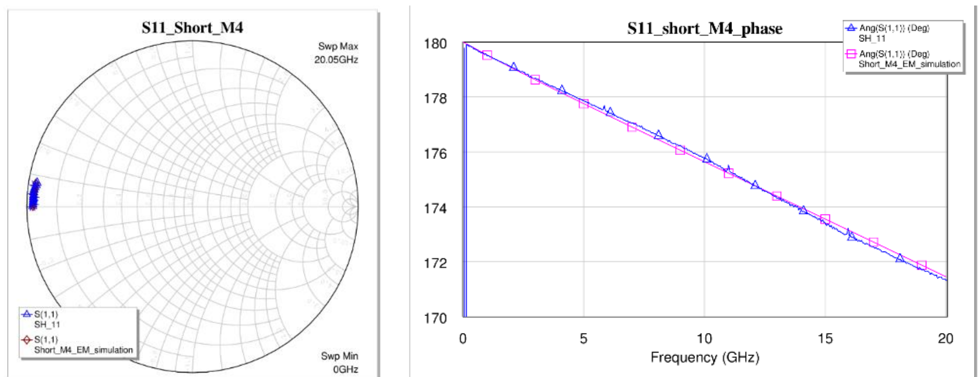


Fig. A.17: *Results of the comparison between measured and EM simulations on short device*

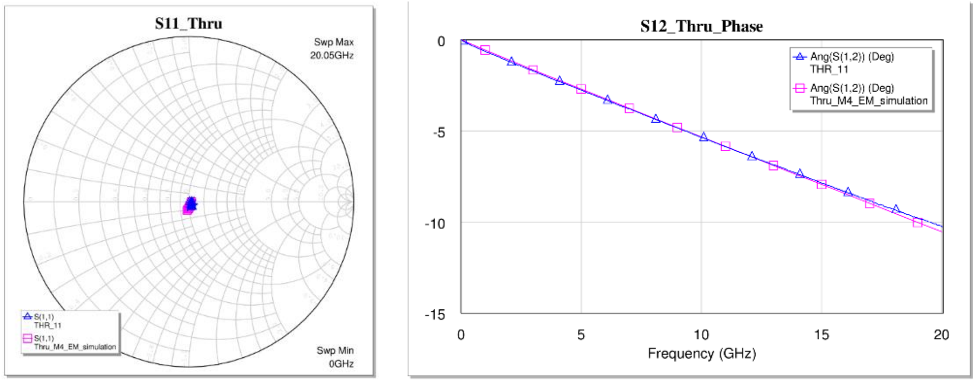


Fig. A.18: *Results of the comparison between measured and EM simulations on thru device*

To get the above seen good fit of test structure S-parameters it has been necessary to identify accurately the substrate parameters, such as ε_r and $\tan\delta$, and also the exact position of the EM ports on top of the pads rapresenting the tip contact point. This goal has been achieved through a multi-measurement approach based on the supplementary passive devices appositely fabricated (e.g., microring resonators on the same sapphire substrate).

After comparing the results between the EM simulation and the measurements on the passive test structures, the simulation of the launcher alone, with the proper position of the EM ports above

identified, has been performed. In particular, simulations have been carried out on the cut geometry (tapered CPW lines only) shown in Fig. A.19:

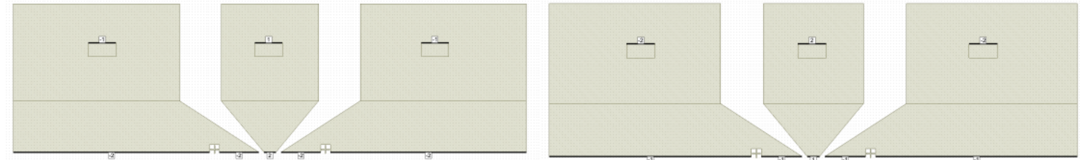


Fig. A.19: *In/Out Launchers in order to obtain the scattering parameters for the de-embedding procedure*

The obtained S-parameters of the launchers, after a further check on the implemented OPEN-SHORT-THRU structures, have been used to extract the S-parameters of the intrinsic device alone simply "subtracting" them from the measured overall device scattering parameters, following the de-embedding procedure described in paragraph A.4.2. In the following images (Fig. A.20 - Fig. A.21) the results of such de-embedding applied, as a check, to the OPEN-SHORT dummy structures are shown.

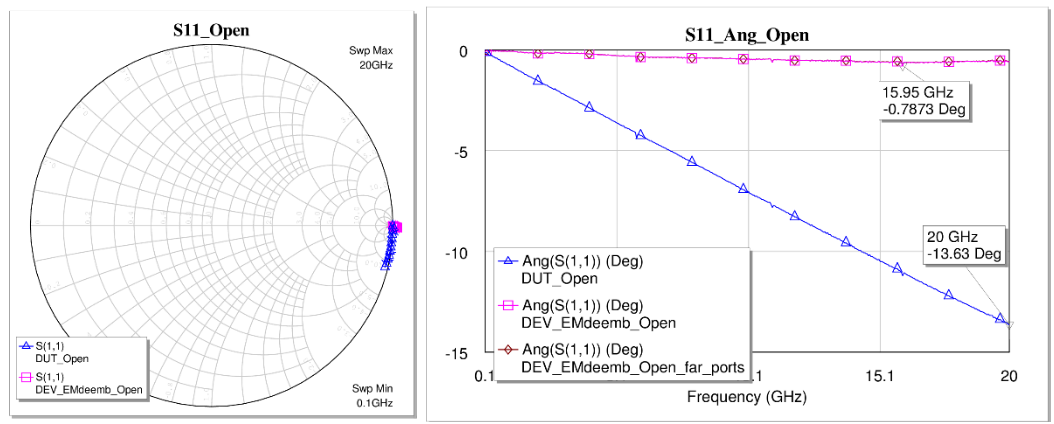


Fig. A.20: *Comparison between S_{11} Raw e de-embedded of Open test-Dev*

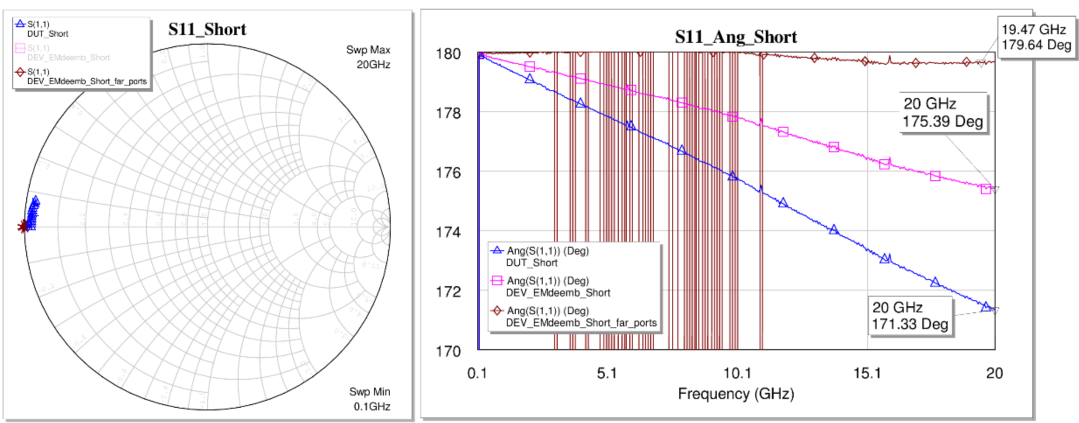


Fig. A.21: *comparison between S_{11} Raw e de-embedded of the Short test-Dev*

As it can be seen, it has been possible to correct the raw data, by achieving a magnitude of the S_{11} close to 1 for the OPEN structure and a phase shift close to 0, starting from a phase shift equal to -13.63 @ 20GHz for the raw data. Concerning the SHORT structure, it has been possible to obtain a phase shift of the S_{11} close to 180° and at the same time a magnitude close to 1, as expected from a short circuit, even it is not an ideal one.

On the basis of the above experimentation, for the de-embedding of the active devices, both Y-parameters and electromagnetic based approaches have been used, obtaining analogous results. The first one has been subsequently adopted when the imperfection induced by the technological steps, introduced inordinate parasitics (losses) not modeled in the electromagnetic approach.

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B: List of publications

B.1 Journal papers

1. Y. Lu, M. Stegmaier, P. Nukala, M. A. Giambra, S. Ferrari, A. Busacca, W. H. P. Pernice, and Ritesh Agarwal, “**Mixed-mode operation of hybrid phase-change nanophotonic circuits**”, Nano Letters Just Accepted Manuscript DOI: 10.1021/acs.nanolett.6b03688

B.2 Conference papers

- M. A. Giambra, L. Zeiss, A. Benfante, S. Stivala, E. Calandra, A. Busacca W. H. P. Pernice, R. Danneau, "**Radiofrequency performances of different Graphene Field Effect Transistors geometries**", 7th International conference on advanced nanomaterials ANM2016", 25 - 27 July 2016, Aveiro, Portugal;
- M. A. Giambra, C. Benz, F. Wu, M.H. Jang, J.-H. Ahn, S. Stivala, E. Calandra, A. Busacca, W.H.P. Pernice, and R. Danneau, "**Performances of double-clamped gate Graphene Field Effect Transistor (GFETs)**", GE Annual Meeting 2016", 22 - 24 June 2016, Brescia, Italy;
- M. A. Giambra, A. Benfante, S. Stivala, E. Calandra, A. Busacca W. H. P. Pernice, R. Danneau, "**Photocurrent generation in Graphene Field Effect Transistors (GFETs)**", GE Annual Meeting 2016", 22 - 24 June 2016, Brescia, Italy;
- 2016 M. A. Giambra, L. Zeiss, A. Benfante, S. Stivala, E. Calandra, A. Busacca W. H. P. Pernice, R. Danneau, "**Impact of GFETs geometries on RF performances**", GE Annual Meeting 2016", 22 - 24 June 2016, Brescia, Italy;
- 2016 M. A. Giambra, L. Zeiss, A. Benfante, E. Calandra, S. Stivala, A. Busacca, W. H. P. Pernice, R. Danneau, "**Microwave parameters dependence on Graphene Field Effect Transistors (GFETs) dimensions**", FOTONICA2016, 6 - 8 June 2016, Roma, Italy;
- M. A. Giambra, A. Benfante, S. Stivala, E. Calandra, A. Busacca W. H. P. Pernice, R. Danneau, "**Photoelectrical response of Graphene Field Effect Transistors (GFETs)**", 6th Edition of the largest European Conference & Exhibition in graphene and 2D Material GRAPHENE2016", 19-22 April 2016, Genova, Italy;
- 2015 M. A. Giambra, S. Marletta, E. Calandra, S. Stivala, A. C. Cino, A. Busacca, C. Benz, W. H. P. Pernice, R. Danneau, "**Fabrication and characterization of graphene field effect transistors (GFET)**", GE 2015 Annual meeting, 24 - 26 June 2015, Siena, Italy;
- M. A. Giambra, S. Stivala, A. C. Cino, A. Busacca, N. Walter, J. Winter, U. Bog, M. Hirtz, F. Schramm, R. Du, M. Ruben, W.H.P. Pernice, R. Danneau, H. Jang, J- H. Ahn, "**Fabrication of graphene ruthenium-complex heterostructures**", GE 2015 Annual meeting, 24 - 26 June 2015, Siena, Italy;
- M. A. Giambra, A. Busacca, S. Stivala, A. Cino, N. Walter, J. Winter, U. Bog, M. Hirtz, F. Schramm, R. Du, M. Ruben, W.H.P. Pernice, R. Danneau, H. Jang, J.H. Ahn, "**Photoresponse of Graphene Ruthenium-Complex Heterostructures**", FOTONICA2015, 6 - 8 May 2015, Torino, Italy, ISBN: 978-1-78561-068-4;

- M. A. Giambra, A. Busacca, S. Stivala, C. Benz, N. Gruhler,W. H. P. Pernice, R. Danneau, "**Fabrication of Graphene Field Effect Transistors (GFET) possessing a photoelectrical response**", GE 2014, 16 - 20 June 2014, Cagliari, Italy, ISBN: 978-88-905519-2-5;
- M. A. Giambra, A. Busacca, S. Stivala, C. Benz, N. Gruhler,W. H. P. Pernice, R. Danneau, "**Fabrication of Graphene Field Effect Transistors (GFET) possessing a photoelectrical response**", Fotonica 2014, 12 - 14 May 2014, Napoli, Italy, ISBN 9788887237191;
- M. A. Giambra, A. Busacca, S. Stivala, C. Benz, W. H. P. Pernice, R. Danneau, "**Fabrication of Graphene Field Effect Transistors (GFET) possessing a photoelectrical response**", Fotonica 2014, 12 - 14 May 2014, Napoli, Italy, ISBN 9788887237191;