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Performance Comparison and Characterization of IPMSM Drives Fed by Symmetrical and Asymmetrical Cascaded H-Bridge Inverters

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Abstract: This paper presents a comparative analysis of interior permanent magnet synchronous motor (IPMSM) drives powered by symmetrical and asymmetrical cascaded H-bridge multilevel inverters. The asymmetric topology operates using multiple DC sources with different voltage values, generating a voltage waveform with more output voltage levels than its traditional counterpart, all while maintaining the same hardware configuration. The main goal is to demonstrate that asymmetrical multilevel inverters are a promising option for improving the performance of electric drives while maintaining cost-efficiency and reliability. The proposed comparison is conducted through simulations in the MATLAB/Simulink R2024a environment, which allows an in-depth analysis of the dynamic performance of the electric drive. Additionally, the variation of the DC link input power of each H-bridge and the Total Harmonic Distortion (THD) of the voltage and current of the output of the converters were studied for different operating conditions in both cases. The obtained results were confirmed through real-time validation, demonstrating the applicability of electric drives powered by asymmetric converters and the advantages, in terms of efficiency, harmonic content and dynamic performance, in certain conditions of operation in terms of speed and applied load.

Keywords: multilevel power converter; modulation techniques; interior permanent magnet synchronous motor; asymmetrical cascaded H-bridge multilevel inverter; THD; power analysis

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1. Introduction

Over the past few decades, environmental concerns have driven significant changes in various industrial sectors, especially in the production, management, and utilization of electrical energy. Consequently, there is a growing interest among the scientific and political communities in addressing environmental issues, with a specific focus on the development of full-electric transportation and the increased use of renewable energy sources for power generation.

Multilevel inverters (MLIs) can play a pivotal role in enhancing the electrification of transportation and enabling the integration of renewable energy into the electrical grid [1]. Among the various MLI topologies documented in the literature [2], the cascaded H-bridge multilevel inverter (CHBMLI) is widely adopted due to its modularity and fault-tolerant capability. Hence, the CHBMLI offers a flexible solution to increase voltage levels by adding H-bridge modules [3]. However, it requires separate DC sources and is only suitable for applications where such sources are readily available, such as PV systems [4], hybrid energy storage systems [5–8], and automotive systems [9]. The CHBMLI is particularly well-suited for grid-connected applications to regulate voltage as a STATCOM [10].

Moreover, MLIs represent a valuable option in electrical drive applications since the electric motor can be driven with voltages with lower harmonic content, consequently

reducing torque ripple, noise, and vibrations [11–14]. In this area of interest, permanent magnet synchronous motors (PMSM) have gained significant attention over the past decades due to several advantages when compared with traditional induction motors. In fact, higher torque density, compactness, efficiency, power factor, and power/current ratios can be achieved by PMSM drives concerning their induction motor counterparts. Several studies also present such a type of electrical drive, regarding the employed control strategy. For instance, the electrical drive proposed in [15] consists of a PMSM powered by an inverter and using direct torque control, delivering excellent dynamic performance, as the applied voltages, the generated torque, and flux are characterized by reduced harmonic distortion. In [16], the impact of an innovative selective harmonic mitigation algorithm is evaluated for a PMSM drive with a CHBMLI. The authors demonstrate that using this algorithm increases the efficiency of the electrical drive. However, it is worth noting that the use of traditional pulse with modulation strategies has improved performance in terms of torque ripple. In [17], a novel space vector pulse width modulation (SVPWM) is proposed for a motor drive system fed by CHBMLI, reducing the switching losses.

On the other hand, the high costs associated with MLIs are due to the large number of required components [18]. Several studies propose innovative MLI topologies to enhance efficiency and generate a greater number of output voltage levels while minimizing the number of required components [1]. A promising approach involves the use of an asymmetric multilevel inverter (AMLI), which allows for a reduction in the number of power components. Therefore, further advantages can be obtained by adopting asymmetrical multilevel power converters in interior permanent magnet synchronous motor (IPMSM) drives. Compared to traditional inverters, MLIs can generate voltage waveforms with a higher number of levels, allowing for a more precise approximation of the ideal sinusoidal trend. Additionally, MLIs overcome the operational limitations of conventional inverters, offering several advantages, such as lower harmonic content in the output voltages, reduced voltage stress on power components in terms of variability in time of the voltage applied to the power components, and decreased electromagnetic interferences [1,19].

AMLI structures are created by employing different voltage amplitudes across the DC-link capacitors. This approach enables an increase in voltage levels while maintaining the same hardware configuration, compared to symmetric approaches, thereby reducing overall costs. Many researchers have proposed innovative asymmetric topologies. For example, in [20], the authors described the operation of the proposed innovative MLI structure capable of generating an output voltage with 13 levels in a symmetric configuration; whereas, in the asymmetric configuration, it can produce an output voltage waveform with 17 levels, achieving a THD of 3% for the 17 levels and an efficiency of 97%. The novel K-type AMLI presented in [21] achieves the highest experimental efficiency of 96.74%, with a THD of the output voltage without filters at 5.3%. Boora et al. described the topology of modular inverters. These converters consist of multiple cascade-connected cells, generating 57 voltage levels with a voltage THD of 2% [22]. In [23], a new topology of cascaded inverters was presented. Due to the substantial increase in voltage levels with fewer semiconductor switches, this topology can be a good candidate for converters used in high-power applications. Among the AMLIs proposed in the recent literature, an interesting and straightforward solution is the asymmetrical cascaded H-bridge multilevel inverter (ACHBMLI) [24], which inherits all the advantages of the CHBMLI structure and allows for an increase in voltage levels by properly choosing the DC voltage amplitude, without adding H-bridge modules and while maintaining reduced hardware complexity. The main challenge of this topology structure concerns the choice of DC voltage amplitudes. Another type of modular converter is the modular converter [25]. These multilevel inverters have a single DC-link, unlike the CHBMLI, and are equipped with inductances between the converter and the load. Modular multilevel converters (MMC) are solutions for high-power applications and are suitable for grid-connected high-power systems, as stated in [26–28]. Such MLI types can generate high-quality voltages and are widely used in grid-connected applications, such as high-voltage DC transmission or energy storage systems [29–31]. It has

to be noted that, even though the field of applications of ACHBMLIs is relevant [10,32–36], their adoption in the area of electrical drives is much less addressed in the recent literature and only a few papers deal with this topic [37,38]. Some other articles discuss different types of AMLIs in electrical drive applications, reporting good results in terms of efficiency and THD [39–42]. However, the ACHBMI structure for the proposed application has yet to be deeply investigated.

Concerning the modulation techniques, in the literature, there are two methods to select DC voltage amplitudes: the binary method, with a voltage ratio among the DC sources of 1:2:4…, and the tertiary method, with a voltage ratio of 1:3:9…[10]. An interesting improvement is discussed in [43], where the ratio among the three sources of ACHBMLI is 1:2:6. According to [44], staircase modulation is the most suitable method to control an ACHBMLI converter. This modulation strategy allows obtaining a staircase voltage waveform using a simple real-time algorithm that can be implemented in common electronic devices. However, the main drawback of this approach is the presence of low-order voltage harmonics that increase as the modulation index decreases. Thus, this aspect limits the application fields of this technique. Therefore, this work aims to analyze the performance of ACHBMLI's performance in terms of voltage harmonics, conversion efficiency, power distribution among the voltage levels, and dead-time effects on the output voltages with multi-carrier pulse-width modulation (MC PWM) strategies is still lacking in the recent literature. PWM allows for the generation of output voltage waveforms from the inverter with low harmonic content, with only high-frequency harmonics present. However, this technique requires a high number of switching phases, leading to increased switching losses.

In this context, this paper describes the performance comparison in terms of both the voltage harmonic content and the efficiency of IPMSM drives supplied by specific topologies of symmetric and asymmetric converters. The aim of this work is focused on demonstrating that the adoption of power converters with asymmetrical topology in electrical drive applications can be a very valuable solution for increasing the techno-economic performance of the whole system. Another novelty of this paper consists of adapting the PWM technique for ACHBMLI through the application of specific logic functions. The choice of a seven-level converter is justified by the fact that this topology is a good compromise between the number of levels and the performance. For real-time validation, a comparative analysis was conducted to evaluate the performance of an electrical drive powered by symmetric and asymmetric H-bridge multilevel inverters, examining the system's dynamic performance and analyzing the converters' losses. Finally, this work brings an in-depth investigation of the dynamic performance of the whole system powered either with symmetrical or asymmetrical converters, highlighting the advantages and drawbacks that the latter could bring. This analysis, at present day and from the author's knowledge, has not yet been exploited.

This paper consists of the following sections: Section 2 describes the mathematical models of the CHBMLI in symmetric and asymmetric configurations and the PMSM taken into account; Section 3 reports the implementation of the adopted control strategy and the corresponding modulation technique; whereas Section 4 discusses the simulation results and draws the related conclusions; Section 5 describes the test bench used for the real-time validation; finally, Section 6 presents and discusses the experimental results.

2. CHBMLI and IPMSM Mathematical Models

The traditional CHBMLI can generate a load voltage waveform with N_s number of levels that depend on the number of the cascaded connected H-bridge n_c. N_s can be expressed as:

$$N_s = 2n_c + 1. \tag{1}$$

For the ACHBMLI in binary configuration the number of voltage levels N_a, as reported in [45], is expressed as:

$$N_a = 2^{n_c+1} - 1. \tag{2}$$

Therefore, a CHBMLI with two H-bridges can produce a voltage waveform with five levels, while an ACHBMLI in binary configuration can produce a voltage waveform with seven levels. Therefore, it is evident that the ACHBMLI can produce a voltage waveform with more levels (and, thus, higher quality) than the CHBMLI with the same number of connected H-bridges. For instance, Figure 1 compares the structures of a three-phase seven-level CHBMLI and an ACHBMLI; it can be noted that both inverters can generate a voltage waveform with seven levels, but the ACHBMLI is composed of three fewer H-bridges.

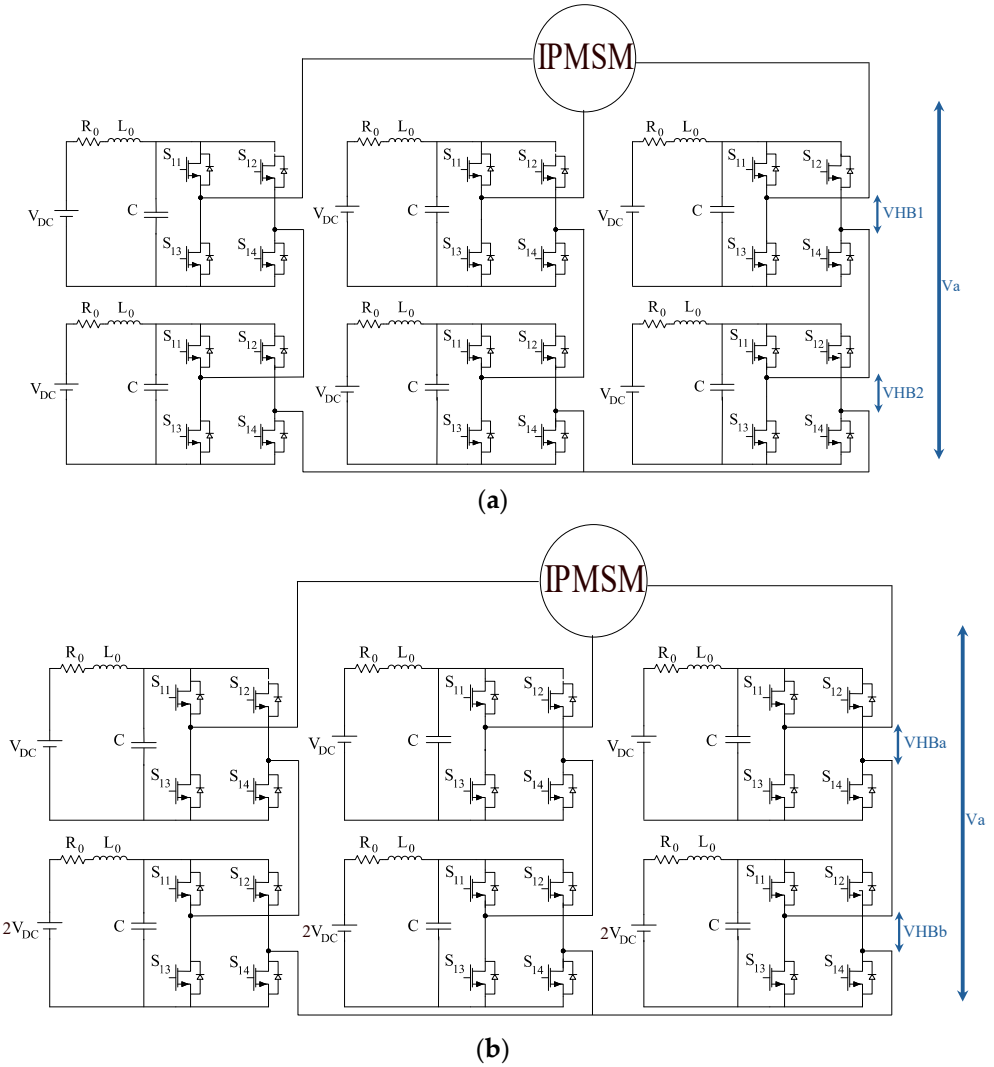


Figure 1. Three-phase: (**a**) 5-level CHBMLI and (**b**) 7-level ACHBMLI.

The mathematical model of the generic phase x of a CHBMLI is reported below:

$$\begin{cases} v_x(t) = \sum_{i=1}^{n_C} v_{HBi}(t) = \sum_{i=1}^{n_C} v_{Ci}(t)(S_{i1} - S_{i2}) \\ \frac{di_{0i}(t)}{dt} = -\frac{R_0}{L_0} i_{0i}(t) - \frac{v_{Ci}(t)}{L_0} + \frac{V_{DC}}{L_0} \\ \frac{dv_{Ci}(t)}{dt} = -\frac{1}{C} i_x(t)(S_{i1} - S_{i2}) + \frac{1}{C} i_{0i}(t) \end{cases}, \quad (3)$$

where $v_{HBi}(t)$ is the output voltage of the generic H-bridge, S_{i1}, S_{i2} $(i = 1 \ldots 4)$ are the gate signals of the power components, $v_x(t)$ is the phase voltage of the single phase, that is a sum of the voltage of cascaded H-bridge, $i_x(t)$ is the load current of the generic phase, V_{DC} refers to the voltage of the DC generator, $i_{0i}(t)$ represents the input current of the i-th H-bridge, and $v_{Ci}(t)$ denotes the voltage across the i-th DC-link capacitor. The circuit

parameters are as follows: R0 is the power supply circuit resistance, power supply circuit resistance is L0, and DC-link capacity is C. The mathematical model of the generic phase of the converter in asymmetric configuration is described as follows:

$$\begin{cases} v_{HBa}(t) = v_{Ca}(t)(S_{a1} - S_{a2}) \\ \frac{di_{0a}(t)}{dt} = -\frac{R_0}{L_0} i_{0a}(t) - \frac{v_{Ca}(t)}{L_0} + \frac{V_{DC}}{L_0} \\ \frac{dv_{Ca}(t)}{dt} = -\frac{1}{C} i_x(t)(S_{a1} - S_{a2}) + \frac{1}{C} i_{0a}(t) \end{cases}, \tag{4}$$

$$\begin{cases} v_{HBb}(t) = v_{Cb}(t)(S_{b1} - S_{b2}) \\ \frac{di_{0b}(t)}{dt} = -\frac{R_0}{L_0} i_{0b}(t) - \frac{v_{Cb}(t)}{L_0} + \frac{2V_{DC}}{L_0} \\ \frac{dv_{Cb}(t)}{dt} = -\frac{1}{C} i_x(t)(S_{b1} - S_{b2}) + \frac{1}{C} i_{0b}(t) \end{cases}, \tag{5}$$

$$v_x(t) = v_{HBa}(t) + v_{HBb}(t), \tag{6}$$

where *HBb* is the H-bridge that has DC-link voltage twice *HBa*, v_{HBa} and v_{HBb} are the output voltage of *HBa* and *HBb*, respectively, S_{a1}, S_{a2}, S_{b1} and S_{b2} are the gate signals of the asymmetric inverter, while i_{0a} and i_{0b} represent the input current of the H-bridges, and v_{Ca} and v_{Cb} are the voltage across the respective DC-link capacitor.

To obtain a model that considers the current conduction of the diode, the generalized switching functions (GSF) [16] must be implemented:

$$\begin{cases} S_{i1} = [(i_x(t) \geq 0)\ G_{i1}] + [(i_x(t) < 0)\ \overline{G_{i3}}] \\ S_{i3} = [(i_x(t) \leq 0)\ G_{i3}] + [(i_x(t) > 0)\ \overline{G_{i1}}] \\ S_{i2} = [(i_x(t) \leq 0)\ G_{i2}] + [(i_x(t) > 0)\ \overline{G_{i4}}] \\ S_{i4} = [(i_x(t) \geq 0)\ G_{i4}] + [(i_x(t) < 0)\ \overline{G_{i2}}] \end{cases} \tag{7}$$

where the gate signals, denoted as S_{ik}, depend on the load current and the generic signals generated by the modulator block G_{ik}. These functions are referred to as generic HBi.

The power losses involved in such a type of converter can be primarily divided into conduction losses, P_{cond}, due to the current flow through the components, and switching losses, P_{sw}, during the switching turn-on and turn-off phases of the components.

Therefore, the efficiency of the converter can be determined as follows:

$$\eta_{\%} = \frac{P_{in}}{P_{in} + P_{sw} + P_{cond}}\ 100, \tag{8}$$

where $\eta_{\%}$ represents the inverter efficiency, expressed in percentage, P_{in} is the input power of the converter.

Regarding the CHBMLI and ACHBMLI configurations, the power losses are different even if they have the same topology structures. Moreover, the power loss distribution among the H-bridge modules is influenced by the modulation techniques. Indeed, the cascaded connected H-bridge modules can work simultaneously or non-simultaneously in dependence on the modulation scheme employed.

In terms of the voltage stress on the power components, the CHBMLI and ACHBMLI present different conditions. Indeed, the power components of the H-bridge module that has a double value of V_{DC} in the ACHBMLI configuration present a higher voltage stress than the counterpart in the CHBMLI configuration.

Concerning the implementation of the PMSM mathematical model, the more general anisotropic structure with interior permanent magnets has been taken into consideration, traditionally named IPMSM. The Clarke–Park transformation was employed to represent

all machine quantities in a $dq0$-axes system rotating at synchronous speed. In this way, it is possible to obtain the following system in the Laplace domain:

$$\begin{cases} V_d = RI_d + L_d s I_d - p\omega L_q I_q \\ V_q = RI_q + L_q s I_q + p\omega L_d I_d + p\omega \lambda_{PM}, \\ V_o = RI_o + L_o s I_o \end{cases} \quad (9)$$

where V_d, V_q and V_o are the $dq0$-axes stator voltage components, I_d, I_q and I_o are the $dq0$-axes current components, p is the number of poles, R is medium stator resistance, L_d, L_q and L_o are $dq0$-axes inductance components, and λ_{PM} is the flux generated by the permanent magnets.

As previously described, this work aims to analyze the impact of the ACHBMLI configuration in electrical drive applications. In this context, the mathematical models considered in this work have been implemented in MATLAB/Simulink® R2024a environment to investigate and compare the converter performance in terms of harmonic distortion. Indeed, by considering several working conditions, the harmonic distortion on the voltage and current waveforms have been analyzed. Moreover, the comparison of the working operation between the CHBMLI and ACHBMLI configurations has been studied.

3. Modulation Technique and Control Strategy

In this work, the chosen modulation technique is the MC PWM due to its simple implementation and good response in terms of harmonic content. Among the MC PWM strategies reported in the recent literature [46], the phase disposition (PD) modulation scheme has been implemented; the modulation schemes employed for the three-phase seven-level CHBMLI, which is appliable to asymmetrical configurations, consist of three modulation signals (M1, M2, and M3) and six carrier signals (c1, c2, c3, c4, c5, and c6), as is shown in Figure 2.

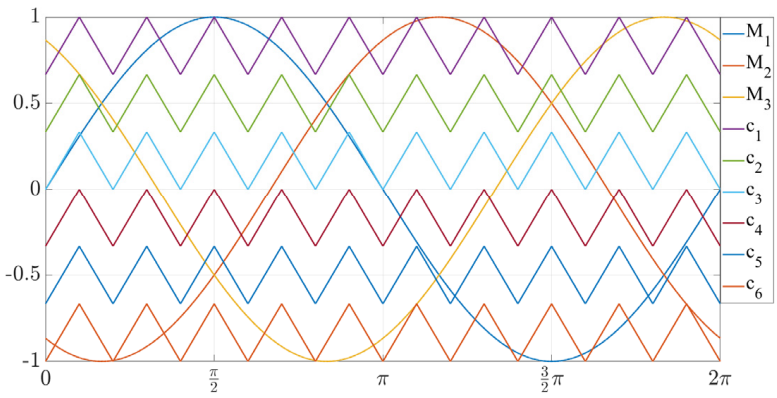


Figure 2. Modulation schemes PD PWM for three-phase 7-level CHBMLI.

In the specific case of electrical drive applications, the variability of the rotor speed and generated torque can be significant, especially for dynamic mechanical loads. Therefore, the amplitude and the frequency of the modulation signals must be adjusted to meet the requirements of the load in terms of speed and torque. Nevertheless, the voltage waveform generated through the MC PWM technique has a low harmonic content, and the only high-frequency harmonics are centered at frequencies that are multiples of the carrier frequency. Therefore, the overall high-frequency voltage harmonics are relatively easy to filter, consequently achieving a very low THD of the stator currents. However, high-frequency harmonics increase the iron loss of the IPMSM, which represents one of the major drawbacks concerning the PWM techniques applied in the field of electric drives.

As aforementioned, the PD PWM can be also used for ACHBMLI, even if some modifications are needed. Moreover, the signals of the upper H-bridges (the H-bridges with a DC voltage equal to V_{DC}) need to be modified [46].

The modified gate signals were obtained by using the following logic functions:

$$\begin{cases} S_{x1} = (S_{11} \wedge S_{21} \wedge S_{31}) \vee (\overline{S_{11}} \wedge \overline{S_{21}} \wedge S_{31}) \\ S_{x2} = (S_{12} \wedge S_{22} \wedge S_{32}) \vee (\overline{S_{12}} \wedge \overline{S_{22}} \wedge S_{32}) \\ S_{x3} = (S_{13} \wedge S_{23} \wedge S_{33}) \vee (\overline{S_{13}} \wedge \overline{S_{23}} \wedge S_{33}) \\ S_{x4} = (S_{14} \wedge S_{24} \wedge S_{34}) \vee (\overline{S_{14}} \wedge \overline{S_{24}} \wedge S_{34}) \end{cases}, \quad (10)$$

where S_{1j}, S_{2j} and S_{3j} ($j = 1 \ldots 4$) represent the traditional gate signal for seven-level CHBMLI and S_{xj} are the new gate signals for the upper H-bridges of the ACHBMLI. Therefore, the control signals for the upper H-bridges were obtained by comparing the modulation signal with the carrier signal, like a standard MC MPWM. Subsequently, as depicted in Figure 3, the logic circuit processes all signals to determine the gate signals.

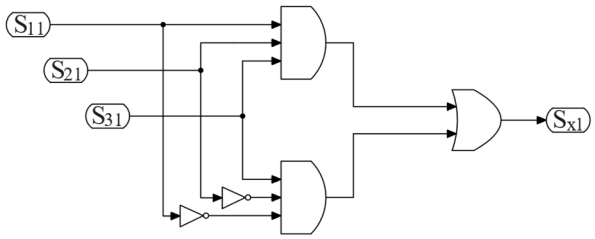


Figure 3. Module of the logic circuits employed to modify the control signals.

The implementation of the logical functions expressed in (10) is achieved by employing the four logical circuit modules (Figure 3).

Concerning the control strategy adopted for this work, as shown in Figure 4, the field-oriented control has been chosen with the integration of a multilevel inverter (either symmetrical or asymmetrical). The MATLAB/Simulink® R2024a environment was employed to simulate the behavior of the whole electrical drive system. The control scheme comprises both speed and current closed loops. The speed error is processed by a PI regulator to obtain the reference current, whereas the reference direct-axis current component is set equal to zero. From these signals, the reference direct-axis and quadrature-axis reference voltages are obtained, namely v_d^* and v_q^*, respectively. Finally, the Clarke and Park transformations allow the dq signals to convert into a three-phase reference frame, from which the voltages are sent to the three modulation signals of the MC PWM pattern. Therefore, through these modulation signals, it is possible to derive all the switching signals of each power component of the ACHBMLI. The Simulink model implemented is shown in Figure 5. Four different blocks can be identified, and they correspond to the models of IPMSM, power converter, modulator, and adopted control strategy.

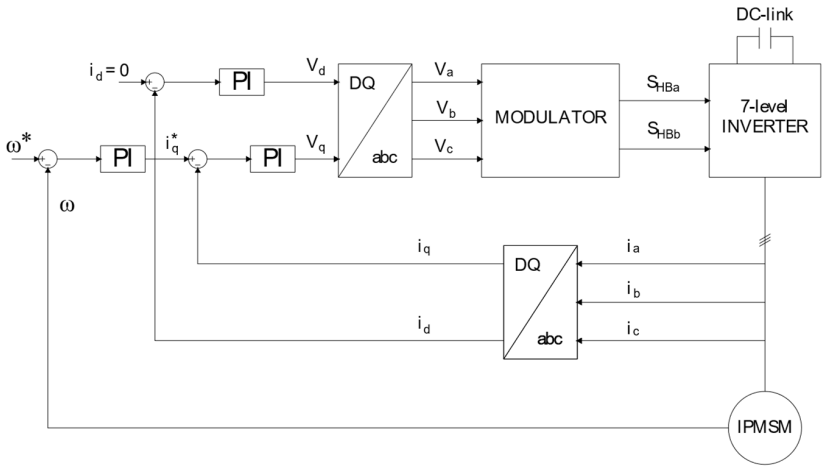


Figure 4. Field-oriented control diagram for an electrical drive system.

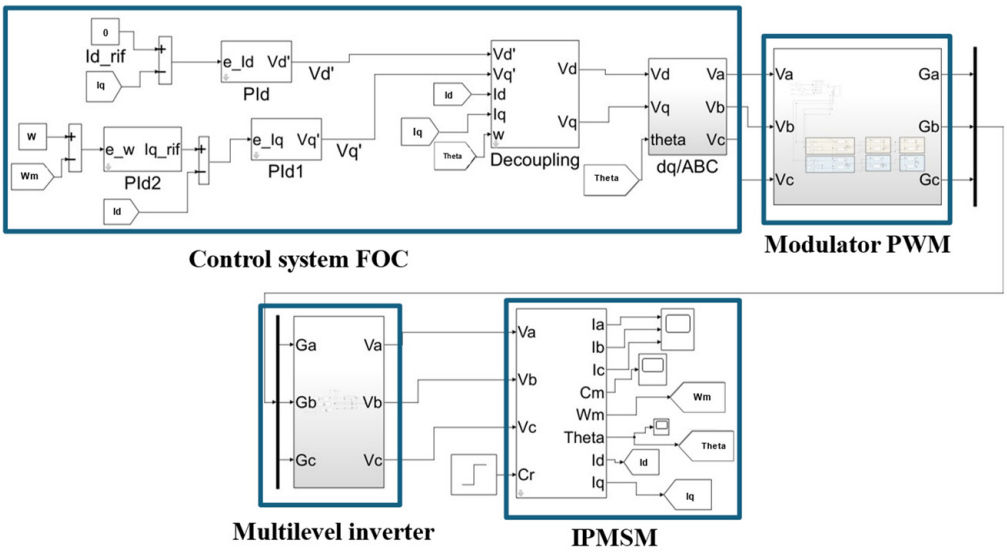


Figure 5. Simulink model implemented for the proposed study.

4. Simulation Results and Discussions

This section aims to show the simulation results and to compare the performances between symmetrical and asymmetrical converters that feed IPMSM drives. Both converters are controlled with the PD technique described in Section 3. The comparison is performed by analyzing the trends in time of stator input voltages and currents, output speed, electromagnetic torque, input H-bridge power, and THD values of the three-phase voltages. The THD is important for assessing the quality of AC electricity supply and can be calculated as follows:

$$THD = \sqrt{\frac{\sum_{h=1}^{\infty}\left(V_h^2 - V_1^2\right)}{V_1^2}} \cdot 100, \tag{11}$$

where V_h is the value of the *hth* harmonic and V_1 represents the fundamental harmonic value.

Table 1 summarizes the parameters of the symmetrical and asymmetrical inverters considered for this study. It must be highlighted that some circuit parameters, such as the DC-link capacitors and the typology of power components, have not been changed to provide a consistent comparison between the two inverters. The main data of the IPMSM used for the proposed analysis are reported in Table 2. The technical features of the inverter were chosen to be perfectly adaptable with the available IPMSM; indeed, both the CHBMLI and ACHBMLI are designed to generate line-to-line voltages higher than the rated voltage of the IPMSM.

Table 1. Data for symmetrical and asymmetrical inverters.

Quantity	Symbol	Value
Input voltage CHBMLI	V_{iDC}	75 V
Input voltage ACHBMLI	V_{DC}	50 V
Power supply circuit resistance	R_0	0.1 Ω
Power supply circuit inductance	L_0	1 µH
DC-link capacitance	C	2.2 mF
Carrier frequency	f_{PWM}	10 kHz
Dead time	t_d	1 µs

The simulations were designed with the following working operating conditions:

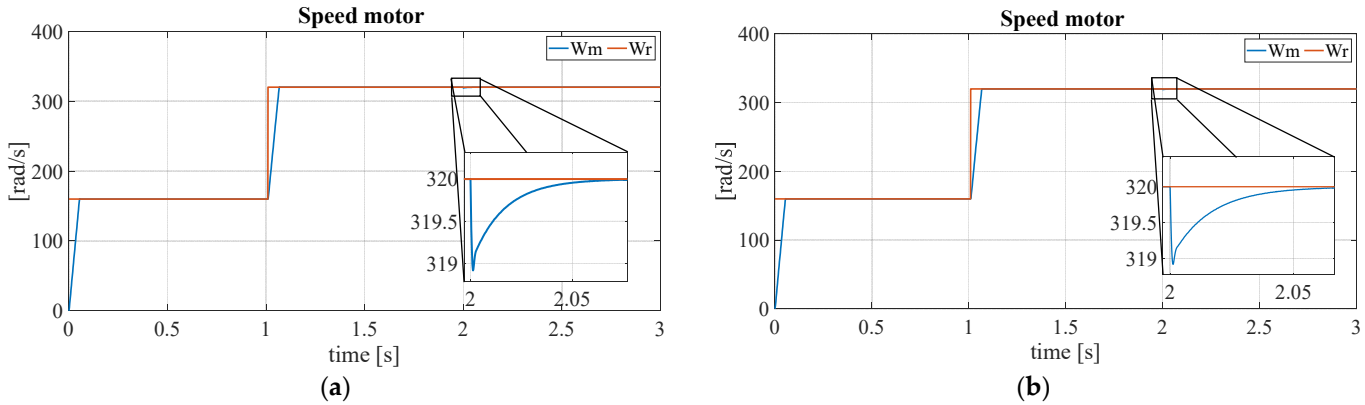
(1) At t = 0 s, the motor is driven with a reference speed equal to 50% of its rated value at no-load conditions.

(2) At t = 1 s, the reference speed is applied to the motor without any mechanical load.
(3) At t =2 s, the rated load torque is applied to the motor.

Table 2. IPMSM data.

Quantity	Symbol	Value
Rated voltage	V_n	150 V
Rated current	I_n	8.2 A
Number of pole pairs	p	3
Rated speed	ω	320 rad/s
Maximum torque	C_m	1.8 Nm
Average stator resistance	R	2.21 Ω
Direct-axis inductance	L_d	9.77 mH
Quadrature-axis inductance	L_q	14.94 mH
Flux emitted by permanent magnets	λ_{PM}	0.0844 Wb
Moment of inertia	J	0.001 Kg m^2
Viscous friction coefficient	b	0.001 Nms

Figure 6a,b shows the comparison between the motor speed of the IPMSM fed by the five-level CHBMLI and the seven-level ACHBMLI configurations.



(**a**) (**b**)

Figure 6. Time trends of the motor speed (**a**) 5-level CHBMLI; (**b**) 7-level ACHBMLI.

It can be noted that, in both cases, the field-oriented control aims to rapidly reduce the speed error, allowing the PMSM speed motor to quickly equal the reference speed within a few PWM cycles in any of the previously described conditions. In addition, the adoption of the asymmetrical topology does not affect the dynamic performance of the drive confirming the good performance of the proposed power converter architecture, even during the application of the rated load or during sudden speed changes. Therefore, it can be stated that the two-speed trends of Figure 6 are very close to each other, leading to the fact that the use of an ACHBMLI allows achieving the same speed performance, but with a reduced number of power components, decreasing costs and increasing reliability and flexibility of the system.

Similar results can be appreciated in Figure 7, which illustrates the system response in terms of electromagnetic torque to variations in reference speed and load for both symmetrical and asymmetrical power converter configurations. Very small differences can be detected by comparing the two trends; in both cases, the electromagnetic torque, after a short transient period, stabilizes its value in any operating conditions previously reported. The slight difference is detected during the transient period applied at 2 s, where the application of the rated load causes a lower undershoot for the ACHBMLI (0.11% instead of 0.12%).

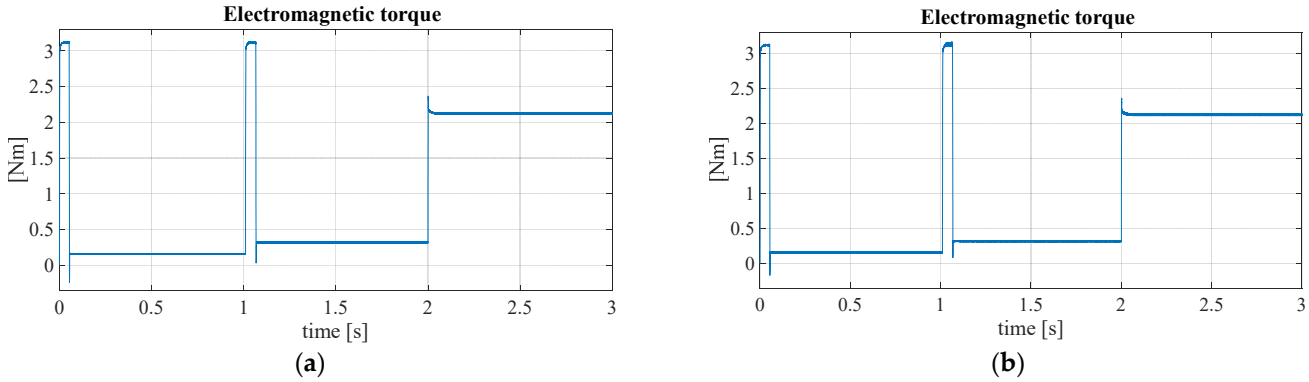


Figure 7. Time trends of electromagnetic torque: (**a**) 5-level CHBMLI; (**b**) 7-level ACHBMLI.

The time trends of the line-to-line voltages are depicted in Figure 8. As well as for the previous results, it can be observed how similar the voltage transient and steady-state responses to changes in load and reference speed are for both symmetrical and asymmetrical converters.

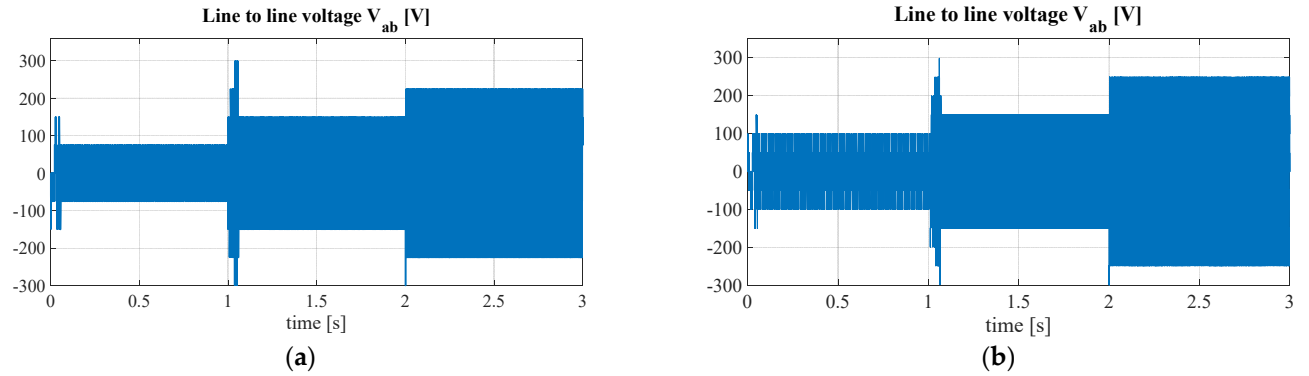


Figure 8. Temporal evolution of three-phase stator voltages: (**a**) generated by the 5-level CHBMLI; (**b**) generated by the 7-level ACHBMLI.

To show how the output voltage from the converters varies under different operating conditions, Figures 9–11 report the phase voltage waveforms Va and the individual voltage contributions of each single bridge (for CHBMLI: VHB1 and VHB2; while for the asymmetric configuration: VHBa and VHBb).

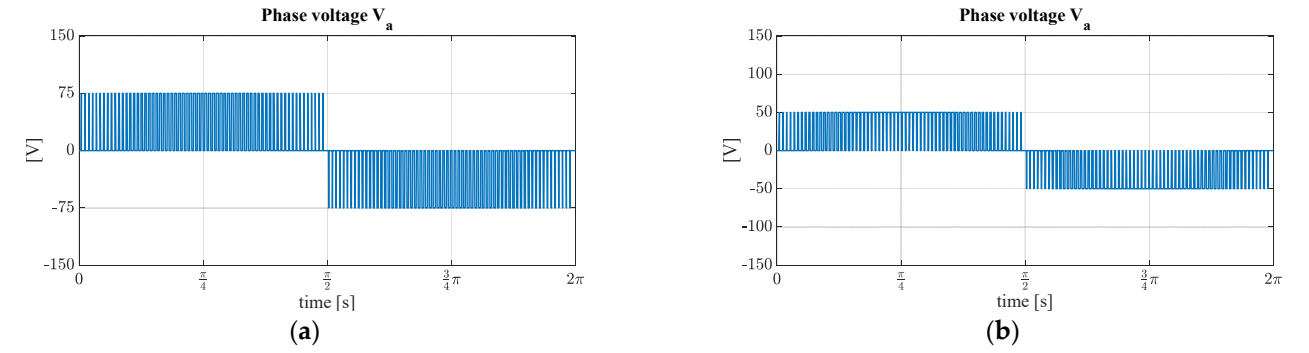


Figure 9. *Cont.*

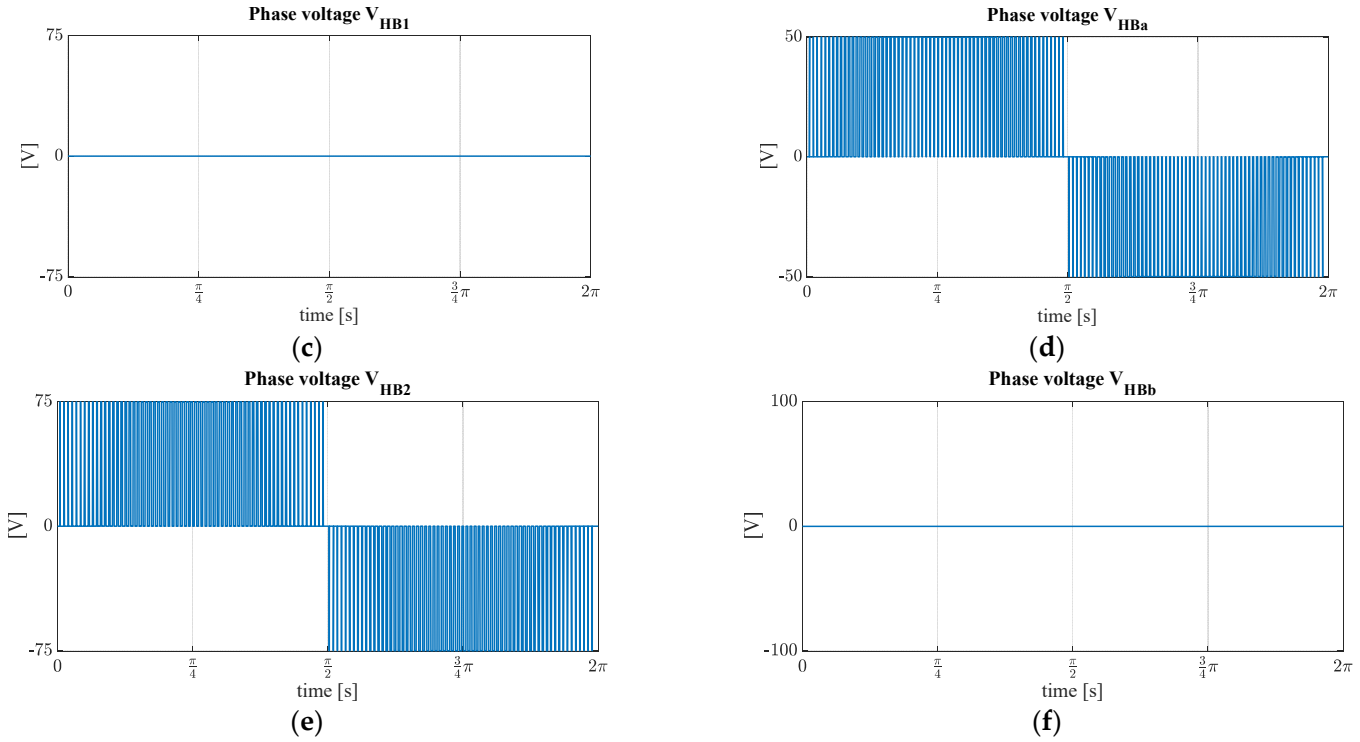


Figure 9. A single period of the Va voltage at steady state in the first condition: (**a**) generated by the 5-level CHBMLI; (**b**) generated by the 7-level ACHBMLI; (**c**) generated by the *HB1*; (**d**) generated by the *HBa*; (**e**) generated by the *HB2*; (**f**) generated by the *HBb*.

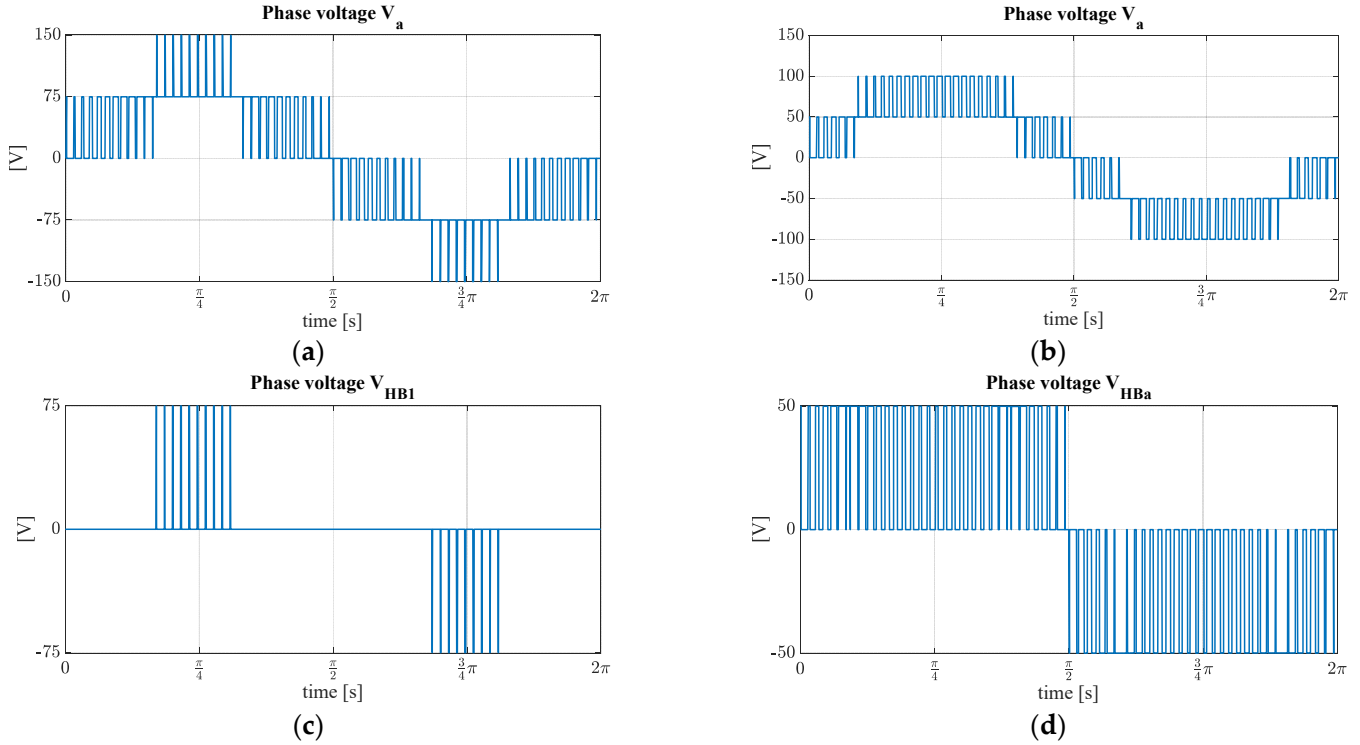


Figure 10. *Cont.*

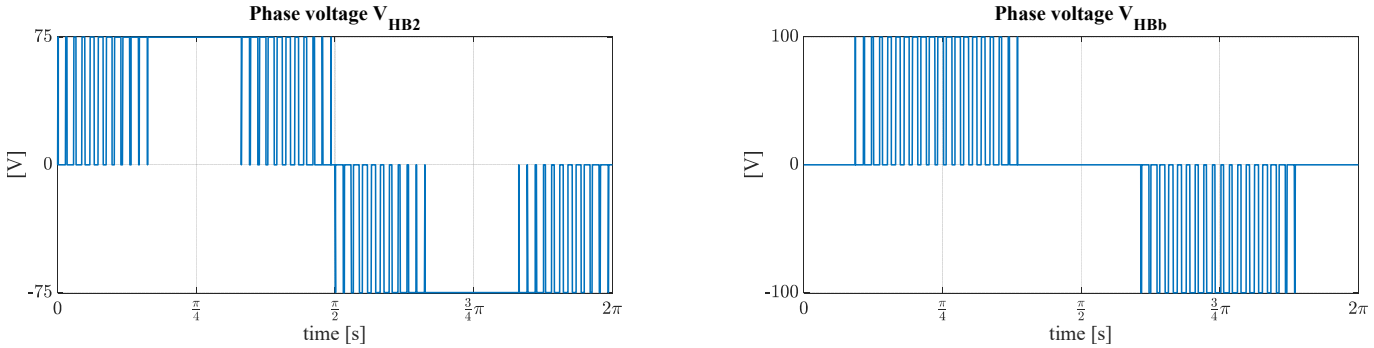


Figure 10. A single period of the Va voltage at steady state in the second condition: (**a**) generated by the 5-level CHBMLI; (**b**) generated by the 7-level ACHBMLI; (**c**) generated by the *HB1*; (**d**) generated by the *HBa*; (**e**) generated by the *HB2*; (**f**) generated by the *HBb*.

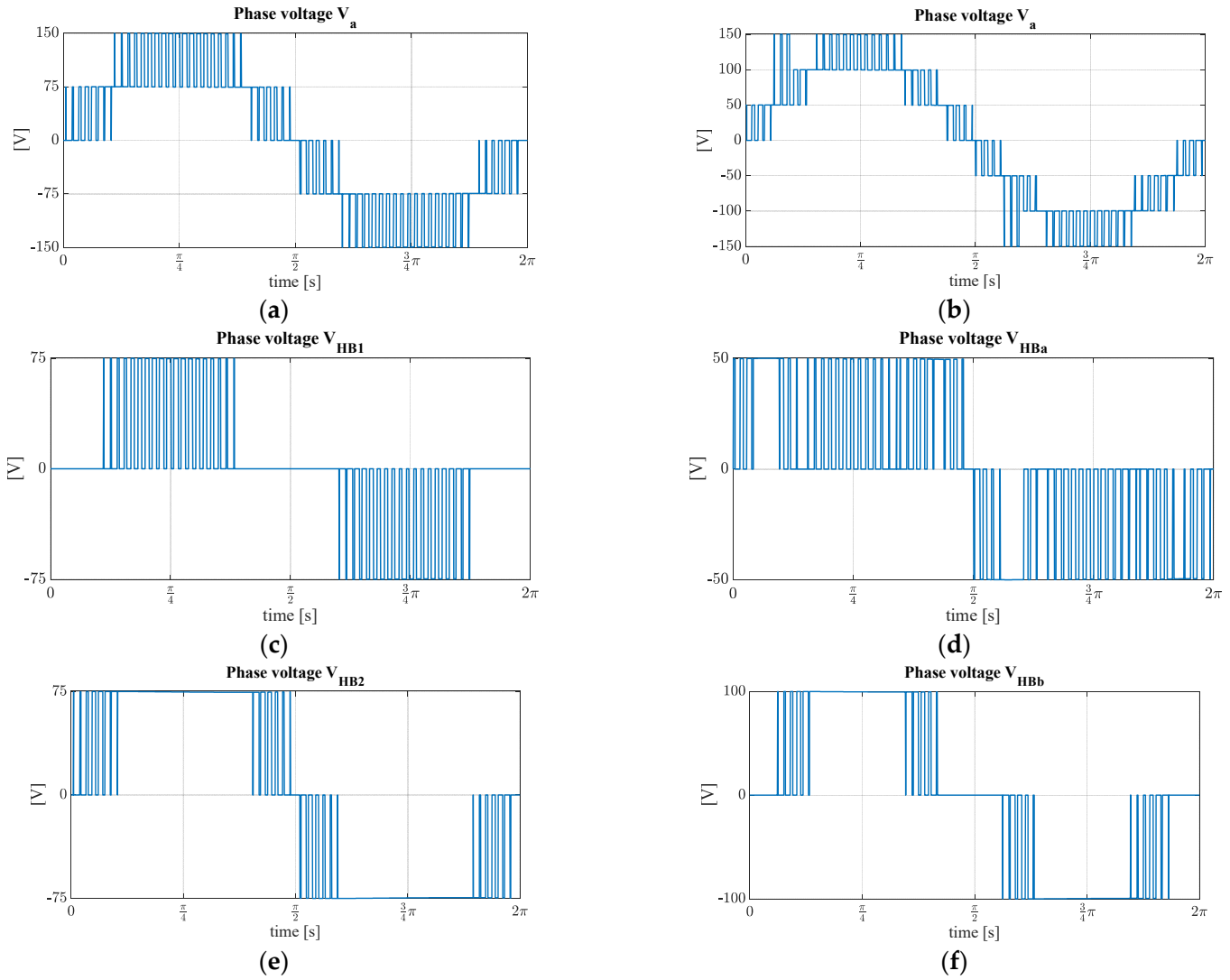
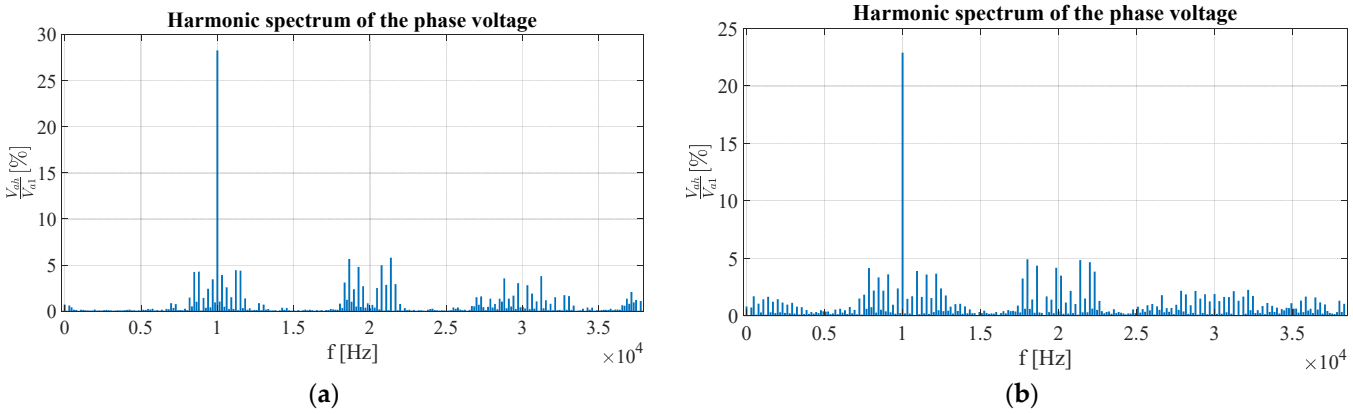


Figure 11. A single period of the Va voltage at steady state in the third condition: (**a**) generated by the 5-level CHBMLI; (**b**) generated by the 7-level ACHBMLI; (**c**) generated by the *HB1*; (**d**) generated by the *HBa*; (**e**) generated by the *HB2*; (**f**) generated by the *HBb*.

For the working operating condition number one, as shown in Figure 9, the output voltage consists of three levels for both converters because, for both converters, only one bridge is modulated. In detail, in the working operating condition number two, the speed reference increases; as a result, the inverter generates an output voltage with a greater number of levels compared to the previous time intervals. In these conditions, the voltage generated by both converters is at five levels because, as shown in Figure 10, for the CHBMLI and ACHBMLI, all H-bridges are active.

Figure 12 displays the harmonic components of the phase voltage waveforms and the motor's supply current for both cases when the speed and the torque are set at their rated values. The graphs show the harmonics as a percentage of the first harmonic, both for voltage and current. In all the graphs, the first harmonic of current or voltage is not depicted because it is significantly greater than the higher harmonics.



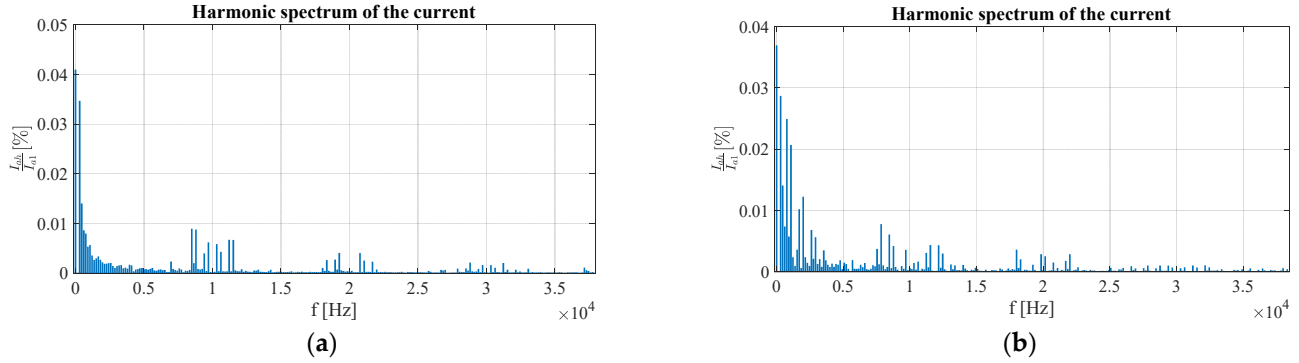
(**a**) (**b**)

Figure 12. Harmonic spectra: (**a**) voltage CHBMLI; (**b**) voltage ACHBMLI.

In the working operating condition number three, where the rated load is applied to the system, the ACHBMLI generates seven-level voltages, with all the converter bridges in operation, as shown in Figure 11, which also highlights some differences between the drive powered by CHBMLI and ACHBMLI. It should be noted that the seven-level voltage waveform exhibits some undesired voltage levels between 50 V and 150 V, both in the positive and negative cycles. Simulation analysis indicates that this phenomenon is caused by the current flow path through the freewheeling diodes, which is influenced by the phase shift between voltage and current. As a result, the output voltage becomes the sum of the input DC voltages. Specifically, the second voltage level, ranging from 50 V to 100 V or −50 V to −100 V, is generated by the combination of both H-bridges connected in cascade for each phase.

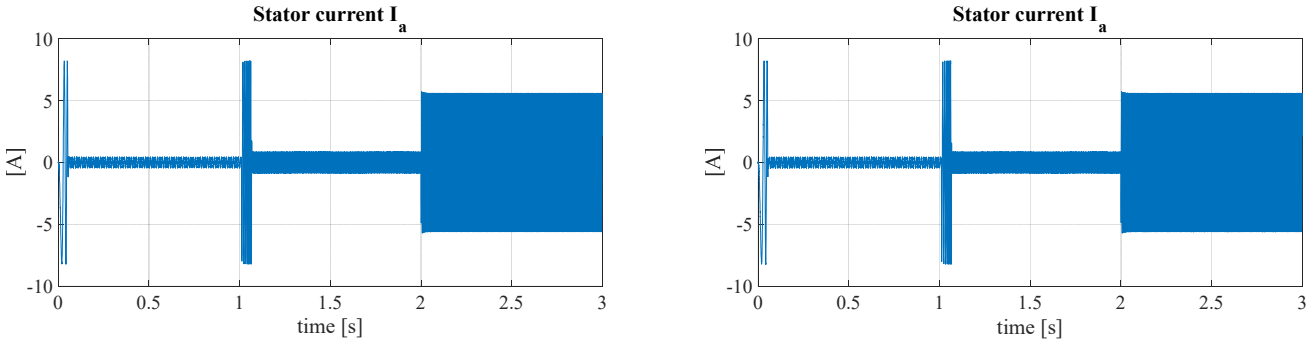
Focusing on Figure 12a,b, in both cases, the harmonic spectrum resembles that of a waveform generated using MC PWM, where the only harmonics detected are those around the multiples of the carrier frequency. Furthermore, in both cases, the dominant harmonic is at 10 kHz. When analyzing the current spectra, in Figure 13a,b, in addition to the high-frequency harmonics, low-frequency harmonics are also present. This is because the load itself significantly attenuates the high-frequency harmonics. Finally, for this particular operating condition, the THD of the voltage THD_V for the symmetric converter is 37.3473% while, for the asymmetric converter, it is equal to 27.1%. On the other hand, the THD of the stator's current THD_I is equal to 0.857% for the symmetric converter and 1.1097% for the asymmetric one.

For completeness, Figure 14a,b shows the time trends of the stator currents when the drive is fed by a traditional and an asymmetric inverter configuration, respectively. As well as in the other reported results, the dynamics are not affected using ACHBMLI. In both cases, the root mean square value of the first harmonic of the current for the third operating is 3.9 A.



(**a**) (**b**)

Figure 13. Harmonic spectra: (**a**) current CHBMLI; (**b**) current ACHBMLI.

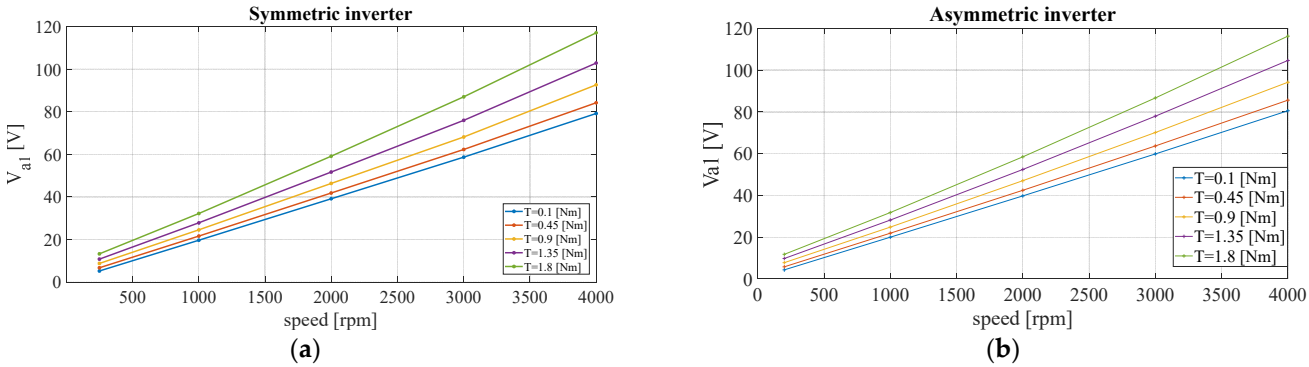


(**a**) (**b**)

Figure 14. Temporal evolution of three-phase stator currents: (**a**) generated by the 5-level CHBMLI; (**b**) generated by the 7-level ACHBMLI.

Further simulations have been conducted to investigate how the THD and the rms value of the first harmonic of phase voltage and current vary under different operating conditions. In these simulations, the torque values are parameterized from 0.1 to 1.8 Nm with steps of 0.45 Nm across a speed ranging from 200 rpm to 4000 rpm.

In Figure 15, all root mean squares of the first harmonic of phase voltage V_{a1} are presented for both converters. As well as for the previous cases, the two graphs are almost identical; in fact, the values that the voltage assumes in both cases are very similar for the same operating conditions. By observing the trend of V_{a1} for constant torque values, it is evident that its value significantly increases with an increase in rotor speed. Additionally, it can be observed that, for a given speed, an increase in load torque corresponds to an increase in V_{a1}.



(**a**) (**b**)

Figure 15. Root mean square of first harmonic phase voltage for various operating conditions: (**a**) CHBMLI; (**b**) ACHBMLI.

Other interesting results are summarized in Figure 16, which shows the comparison of THD_V between CHBMLI and ACHBMLI. It is worth noting that the THD_V of voltages varies under different operating conditions. At low speeds, the value of THD_V is very high and consistently exceeds 150%. However, as the speed increases, it decreases rapidly, stabilizing at much lower values ranging between 15% and 25%, for both the symmetric and asymmetric converters. This is justified by the fact that, at a constant load torque, the speed increase results in both CHBMLI and ACHBMLI generating more voltage levels.

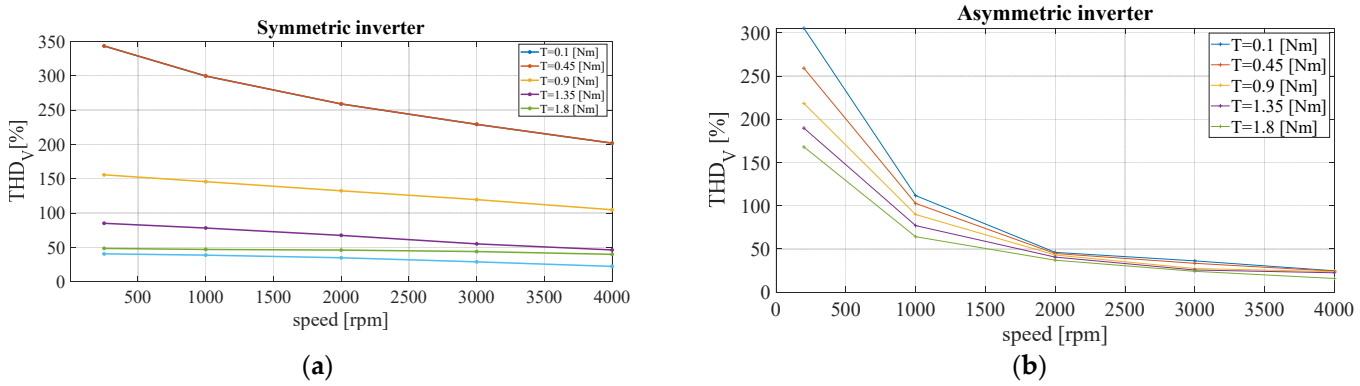


Figure 16. Trend of THD_V for (**a**) CHBMLI; (**b**) ACHBMLI.

In Figure 17, the root mean square of the first harmonic of current I_{a1} is presented for various operating conditions. In this case, Figure 17a,b are very similar to each other. In general, it can be asserted that the current increases with increasing speed for a given load torque and an increase in the load torque corresponds to an increase in the value of I_{a1}.

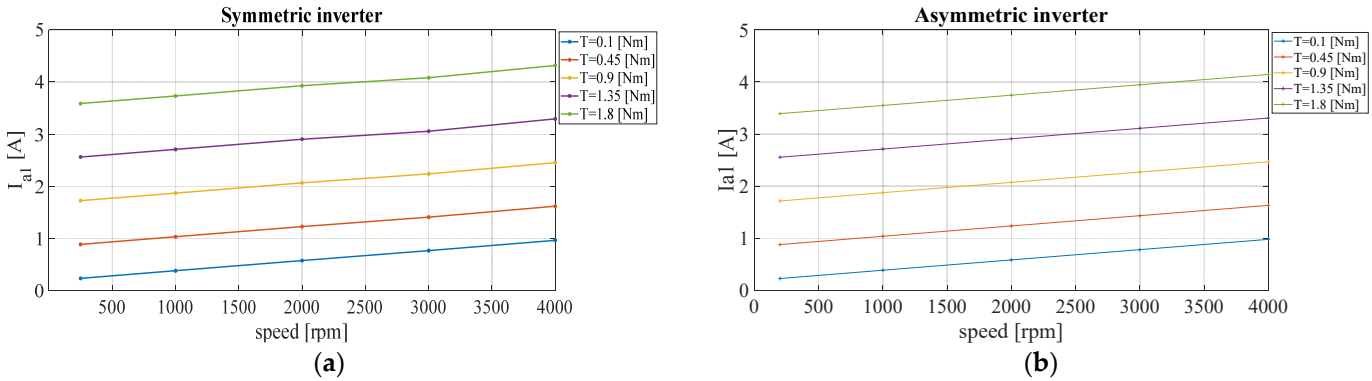


Figure 17. Trend of I_{a1} for (**a**) CHBMLI; (**b**) ACHBMLI.

Figure 18 depicts the trends of THD_I for both ACHBMLI and CHBMLI. The THD_I values obtained from the asymmetric converter are nearly the same as those of the symmetric one. Finally, based on the observations made and the obtained data, it can be asserted that the ACHBMLI has the same performance as the CHBMLI, both in terms of dynamic characteristics and voltage harmonic content.

In addition, it is also interesting to analyze the percentage of power absorbed by each H-bridge to study how this value varies with changing operating conditions (Figure 19). It should be noted that the CHBMLI consists of three H-bridges: *HB1* and *HB2*, while the ACHBMLI consists of *HBa* and *HBb*.

For the CHBMLI, at low-speed values, only *HB2* absorbs power. However, with an increase in speed, the load requires more power, therefore *HB1* must also supply power. Naturally, as the other H-bridges come into operation, *HB2* will absorb a decreasing percentage of power because the remaining power will be provided by the other H-bridge. As mentioned earlier, for low-speed values, *HB1* will be turned off. However, if the speed

increases, it will start to supply power to the load and, typically, at a constant load torque, the percentage of absorbed power will increase with increasing speed.

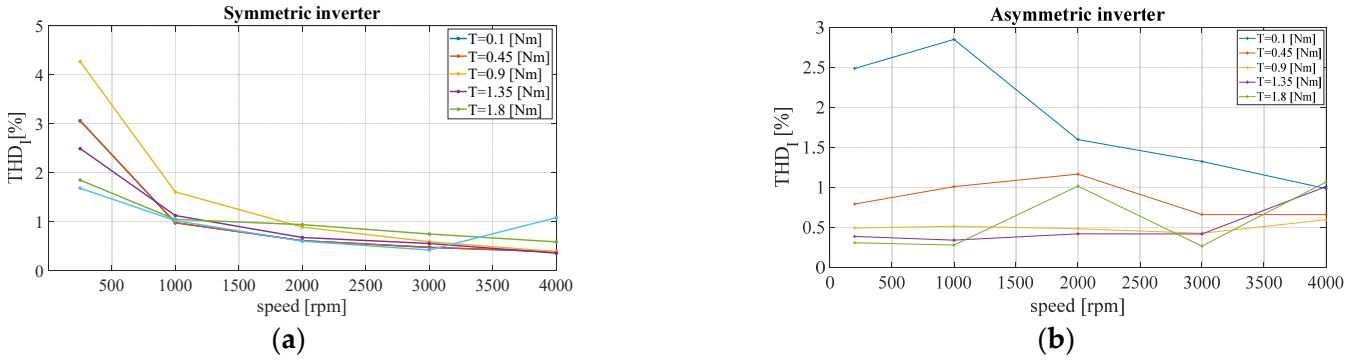


Figure 18. Trend of THD_I: (**a**) CHBMLI; (**b**) ACHBMLI.

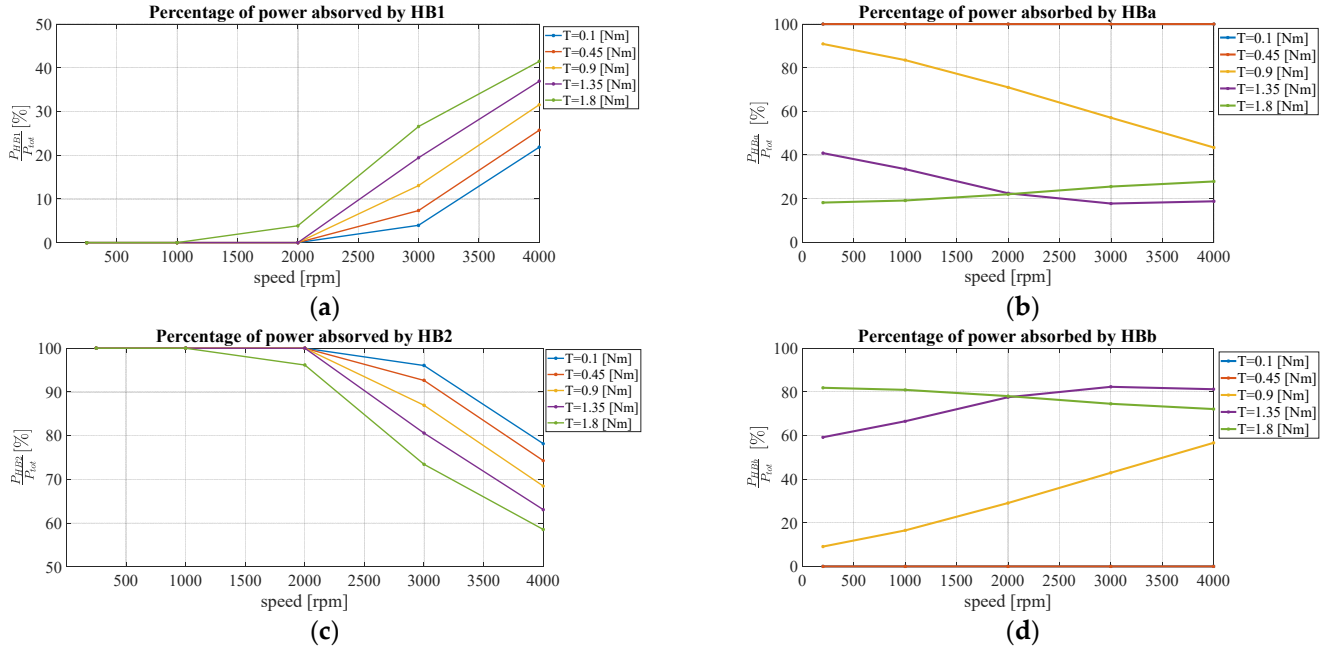


Figure 19. Percentage of power absorbed by: (**a**) *HB1*; (**b**) *HBa*; (**c**) *HB2*; (**d**) *HBb*.

For the ACHBMLI, at low torque values (less than 0.9 Nm), only *HBa* will absorb power while *HBb* remains turned off. When considering a load torque of 0.9 Nm, *HBb* will begin to function and absorb increasing power with increasing speed. However, if the load torque is 1.35 Nm, the power absorbed by *HBb* increases with speed, even though at higher speeds above 3000 rpm, the power absorbed as a percentage will decrease. While, when the load torque is 1.8 Nm, at 200 rpm, *HBb* will absorb 80% of the power, which then decreases with increasing speed.

5. Test Bench Equipment

This section describes the test bench equipment used for the real-time validation. As shown in Figure 20, the implemented controller is mounted on the power electronics and drive (PED) board V4 (Elettronica Dedicata Inc., Chiari, Italy), with key specifications listed in Table 3. While the flow chart of the system is shown in Figure 21.

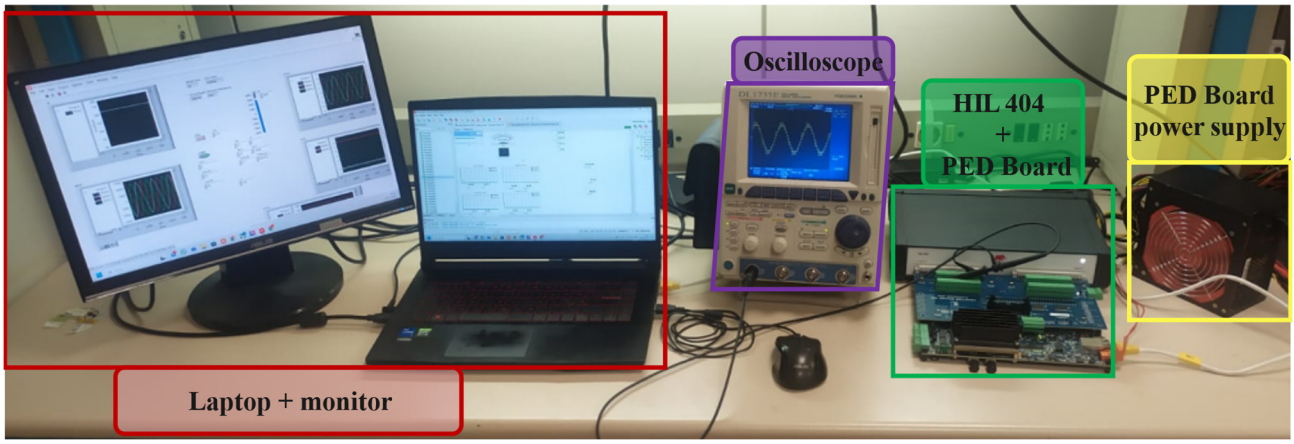


Figure 20. Test bench equipment.

Table 3. PED-Board v4 characteristics.

Hardware	Features
PWM Channels	30x, 0 ÷ 15 V or 0 ÷ 5 V selecTABLE voltage
14 bit-ADC	8 channels, Simultaneous sampling of 1.45 µs conversion time, 8 channels of differential input o −5 V ÷ 5 V or 0 V ÷ 10 V configurable inputs magnetic induction
14-bit-ADC	8 channels, Simultaneous sampling of 1.45 µs conversion time, 8 channels of Differential input o −5 V ÷ 5 V or 0 V ÷ 10 V configurable inputs
10 bit-ADC	8 channels, up to 200 kS/s
Digital I/O	46 × 3.3 V standard
Ethernet	programming, debugging and operation

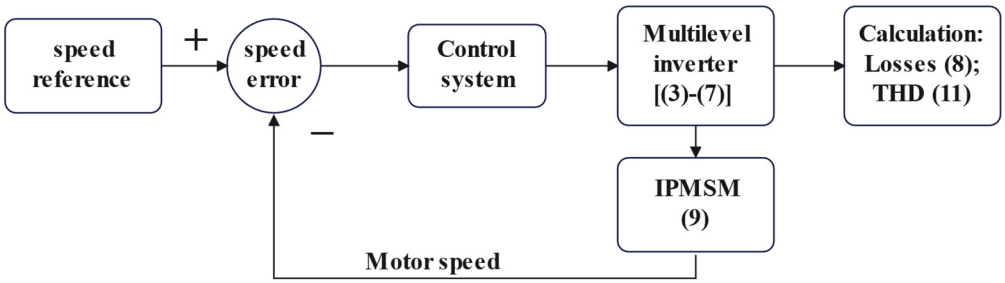


Figure 21. Flowchart of system.

The control algorithm is fully developed in the LabVIEW graphical programming language environment. Specifically, the algorithm consists of two main full-parallel structures: the first structure is a high-frequency cycle that implements the modulator, including carrier signals, dead-time, and PWM signal generation; whereas the second structure handles the acquisition, control, and modulation signal generation operations. The initialization of this process is synchronized to trigger data sampling and control action application at the carrier's peak-to-peak values. Consequently, the sampling frequency is twice the virtual switching frequency. Once compiled into the FPGA, the algorithm can be managed via a real-time control panel through a PC.

The electrical drive systems under test are emulated by Typhoon hardware-in-the-Loop (HIL) 404, whose main features are reported in Table 4, where the models of the CHBMLI, ACHBMLI and IPMSM have been implemented.

Table 4. HIL404 characteristics.

Quantity	Symbol	Value
Input voltage CHBMLI	V_{iDC}	75 V
Input voltage ACHBMLI	V_{DC}	50 V
Power supply circuit resistance	R_0	0.1 Ω
Power supply circuit inductance	L_0	1 µH
DC-link capacity	C	2.2 mF
Carrier frequency	f_{PWM}	10 kHz
Dead time	t_d	1 µs

Finally, the test bench is equipped with an oscilloscope, whose main technical data are summarized in Table 5, and a PC to control the PED board in real-time operations. A specially designed user interface has been developed in the LabView environment.

Table 5. Technical data of the electronic scope.

Hardware	Features
Bandwidth	500 MHz
Sample rate	2 GS/s
Number of channels	4
Vertical sensitivity	2 mV/div to 10 V/div
Horizontal sensitivity	1 ns/div to 50 s/div
Display	6.4” color TFT LCD monitor
Hardware	Features

6. Real-Time Validation

As previously described, this paper presents a comparative analysis between a seven-level ACHBMLI and a five-level CHBMLI in an electric variable-speed drive system.

In this section, a real-time validation has been carried out using the test bench described in the previous section. The same operating conditions in terms of speed and load applied to the drive and outlined in Section 4 were stated. The objective is to compare the dynamic and steady-state performance of the same electric drive when powered by either a seven-level ACHBMLI or a five-level CHBMLI. Therefore, the trends of the speed of the IPMSM, its electromagnetic torque, the supply voltage, and the phase current are compared under the aforementioned power configurations. For instance, Figure 22 compares the motor speed dynamics, highlighting that almost identical results are achieved between both MLI configurations, confirming the validity of the simulation results. If compared with the latter, the transient behavior exhibits slower response times, longer settling times and a maximum of 5% overshoot.

Figure 23 shows the time trend comparison of the torque generated by the IPMSM powered by (a) a seven-level ACHBMLI and (b) a five-level CHBMLI. As well as for the previous case, the two trends are similar to the simulation results, even though a slightly higher torque ripple is detected in the asymmetrical structure. Unlike the previous figures, the time trends of the line-to-line voltages of the two inverters are different, as depicted in Figure 24. Specifically, the peak value of the line-to-line voltage in the first operating condition is 100 V for the asymmetric inverter, while it is only 75 V for the symmetric structure. This difference is justified by the fact that the two inverters have a different number of H-bridges and different DC-link voltage values. The same conclusions can be

drawn for the second operating condition, while, once the load is applied, all the H-bridges of the inverters become active, resulting in equal peak voltage. Although the peak values of the line-to-line voltage of the two inverters are different, the root mean square values of their first harmonics are equal.

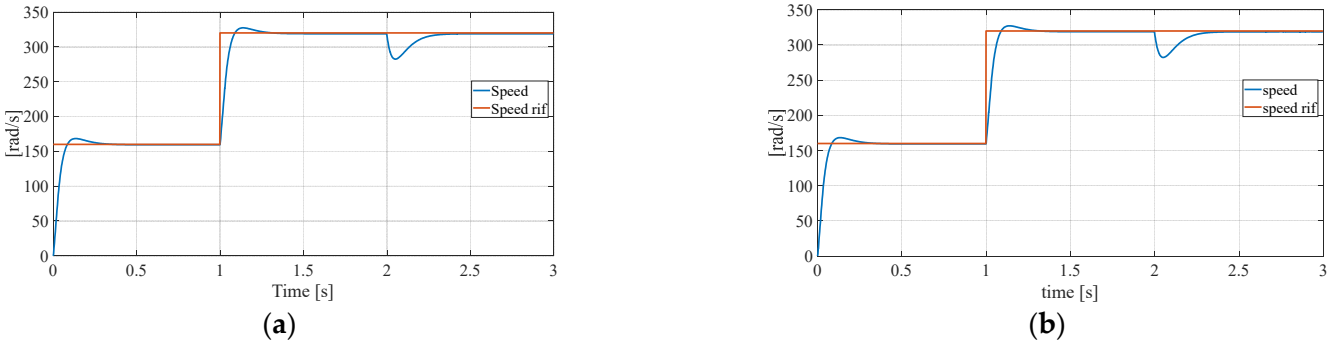


Figure 22. Time trends of the real-time of the motor speed test (**a**) 7-level ACHBMLI; (**b**) 5-level CHBMLI.

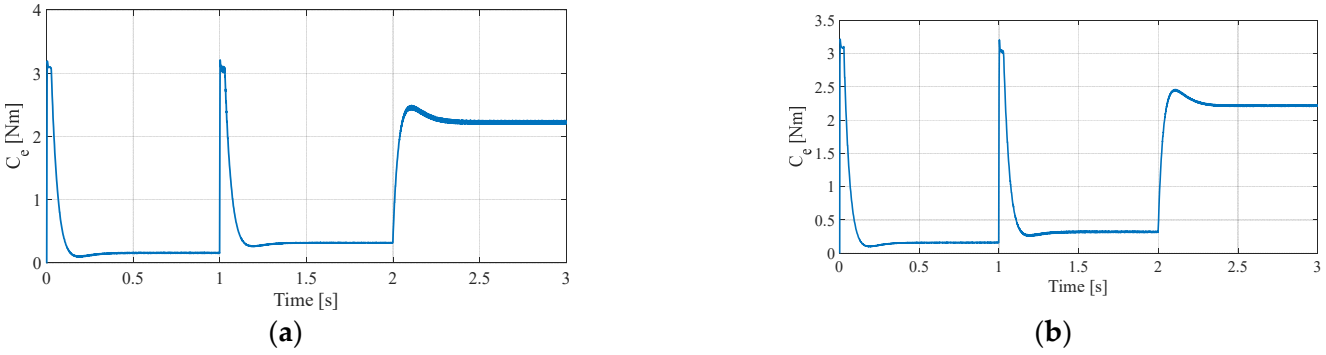


Figure 23. Time trends of the real-time of the electromagnetic torque test: (**a**) 7-level ACHBMLI; (**b**) 5-level CHBMLI.

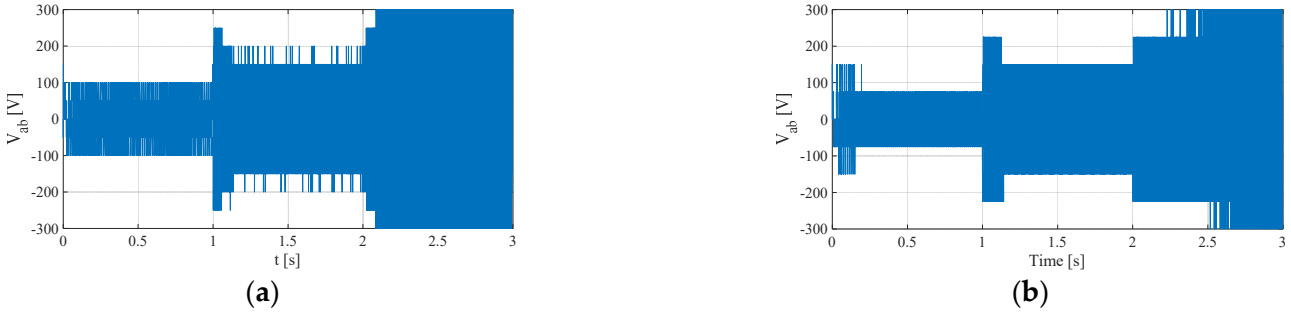
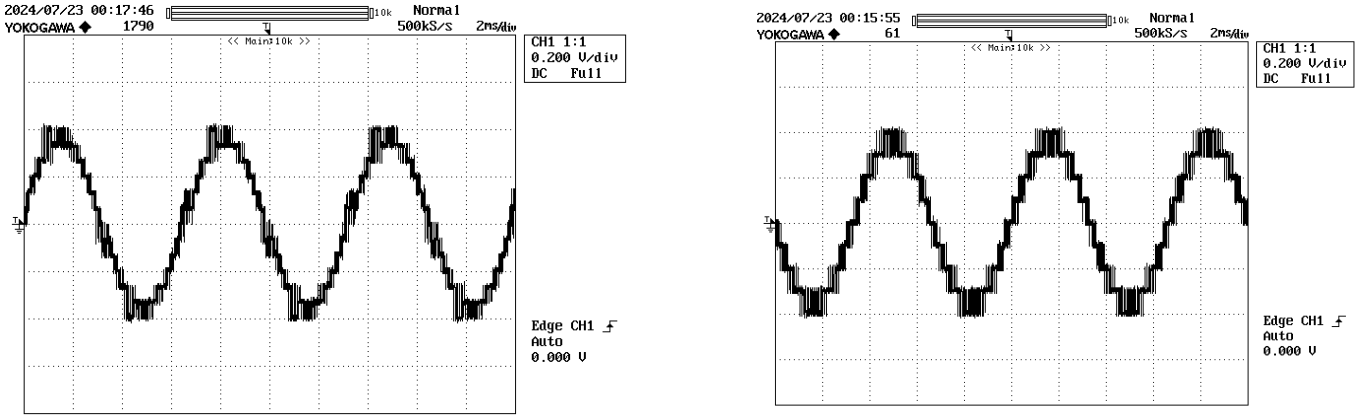


Figure 24. Temporal evolution of the real-time validation of three-phase stator voltages generated by: (**a**) 7-level ACHBMLI and (**b**) 5-level CHBMLI.

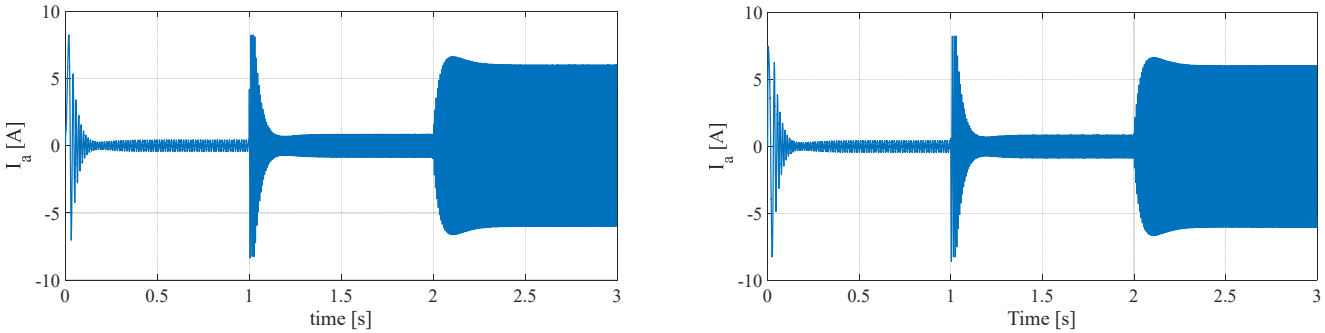
For example, in the first operating condition, both have an RMS value of 49.8 V. The same voltages previously described are zoomed and measured through the scope connected to an output pin from the HIL 404, with adequate voltage scaling to adapt the Typhoon output voltage to the ADC signals acquired from the PED microcontroller. As is evident, the asymmetrical inverter can generate line voltages with a greater number of levels. Figure 25a shows the same undesirable peaks caused by the activation of some power components of the ACHBMLI, as discussed in Section 4.

Further results are shown in Figure 26, which compares the time trends of the currents flowing in one of the three phases. As shown by the simulation results, the current behavior in the real-time validation is not affected by the type of inverter powering the IPMSM.



(**a**) (**b**)

Figure 25. Line-to-line voltage seen through the oscilloscope (**a**) generated by the 7-level ACHBMLI; (**b**) generated by the 5-level CHBMLI.



(**a**) (**b**)

Figure 26. Temporal evolution of three-phase stator currents: (**a**) 7-level HCHBMLI; (**b**) 5-level CHBMLI.

Other interesting results are shown in Figure 27, which reports an analysis regarding the THD% comparison between the line voltages and the output currents of the two converters for 20 different operating conditions in terms of reference speed and load applied to the drive.

The THD% values of the line voltage in the asymmetric converter are lower than its symmetric counterpart for all operating conditions in terms of load and speed. The higher values of THD% are caused by the low-frequency harmonics that are present in the voltage generated by the ACHBMLI, as mentioned in Section 4.

On the other hand, the THD% values referred to the current are much more comparable between ACHBMLI and CHBMLI. It can be highlighted that the advantage of applying AMLI is more evident for low-speed conditions, as lower THD% are achieved. However, for speed or load conditions close to the rated values, higher THD_I% is detected, including low-order harmonics that could affect the motor performance in terms of torque ripple, leading to vibrations and disturbances. This fact can negatively impact the adoption of such a system in certain automotive applications.

Figure 28 compares the efficiency of the seven-level ACHBMLI and the five-level CHBMLI. Generally, the efficiency increases with an increase in speed and resistant torque;

but, overall, the efficiency of the asymmetric converter is, though still comparable, lower than that of its symmetric counterpart.

The efficiency of the asymmetric converter is lower because, even though the total voltage of the DC-links is the same (150 V) and the same current flows through them, the ACHBMLI experiences higher losses. This is because, to obtain a voltage wave with a higher number of levels, the *HBa* must switch at a higher frequency, which significantly increases the switching losses.

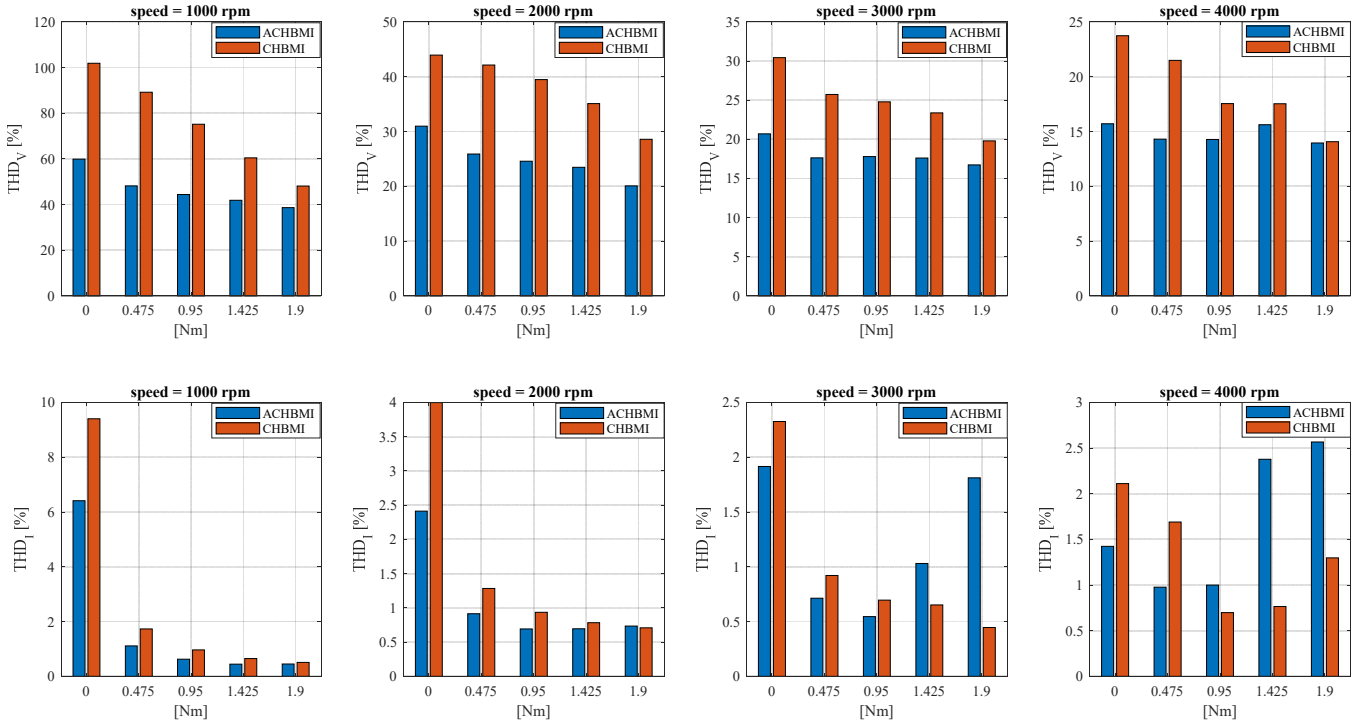


Figure 27. Comparison of THD under several working operations.

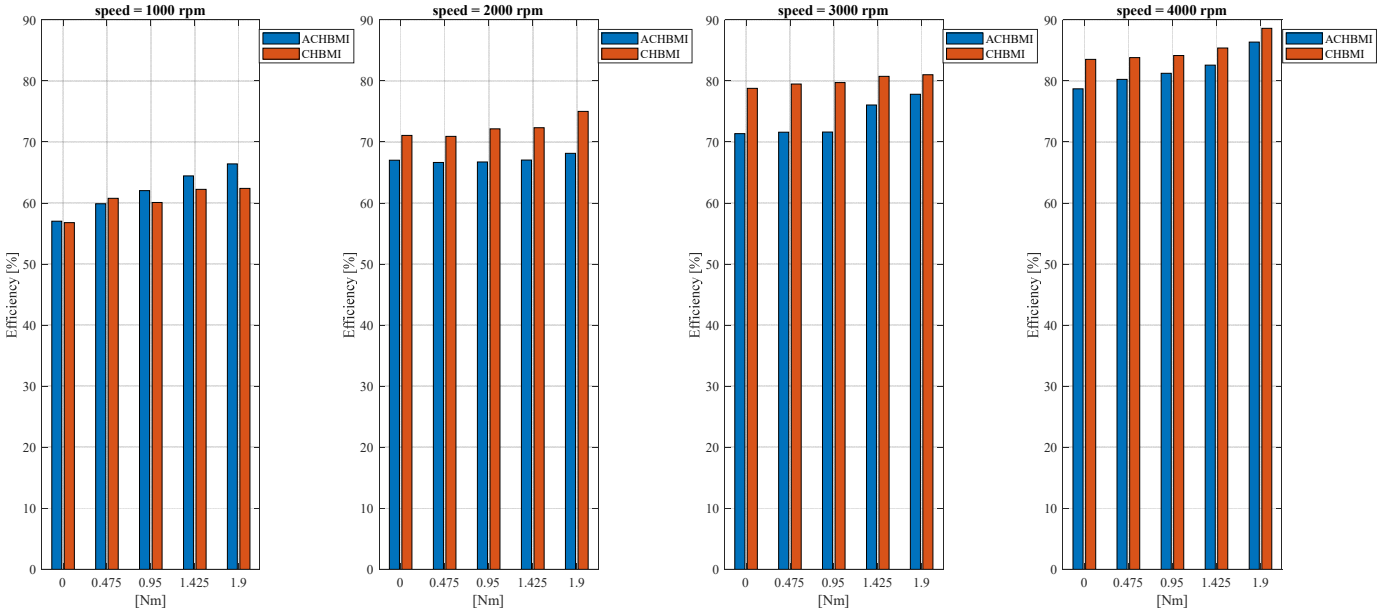


Figure 28. Comparison of efficiency under several working operations.

In conclusion, the real-time analysis of the two drives was conducted through the study of the dynamic performance of the electric drive, the THD of voltage and current, and the efficiency of both power converters. The following aspects can be highlighted:

- By analyzing the dynamic behavior of the system in terms of motor speed, it can be confirmed that the ACHBMLI has a good dynamic response, as well as a symmetrical configuration.
- The seven-level ACHBMLI and the five-level CHBMLI have the same number of components, but the asymmetric inverter, due to the different voltage values of DC sources, can generate output voltage with more levels. Therefore the THD_V% of ACHBMLI is lower than that of CHBMLI. This aspect highlights that a lower harmonic content reduces the iron losses in an electric motor; therefore, the IPMSM powered by the seven-level ACHBMLI will result in fewer iron losses compared to the same motor powered by the five-level ACHBMLI.
- For low values of speed and torque, the asymmetric inverter has greater performance regarding the THD% values; but, as the load torque increases, the THD_I% becomes greater than the values of the traditional inverter. This is mainly due to the low-frequency harmonics generated by the asymmetric converter, which is shown in Figure 13b. The electric motor behaves as a low-pass filter and, as a consequence, is unable to filter out these harmonics.
- As shown in Figure 27, in general, the symmetric converter exhibits better efficiency, except at 1000 rpm, where the asymmetric converter performs better. However, under all operating conditions, the efficiency of both converters remains comparable.

It can be stated that the results obtained through the proposed real-time validation confirm the feasibility of multilevel asymmetrical power converters for electrical drive applications. Based on the drawn conclusions, even though the ACHBMLI demonstrates excellent dynamic performance, it outperforms its symmetric counterpart when the drive operates at low speeds.

7. Conclusions

This paper has presented a performance comparison of IPMSM drives powered by symmetrical and asymmetrical multilevel power converters. This study was conducted through simulations in the MATLAB/Simulink® R2024a environment and real-time validation, discussing the dynamic performance and the harmonic content in both the voltage and current waveforms of the electric motor. The results have shown that ACHBMLI drives do not affect either the transient or the steady-state behavior of the system, allowing the achievement of similar performance. On the other hand, IPMSM drives fed by asymmetrical inverters can be affected by a slightly higher harmonic content, which is, in any case, acceptable for all the examined possibilities in terms of the working operation of the drive. Finally, it was observed that the percentage of power absorbed by each of the H-bridges varies for different operating conditions, depending on the number of levels of the generated voltage. Therefore, based on these results, it can be stated that the overall performance of the two systems is quite similar. AMLI drives can be a promising technology in many applications, such as automotive, where flexibility, reliability and simplicity are crucial elements during the design stage of the whole system. Finally, an in-depth investigation was conducted to compare the THD% of the three-phase five-level ACHBMLI and the three-phase five-level CHBMLI, revealing that the asymmetric converter in several AC drive operating conditions has a lower harmonic content of voltages, with comparable dynamic performances.

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