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Wide Bandgap Power Electronics A System-Level Approach to Efficiency and EMI

IL DOTTORE

Giuseppe Galioto

IL COORDINATORE

Prof. Marco La Cascia

I TUTOR

Prof. Giuseppe Costantino Giaconia

Prof. Antonino Sferlazza

Prof. Gianpaolo Vitale

Prof. Giuseppe Lullo

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Preface

This dissertation is submitted in fulfillment of the requirements for the degree of Doctor of Philosophy in Information and Communication Technologies at University of Palermo (Italy). The research presented herein was carried out between November 2022 and November 2025 under the supervision of Prof. Giuseppe Costantino Giaconia, within the Department of Engineering, in the Electronics Programmable Systems Laboratory (ESDPLAB). The research was co-supervised by prof. Antonino Sferlazza, prof. Gianpaolo Vitale and prof. Giuseppe Lullo.

Part of the activity was developed during the visiting period at the CNRS-LAAS in Toulouse (France), from January 2025 to July 2025, under the supervision of Prof. Corinne Alonso.

The primary focus of this thesis consists in assessing of the impact of employing high-switching frequency devices in power electronics converters in different use-cases. The motivation for this work stems from the ever increasing demand for high-efficiency, high-power density, lower volume and cost of power electronics modules.

The content of this thesis is based on original work conducted by the author. Portions of the research have been presented at conferences and/or published in peer-reviewed journals. A list of publications arising from this work is included at the end of the thesis.

Although the work is presented as a cohesive narrative, it has benefited greatly from the insights, collaboration, and support of numerous individuals and institutions. I gratefully acknowledge their contributions and provide detailed acknowledgments in the following section.

This thesis reflects my own work and has not been submitted previously, in whole or in part, for the award of any other degree or diploma.

Giuseppe Galioto
Palermo, April 2026

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Abstract

Wide bandgap (WBG) semiconductor devices, particularly gallium nitride (GaN) and silicon carbide (SiC), offer superior switching characteristics and enhanced power density compared to silicon devices. However, their integration into practical converter systems presents challenges including electromagnetic interference (EMI) generation, stringent gate driver requirements, and the need for co-design of power stages with magnetic components and control strategies. This dissertation addresses these challenges through a comprehensive system-level investigation of WBG devices in high-frequency power conversion applications, emphasizing efficiency optimization and EMI mitigation.

An embedded measurement platform was developed for precise characterization of GaN and SiC devices using equivalent-time sampling techniques, revealing frequency-dependent parameters including input capacitance variations and on-resistance degradation at elevated switching frequencies. Various converter topologies were systematically analyzed: synchronous buck converters at 1 MHz, two-phase interleaved configurations, dual active bridge (DAB) architectures for on-board chargers, and three-level active neutral point clamped (3L-ANPC) multilevel DAB converters for high-voltage operation. Advanced control strategies were developed, including average current mode control with triple phase-shift modulation, demonstrating robust performance across resistive, battery, and motor drive loads through hardware-in-the-loop validation.

Power density enhancement was pursued through coreless planar inductors on multilayer PCBs. Three-dimensional finite element analysis demonstrated compliance with conducted emission standards while achieving significant volume reduction. Experimental prototypes at 1 MHz validated the methodology, though thermal constraints limited high-power applications. EMI suppression strategies combined passive layout optimization with active compensation approaches. A novel double GaN half-bridge topology with series inductors achieved emission reduction, voltage ringing suppression, and zero-voltage switching.

Key contributions include validated behavioral models capturing frequency-dependent characteristics, design methodologies for coreless magnetics balancing power density and thermal performance, control strategies enabling wide-range soft-switching, and integrated EMI suppression techniques. Limitations include measurement bandwidth constraints, coreless inductor thermal boundaries, and experimental validation gaps for active EMI topologies. Future directions encompass experimental validation of active EMI filters, integration with battery management systems, UWBG device characterization, and development of autonomous multi-objective optimization frameworks. This dissertation advances WBG power electronics by bridging device-level characteristics with system-level performance, providing practical insights for next-generation high-efficiency, high-power-density converters in electric vehicles, renewable energy, data centers, and industrial applications.

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List of Symbols

A	cross-sectional area	m^2
$A_{CM}(f)$	common-mode attenuation	dB
$A_{DM}(f)$	differential-mode attenuation	dB
A_{loop}	loop area	mm^2
α_{cu}	temperature coefficient of copper	K^{-1}
B	magnetic flux density	T
c	speed of light	m s^{-1}
C	capacitance	F
C_{DM}	differential-mode capacitance	F
C_{DS}	drain-source capacitance	pF
C_{GD}	gate-drain capacitance	pF
C_{GS}	gate-source capacitance	pF
$C_i(s)$	current PI controller transfer function	–
C_{in}	input capacitance	μF
C_{iss}	input capacitance	pF
C_{oss}	output capacitance	pF
C_{out}	output capacitance	μF
C_{par}	parasitic capacitance	pF
$C_P(s)$	power PI controller transfer function	–
$C_v(s)$	voltage PI controller transfer function	–
D	duty cycle	–
D_1	primary bridge duty cycle	–
D_2	secondary bridge duty cycle	–
D_3	tertiary bridge duty cycle (3L-ANPC)	–
D_{eff}	effective duty cycle	–
di/dt	current slew rate	A ns^{-1}
dv/dt	voltage slew rate	V ns^{-1}
δ	skin depth	μm
ΔB	flux density swing	T
ΔI_L	inductor current ripple	A
ΔQ	charge variation	C
ΔT	temperature rise	K
ΔV_{out}	output voltage ripple	V
ΔV_{th}	threshold voltage variation	V
E_c	critical electric field	MV cm^{-1}
$E_{EMI}(f)$	EMI field strength	$\text{dB } \mu\text{V m}^{-1}$
E_g	bandgap energy	eV
E_{off}	turn-off energy loss	J
E_{on}	turn-on energy loss	J
E_{oss}	output capacitance energy	J

E_{sw}	total switching energy	J
ESR	equivalent series resistance	Ω
ϵ_r	relative permittivity	–
η	efficiency	%
η_{peak}	peak efficiency	%
f_{3dB}	3-dB bandwidth	Hz
f_{ring}	ringing frequency	MHz
f_s	switching frequency (alternate notation)	Hz
f_{sw}	switching frequency	Hz
$G_{v\phi}(s)$	control-to-output voltage transfer function	–
I_{bat}	battery current	A
$I_{bat,ref}$	reference battery current	A
I_{CM}	common-mode noise current	A
I_D	drain current	A
I_{DM}	differential-mode noise current	A
I_G	gate current	A
I_{gss}	gate leakage current	A
I_{in}	input current	A
$I_{L,avg}$	average inductor current	A
$I_{L,peak}$	peak inductor current	A
$I_{L,rms}$	RMS inductor current	A
i_{Ls}	series inductor current	A
I_{out}	output current	A
I_{ref}	reference current	A
k_B	Boltzmann's constant	J K^{-1}
$K_{i,i}$	current controller integral gain	–
$K_{i,v}$	voltage controller integral gain	–
$K_{p,i}$	current controller proportional gain	–
$K_{p,v}$	voltage controller proportional gain	–
κ	thermal conductivity	$\text{W cm}^{-1} \text{K}^{-1}$
l	conductor length	m
L	inductance	H
L_{comm}	commutation loop inductance	nH
L_{crit}	critical inductance for CCM	μH
L_{cs}	common source inductance	nH
L_{DM}	differential-mode inductance	H
L_g	gate inductance	nH
L_{loop}	loop inductance	nH
L_m	magnetizing inductance	μH
$L_{parasitic}$	parasitic inductance	nH
L_{PCB}	PCB trace inductance	nH
L_{pkg}	package inductance	nH
L_s	series inductance (DAB)	μH
μ_0	permeability of free space	H m^{-1}
μ_n	electron mobility	$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$
μ_r	relative permeability	–
n	transformer turns ratio	–
N	number of turns	–

P	power transfer	W
P_{cond}	conduction power loss	W
P_D	deadtime loss	W
P_G	gate charge loss	W
P_{IC}	IC control circuit loss	W
$P_{L,DCR}$	inductor DCR loss	W
P_{loss}	total power loss	W
P_{out}	output power	W
P_{ref}	reference power	W
P_{sw}	switching power loss	W
P_v	volumetric core loss	W m^{-3}
PUE	power usage effectiveness	–
Q	quality factor	–
Q_g	total gate charge	nC
Q_{rr}	reverse recovery charge	nC
R_{AC}	AC resistance	Ω
R_{DC}	DC resistance	Ω
$R_{DS,on}$	drain-source on-resistance	Ω
R_G	gate resistance	Ω
R_L	load resistance	Ω
$R_{on,sp}$	specific on-resistance	$\text{m}\Omega \text{ cm}^2$
R_{th}	thermal resistance	K W^{-1}
$R_{th,cs}$	case-to-sink thermal resistance	K W^{-1}
$R_{th,jc}$	junction-to-case thermal resistance	K W^{-1}
$R_{th,sa}$	sink-to-ambient thermal resistance	K W^{-1}
ρ_{cu}	copper resistivity	$\Omega \text{ m}$
s	trace spacing	mm
S_{11}	S-parameter (input reflection)	–
S_{12}, S_{21}, S_{22}	S-parameters	–
$SA(f)$	spectral amplitude	–
SOC	state of charge	%
SRF	self-resonant frequency	MHz
$t_{c(off)}$	turn-off delay time	ns
$t_{c(on)}$	turn-on delay time	ns
t_{cu}	copper thickness	mm
t_{dead}	dead time	ns
t_f	fall time	ns
T_j	junction temperature	$^{\circ}\text{C}$
$T_{j,max}$	maximum junction temperature	$^{\circ}\text{C}$
t_{off}	off-time duration	s
t_{on}	on-time duration	s
t_r	rise time	ns
T_s	switching period	s
THD	total harmonic distortion	%
τ	time constant	s
θ	temperature	$^{\circ}\text{C}$
u_i	current measurement uncertainty	A
V_1	primary bridge voltage	V

V_2	secondary bridge voltage	V
V_{bat}	battery voltage	V
V_{CM}	common-mode noise voltage	V
V_{DS}	drain-source voltage	V
V_{GS}	gate-source voltage	V
V_{in}	input voltage	V
v_{Ls}	series inductor voltage	V
V_{mag}	magnetic component volume	m ³
V_{nom}	nominal battery voltage	V
V_{out}	output voltage	V
$V_{overshoot}$	voltage overshoot	V
V_{ref}	reference voltage	V
v_{sat}	electron saturation velocity	cm s ⁻¹
V_{th}	threshold voltage	V
φ	phase shift angle	rad
w	trace width	mm
Z_0	characteristic impedance	Ω
Z_{11}	input impedance	Ω
Z_{CMC}	common-mode choke impedance	Ω

List of Acronyms

Acronym	Definition
2DEG	2-Dimensional Electron Gas
3L-ANPC	3-Level Active Neutral Point Clamped
AC	Alternating Current
AC-DC	Alternating Current to Direct Current
ADC	Analog-to-Digital Converter
AEC-Q101	Automotive Electronics Council Qualification
AEF	Active EMI Filter
AlGaN	Aluminum Gallium Nitride
AlN	Aluminum Nitride
ANPC	Active Neutral Point Clamped
BESS	Battery Energy Storage System
BFOM	Baliga's Figure of Merit
BHFFOM	Baliga's High-Frequency Figure of Merit
BOM	Bill Of Materials
c-BN	cubic Boron Nitride
CC	Constant Current
CC/CV	Constant Current/Constant Voltage
CCM	Continuous Conduction Mode
CEC	California Energy Commission
CHFFOM	Combined High-Frequency Figure of Merit
CISPR	Comité International Spécial des Perturbations Radioélectriques
CM	Common Mode
CMC	Common-Mode Choke
CMTI	Common-Mode Transient Immunity
CV	Constant Voltage
D-mode	Depletion mode
D2PAK	Double Decawatt PAKage
DAB	Dual Active Bridge
DC	Direct Current
DC-DC	Direct Current to Direct Current
DCM	Discontinuous Conduction Mode
DCR	DC Resistance
DFN	Dual Flat No-lead
DIP	Dual Inline Package
DM	Differential Mode
DMA	Direct Memory Access
DPC	Direct Plated Copper
DPS	Dual Phase-Shift
DPT	Double-Pulse Test

DSP	D igital S ignal P rocessor
DUT	D evice U nder T est
E-mode	E nhancement m ode
EMC	E lectromagnetic C ompatib l ity
EMI	E lectromagnetic I nterference
EPR	E xtended P ower R ange
EPS	E xtended P hase- S hift
ESR	E quivalent S eries R esistance
ETS	E quivalent T ime S ampling
EV	E lectric V ehicle
FCC	F ederal C ommunications C ommission
FEA	F inite E lement A nalysis
FEM	F inite E lement M ethod
FOM	F igure of M erit
FPGA	F ield- P rogrammable G ate A rray
FR-4	F lame R etardant grade 4 (PCB material)
FSM	F inite S tate M achine
Ga₂O₃	G allium O xide (Beta phase)
GaN	G allium N itride
GIT	G ate I njection T ransistor
GPIO	G eneral P urpose I nterface O utput
GSSA	G eneralized S tate- S pace A veraging
GTO	G ate T urn- O ff T hystistor
HAL	H ardware A bstract I on L ayer
HEMT	H igh- E lectron- M obility T ransistor
HFET	H eterojunction F ield- E ffect T ransistor
HFFOM	H igh- F requency F igure of M erit
HIL	H ardware- I n-the- L oop
HRTIM	H igh- R esolution T IME R esource
HVDC	H igh V oltage D irect C urrent
IBC	I nterleaved B uck C onverter
IC	I ntegrated C ircuit
IDM	I ntegrated D evice M anufacturer
IEC	I nternational E lectrotechnical C ommission
IEEE	I nstitute of E lectrical and E lectronics E ngineers
IGBT	I nsulated G ate B ipolar T ransistor
ISM	I ndustrial, S cientific and M edical (frequency band)
JEDEC	J oint E lectron D evice E ngineering C ouncil
JFOM	J ohnson's F igure of M erit
KFOM	K eyes' F igure of M erit
KPI	K ey P erformance I ndicator
LGA	L and G rid A rray
LLC	LLC R esonant C onverter (I nductor- I nductor- C apacitor)
LMS	L east M ean S quares
LUT	L ook- U p T able
LVRT	L ow V oltage R ide- T hrough
MCU	M icrocontroller U nit

MIL-STD	MILitary STandarD
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPC	Model Predictive Control
MVDC	Medium Voltage Direct Current
NPC	Neutral Point Clamped
OBC	On-Board Charger
PCB	Printed Circuit Board
PFC	Power Factor Correction
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PSU	Power Supply Unit
PV	Photovoltaic
PWL	Piecewise Linear
PWM	Pulse Width Modulation
QFN	Quad Flat No-lead
RCP	Rapid Control Prototyping
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RLS	Recursive Least Squares
RMS	Root Mean Square
S-parameter	Scattering parameter
SAR	Successive Approximation Register
SBC	Synchronous Buck Converter
SGT	Schottky Gate Transistor
Si	Silicon
SiC	Silicon Carbide
SiP	System in Package
SJ	Superjunction
SMA	Subminiature version A (connector)
SMD	Surface Mount Device
SoC	State of Charge
SOC	State Of Charge
SOIC	Small Outline Integrated Circuit
SPS	Single Phase-Shift
SRF	Self-Resonant Frequency
SSA	State-Space Averaging
SST	Solid-State Transformer
STATCOM	STATic Synchronous COMpensator
TFOM	Thermal Figure of Merit
TIM	Thermal Interface Material
TO-220	Transistor Outline 220
TO-247	Transistor Outline 247
TPS	Triple Phase-Shift
UPS	Uninterruptible Power Supply
USB-PD	Universal Serial Bus Power Delivery
UVLO	Under-Voltage Lock-Out

UWBG	U ltrawide B andgap
V2G	V ehicle-to- G rid
VFD	V ariable F requency D rive
VHF	V ery H igh F requency
VNA	V ector N etwork A nalyzer
VSI	V oltage S ource I nverter
WBG	W ide B andgap
ZCS	Z ero- C urrent S witching
ZVS	Z ero- V oltage S witching

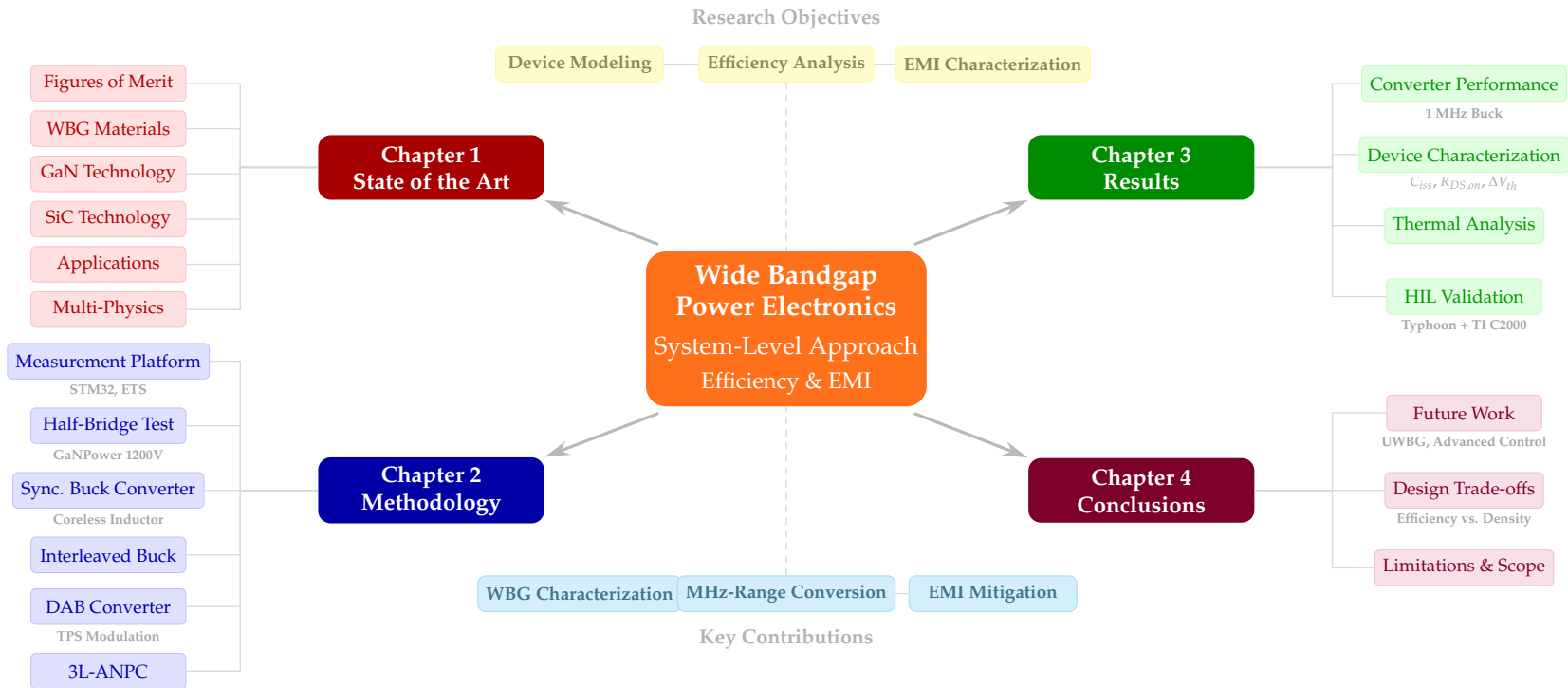


FIGURE 1: Conceptual map of the dissertation.

Research Sections → Publications Mapping

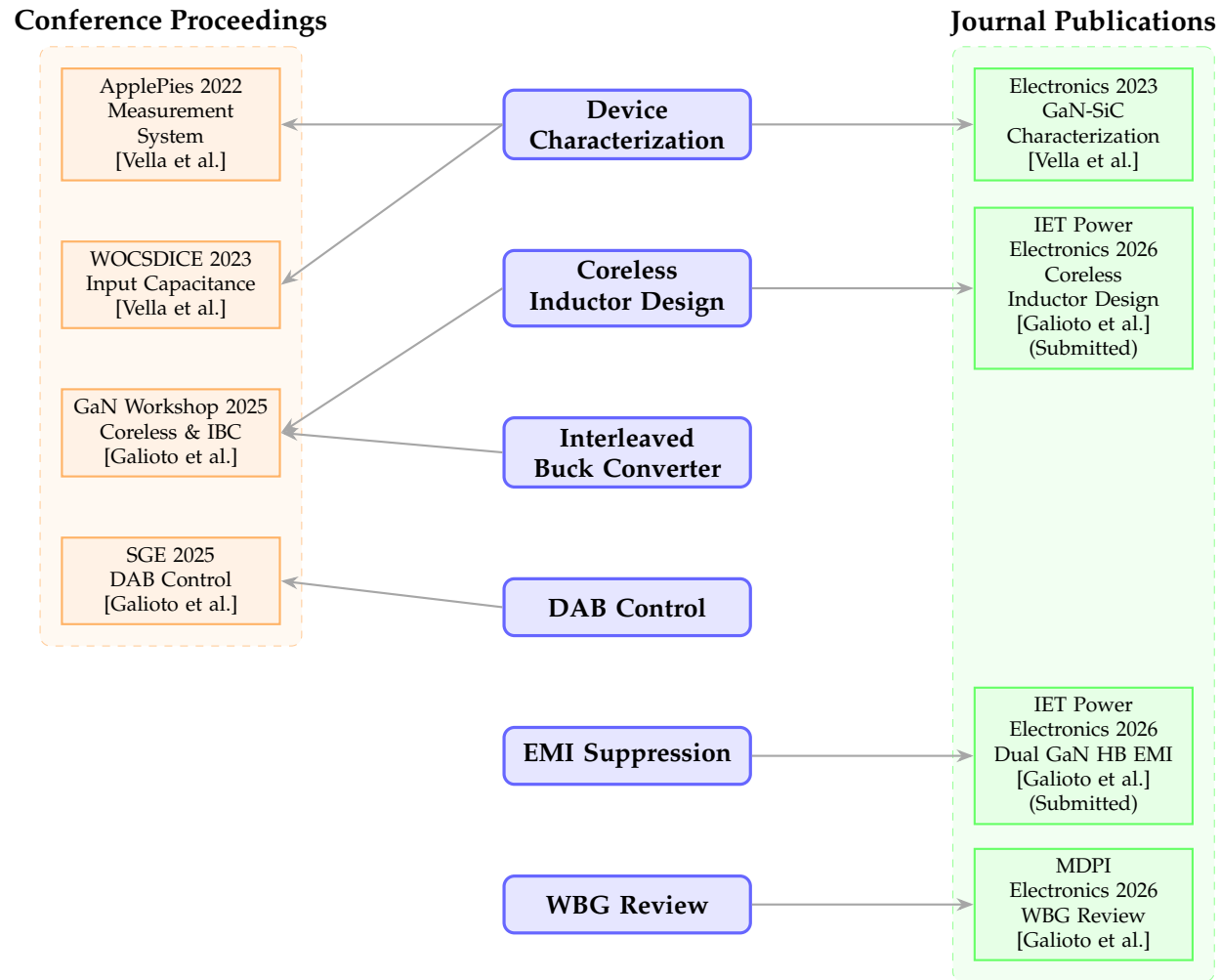


FIGURE 2: Conceptual map of thesis research sections and resulting publications.

Chapter 1

Introduction and state of the art

Chapter Overview

This chapter presents the research motivation, background, and the scope of WBG devices in different applications. Reviews current state-of-the-art in GaN and SiC devices, converter topologies, EMI challenges, and control strategies, highlighting gaps in system-level integration.

1.1 The Transition to Wide Bandgap Semiconductors

Nowadays, governments and industries increasingly require cleaner and more sustainable electrical energy utilization. The global power electronics sector is experiencing a significant transformation driven by demands for sustainable energy systems, improved operational efficiency, and lower carbon emissions. Central to this transformation is the shift from traditional silicon-based semiconductors to wide-bandgap (WBG) and ultrawide-bandgap (UWBG) materials, specifically Silicon Carbide (SiC) and Gallium Nitride (GaN). This transition constitutes a significant technological advancement that addresses several key challenges in contemporary power conversion systems. Compactness and efficiency become fundamental requirements for all power electronics components in applications such as industrial automation, space systems, automotive technology, consumer electronics, data centers and telecommunications.

The climate crisis has elevated energy efficiency to a global priority. In 2023, energy-related carbon dioxide CO₂ emissions reached 37.4 Gt, representing an increase of 410 Mt, or approximately 1.1% compared to 2022 [1]. Although the adoption of clean energy technologies such as solar power, wind energy, and electric vehicles has slowed the rate of emissions growth, these high emission levels indicate that incremental improvements are insufficient and substantial efficiency gains are essential. Power converters based on semiconductor switches regulate energy flow in nearly all electrical systems, including renewable energy installations, electric vehicles, industrial motor drives, and data centers. Incremental increases in converters efficiency can significantly reduce overall energy consumption and emissions.

Figure 1.1 shows the historical trend of global carbon dioxide emissions from energy and industrial sources (1970–2024), reproduced from Friedlingstein et al. [2]. It provides a visual overview to the urgency of reducing emissions growth.

This trend highlights the essential role of efficient and robust power conversion in shaping the performance, reliability, sustainability, and safety of modern electrical

and electronics systems and infrastructure. Enhancements at both the component and system levels contribute directly to measurable reductions in emissions.

Figure 1.2 illustrates the cascading benefits of improved power electronics efficiency across different application sectors, demonstrating how WBG technology contributes to overall system sustainability through environmental, economic, and technical improvements.

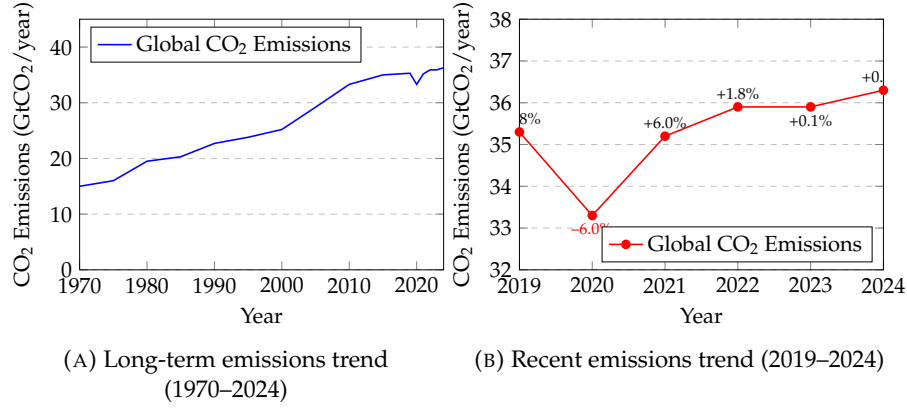


FIGURE 1.1: Global energy-related and industrial CO₂ emissions (1970–2024). (a) CO₂ Emissions over the last 54 years, (b) CO₂ Emissions in last 5 years showing year-over-year percentage changes. Data arranged from: Deng et al. [3].

Efficiency Improvements and System Benefits

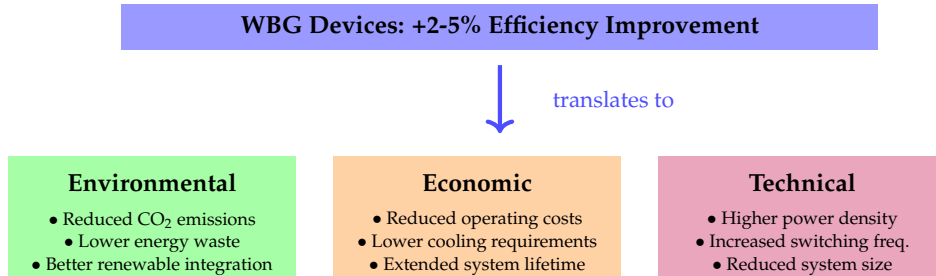


FIGURE 1.2: Key benefits of WBG technology across different application sectors

WBG devices enable significant efficiency improvements beyond traditional silicon due to their superior material properties. The intrinsic characteristics of WBG materials support operation at elevated temperatures, voltages, and frequencies, while minimizing switching and conduction losses relative to silicon-based devices. Enhanced efficiency reduces heat generation, enabling smaller cooling systems and more compact, lightweight designs. In electric vehicle inverter applications, incremental efficiency gains directly extend driving range and battery lifespan, thereby providing measurable environmental and economic advantages.

In addition to environmental benefits, the adoption of WBG devices is driven by significant economic incentives across various industries. In large-scale facilities such as data centers and industrial plants, continuous operation of power conversion systems means that even a one percent increase in efficiency can result in substantial annual energy savings. In the vehicle electrification framework, more

efficient inverters and chargers increase driving range and decrease battery degradation, thereby extending operational life and reducing total ownership costs. At the grid level, the widespread implementation of efficient power electronics reduces demand on generation capacity and transmission infrastructure, effectively providing additional capacity through loss reduction.

Table 1.1 quantifies the economic advantages of WBG adoption across different application sectors, illustrating the compelling return on investment despite higher initial device costs. WBG semiconductors, particularly SiC and GaN, represent a strategic solution for global sustainability and economic competitiveness, enabling revolutionary improvements in power conversion efficiency, power density, and thermal performance across critical applications from electric vehicles to renewable energy systems.

TABLE 1.1: Economic benefits of WBG device across application sectors

Sector	Application	η Gain	Savings	Payback
Data Centers	Server PSUs (10 MW)	94→97%	\$450k/yr [4], [5]	1.5 yrs
EV	Traction inverter	96→99%	+20 km range [6], [7]	Immediate
Solar PV	String inverter (1 MW)	96→98.5%	\$35k/yr [8], [9]	2 yrs
Industrial	VFD drive (500 kW)	95→98%	\$22k/yr [10], [11]	2.5 yrs
Telecom	5G base station	92→95%	\$8k/site/yr [12], [13], [14]	1.8 yrs
Aerospace	Aux. power unit	93→97%	−15 kg [15], [16]	Immediate

1.2 WBG and UWBG power semiconductor devices

WBG and ultrawide-bandgap (UWBG) materials have generated significant interest in the semiconductor device sector due to their large band gaps, which enhance device performance [17]. These material properties facilitate the development of durable and efficient devices for high-power, high-frequency, and extreme-environment applications.

WBG materials, including SiC and GaN, demonstrate versatility across optics, power electronics, and radio frequency (RF) technology. Their capacity to operate reliably in high-temperature and harsh environments has expanded their applications and market presence. Recent progress in WBG materials has stimulated further research into UWBG materials, which provide even larger band gaps.

WBG and UWBG materials exhibit high resistance to electric-field breakdown due to their wide band gaps, offering several advantages for electronic devices and systems. These benefits include increased efficiency, high-temperature operation, reduced device size and lower overall system costs. The advancement of these technologies may also help reduce carbon emissions.

GaN is widely used in lighting technology and has made significant contributions to radar, telecommunications, and power electronics. SiC is primarily utilized in medium- to high-power electronics and serves as a key substrate for GaN-based RF technology. SiC and GaN exhibit both cooperative and competitive dynamics, shaping current applications and influencing market trends. These developments have established WBG materials as foundational in technology and support ongoing research into UWBG materials.

Table 1.2 shows the different properties of WBG and UWBG materials, as reported in [18].

TABLE 1.2: Material properties of semiconductors for power electronics [18]

Parameter	Si	4H-SiC	GaN	β -Ga ₂ O ₃	AlN	c-BN	Diamond
E_g (eV)	1.12	3.23	3.4	4.9	6.2	6.4	5.5
E_c (MV/cm)	0.3	2.5	3.3	8	15	12	10
μ_n (cm ² /Vs)	1440	950	2000	250	850	200	4500
v_{sat} (10 ⁷ cm/s)	1	2	2.4	1.1	1.4	2.0	2.3
κ (W/cm·K)	1.5	3.7	2.5	0.1–0.3	2.85	13	23

TABLE 1.3: Symbol definitions and property explanations for Table 1.2

Symbol	Description
E_g	Bandgap energy: determines the energy required to excite an electron from the valence to the conduction band. Larger band gaps enable higher breakdown voltages and operation at higher temperatures.
E_c	Critical electric field: maximum electric field the material can sustain before breakdown. Higher values enable thinner drift regions and lower on-resistance for a given voltage rating.
μ_n	Electron mobility: measure of how quickly electrons move through the material under an electric field. Higher mobility reduces on-resistance and improves high-frequency performance.
v_{sat}	Electron saturation velocity: maximum drift velocity electrons achieve at high electric fields. Higher saturation velocity enables faster switching transitions.
κ	Thermal conductivity: ability to conduct heat away from active regions. Higher thermal conductivity improves power handling and reliability.

Figure 1.3 provides a comprehensive performance comparison between silicon and U/WBG devices across multiple key parameters.

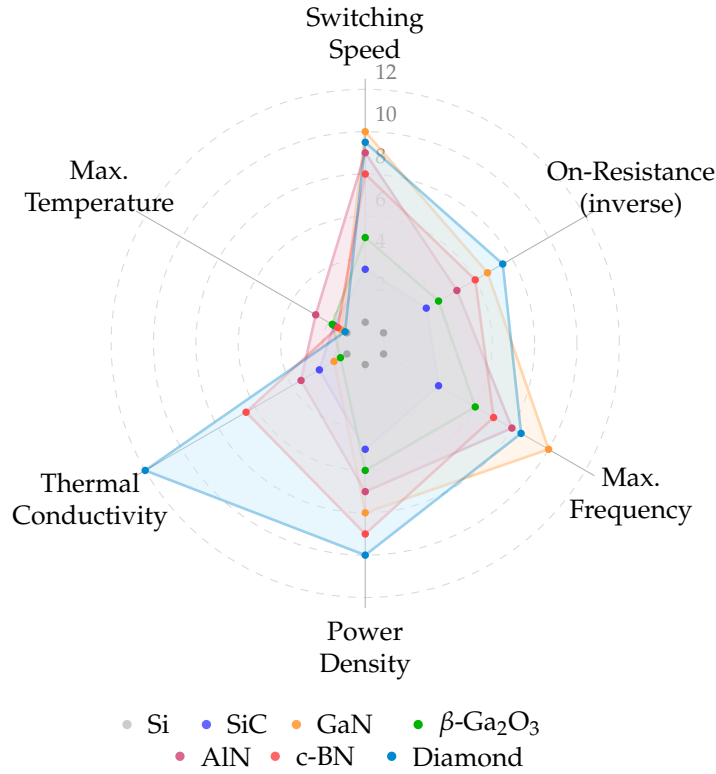


FIGURE 1.3: Radar chart comparison of power semiconductor materials. Normalized performance relative to Si (adapted from [17], [18]).

Quantitative device performance metrics

Several figures of merit (FOMs) have been developed to enable quantitative comparison of semiconductor technologies by integrating material properties into single metrics relevant to specific power electronic applications.

— Baliga's Figure of Merit

The most fundamental is Baliga's Figure of Merit (BFOM) [19], which characterizes the trade-off between on-resistance and breakdown voltage for unipolar power devices:

$$\text{BFOM} = \frac{\epsilon_r \mu_n E_c^3}{4} \quad (1.1)$$

where ϵ_r is the relative permittivity, μ_n is the electron mobility, and E_c is the critical electric field. This metric is particularly relevant for power-switching applications, where minimizing conduction losses is essential. The BFOM predicts the specific on-resistance ($R_{on,sp}$) achievable for a given breakdown voltage, with higher BFOM values indicating lower conduction losses.

— High-Frequency Figure of Merit

For high-frequency applications, where switching losses dominate, the High-Frequency Figure of Merit (HFFOM) [19] provides a more appropriate comparison:

$$\text{HFFOM} = \frac{\mu_n E_c^2}{2\pi} \quad (1.2)$$

The HFFOM accounts for both the switching speed (through mobility) and voltage-handling capability, making it particularly relevant for resonant converters and RF applications. This FOM is proportional to the product of electron velocity and breakdown field, indicating how quickly a device can switch at high voltages.

— **Johnson's Figure of Merit**

Johnson's Figure of Merit (JFOM) [20], originally developed for RF and microwave power applications, characterizes the maximum power-frequency product:

$$\text{JFOM} = \left(\frac{v_{sat} E_c}{2\pi} \right)^2 \quad (1.3)$$

where v_{sat} is the saturated electron drift velocity. The JFOM is particularly important for high-power RF amplifiers and oscillators, as it predicts the theoretical maximum frequency at which a device can deliver useful power. For power electronics applications involving high di/dt and dv/dt , the JFOM provides insight into transient performance capabilities.

— **Keyes' Figure of Merit**

Keyes' Figure of Merit (KFOM) [21] evaluates thermal management capabilities, which become increasingly critical as power densities increase:

$$\text{KFOM} = \frac{\lambda \cdot v_{sat}}{\epsilon_r} \quad (1.4)$$

Where λ is the thermal conductivity, this FOM combines electrical speed (through v_{sat}) with thermal dissipation capability, making it essential for assessing device reliability and maximum operating power density. Materials with high KFOM can operate at higher power densities without thermal runaway.

— **Combined High-Frequency Figure of Merit**

The Combined High-Frequency Figure of Merit (CHFFOM) [22] extends the HFFOM to include thermal effects:

$$\text{CHFFOM} = \frac{\lambda \mu_n E_c^2}{2\pi} \quad (1.5)$$

This metric is particularly valuable for evaluating materials in high-frequency, high-power-density applications where both switching performance and thermal management are critical constraints, such as in integrated power modules and multi-chip configurations.

— **Baliga's High-Frequency Figure of Merit**

Baliga's High-Frequency Figure of Merit (BHFFOM) [23], also known as the switching figure of merit, specifically addresses the gate charge-resistance product:

$$\text{BHFFOM} = \frac{\epsilon_r \mu_n^2 E_c^5}{4} \quad (1.6)$$

This FOM is crucial for assessing switching losses in hard-switching applications, as it accounts for both the on-state resistance and the charge required to switch the device. Lower gate charge, combined with low on-resistance (as predicted by high BHFFOM), minimizes switching losses and enables faster switching transitions.

— Thermal Figure of Merit

The Thermal Figure of Merit (TFOM) [24] specifically addresses heat dissipation capability:

$$\text{TFOM} = \frac{\lambda}{k_B T} \quad (1.7)$$

where k_B is Boltzmann's constant and T is absolute temperature. For practical comparisons, a simplified thermal FOM that normalizes thermal conductivity to that of silicon is often used, as shown in Table 1.4.

Table 1.4 presents normalized values of these figures of merit for various semiconductor materials, clearly illustrating the superior performance potential of WBG and UWBG materials across multiple performance dimensions.

TABLE 1.4: Normalized to Si figures of merit for power semiconductor materials. Data from [17], [18], [19], [20], [21], [22].

Material	BFOM	HFFOM	JFOM	KFOM	CHFFOM	BHFFOM	TFOM
Si	1	1	1	1	1	1	1
4H-SiC	317	13.7	20	4.8	29	5.6e2	3.3
GaN	846	27.5	33	1.4	56	3.8e3	2.2
Ga ₂ O ₃	3444	10.5	14	0.9	30	1.1e4	0.8
AlN	3360	57.6	68	13.8	562	2.3e4	9.2
Diamond	5.0e4	81.2	163	46.2	2114	7.4e5	33

WBG materials demonstrate significant performance advantages in these metrics. SiC exhibits a factor 300 improvement in the BFOM, while GaN achieves nearly an 850-x increase. Both materials also display greater enhancements in high-frequency performance metrics. The BHFFOM further highlights also these benefits with SiC and GaN. These results clarify the strong research and commercial focus on WBG technologies, particularly due to their pronounced switching-loss advantages compared to conduction-loss benefits.

The relative importance of different FOMs varies significantly across application domains:

- **Low-frequency power conversion (50-100 kHz):** BFOM dominates, favoring SiC for >1200V and GaN for <900V applications. Here, conduction losses typically exceed switching losses, making on-resistance minimization a primary concern.
- **High-frequency power conversion (200 kHz - 1 MHz):** HFFOM and BHFFOM become critical, strongly favoring GaN. The combination of low

gate charge and fast switching enables a dramatic reduction in total losses despite potentially higher conduction losses than SiC at equivalent voltage ratings.

- **Very high frequency (>1 MHz) and RF power:** JFOM becomes dominant, where GaN's superior electron velocity provides clear advantages. Applications include resonant wireless power transfer and RF amplifiers.
- **High-temperature operation (>175°C):** KFOM and TFOM are critical, where SiC's superior thermal properties (junction temperature rating of 200°C vs 150-175°C for GaN) provide system-level advantages despite potentially lower electrical FOMs in some metrics.
- **Extreme power density (>500 W/in³):** CHFFOM becomes essential, requiring optimization of both electrical and thermal performance.

It is important to note that these theoretical advantages must be realized through careful device design, optimized manufacturing processes, and system-level integration. The following subsection examines how these material-level advantages translate into practical system benefits.

System-level implications

The advanced material properties of WBG devices result in measurable improvements at the system level, including enhanced efficiency, reliability, and performance. Figure 1.4 illustrates the effects of WBG adoption throughout the power conversion system.

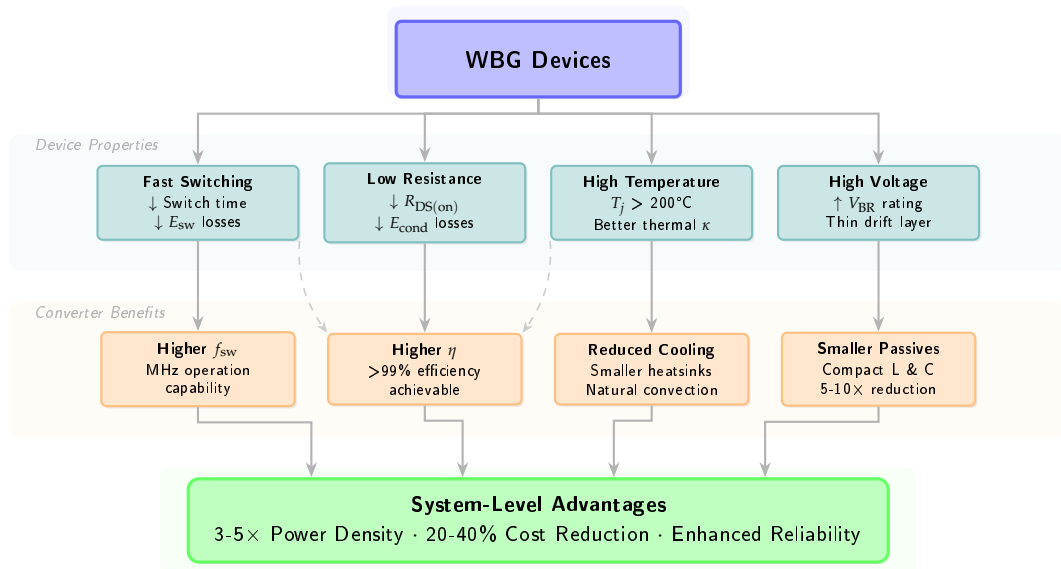


FIGURE 1.4: System-level benefits of WBG semiconductor adoption

The ability to operate at higher switching frequencies is particularly significant. Increasing switching frequency from typical silicon ranges of 20-50 kHz to 200-500 kHz, or even to MHz ranges, with GaN devices enables a proportional reduction in magnetic component size and weight. For a given power level, the volumes of the inductor and transformer scale approximately inversely with frequency, leading to dramatic system miniaturization. This relationship is captured by:

$$V_{mag} \propto \frac{P \cdot \Delta B}{f_{sw}} \quad (1.8)$$

where V_{mag} is the magnetic component volume, P is power, ΔB is the flux density swing, and f_{sw} is the switching frequency.

However, increased challenges in managing electromagnetic interference (EMI), gate drive design, and PCB layout must be afforded and investigated. The faster switching transitions that enable higher frequencies also generate more high-frequency noise and impose stricter requirements on parasitics control. As switching frequency increases beyond 500 kHz, core losses in magnetic materials can begin to offset volume reduction benefits, requiring careful magnetic material selection [25], [26]. Additionally, skin and proximity effects in windings become increasingly significant, often necessitating specialized construction techniques such as Litz wire or PCB-integrated magnetics.

The superior thermal performance indicated by the KFOM and TFOM metrics enables more aggressive thermal management strategies. SiC devices, with their ability to operate at junction temperatures up to 200°C (compared to 150°C for Si and 150-175°C for commercial GaN), can significantly reduce cooling system requirements. In automotive traction inverters, this has enabled 30-40% reduction in cooling system volume and elimination of liquid cooling in some cases [27], [28]. However, the lower thermal conductivity of GaN relative to SiC must be carefully managed in high-power-density applications through advanced packaging and thermal interface materials [29].

Reliability and practical constraints

While WBG devices offer compelling performance advantages, their successful deployment requires careful attention to reliability considerations and practical constraints. The relative immaturity of WBG manufacturing processes compared to silicon means that long-term reliability data is still being accumulated. Key reliability concerns include:

- **Dynamic on-resistance degradation:** Some GaN devices exhibit increases in on-resistance under specific operating conditions, particularly after blocking high voltages for extended periods [30].
- **Threshold voltage instability:** Both SiC and GaN devices can experience shifts in threshold voltage due to charge trapping effects, potentially affecting switching behavior and requiring compensation in gate drive design [31].
- **Thermal management:** Despite superior thermal properties, the higher power densities achievable with WBG devices can actually increase thermal management challenges. Hotspot temperatures may be more severe due to the concentrated power dissipation in smaller device areas.
- **Manufacturing yield and cost:** WBG wafer manufacturing remains more expensive than silicon, with substrate costs and lower yields contributing to higher device prices, though these gaps are steadily narrowing.

Understanding and mitigating these reliability concerns through proper characterization, device selection, and circuit design is essential for successful WBG implementation, as will be discussed in subsequent sections of this chapter.

Representative KPIs

To comprehensively evaluate and compare power electronic systems, several key performance indicators (KPIs) are used. Table 1.5 summarizes the most critical metrics and their typical values for silicon versus WBG-based systems [32].

TABLE 1.5: Key performance indicators: Si vs. WBG comparison [32]

KPI	Description	Si	WBG
η_{peak}	Maximum conversion efficiency	94–97%	98–99.5%
Power Density	Power per unit volume	3–8 kW/L	15–50 kW/L
Specific Power	Power-to-weight ratio	2–5 kW/kg	8–20 kW/kg
f_{sw}	Switching frequency	20–100 kHz	0.2–2 MHz
$T_{j,\text{max}}$	Maximum junction temperature	150°C	175–200°C
THD	Total harmonic distortion	3–8%	1–3%
dv/dt	Voltage slew rate	5–15 kV/ μs	50–200 kV/ μs
di/dt	Current slew rate	1–5 kA/ μs	10–50 kA/ μs

These KPIs must be considered holistically rather than individually, as optimizing one parameter often involves trade-offs with others. For instance, maximizing switching frequency improves power density but may compromise EMI performance and efficiency if not properly managed.

1.3 WBG devices: SiC and GaN

The commercial landscape of WBG semiconductors has matured significantly, with SiC and GaN devices now available from numerous manufacturers worldwide. The distinct characteristics of these two materials have led to natural market segmentation, with SiC dominating higher-voltage applications (>1200V) and GaN excelling in medium-voltage (200-900V) high-frequency applications.

Applications of WBG Semiconductors in Power Electronics

The superior properties of WBG semiconductors have enabled their deployment across an increasingly diverse range of power electronics applications. Figure 1.5 summarizes the primary application domains for SiC and GaN devices, along with typical voltage and power levels.

— Automotive and Transportation Applications

SiC transistors are widely implemented in traction inverters for hybrid and electric vehicles—Tesla, for instance, has utilized SiC technology since 2017, achieving 5-8% improvement in vehicle range through increased inverter efficiency [27], [33]. The transition from Si IGBTs to SiC MOSFETs in automotive applications has been driven by multiple factors: reduced cooling system requirements (enabling 30-40% reduction in radiator volume), increased power density (allowing more compact inverter designs), and improved cold-weather performance due to lower conduction losses [28], [34].

Beyond traction inverters, SiC devices are also used, though to a lesser extent, in on-board chargers (OBCs) and DC-DC converters for high-performance vehicles. In OBC applications, SiC enables bidirectional power flow with

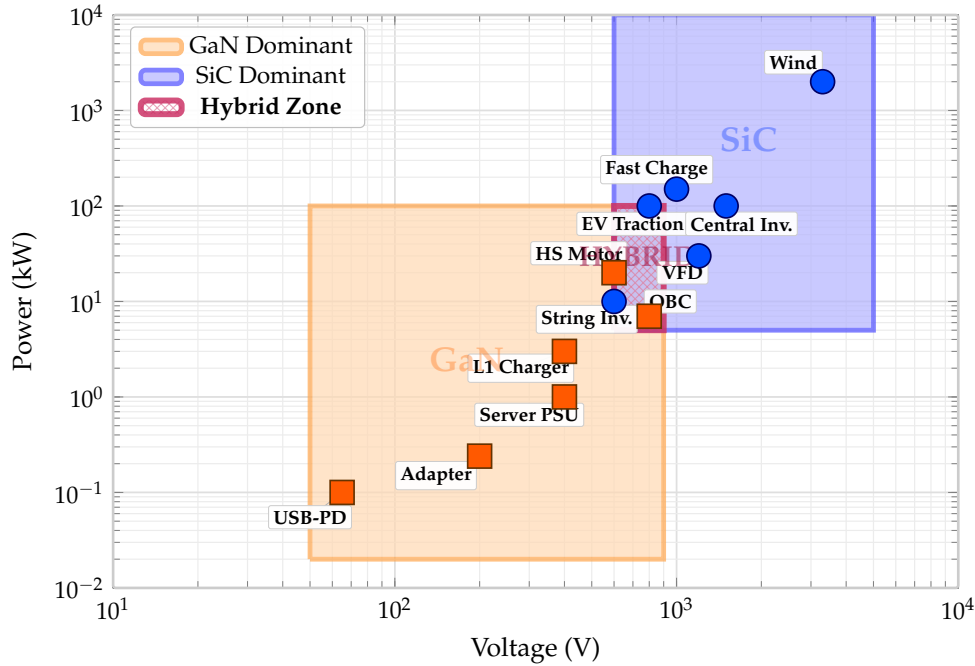


FIGURE 1.5: Application landscape for WBG power devices.

efficiencies exceeding 96% across the entire power range, facilitating vehicle-to-grid (V2G) integration [35], [36]. However, GaN devices are increasingly competing with SiC in lower-power OBC segments (typically below 11 kW) and DC-DC converter applications, where their superior switching speed and lower gate charge offer advantages in high-frequency operation [37]. GaN becomes particularly preferable over SiC in:

- **Low-to-medium power OBCs** (3.3–11 kW): GaN's lower switching losses at frequencies above 100 kHz enable higher power density and reduced passive component size, while maintaining competitive costs at these power levels [38].
- **Isolated DC-DC converters** (400 V to 12/48 V): GaN's fast switching enables resonant and quasi-resonant topologies with switching frequencies exceeding 500 kHz, significantly reducing magnetic component volume [39].
- **Cost-sensitive applications**: At power levels below 10 kW, GaN offers a favorable cost-performance trade-off compared to SiC, particularly when system-level benefits (smaller magnetics, reduced cooling) are considered [40].

The coexistence of GaN and SiC in automotive power electronics reflects a power-level segmentation: SiC dominates high-power traction inverters (>100 kW) and fast charging (>50 kW), while GaN finds its niche in auxiliary power systems where high frequency and compactness are prioritized over absolute voltage blocking capability. Table 1.6 summarizes the adoption of WBG devices in electric vehicle applications by major manufacturers [41], [42].

TABLE 1.6: WBG Device Adoption in Electric Vehicle Applications [41], [42]

Manufacturer	Model	Tech.	Application	Performance Gain	Year
Tesla	Model 3/Y	SiC	Traction inverter	+8% range	2017
BYD	Han EV	SiC	Traction + OBC	+5% efficiency	2020
Lucid	Air	SiC	900V inverter	+10% range	2021
Hyundai	IONIQ 5	SiC	800V charging	18 min charge	2021
Mercedes	EQS	SiC	Traction inverter	+6% range	2022
BMW	iX	GaN	OBC	40% size reduction	2022
Porsche	Taycan	SiC	800V system	270kW charging	2019
Volkswagen	ID.7	SiC	APP310 inverter	+5% efficiency	2023

— Consumer Electronics and Power Delivery

GaN transistors, in contrast, are more commonly used in power supplies and chargers for consumer electronics like smartphones and laptops. Thanks to their ability to operate at switching frequencies exceeding 1 MHz [43], [44], GaN enables the development of more compact and powerful chargers—up to three times smaller than traditional Si-based AC–DC converters. The high-frequency operation allows for a significant reduction in passive component size: at 1 MHz, inductors and capacitors can be reduced to 10-20% of their 100 kHz equivalents [45].

GaN devices are also increasingly used in premium photovoltaic (PV) inverters where efficiency improvements of 0.5-1% translate to significant lifetime energy gains. For a typical 5 kW residential system, a 1% efficiency improvement yields approximately 400-500 kWh additional energy annually, corresponding to €50-80 in extra revenue over a 25-year lifetime [46]. Recent developments include multi-level topologies (NPC, T-type, ANPC) that leverage GaN’s fast switching to achieve peak efficiencies of 99.2% in the 5-20 kW range [47].

Voltage-Dependent Application Segmentation

As the costs of SiC and GaN devices continue to decrease (approximately 20% year-over-year for the past 5 years) and their maximum operating voltages improve, WBG semiconductors are expected to find use in a broader range of applications [48]. The manufacturing maturity of WBG technologies has improved substantially, with 150 mm (6-inch) SiC wafers becoming standard and 200 mm (8-inch) wafers entering production in 2023-2024 [49]. Figure 1.6 illustrates the voltage-dependent application segmentation for WBG devices.

Low-Voltage Domain (< 400 V)

GaN is anticipated to become the dominant technology with market share projections exceeding 60% by 2028 [50]. This voltage range covers the upper limit of standard residential power supplies (both single-phase and three-phase). It includes common domestic appliances, consumer electronics, their chargers, and power systems in data centers. The sub-400V segment represents approximately 40% of the total power electronics market by revenue, making it a critical section for WBG adoption.

Recent developments in integrated GaN solutions have enabled single-chip power converters with integrated drivers and protection circuits, further

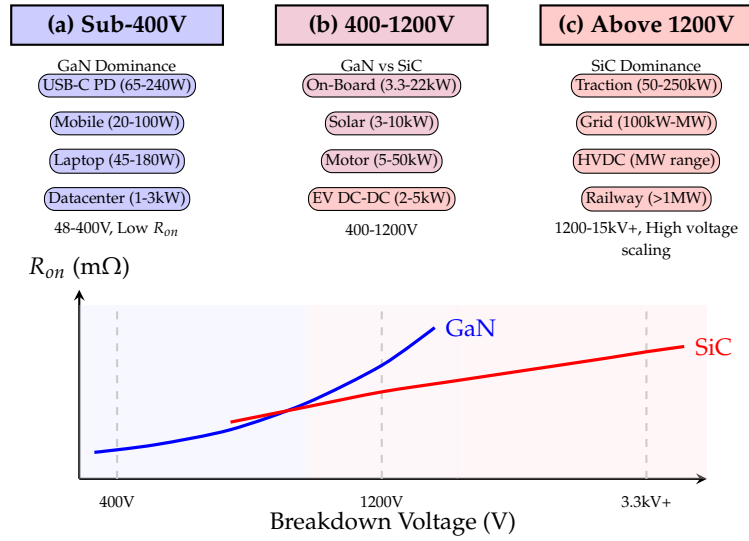


FIGURE 1.6: Voltage-dependent application segmentation for WBG devices

accelerating adoption in this segment. Monolithic integration of GaN power devices with gate drivers on a single chip reduces parasitic inductances to below 200 pH, enabling switching frequencies beyond 10 MHz with minimal overshoot [51]. Key application areas include:

- **Server and datacenter power supplies:** GaN-based power supplies achieve 98% efficiency at intermediate loads (40-60% of rated power), significantly improving energy usage effectiveness (PUE) metrics. Google and Meta have reported 2-3% improvement in datacenter PUE through widespread adoption of GaN PSUs [52], [53].
- **Fast charging infrastructure:** USB Power Delivery (PD) 3.1 extended power range (EPR) enables up to 240W delivery over USB-C cables, with GaN enabling compact, efficient chargers for laptops, tablets, and multi-device charging stations [54].
- **Motor drives for appliances:** Variable-speed motor drives using GaN achieve > 95% efficiency in washing machines, HVAC systems, and power tools, with 50-60% volume reduction compared to Si alternatives [55].
- **Wireless power transfer:** High-frequency GaN enables efficient resonant converters for inductive and capacitive wireless charging systems operating at 6.78 MHz and 13.56 MHz ISM bands [56].

Medium-Voltage Domain (400–1200 V)

In this mid-voltage range, both GaN and SiC are expected to be used side-by-side, depending on the power demands and switching frequency requirements of specific applications [57], [58]. This category includes inverters for renewable energy systems (achieving 99% peak efficiency), industrial motor drives (enabling variable-frequency drives up to 100 kHz), and various automotive applications.

The 400-1200V segment exhibits the most intense competition between GaN and SiC technologies, with the optimal choice depending on multiple factors:

- **Power level:** GaN typically dominates below 10 kW, while SiC shows advantages above 20 kW due to larger die sizes and better current-handling capabilities [59].
- **Switching frequency:** Applications requiring > 500 kHz favor GaN due to lower switching losses and reduced electromagnetic compatibility (EMC) filter requirements, while lower-frequency applications (< 100 kHz) show minimal benefit from GaN over SiC [60].
- **Thermal constraints:** SiC's higher operating temperature capability (175°C vs 150°C for GaN) provides advantages in thermally-constrained applications with limited cooling [17].

The automotive sector, in particular, is a key area for both technologies, driven by the growing push for electric and hybrid vehicles. The emergence of 800V and 900V automotive architectures has accelerated WBG adoption, with 800V systems enabling 350 kW charging (providing 100 km range in 3-5 minutes) and reducing cabling weight by 40-50% [61], [62]. Industrial applications include:

- **Solar inverters:** Three-phase string inverters (3-10 kW) and central inverters (100 kW - 1 MW) achieving California Energy Commission (CEC) weighted efficiencies of 98.5- 99.0% [63].
- **Energy storage systems:** Bidirectional DC-AC converters for battery energy storage systems (BESS) with power ratings from 10 kW (residential) to 1 MW (utility-scale) [64].
- **Industrial motor drives:** Variable frequency drives (VFDs) for pumps, fans, and compressors with power ratings up to 500 kW, where increased switching frequency enables acoustic noise reduction and improved torque ripple performance [65].
- **Uninterruptible power supplies (UPS):** Three-phase UPS systems (10-100 kW) achieving 97-98% efficiency in double-conversion topology, reducing cooling requirements and improving reliability [66].

High-Voltage Domain (> 1200 V)

SiC is supposed to take the lead in high-voltage applications, with commercial devices now available up to 3.3 kV and 6.5 kV devices in development [67], [68]. Research prototypes of 10 kV and 15 kV SiC devices have been demonstrated, opening the possibility of medium-voltage direct current (MVDC) power distribution [69]. Applications include:

- **Electric railway traction:** Electric train propulsion (reducing system weight by 30-40%) operating at 1.5 kV DC (light rail), 3 kV DC (regional trains), and 15-25 kV AC (high-speed rail) [70], [71]. For electric trains, which often operate at voltages up to 5 kV, SiC is nearing readiness to replace existing silicon solutions (mainly GTOs and IGBTs), offering better performance and efficiency. Japanese Railway companies have demonstrated SiC-based traction systems achieving 40% reduction in inverter volume and 50% reduction in cooling system size [72].

- **Wind power systems:** Medium-voltage converters (2-5 MW) for wind turbines improving capacity factor by 2-3% through reduced losses and enhanced low-voltage ride-through (LVRT) capabilities [73], [74]. The ability to operate at higher junction temperatures minimizes the complexity of the cooling system in offshore installations where maintenance access is limited.
- **Grid infrastructure:** HVDC transmission systems, STATCOM (Static Synchronous Compensator), and solid-state transformers (SST) for smart grid applications [75], [76]. SiC-based modular multilevel converters (MMC) have demonstrated significant advantages in HVDC applications, with first commercial installations in 2022-2023 [77].
- **Medium-voltage motor drives:** Industrial applications requiring 2.3 kV, 3.3 kV, or 4.16 kV motor drives for large pumps, compressors, and fans in oil & gas, mining, and petrochemical industries [78].

Manufacturer	Tech	Applications	Key Features & Challenges
BelGaN	GaN	Consumer, Ind., Auto	Europe's leading auto-qualified foundry; reliability focus.
Cambridge GaN Dev.	GaN	General Power	E-mode ICeGaN; std driver compatible; higher cost.
EPC	GaN	Enterprise, Solar, Auto	High power density; thermal mgmt challenge.
Innoscence	GaN	Consumer, DC, Solar	World's largest GaN IDM; 8" wafer; low-cost, high-vol.
Odyssey Semi.	GaN	EV, Ind. Motors, Grid	Vertical GaN >1kV; reliability & multi-fab challenges.
Tagore Tech.	GaN	RF, Power Mgmt	Fabless GaN-on-Si; export restrictions & pricing pressures.
VisiC Tech.	GaN	EV Drivetrain Inv.	D3GaN (d-mode); robust vs. gate ringing.
Wise Integration	GaN	Chargers, Data Mgmt	Digital controller (WiseWare); analog limited >500kHz.
Leapers Semi.	SiC	EV, Industrial	High-reliability modules; same pkg for IGBT & SiC.
Microchip Tech.	SiC	e-Mobility, Utility	Lower system cost vs. higher device cost; engineer shortage.
onsemi	SiC	Auto, Ind., Sustainable	Reliability & cost focus; 200mm wafer challenge.
Qorvo	SiC	Ind., DC, EV	650-1200V FETs; efficiency & density; EMI & layout risks.
Semikron Danfoss	SiC	Auto, Ind., Renewable	Power module specialist; SiC limited by fab capacity.
WeEn Semi.	SiC	PV, Storage, EV, Supplies	Addresses high cost; limited surge capability.
Infineon	Both	Auto, Ind., Consumer	Broad Si/SiC/GaN portfolio; strong patents; system cost analysis.
Nexperia	Both	Power Mgmt, Auto, Ind.	WBG cost focus; complex supply chain.
Texas Instr.	Both	General Power	Integrated drivers; reduces BOM cost vs. higher FET price.
X-Fab	Both	Auto, Ind., Medical	Specialty foundry; WBG needs a full system redesign.
Power Integrations	Both	Supplies, Mobile, EV	SiP (InnoSwitch); GaN @400V, SiC @1.7kV.
Navitas Semi.	Both	EV, Solar, DC	GaNFast ICs & GeneSiC; enables advanced topologies.
Renesas	Both	Auto, Renewable, Ind.	High-density SiC; acq. Transphorm '24; capacity planning.
Rohm Semi.	Both	EV, RF, Ind. Power	Broad portfolio; GaN gate-drive & layout; SiC vs. IGBT cost.
STMicro	Both	Auto, Renewable	Leading IDM; efficiency, high-temp, compact; limited capacity.
Wolfspeed	Both	EV, 5G, Renewable, Aero	Vertical integration; \$6.5B 200mm SiC fab; efficiency gains.

TABLE 1.7: WBG Manufacturers , data taken from [79]

Wide Bandgap Market Analysis

The WBG semiconductor market has experienced exponential growth, driven by electrification trends, renewable energy deployment, and efficiency regulations. Understanding the commercial landscape requires examination of both established players and emerging companies across the value chain.

Table 1.7 provides a comprehensive overview of major manufacturers in the SiC and GaN markets, highlighting their focus areas, key technologies, and strategic challenges.

1.4 Gallium Nitride technology

Among WBG materials, GaN has gained significant traction in recent years due to its exceptional properties and potential for revolutionizing power electronics [80]. GaN technology offers several advantages over both silicon and SiC, particularly in medium voltage (600V-1200V) applications. Key features of GaN technology include:

- **Higher electron mobility:** GaN exhibits electron mobility up to $2000 \text{ cm}^2/\text{V}\cdot\text{s}$, significantly higher than that of silicon or SiC, enabling faster switching and lower on-resistance [81].
- **Higher critical electric field:** GaN can withstand electric fields up to 3.3 MV/cm , allowing for the design of more compact and efficient devices with thinner drift regions.
- **Lower parasitic capacitance:** GaN devices typically have lower input and output capacitances, contributing to faster switching speeds and reduced switching losses.
- **Ability to form heterojunctions:** The unique ability to create heterojunctions between GaN and AlGaN layers enables the development of high-electron-mobility transistors (HEMTs) with exceptional performance characteristics.
- **Lateral device structure:** Unlike vertical SiC MOSFETs, GaN HEMTs employ lateral structures that simplify fabrication and enable monolithic integration.
- **Emerging vertical structures:** Recent developments by manufacturers such as onsemi, Odyssey Semiconductor, and NexGen Power Systems have introduced vertical GaN devices that combine the advantages of GaN material properties with the scalability and high-voltage capability of vertical architectures.

GaN HEMTs

GaN has long been recognized as a promising material for power semiconductor devices. However, its practical applications were historically constrained by the requirement for rare and costly substrate materials. Recent global research initiatives have enabled the fabrication of reliable GaN transistors on affordable silicon substrates, which is essential for their commercial viability.

GaN supports higher electric fields, which allows for the design of significantly smaller switching devices compared to silicon-based counterparts. This

characteristic is especially advantageous in high-voltage applications, defined as 600 V and above, because the terminal capacitances of GaN and Si-based devices of similar ratings typically differ by nearly an order of magnitude.

Generally, the GaN HEMT is a planar device with lateral current flow, contrasting with Si superjunction (SJ) MOSFETs and their predominantly vertical current flow. The fabrication begins with a Si substrate, chosen for its mature supply infrastructure and low cost. Transition layers are epitaxially grown onto the Si substrate to improve crystal lattice matching between Si and GaN, followed by additional layers of GaN, AlGaN, and p-doped GaN, with subsequent metallization and passivation layers. The transistor channel forms at the highly conductive GaN/AlGaN interface where the 2DEG exists, controlled via gate voltage. Since the distance between drain and gate essentially determines the drain-to-source breakdown voltage, the typical device cross-section is asymmetric. Nevertheless, the device also operates in reverse—when the drain potential falls below the source potential, the drain and source effectively exchange roles. Thus, even when the gate-to-drain voltage reaches the threshold level, the 2DEG forms a continuous channel and the switch conducts in the reverse direction. Unlike Si MOSFETs, a physical body diode does not exist in GaN HEMTs.

A critical feature of GaN switches is their implementation as heterojunction high-electron-mobility transistors (HEMTs). In these devices, the conducting channel forms at the aluminum gallium nitride/gallium nitride (AlGaN/GaN) interface through the presence of a highly conductive two-dimensional electron gas (2DEG) [81]. Consequently, typical GaN transistors are lateral devices that lack physical p-n junctions. This structural distinction allows GaN transistors to function both as power transistors and as diodes, enabling channel current conduction in the reverse direction.

GaN Power Devices: Classifications and Operation

Depletion-Mode (D-mode) and Enhancement-Mode (E-mode) form the two broad categories of lateral HEMT devices. More recently, there has been a growing interest in vertical GaN devices for high-voltage (>900V) applications. Figure 1.7 shows a representation of these three device categories.

The depletion-mode GaN transistor comprises three main electrodes: gate, source, and drain. In its structure, both source and drain electrodes penetrate the top AlGaN layer to form ohmic contacts with the underlying 2DEG. Without intervention, this configuration would create a short circuit between the source and the drain. However, to prevent current flow, the 2DEG's electron "pool" needs to be depleted. This is achieved by placing a gate electrode atop the AlGaN layer. Applying a negative voltage to the gate, relative to both the drain and source electrodes, removes electrons from the 2DEG, depleting the pool and inhibiting current flow.

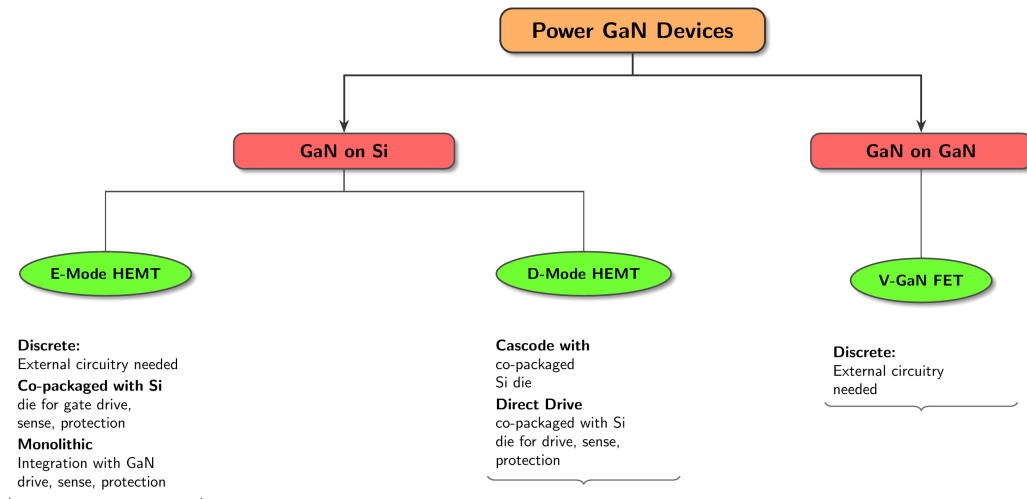


FIGURE 1.7: Classification of GaN HEMTs devices, adapted from [80]

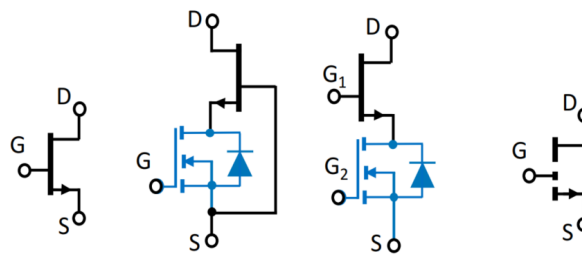


FIGURE 1.8: Different types of GaN devices: Normally-on (d-mode), Normally-off Cascode (d-mode), Direct Drive (d-mode), Normally off (e-mode)

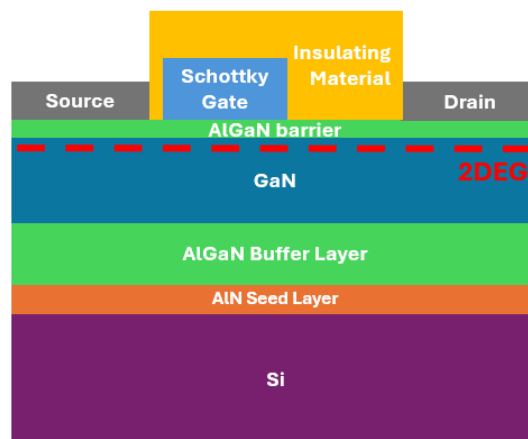


FIGURE 1.9: GaN D-Mode Internal Structure

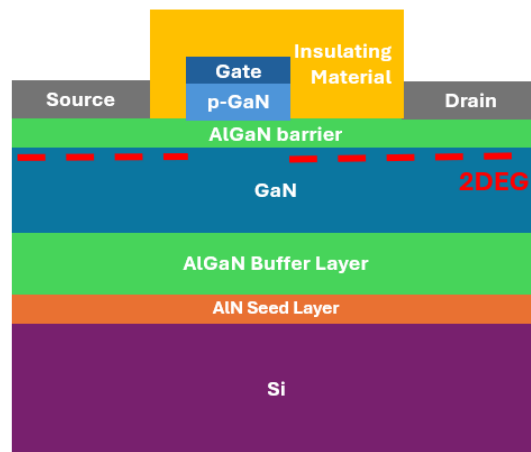


FIGURE 1.10: GaN E-Mode Internal Structure

In the well-known cascode configuration [82], only the MOSFET is controlled, making this approach compatible with typical gate-driving solutions. However, the drawbacks include relatively high switching losses due to MOSFET reverse-recovery charge, complex switching dynamics, and elevated voltage stress on the MOSFET.

An alternative concept utilizing normally-on switches operates the series MOSFET as a safety switch when negative voltage is unavailable; it remains constantly "on" during regular operation. In this directly driven approach, a dedicated gate driver switches the GaN gate between a relatively large negative voltage and zero.

— D-Mode HEMT

GaN power HEMTs are typically fabricated on Si substrates. Since these lateral devices conduct current at the AlGaN/GaN interface where the 2DEG forms, a relatively thin GaN layer can be deposited on the Si substrate with an intermediate buffer layer to ease the lattice mismatch between materials. Most production occurs on 150 mm wafers, though some manufacturers, like Innoscience, use 200 mm substrates. The D-mode device allows the natural 2DEG channel to form under zero gate bias, rendering it normally-on. These devices typically exhibit negative threshold voltages (V_{th}) ranging from -5 V to -20 V.

In most power applications, normally-on devices are highly undesirable from a system implementation perspective. Consequently, D-mode HEMTs are typically combined with either a cascoded low-voltage (LV) Si MOSFET or implemented in a Direct Drive approach. Each of these configurations is examined in detail below.

— Cascoded D-mode/Si MOSFET

Transphorm and Nexperia exemplify companies manufacturing cascode devices. Figure 1.8 illustrates the schematic of this cascode circuit. The primary advantage of this approach lies in the gate drive simplicity. Since a Si MOSFET with threshold voltages in the 3–4 V range and gate oxide ratings typically of ± 20 V is driven, the driver operates with a wide operational window. The cascode configuration thus provides robust safety margins and

excellent noise immunity. Unipolar gate drivers, such as those employed in Si applications, can be utilized. Additionally, the cascode circuit offers advantages in third-quadrant operation due to the presence of the freewheeling Si MOSFET body-diode and exhibits a lower temperature coefficient for $R_{ds(on)}$, which is beneficial in high-temperature applications. Gate leakage current (I_{gss}) can be up to two orders of magnitude lower in cascode circuits compared to typical e-mode devices. With higher gate margins, thermally efficient TO-247 package offerings become available, and automotive AEC-Q101-qualified devices are accessible.

However, disadvantages of the cascoded approach include higher gate and output capacitance, reverse recovery losses from the Si MOSFET body diode, potential reliability concerns for the Si MOSFET under high slew rate switching conditions, reduced slew rate control, and lower efficiencies at voltages below 200 V due to the proportionally larger contribution from the Si device's $R_{ds(on)}$. Switching losses can also be higher compared to e-mode devices.

— Direct Drive

Texas Instruments (TI) and VisIC Technologies both manufacture integrated gate drive D-mode GaN products. The direct drive approach addresses several disadvantages of the cascode circuit mentioned above. Intelligent gate control that avoids Si MOSFET reverse recovery, low-inductance driver/HEMT package integration, integrated protection circuitry, and slew-rate control enable higher closed-loop performance.

The D-mode cascode and direct drive products currently target the 200–800 V range for industrial and automotive applications, including telecom server power supplies, inverters for solar and battery systems, industrial automation, and onboard charging for electric vehicles. In many of these applications, particularly in higher voltage/power domains, they compete directly with SiC devices.

— E-Mode HEMT [83]

Two alternative approaches employ a p-doped GaN gate to modify the band structure and shift the threshold voltage to positive values, creating normally-off devices:

- If this p-gate is contacted via a Schottky contact, it remains quasi-isolated, and the resulting Schottky gate transistor (SGT) is compatible with typical driving schemes. However, the gate exhibits high sensitivity to overvoltages, requiring accurate gate voltage control.
- The alternative concept is the gate injection transistor (GIT), which combines a p-GaN gate with an ohmic contact. This creates a non-isolated gate structure with diode-like input characteristics that is optimally driven by a small continuous gate current in the "on" state, while providing a highly reliable and robust gate structure with excellent performance.

The most commercially prevalent construction of e-mode HEMTs utilizes a p-GaN layer on the gate, typically achieving V_{th} values in the 1–2 V range. The intrinsic advantages of HEMTs in switching applications are preserved,

often resulting in lower switching losses. A key disadvantage of e-mode devices is their low V_{th} , which can result in poor gate immunity to noise and dV/dt transients. For reliability considerations, the maximum gate voltage is typically restricted to 6–7 V, and a negative voltage may be required to turn off the device. Packaging and gate resistance (R_g) selection have become increasingly critical to ensure safe and robust device operation. Low gate inductance (L_g) and common source inductance (L_{cs}) are essential for controlling overshoot and ringing to prevent false turn-on. Active Miller clamps may be necessary, along with Kelvin source connections for improved gate voltage control. Dead-time losses in demanding switching applications can be significant, especially under adverse gate voltage conditions, due to higher reverse source-drain voltages (V_{sd}) resulting from the absence of a freewheeling diode.

Lateral and vertical structure

The employment of an AlGaN/GaN heterostructure in lateral GaN devices enables the formation of a two-dimensional electron gas (2DEG) at the heterointerface, where charge carriers exhibit exceptionally high mobility values ($\mu = 2000 \text{ cm}^2/(\text{V}\cdot\text{s})$). This phenomenon arises because the 2DEG functions as a quantum confinement layer in which electrons propagate without scattering from adjacent ionized impurities. Transistors fabricated using this technology are designated as High-Electron-Mobility Transistors (HEMTs). Furthermore, the piezoelectric polarization charge inherent to the AlGaN/GaN heterostructure yields a high electron concentration in the 2DEG layer (e.g., 10^{13} cm^{-2}). These combined properties facilitate the development of transistors with distinctive and highly competitive performance characteristics.

The lateral configuration also has some attractive features compared to the vertical configuration. It allows monolithic integration of sensing, protection, and drive circuits with relatively simple isolation and efficient shielding between different components. Additionally, it allows easy access to all terminals (including the high-voltage terminal) and enables integration of half-bridge devices and multiple power devices operating on a common substrate. In some cases, it allows a physical connection of the substrate to a heat sink and enables simple hybrid integration with silicon devices via surface wire bonding. Furthermore, the lateral configuration allows simpler and cheaper packaging and enables devices to be self-terminated (i.e., they do not require an additional termination region to shape the electric field at the edge of the device, as in the case of vertical structures).

The vertical configuration, however, remains a preferred option for higher power levels [84]. Recent advances by manufacturers such as onsemi, Odyssey Semiconductor, and NexGen Power Systems have demonstrated the viability of vertical GaN power devices fabricated on native GaN substrates [85], [86], [87]. These vertical GaN transistors leverage true bulk GaN substrates to achieve blocking voltages exceeding 1.2 kV with competitive specific on-resistance values. Onsemi's vertical GaN development program has shown that vertical architectures can provide superior current density ($>600 \text{ A/cm}^2$), improved thermal management through backside cooling, and better voltage scaling compared to lateral devices [86], [87]. The vertical structure eliminates the current spreading limitations inherent to lateral devices and enables more efficient utilization of the drift region, resulting in lower conduction losses at higher voltage ratings.

1.5 Emerging Multi-Physics Design Challenges

The transition to gallium nitride (GaN) technology in power electronics has opened new frontiers in efficiency and compactness, primarily due to its ability to operate at significantly higher switching frequencies compared to traditional silicon devices [84], [88]. However, with these benefits come a set of intricate, multi-physics challenges that must be addressed during the design and integration process. These challenges arise from the complex interactions between electromagnetic, thermal, and mechanical domains, necessitating a holistic co-design approach [89].

Electromagnetic Interference Challenges

One of the most critical concerns is the rapid voltage and current transients associated with high-speed switching. The sharp edges of switching waveforms with dv/dt values exceeding 100 V/ns and di/dt values reaching 10 A/ns introduce substantial electromagnetic interference (EMI), which can exceed CISPR 25 Class 5 limits by 20-30 dB without proper mitigation [90]. This necessitates meticulous attention to layout optimization, grounding strategies, and shielding techniques during the physical design phase.

The EMI generation mechanism in WBG converters differs from that in Si-based systems due to faster transients and higher-frequency harmonics. The EMI generation can be quantified using the following relationship for far-field emissions:

$$E_{EMI}(f) = 20 \log_{10} \left(\frac{2I_{peak}L_{loop}f}{c} \right) + 20 \log_{10} \left(\frac{1}{r} \right) \quad (1.9)$$

where I_{peak} is the peak current, L_{loop} is the loop inductance, f is the frequency, c is the speed of light, and r is the distance from the source. For near-field emissions in the typical measurement range (< 3 m), more complex models accounting for both electric and magnetic coupling are required [91].

The spectral characteristics of EMI from GaN converters extend to significantly higher frequencies than Si equivalents. While Si IGBTs typically produce emissions primarily below 30 MHz, GaN devices generate substantial EMI up to 500 MHz and beyond, requiring broadband filtering strategies and careful PCB stackup design [92]. Recent developments in EMI mitigation include:

- **Active EMI filtering:** Achieving 30-40 dB attenuation using active gate drivers with adjustable slew rate control or active EMI cancellation circuits that inject counter-phase voltage or currents [93], [94]. These techniques can reduce passive filter volume by 50-70% while maintaining compliance with EMC standards.
- **Spread spectrum modulation:** Reducing peak emissions by 10-15 dB through randomized or triangular frequency modulation around the nominal switching frequency [95], [96]. The technique is particularly effective for conducted emissions in the 150 kHz-30 MHz range.
- **Optimized gate driving:** Controlled dv/dt shaping using external gate resistors, ferrite beads, or active gate drivers with programmable slew rates, balancing EMI reduction against increased switching losses [97].
- **Advanced PCB stackup designs:** Embedded shielding layers, careful routing of high di/dt paths, and use of stitching vias to minimize loop inductances and prevent common-mode current circulation [92].

Parasitic Effects and Layout Optimization

Furthermore, the high di/dt and dv/dt values inherent to GaN switching events create strong parasitic interactions. These parasitics — originating from packaging inductances (typically 1-5 nH), PCB trace geometries (0.5-2 nH/cm), and component placement — can lead to voltage overshoots exceeding 30% of the DC bus voltage, current ringing with amplitudes up to 50% of the nominal current, and potential instability in the power stage [98].

The impact of parasitic inductance on switching behavior can be expressed through the voltage overshoot relationship:

$$V_{overshoot} = L_{parasitic} \cdot \frac{di}{dt} \quad (1.10)$$

where $L_{parasitic}$ includes contributions from device packaging, PCB traces, and interconnections. For a typical GaN switching event with $di/dt = 10$ A/ns, even 2 nH of parasitic inductance produces 20 V of overshoot, which becomes critical in high-voltage applications [99].

The parasitic ringing frequency is determined by:

$$f_{ring} = \frac{1}{2\pi\sqrt{L_{parasitic} \cdot C_{parasitic}}} \quad (1.11)$$

Where $C_{parasitic}$ includes device output capacitance, PCB capacitance, and stray capacitances. Typical ringing frequencies range from 50 MHz to 500 MHz, depending on layout and packaging [100].

Table 1.8, extracted from [101], [102], [103], provides typical parasitic values for different packaging technologies and their impact on circuit performance.

TABLE 1.8: Typical Parasitic Values and Performance Impact for WBG Devices [101], [103], [104], [105], [106], [107]

Package	L_{pkg} (nH)	L_{PCB} (nH)	C_{par} (pF)	Performance Impact
TO-247	10–15	5–10	5–10	40% overshoot, <100 kHz
D2PAK	5–8	3–5	3–5	25% overshoot, <500 kHz
SMD (GaN)	0.5–2	1–3	1–2	10% overshoot, >1 MHz
Chip-scale	0.1–0.5	0.5–1	0.5–1	<5% overshoot, >5 MHz
DFN (QFN)	1–3	2–4	2–3	15% overshoot, 200–800 kHz
LGA	0.3–1	0.8–2	1–2	8% overshoot, 1–3 MHz

Design guidelines for minimizing parasitic effects include:

- **Power loop inductance:** < 2 nH for MHz operation, achievable through symmetric layout, wide traces, and multilayer PCBs with adjacent current-carrying layers [108].
- **Gate loop inductance:** < 1 nH for stable operation, requiring careful driver placement and Kelvin source connections to prevent gate voltage oscillations [109].
- **Kelvin source connections:** For accurate gate voltage control and prevention of parasitic turn-on, particularly critical in half-bridge configurations where high dv/dt can couple through Miller capacitance [110].

- **Symmetric layout for paralleled devices:** Equal trace lengths and widths to ensure current sharing and prevent oscillations between parallel devices, with current imbalance typically $< 10\%$ [111].
- **Return current path optimization:** Minimizing the area enclosed by supply and return currents through ground plane design and strategic via placement [112].

Advanced techniques include 3D electromagnetic simulation using finite element analysis (FEA) tools to extract parasitic parameters, time-domain behavioral modeling to predict switching waveforms including parasitics, and iterative optimization of PCB layouts guided by simulation results [113], [114].

Thermal Management Considerations

Thermal management also becomes increasingly complex [115], [116]. Although GaN devices generate less total heat due to lower switching and conduction losses (typically 50-70% of equivalent Si devices), their compact size results in power densities exceeding 1000 W/cm^2 . This concentration of heat flux creates localized hot spots that can exceed safe operating temperatures if not properly managed [117].

The junction temperature rise can be calculated using the thermal resistance network:

$$\Delta T_j = P_{loss} \cdot (R_{th,jc} + R_{th,cs} + R_{th,sa}) \quad (1.12)$$

where P_{loss} is the total power dissipation, and $R_{th,jc}$, $R_{th,cs}$, and $R_{th,sa}$ are the junction-to-case, case-to-sink, and sink-to-ambient thermal resistances respectively. For GaN devices with small die sizes, $R_{th,jc}$ is typically 1-3 K/W, while $R_{th,cs}$ depends heavily on thermal interface material (TIM) quality and mounting pressure [118].

For transient thermal analysis, the Cauer or Foster thermal networks provide time-dependent temperature prediction:

$$T_j(t) = T_{ambient} + P_{loss} \sum_{i=1}^n R_{th,i} \left(1 - e^{-t/\tau_i}\right) \quad (1.13)$$

where $R_{th,i}$ and τ_i are the thermal resistances and time constants of each network layer [119].

1.6 Modeling and Characterization of WBG Devices

The characterization of WBG devices poses unique challenges due to their fast switching and frequency-dependent behavior, requiring specialized measurement techniques and systems. The development of switching power converters based on WBG semiconductors brings numerous performance advantages while also introducing significant characterization challenges encompassing device modeling [120], switching loss characterization [121], conduction loss analysis [122], and electromagnetic interference effects [123].

Figure 1.11 illustrates the comprehensive characterization framework required for WBG devices, encompassing static, dynamic, and thermal measurements across multiple operating conditions.

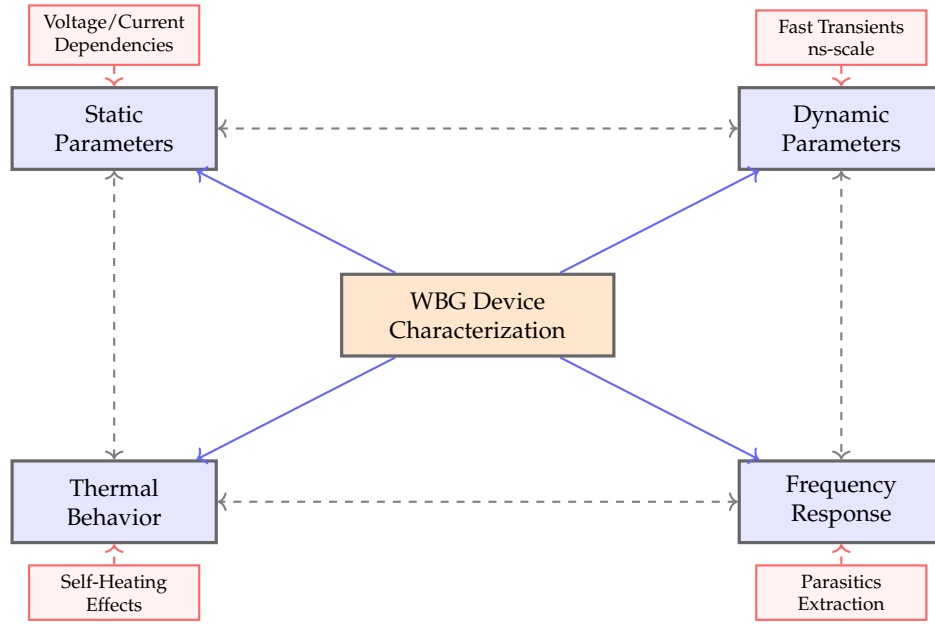


FIGURE 1.11: Characterization framework for WBG devices

Dynamic On-Resistance Characterization

One of the most critical parameters for WBG device characterization is the dynamic on-resistance ($R_{DS,on}$), which exhibits frequency-dependent behavior that differs significantly from traditional silicon devices. Recent studies have demonstrated that GaN devices can show up to 200% increase in $R_{DS,on}$ under certain switching conditions compared to their static values [122]. Wang et al. [122] developed a comprehensive frequency-dependent characterization methodology for $R_{DS,on}$ in GaN devices using finite element simulation techniques covering different GaN device architectures. Their thorough analysis demonstrated a significant increase in $R_{DS,on}$ at frequencies above 1 MHz, with the measurement results showing substantial influence from layout parasitics and interconnection design.

Measurement System Architectures and Techniques

The characterization of WBG devices requires sophisticated measurement systems capable of capturing fast switching transients and high-frequency behavior with sufficient accuracy and bandwidth. Traditional characterization approaches often fall short when dealing with the extreme performance characteristics of modern GaN and SiC devices, which can exhibit rise times below 10 ns and dv/dt values exceeding 200 V/ns.

Li et al. [124] developed precise dynamic $R_{DS,on}$ extraction methodologies designed explicitly for GaN HEMTs operating under high frequency and high voltage conditions. Their approach addressed the fundamental challenges of measuring rapidly changing parameters in the presence of significant parasitic effects and electromagnetic interference. The methodology incorporates advanced de-embedding techniques to separate device characteristics from measurement system artifacts, achieving measurement accuracies of 2% or better at switching frequencies up to 10 MHz.

Table 1.9 provides a comprehensive comparison of different characterization methods for WBG devices, highlighting their advantages, limitations, and applicable frequency ranges.

TABLE 1.9: Comparison of WBG Device Characterization Methods [125], [126], [127], [128], [129]

Method	Advantages	Limitations	Freq. Range	Uncertainty
Double-Pulse	Industry standard, accurate	Single op. point	DC–10 MHz	±2–5%
Continuous	Real conditions	Thermal effects	0.1–5 MHz	±5–10%
Pulse I-V	No self-heating	Limited dynamics	DC–1 MHz	±1–3%
S-Parameter	High freq. behavior	Complex setup	1 MHz–10 GHz	±3–7%
Calorimetric	Direct loss meas.	Slow response	DC–1 MHz	±1–2%

Key Performance Indicators and Measurement Challenges

Threshold Voltage Stability

Threshold voltage stability represents one of the most critical reliability parameters for WBG devices, particularly for SiC MOSFETs, where threshold voltage drift can significantly impact long-term performance. Recent studies have shown that SiC MOSFETs can exhibit threshold voltage shifts of up to 20% over 1000 hours of operation under high-temperature reverse bias conditions [130]. Lelis et al. [130] established a fundamental understanding of threshold voltage instability mechanisms in SiC MOSFETs and developed comprehensive guidelines for reliability testing protocols. Their work identified the critical role of near-interface traps in determining long-term stability and proposed accelerated testing methods that can predict device lifetime with 95% confidence intervals.

Input Capacitance Characterization

Input capacitance characterization is crucial for understanding the gate drive requirements and switching behavior of WBG devices. The input capacitance of GaN and SiC devices exhibits strong voltage and frequency dependence, making accurate characterization challenging yet essential for optimal gate-drive design. Recent measurements have shown that GaN HEMT input capacitance can vary by more than 300% across the operating voltage range, significantly impacting gate drive requirements [131].

The relationship between gate resistance, time constant, and input capacitance can be expressed as:

$$C_{iss} = \frac{\tau}{R_G} = \frac{1}{2\pi f_{3dB} R_G} \quad (1.14)$$

where τ is the time constant related to gate voltage transition, R_G is the external gate resistance, and f_{3dB} is the 3-dB bandwidth of the gate drive circuit.

Switching Loss Analysis

Switching loss characterization is one of the most challenging aspects of WBG device evaluation, due to the fast switching speeds and the complex interactions between device characteristics and circuit parasitics. Azpurua et al. [121] developed comprehensive time- and frequency-domain characterization techniques for switching losses in GaN FET power converters, demonstrating that traditional loss calculation methods can underestimate actual losses by up to 40% in high-frequency applications.

Power switching losses occur during transitions between on and off states and can be expressed as:

$$P_{sw} = f_s \cdot (E_{on} + E_{off}) = f_s \cdot \left[\int_0^{t_{on}} v_{ds}(t) \cdot i_d(t) dt + \int_0^{t_{off}} v_{ds}(t) \cdot i_d(t) dt \right] \quad (1.15)$$

where f_s is the switching frequency, E_{on} and E_{off} are the turn-on and turn-off energy losses, respectively, and the integrals are evaluated over the switching transition periods.

Device Architecture Considerations

Table 1.10 provides an enhanced comparison of different WBG device architectures, including recent developments in vertical GaN and cascode configurations.

TABLE 1.10: Different WBG Devices with Performance Metrics [17], [132], [133], [134], [135], [136]

Parameter	GaN HEMT	GaN Cascode	SiC MOSFET	Si SJ MOSFET	Si IGBT
Voltage (V)	600–650	600–900	650–3300	600–900	600–6500
Current (A)	1–90	10–60	5–200	5–100	10–3600
$R_{DS,on} \cdot A$ (mΩcm ²)	1–5	3–8	3–15	10–50	—
Max f_{sw} (MHz)	1–40	0.5–10	0.1–2	0.05–1	0.02–0.1
dv/dt (V/ns)	50–200	30–100	20–100	5–50	1–20
Q_g (nC)	1–20	10–50	20–300	20–200	100–5000
Max T_j (°C)	150–175	150	175–200	150	175
Reverse Recovery	None	Limited	Moderate	High	Very High
FOM ($R \cdot Q$)	Best	Good	Good	Moderate	Poor
Cost (\$/A)	Medium	Med-High	High	Low	Low

GaN High Electron Mobility Transistors (HEMTs) represent a unique device architecture that combines superior electrical performance with challenging characterization requirements.

Most commercially available GaN devices are lateral heterojunction field-effect transistors (HFETs) or high-electron-mobility transistors (HEMTs), typically rated at 600–650V. Enhancement-mode GaN devices are usually operated in the OFF state through various techniques, including p-doped GaN layers grown on an AlGaN barrier [131]. Recent developments have achieved threshold voltages exceeding 2V with gate voltage ratings up to 7V, making them compatible with standard gate drivers. Cascode configurations combine depletion-mode GaN HEMTs with low-voltage enhancement-mode silicon MOSFETs to achieve normally-OFF operation while maintaining the superior switching characteristics of GaN technology.

Silicon Carbide MOSFETs exhibit characteristics that are fundamentally different from both silicon MOSFETs and GaN HEMTs, requiring specialized characterization approaches that account for their unique properties. The wide bandgap of 3.3 eV enables breakdown electric fields exceeding 3 MV/cm, allowing for thinner drift regions and lower specific on-resistance compared to silicon devices. Kumar et al. [137] provided a comprehensive review of wide-bandgap

devices and their power-electronics applications, highlighting the complementary nature of GaN and SiC technologies across different application domains.

1.7 GaN-based Converter Topologies

Implementing GaN devices in power converter topologies requires careful consideration of their unique characteristics and operating requirements. This section examines three key topologies — two-level inverters, buck converters, and interleaved buck converters — highlighting the design challenges and opportunities presented by GaN technology.

Two-Level Inverters with GaN Devices

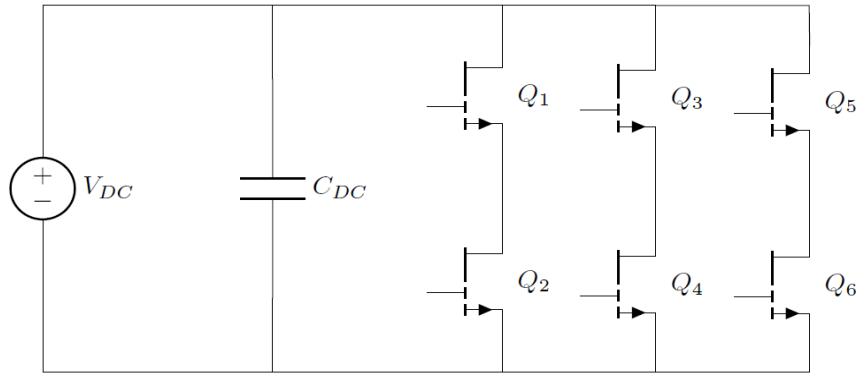


FIGURE 1.12: GaN-based 2-Level Three-phase VSI

Two-level voltage-source inverters (VSIs) are among the most widely deployed power-conversion topologies, particularly in motor-drive applications. The integration of GaN devices in two-level inverters enables significant improvements in switching frequency, efficiency, and power density compared to silicon-based implementations.

The half-bridge leg configuration, fundamental to two-level inverters, presents unique challenges when implemented with GaN devices. The extremely fast switching transitions ($di/dt > 10 \text{ A/ns}$, $dv/dt > 50 \text{ V/ns}$) create several critical design considerations:

- **Commutation loop inductance** becomes the dominant factor affecting switching performance. The parasitic inductance L_{comm} in the power loop directly impacts the voltage overshoot during turn-off:

$$V_{overshoot} = L_{comm} \cdot \frac{di}{dt} \quad (1.16)$$

For typical GaN switching speeds and a commutation loop inductance of 10 nH, voltage overshoots can exceed 100 V, necessitating derating of the device voltage or implementation of active clamping circuits [98].

- **Gate drive design** requires special attention due to the low threshold voltage (typically 1.5-2.5 V) and high-frequency operation. The gate driver must

provide sufficient drive current to charge/discharge the input capacitance rapidly while maintaining adequate noise immunity. Typical gate resistances range from 0.5 to 5 Ω , with lower values reducing switching time but increasing ringing and EMI.

- **Dead-time optimization** presents a trade-off between shoot-through protection and efficiency. GaN devices typically require shorter dead times (10-50 ns) compared to silicon MOSFETs due to their faster switching, but insufficient dead time can lead to catastrophic failures. Advanced techniques such as adaptive dead-time control can minimize body diode conduction losses while ensuring reliable operation.

The switching loss characteristics of GaN-based two-level inverters differ significantly from silicon implementations. The turn-on loss is typically dominated by the reverse recovery of the complementary device's output capacitance. In contrast, the turn-off loss is primarily determined by the current fall time and voltage rise overlap. The total switching energy can be approximated as [121]:

$$E_{sw} = E_{on} + E_{off} = \frac{1}{6} V_{DS} I_D (t_r + t_f) + E_{oss} \quad (1.17)$$

where t_r and t_f are the current rise and fall times, E_{oss} is the output capacitance related loss.

Buck Converters

The synchronous buck converter represents an ideal topology for demonstrating GaN advantages in DC-DC conversion applications. Operating at frequencies exceeding 1 MHz, GaN-based buck converters achieve power densities above 1 kW/in³ while maintaining efficiencies greater than 95% [138].

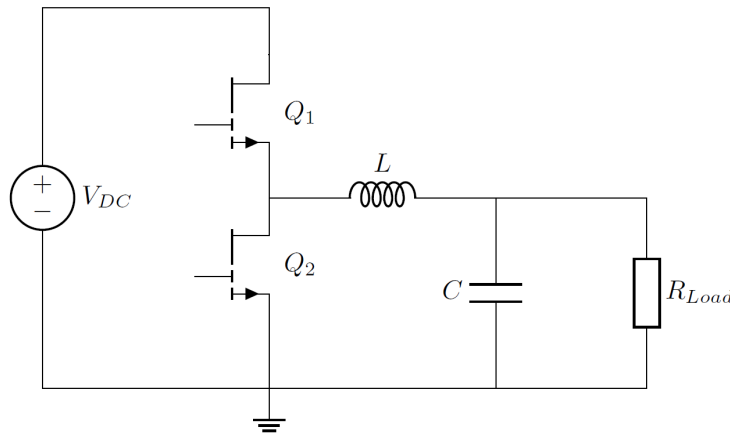


FIGURE 1.13: GaN-based Buck converter

The design of GaN buck converters requires careful attention to several key aspects:

- **Inductor design** becomes critical at high switching frequencies. The inductor value L is typically selected to maintain continuous conduction mode (CCM)

operation with acceptable current ripple:

$$L = \frac{V_{out}(V_{in} - V_{out})}{V_{in} \cdot f_{sw} \cdot \Delta I_L} \quad (1.18)$$

where f_{sw} is the switching frequency and ΔI_L is the peak-to-peak inductor current ripple (typically 20-40% of DC current). At MHz frequencies, the required inductance values are small (hundreds of nH to a few μ H), making parasitics and tolerances more critical.

- **Output capacitor selection** must balance ESR, capacitance, and voltage rating. The output voltage ripple has two components:

$$\Delta V_{out} = \Delta I_L \cdot ESR + \frac{\Delta I_L}{8f_{sw}C_{out}} \quad (1.19)$$

At high frequencies, the ESR contribution often dominates, necessitating the use of low-ESR ceramic capacitors or parallel combinations of different capacitor types.

- **PCB layout** has a first-order impact on performance. Critical design rules include:
 - Minimizing the high di/dt loop formed by input capacitor, high-side FET, low-side FET, and ground return (target < 5 nH)
 - Kelvin sensing connections for gate drives to minimize common-source inductance effects
 - Careful routing of switching node to minimize coupling to sensitive signals
 - Adequate copper thickness and area for thermal management (typically 2-4 oz copper)

The efficiency of GaN buck converters shows characteristic behavior across the load range. Light-load efficiency is dominated by gate drive losses ($P_{gate} = f_{sw} \cdot Q_g \cdot V_{GS}$) and switching losses, while heavy-load efficiency is limited by conduction losses ($P_{cond} = I_{rms}^2 \cdot R_{DS(on)}$). The optimum switching frequency at a given load can be determined by minimizing total losses.

Interleaved Buck Converters

Interleaving multiple buck converter phases provides significant advantages in high-current applications, including the cancellation of input/output current ripple, improved transient response, and enhanced thermal distribution. GaN devices are particularly well-suited for interleaved topologies due to their low gate charge, enabling efficient paralleling [139].

For an N-phase interleaved buck converter with phase shift $\phi = 360/N$, the input current ripple is reduced by a factor approaching N at optimal phase count. The effective ripple frequency seen by input and output capacitors becomes $N \cdot f_{sw}$, enabling a substantial reduction in passive component sizes.

The current sharing between phases depends critically on component matching and on the implementation of control. Passive current sharing relies on matched

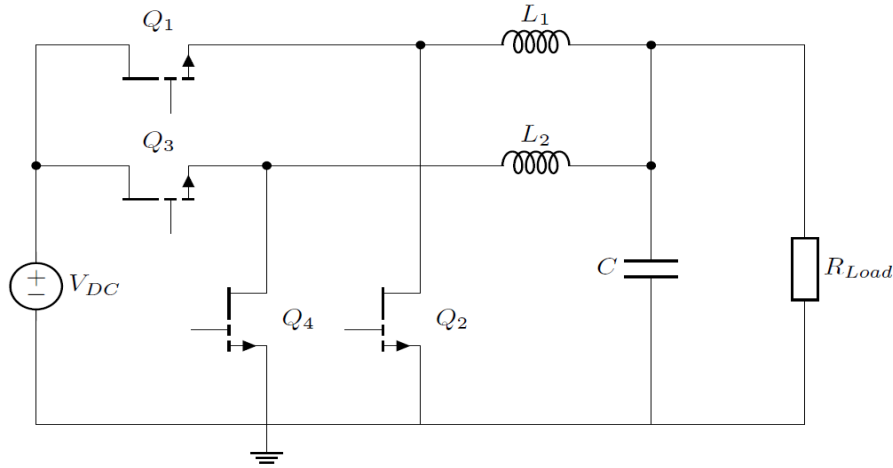


FIGURE 1.14: GaN-based 2-Phase Interleaved Buck Converter

inductances and on-resistances, while active current sharing uses individual phase current sensing and control. The degree of current imbalance can be expressed as:

$$\Delta I_{\text{imbalance}} = I_{\text{out}} \cdot \frac{\Delta L/L + \Delta R_{DS(on)}/R_{DS(on)}}{N} \quad (1.20)$$

Critical design challenges in interleaved GaN converters include:

- **Precise phase alignment:** Timing accuracy of 1-2 ns is required for optimal ripple cancellation at MHz switching frequencies, demanding careful PCB design and gate drive signal routing.
- **Thermal coupling:** Phase interaction through thermal paths can cause thermal runaway in the hottest phase. Thermal modeling and adequate spacing (minimum 5-8 mm) between phases is essential.
- **EMI considerations:** While interleaving can reduce differential-mode EMI through ripple cancellation, common-mode EMI may increase due to multiple switching events. Coordinated gate drive signal rise/fall times and synchronized switching patterns can mitigate this.

Dual Active Bridge Converters

The Dual Active Bridge (DAB) converter has emerged as a leading topology for bidirectional isolated DC-DC conversion, particularly in applications such as on-board chargers (OBCs) for electric vehicles, battery energy storage systems, and solid-state transformers. The DAB's soft-switching capability, galvanic isolation, and high power density make it especially suitable for GaN implementation.

DAB Operating Principles and Modulation

The basic DAB topology consists of two active full-bridge circuits coupled through a high-frequency transformer with series inductance L_s , which can be the transformer leakage inductance, an external inductor, or both. Power transfer

occurs through phase-shift modulation between the primary and secondary bridges.

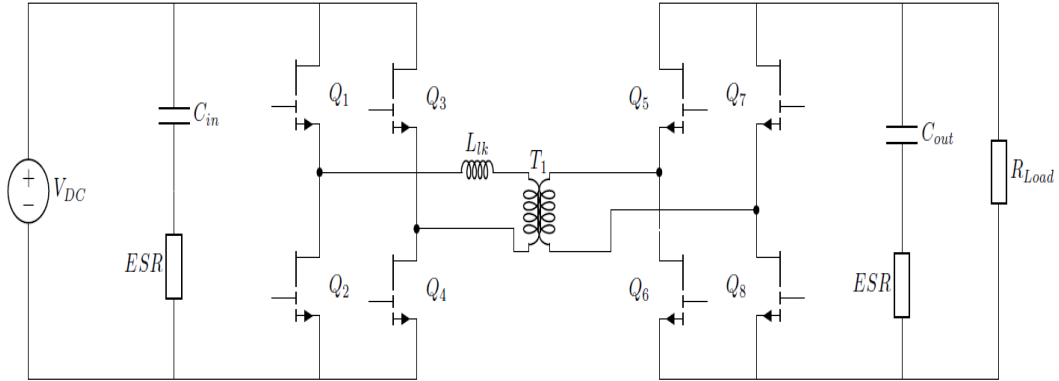


FIGURE 1.15: GaN-based Dual Active Bridge Converter

The instantaneous power transfer is determined by the voltage difference across the series inductance and the phase shift angle ϕ . For square-wave voltage waveforms with amplitude V_1 (primary) and V_2 (secondary), the average power is:

$$P = \frac{nV_1V_2}{2\pi f_s L_s} \phi \left(1 - \frac{|\phi|}{\pi}\right) \quad (1.21)$$

where n is the transformer turns ratio and f_s is the switching frequency [140].

The current flowing through the series inductance is:

$$i_{Ls}(t) = i_{Ls}(0) + \frac{1}{L_s} \int_0^t v_{Ls}(\tau) d\tau \quad (1.22)$$

Zero Voltage Switching (ZVS) conditions represent a critical advantage of DAB converters. ZVS is achieved when the series inductor current at switching instants has sufficient magnitude and appropriate direction to discharge/charge the output capacitance of the switching devices before the complementary device turns on. The ZVS boundary conditions for GaN devices require:

$$|i_{Ls}(t_{sw})| > \frac{C_{oss} V_{bridge}}{t_{dead}} \quad (1.23)$$

where C_{oss} is the output capacitance, V_{bridge} is the bridge voltage, and t_{dead} is the dead time [141].

The ZVS range depends on operating conditions. In single-phase-shift (SPS) modulation, maintaining full ZVS across the entire power range is challenging, particularly at light loads and high voltage conversion ratios. The phase shift required for rated power is:

$$\phi_{rated} = \frac{\pi P_{rated} L_s f_s}{n V_1 V_2} \quad (1.24)$$

Extended Phase Shift (EPS) and Dual Phase Shift (DPS) modulation schemes provide improved ZVS range and reduced reactive current. In DPS modulation,

independent control of primary and secondary bridge phase shifts (ϕ_1 and ϕ_2) enables additional degrees of freedom:

$$P = \frac{nV_1V_2}{4\pi f_s L_s} [2\phi(\pi - \phi) - (\phi_1 + \phi_2)(\pi - \phi_1 - \phi_2)] \quad (1.25)$$

where $\phi = \phi_1 + \phi_2$ is the total phase shift [142].

GaN Implementation Considerations

Implementing DAB converters with GaN devices enables operation at switching frequencies ranging from 500 kHz to several MHz, resulting in reduced magnetic component size and improved transient response. However, several design challenges must be addressed:

Current stress and RMS current: The RMS current through the series inductance directly determines conduction losses. For SPS modulation, the RMS inductor current is:

$$I_{Ls,rms} = \sqrt{\frac{n^2 V_1^2}{12 f_s^2 L_s^2} [\phi^3 + 3\pi^2(\pi - \phi)]} \quad (1.26)$$

At light loads, the reactive current component can significantly exceed the real power component, reducing efficiency. This effect is quantified by the ratio of reactive power to active power:

$$\frac{Q}{P} = \frac{\pi - 2\phi}{2\phi(1 - \phi/\pi)} \quad (1.27)$$

Transformer design: The DAB transformer must handle high-frequency operation while maintaining low leakage inductance (which determines power transfer capability) and adequate insulation. Key design parameters include:

- Series inductance L_s : Typically 1-20 μH depending on voltage and power levels, often dominated by transformer leakage inductance
- Magnetizing inductance L_m : Should be $\gg L_s$ (typically 10-50 times larger) to minimize magnetizing current
- Core selection: MnZn ferrite for up to 500 kHz, NiZn ferrite or nanocrystalline for higher frequencies
- Winding configuration: Interleaved primary-secondary layers to minimize leakage while managing parasitic capacitance

Control and synchronization: Precise timing control is essential for optimal DAB operation. Phase shift resolution of 1-2° is typically required, corresponding to timing precision of 50-100 ns at 500 kHz. Modern digital controllers (FPGAs, high-speed DSPs) enable sophisticated modulation schemes and adaptive control [143].

Multilevel DAB Topologies

For medium-voltage applications (> 1 kV), multilevel DAB topologies extend the voltage and power-handling capabilities while maintaining the advantages of two-level DAB. Standard multilevel configurations include:

Three-Level Neutral Point Clamped (NPC) DAB: Utilizes three-level bridges on primary and secondary sides, reducing voltage stress on individual switches to half the DC bus voltage. This enables the use of lower-voltage GaN devices with superior figures of merit. The voltage stress reduction is:

$$V_{switch,3L} = \frac{V_{dc}}{2} < V_{switch,2L} = V_{dc} \quad (1.28)$$

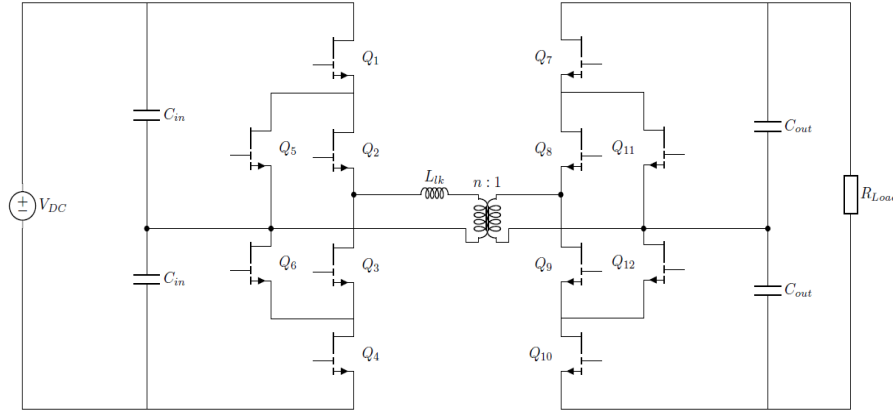


FIGURE 1.16: GaN-based ANPC Multilevel DAB

The three-level DAB provides additional benefits [144]:

- Reduced dv/dt due to smaller voltage steps, minimizing EMI and transformer stress
- Lower output current ripple and harmonic content
- Improved ZVS range through multilevel modulation strategies

However, complexity increases due to additional switches (8 per bridge vs. 4 in two-level) and neutral-point voltage-balancing requirements [145].

Applications in OBC Systems: For electric vehicle on-board chargers, DAB converters provide bidirectional power flow (V2G capability), galvanic isolation (safety requirement), and a wide voltage regulation range (to accommodate varying battery voltage). Typical specifications include:

- Power level: 3-22 kW
- Input voltage: 400 V AC (rectified to 565 V DC)
- Output voltage: 250-450 V (battery pack voltage range)
- Switching frequency: 100-500 kHz (Si IGBTs/MOSFETs), 500 kHz-1 MHz (GaN)
- Efficiency target: > 95% at rated power, > 90% at 10% load
- Power density: 2-4 kW/L (liquid cooled), 1-2 kW/L (air cooled)

GaN-based DAB converters for OBC applications have demonstrated efficiencies exceeding 97% at rated power and power densities above 3 kW/L through operation at 500 kHz with optimized magnetics and advanced modulation [35], [146].

1.8 Power Density Enhancement with embedded magnetics

Achieving high power density in GaN-based converters requires not only fast-switching semiconductors but also optimized magnetic components that can operate efficiently at elevated frequencies. This section examines the integration of coreless inductors design that complement GaN device capabilities.

Coreless Inductor Technology

Traditional magnetic core materials face fundamental limitations at high frequencies due to core losses, which increase with frequency according to the Steinmetz equation:

$$P_v = k \cdot f^\alpha \cdot B^\beta \quad (1.29)$$

where k , α , and β are material-dependent parameters, f is frequency, and B is peak flux density. For typical ferrite materials, core losses become prohibitive above 1-2 MHz, creating a bottleneck for GaN converter miniaturization [147].

Coreless (air-core) inductors eliminate core losses, making them attractive for very high-frequency applications. The inductance of a coreless inductor depends purely on geometry:

$$L = \frac{\mu_0 N^2 A}{l} \quad (1.30)$$

where N is the number of turns, A is the cross-sectional area, and l is the magnetic path length. Without magnetic material to concentrate flux ($\mu_r = 1$), coreless inductors require more turns to achieve a given inductance, resulting in higher DC resistance and larger physical size compared to cored inductors of equal inductance.

The design trade-offs for coreless inductors include:

- **Quality factor optimization** represents the key performance metric. The quality factor $Q = \omega L / R_{DC}$ determines the reactive-to-resistive loss ratio. At frequencies above 5 MHz, well-designed coreless inductors can achieve Q factors exceeding 100, substantially higher than cored inductors at the same frequency.
- **Conductor selection and arrangement** critically affects performance. Litz wire with appropriate strand gauge (typically 44-50 AWG for 1-10 MHz) minimizes AC resistance due to skin and proximity effects.
- **Geometrical optimization** must balance inductance density, resistance, and parasitic capacitance. Typical coreless inductor geometries include:
 - **Solenoid configuration:** Provides the highest inductance-to-volume ratio but significant inter-turn capacitance (typically 5-20 pF), limiting self-resonant frequency (SRF)
 - **Toroidal configuration:** Minimizes stray magnetic fields and EMI, but is more complex to manufacture
 - **Planar spiral inductors:** Enable PCB integration for inductances < 500 nH, with Q factors of 20-40 at 10 MHz using thick copper or gold metallization [148]

Integration Strategies

The integration of GaN devices with optimized magnetics requires system-level co-design. Key integration strategies include:

Frequency scaling: As switching frequency increases from 500 kHz to 5 MHz, inductor and transformer core volumes can shrink by factors of 5-10, but careful loss management is essential. The optimal frequency typically occurs where semiconductor switching losses equal magnetic losses.

Coupled inductors: In multi-phase converters, magnetic coupling between phase inductors enables ripple cancellation and transient response improvement while reducing total magnetic volume by 30-50%.

Integrated magnetic structures: Combining multiple magnetic functions (filtering inductors, transformers, common-mode chokes) into single structures with shared flux paths reduces size and cost while improving performance [149].

1.9 EMI Suppression Strategies

Electromagnetic interference (EMI) represents one of the most significant challenges in high-frequency GaN converters. The fast-switching transients that enable high efficiency and power density simultaneously generate high-frequency noise that can interfere with nearby electronics and must be attenuated to meet regulatory standards (CISPR 25 for automotive, FCC Part 15 for commercial electronics, and MIL-STD-461 for military applications).

EMI Generation Mechanisms in GaN Converters

EMI in power converters arises from high di/dt and dv/dt during switching transitions [150]. For GaN devices with switching speeds exceeding 50 V/ns and 10 A/ns, the generated EMI extends well into the VHF range (30-300 MHz) and beyond.

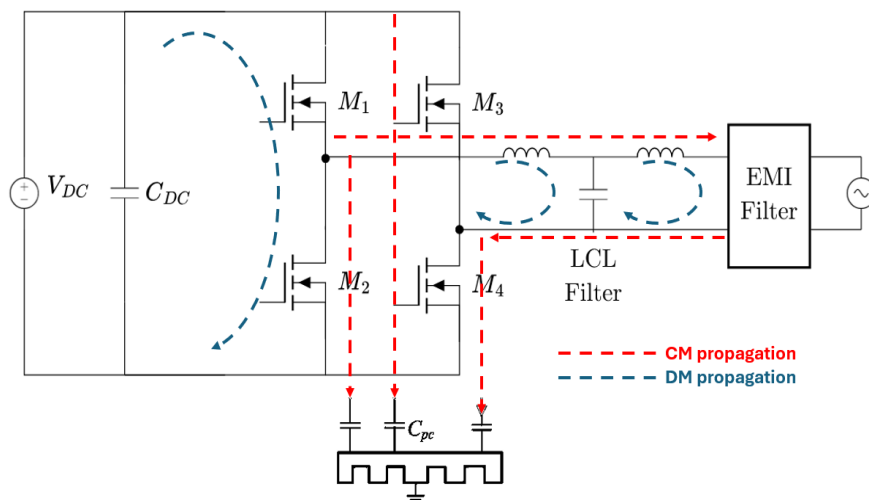


FIGURE 1.17: DM and CM emissions, adapted from [151]

Differential-mode (DM) EMI is generated by the switching current loop and propagates through power input/output terminals. The DM noise current can be

modeled as:

$$I_{DM}(f) = \frac{di/dt}{2\pi f} \cdot SA(f) \quad (1.31)$$

where $SA(f)$ is the spectral amplitude of the trapezoidal switching current waveform [152].

Common-mode (CM) EMI results from voltage variations of the converter ground reference with respect to earth ground, coupled through parasitic capacitances. The CM noise voltage is:

$$V_{CM} = \frac{1}{2}(V_+ + V_-) = \frac{dv/dt}{2\pi f} \cdot SA(f) \quad (1.32)$$

where V_+ and V_- are the voltages on the positive and negative power lines with respect to ground.

The parasitic capacitances coupling high dv/dt nodes to ground are the primary CM noise sources. In a typical buck converter:

$$I_{CM} = C_{par} \frac{dv_{sw}}{dt} \quad (1.33)$$

where C_{par} includes heatsink-to-device capacitance (1-100 pF), PCB trace-to-ground plane capacitance (10-200 pF), and other stray capacitances.

Passive EMI Filtering

Traditional passive LC filters form the first line of defense against conducted EMI. A typical two-stage EMI filter includes:

Differential-mode filtering: Implemented using series inductors L_{DM} and shunt capacitors C_{DM} in a π or T configuration. The attenuation provided by a single LC stage is:

$$A_{DM}(f) = 20 \log_{10} \left| \frac{1}{1 - \omega^2 L_{DM} C_{DM}} \right| \text{ [dB]} \quad (1.34)$$

Above the corner frequency $f_c = 1/(2\pi\sqrt{L_{DM}C_{DM}})$, attenuation increases at 40 dB/decade.

Common-mode filtering: Utilizes common-mode chokes (CMCs) with high impedance to CM currents but low impedance to DM currents, plus Y-capacitors connecting power lines to ground. The CM attenuation is:

$$A_{CM}(f) = 20 \log_{10} \left| \frac{Z_{CMC}(f)}{Z_{CMC}(f) + 2Z_s} \right| \text{ [dB]} \quad (1.35)$$

where Z_{CMC} is the common-mode impedance of the choke and Z_s is the source impedance.

However, passive filters for high-frequency GaN converters face challenges:

- Large size and weight to attenuate noise extending to 100+ MHz
- Parasitic elements (winding capacitance, lead inductance) degrade high-frequency performance
- Insertion loss peaks and resonances can amplify certain frequencies
- Cost and component count increase with stricter EMI requirements

Active EMI Filtering

Active EMI filters (AEF) represent an alternative approach that senses EMI noise and injects canceling signals, enabling dramatic size reduction compared to passive filters. The basic AEF concept involves:

1. **Noise sensing:** Detecting DM and/or CM noise currents using current transformers, sense resistors, or capacitive sensing
2. **Signal processing:** Amplifying, phase-shifting, and conditioning the sensed signal
3. **Noise injection:** Injecting an anti-phase signal through power MOSFETs or dedicated injection transformers

The noise cancellation performance depends on amplitude matching and phase alignment between the sensed noise and the injected compensation signal. Ideally, the residual noise after active cancellation is:

$$V_{residual} = V_{noise} \left| 1 - Ae^{j(\theta+\pi)} \right| \quad (1.36)$$

where A is the amplitude ratio and θ is the phase difference between the noise and compensation signal [152].

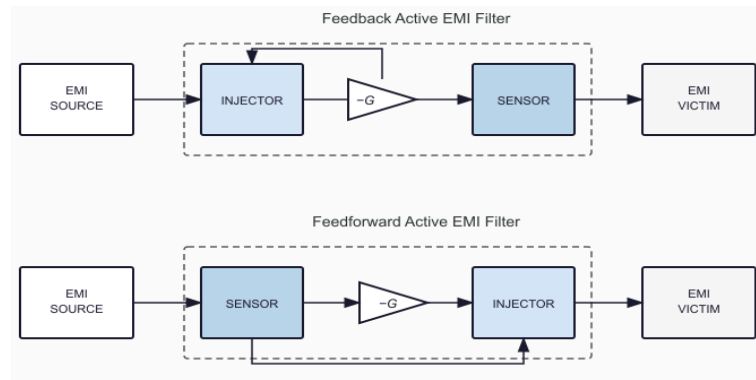


FIGURE 1.18: Active EMI filtering, adapted from [150]

Feed-forward active filters sense the noise at the converter and inject cancellation signals at the input terminals. Typical architectures include:

- **Voltage-driven AEF:** Senses noise voltage and generates canceling current through a transconductance amplifier and injection transformer. Achieves 20-40 dB attenuation from 150 kHz to 30 MHz [153].
- **Current-driven AEF:** Senses noise current and replicates it with opposite polarity. Better suited for DM noise cancellation in high-current applications [154].
- **Hybrid active-passive filters:** Combines active cancellation for lower frequencies (< 2 MHz) where passive filters are bulky, with passive filtering for higher frequencies where active circuits struggle with bandwidth and stability.

Digital active EMI filtering leverages DSPs or FPGAs to implement sophisticated noise cancellation algorithms:

- Adaptive filtering using LMS (Least Mean Squares) or RLS (Recursive Least Squares) algorithms to adjust compensation for varying operating conditions automatically
- Multi-frequency cancellation targeting specific harmonic frequencies
- Predictive noise cancellation using switching state information to anticipate noise generation

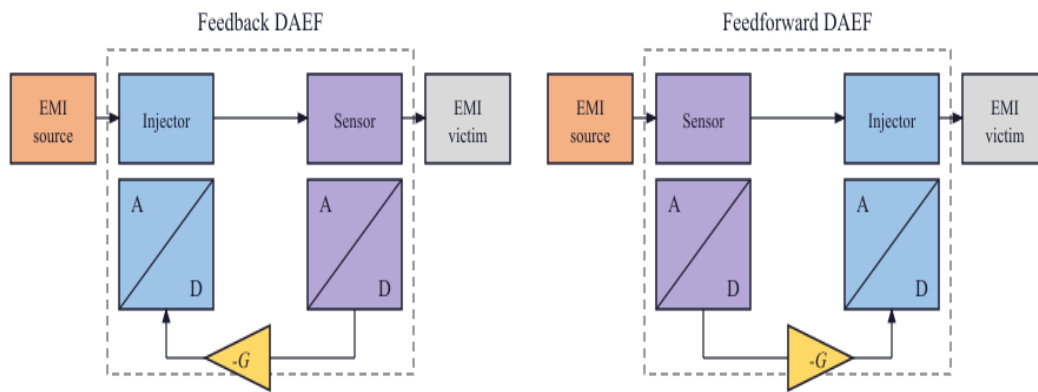


FIGURE 1.19: Digital Active EMI filtering, adapted from [150]

Layout-Based EMI Mitigation

PCB layout optimization provides "free" EMI reduction without additional components. Critical layout techniques include:

Critical loop area minimization: High di/dt loops must be minimized to reduce magnetic field emission and coupling. The loop inductance scales approximately with area:

$$L_{loop} \approx \mu_0 \frac{A_{loop}}{h} \quad (1.37)$$

where A_{loop} is the loop area and h is the conductor spacing.

Kelvin sensing connections: Separate gate drive sense and power return paths prevent common-source inductance from coupling switching noise into the gate drive circuit, which can cause false triggering or oscillations.

Guard rings and shields: Grounded copper pours surrounding sensitive analog circuits (gate drivers, control, feedback) provide shielding from radiated fields. Multi-layer PCBs with continuous ground planes reduce ground-loop impedance and improve shielding.

Differential signaling: Using differential pairs for high-speed digital signals (PWM, communication) improves noise immunity and reduces emissions through common-mode rejection.

1.10 GaN Devices for Motor Drives

This section examines why GaN devices are excellent for high-speed motor drives but poorly suited for conventional low-speed applications.

High-Speed Drive Advantages: GaN devices excel in high-speed motors ($> 10,000$ rpm) that require switching frequencies above 100 kHz. Their dramatically lower switching losses ($5\text{--}10\times$ better than silicon) enable efficient operation at these high frequencies, while reducing current ripple by up to $25\times$ compared to conventional drives. This results in better torque quality, lower motor losses, improved control bandwidth, and exceptional power densities exceeding 40 kW/L—nearly $3\times$ better than silicon-based drives.

Implementation Challenges: Fast switching speeds (> 50 V/ns) create bearing currents through parasitic coupling that can damage motor bearings, requiring mitigation through insulated bearings, common-mode chokes, or shaft grounding. Cable reflections can double terminal voltages, stressing motor insulation, while high-frequency harmonics increase core losses despite reduced current ripple. These issues require careful system-level design but are manageable in applications that benefit from high switching frequencies.

Why GaN Fails at Low Speed: Conventional low-speed drives ($< 5,000$ rpm) operate at fundamental frequencies around 50 Hz and need only 5–20 kHz switching—well within silicon’s capability. GaN’s high-frequency advantages go unused while its fast switching generates difficult EMI without benefit. The $2\text{--}5\times$ cost premium cannot be justified by the modest $< 2\%$ efficiency gains, leading to payback periods exceeding 8 years. Additionally, GaN’s higher on-resistance increases conduction losses at low frequencies, its low gate threshold (1.5–2.5 V) makes it noise-sensitive in industrial environments, and its fast transitions can damage motors designed for silicon drives.

Optimal Applications: GaN motor drives are economically and technically justified only in high-speed applications ($> 10,000$ rpm) where size, weight, and efficiency are critical—such as EV traction motors, turbochargers (50,000–150,000 rpm), machine tool spindles, and electric aircraft propulsion. For standard industrial motors operating at 900–3,600 rpm, silicon remains superior.

1.11 Conclusion

This comprehensive literature review examines the current state of research and development in wide-bandgap semiconductor technology, with particular emphasis on GaN devices and their applications in power electronics systems. The review has covered multiple critical aspects of this rapidly evolving field, from fundamental device characterization through advanced applications in motor drives and sophisticated control strategies.

The characterization of WBG devices is a foundational requirement for their successful deployment and requires specialized measurement techniques and systems that accurately capture their unique behavior. The transition from silicon to GaN technology necessitates fundamental changes in characterization

approaches, particularly for dynamic parameters such as on-resistance, switching losses, and frequency-dependent behavior.

Electromagnetic interference challenges in high-frequency GaN converters require comprehensive mitigation strategies that address both EMI generation and propagation. Digital active compensation techniques represent a promising approach to addressing these challenges, leveraging advanced signal processing to cancel EMI rather than simply filtering it.

Motor drive applications are among the most promising areas for GaN technology deployment, offering significant advantages in efficiency, power density, and dynamic performance. The benefits are particularly pronounced in high-speed applications where the fundamental frequency is already high, making the higher switching frequencies of GaN technology more attractive.

The future of GaN technology in power electronics appears very promising, with continued improvements in device performance, cost reduction, and expanding applications. However, several challenges remain to be addressed for widespread adoption, including cost considerations, technical challenges related to gate drive design and EMI management, and supply chain maturity. The research opportunities in this field are extensive, ranging from fundamental device physics and characterization techniques to system-level optimization and the development of new applications.

1.12 Motivation of the thesis

Despite their advantages, integrating WBG devices into practical converter systems presents significant challenges. High-speed switching exacerbates EMI generation, imposes stringent layout and gate-driver requirements, and demands advanced thermal management. Furthermore, achieving optimal system-level efficiency requires careful co-design of power stages, magnetic components, and control strategies. In this context, innovative topologies such as interleaved buck converters, Dual Active Bridge (DAB), and multilevel DAB architectures, combined with novel EMI suppression techniques such as Active EMI Filters (AEF), offer promising pathways to harness the full potential of WBG devices.

Additionally, emerging applications in on-board chargers (OBCs), high-speed drives, and power-dense DC-DC converters necessitate systematic evaluation of both device-level characteristics and system-level interactions. The motivation of this work is therefore to provide a comprehensive framework for the characterization, modeling, and application of WBG devices in a wide range of applications, focusing simultaneously on efficiency optimization and EMI mitigation.

1.13 Objectives

The primary aim of this research is to investigate the system-level application of WBG power devices in high-frequency converters and to identify strategies to maximize efficiency while minimizing EMI. To achieve this aim, the research objectives are defined as follows:

- **Characterization of WBG Devices:** Develop an embedded measurement platform for precise characterization of GaN and SiC devices, including switching and conduction losses
- **Analysis of GaN-based Converter Topologies:** Evaluate GaN implementation in two-level inverters, buck converters, and interleaved buck converters, identifying design challenges related to switching transients, losses, thermal management, and EMI.
- **Power Density Enhancement:** Explore the integration of coreless and high-frequency magnetic components to enhance power density without compromising efficiency.
- **Simulation of DAB and Multilevel DAB Converters:** Model and simulate DAB topologies for OBC applications to assess efficiency and voltage stress under various operating scenarios.
- **EMI Suppression Strategies:** Investigate the design and simulation of EMI suppression topologies to mitigate high-frequency emissions in WBG converter systems.

1.14 Thesis overview

The dissertation is structured to provide a coherent progression from foundational knowledge to practical contributions, as outlined below:

1. Introduction and state of the art: Presents the research motivation, background, and the scope of WBG devices in different applications. Reviews current state-of-the-art in GaN and SiC devices, converter topologies, EMI challenges, and control strategies, highlighting gaps in system-level integration.
2. Research and investigation methodology: Describes the modeling, simulation, and experimental methods used to characterize WBG devices, implement converter topologies, and analyze EMI suppression techniques.
3. Experimental results and findings: Reports key results from device characterization, converter simulations, and control algorithm evaluations, emphasizing efficiency gains and EMI reduction.
4. Conclusion: Interprets the findings in a system-level context, examining trade-offs between efficiency, power density, and EMI, and proposing design guidelines for WBG-based circuits and systems. Summarizes the research contributions, validates the achievement of objectives, and identifies avenues for future work in WBG power electronics.

Chapter Summary

Key Literature and Contextual Contributions

This chapter established the research context encompassing:

- **Technological Motivation:** Global CO₂ emissions trends and the role of WBG semiconductors in enabling higher-efficiency power conversion for sustainable energy systems
- **Material Advantages:** Comprehensive comparison of GaN and SiC against silicon, highlighting superior breakdown fields, thermal conductivity, and switching figures of merit
- **Converter Topologies:** State-of-the-art review of synchronous buck, interleaved buck, DAB, and multilevel DAB architectures for high-frequency WBG applications
- **EMI Challenges:** Analysis of EMI generation mechanisms in fast-switching GaN converters and mitigation strategies including passive filtering, active EMI filters, and layout-based techniques
- **Motor Drive Suitability:** Assessment of GaN device applicability in high-speed drives (>10 000 rpm) versus conventional low-speed applications, identifying the technical and economic boundaries
- **Research Gaps:** Identification of open challenges in system-level integration, frequency-dependent device characterization, and co-design of power stages with magnetic components and control strategies

Chapter 2

Research and investigation methodology

Chapter Overview

This chapter presents the research and investigation methodologies employed in this work for characterizing wide bandgap semiconductor devices and implementing GaN-based power electronic systems. The chapter structure follows: embedded measurement platform development and device characterization techniques, power converter design methodologies, passive component optimization and EMI suppression strategies.

2.1 GaN and SiC – Modeling and Characterization

This section presents the methodology employed to develop a dedicated embedded measurement to characterize wide bandgap (WBG) semiconductor devices combining hardware design, firmware implementation, and advanced signal processing.

Device and Controller Selection

Three commercial WBG devices representing different architectures and voltage ratings were selected for characterization. Tables 2.1 and 2.2 summarize the device specifications and optimized operating conditions.

TABLE 2.1: Wide Bandgap Device Selection and Key Specifications

Parameter	Units	GaN Cascode	GaN E-mode	SiC MOSFET
Voltage Rating	V	900	650	900
Current Rating	A	15	15	11.5
Device Type	–	Cascode	Enhancement	MOSFET
Technology	–	GaN HEMT	GaN HEMT	SiC
Package	–	TO-220	TO-220	TO-247

TABLE 2.2: Optimized Operating Conditions for Device Characterization

Parameter	Units	GaN Devices	SiC MOSFET
Supply Voltage, V_{dd}	V	60	50
Operating Current, I_d	A	0.4	2.0
Load Resistance, R_L	Ω	150	25
Frequency Range	kHz	10–1000	10–200
Duty Cycle	%	50	50
Operating Mode	–	Linear	Saturation

Selection Criteria:

- Device selected with comparable current ratings
- Higher bias current for SiC ensures saturation region operation
- Frequency limitation for SiC reflects device stress considerations

The measurement system utilizes an STM32H743ZI microcontroller [155] with advanced peripherals optimized for high-speed data acquisition. Table 2.3 details key specifications.

TABLE 2.3: STM32H743ZI Microcontroller Key Specifications

Feature	Specification	Reference
Core Architecture	ARM® Cortex®-M7 32-bit RISC	[155]
Operating Frequency	480 MHz	[155]
HRTIM Resolution	2.08 ns	[156]
ADC Channels	3×16 -bit SAR	–
ADC Sampling Rate	3.6 Msps	–
Floating Point Unit	IEEE 754 Compliant	[157]
DMA Channels	16	–
Flash Memory	2 MB	–
RAM	1 MB	–

The measurement system architecture is shown in Figure 2.1. The measurement system employs the constant current method to determine the threshold voltage, as described in [158]. With this method, the threshold voltage is calculated as the gate voltage corresponding to a predefined drain current. This constant drain current, $I_{d,c}$, is selected considering the current measurement uncertainty, u_i , and its value was chosen equal to 100 times u_i to avoid noise corruption. In order to calculate the threshold voltage variation in one period (ΔV_{th}), the device is switched with different duty cycles and the threshold voltage is calculated for every duty-cycle value, obtaining the variation in one period, as explained in [159].

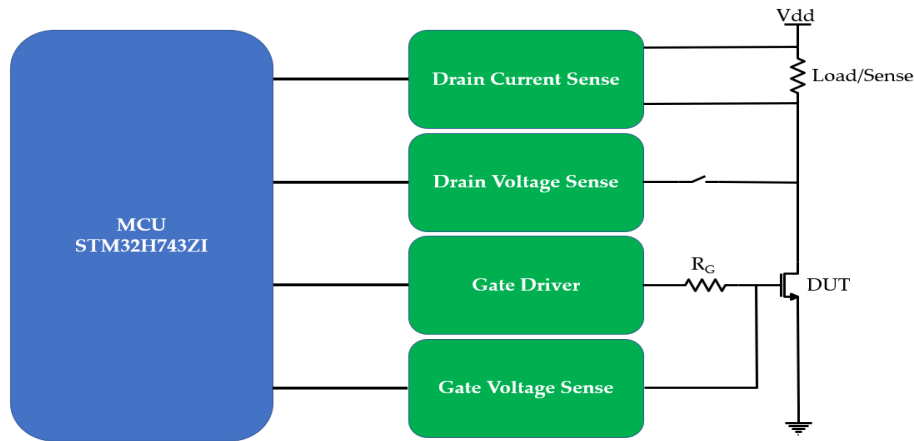


FIGURE 2.1: Measurement System Architecture

The realized hardware for the embedded measurement system is shown in Figure 2.2.

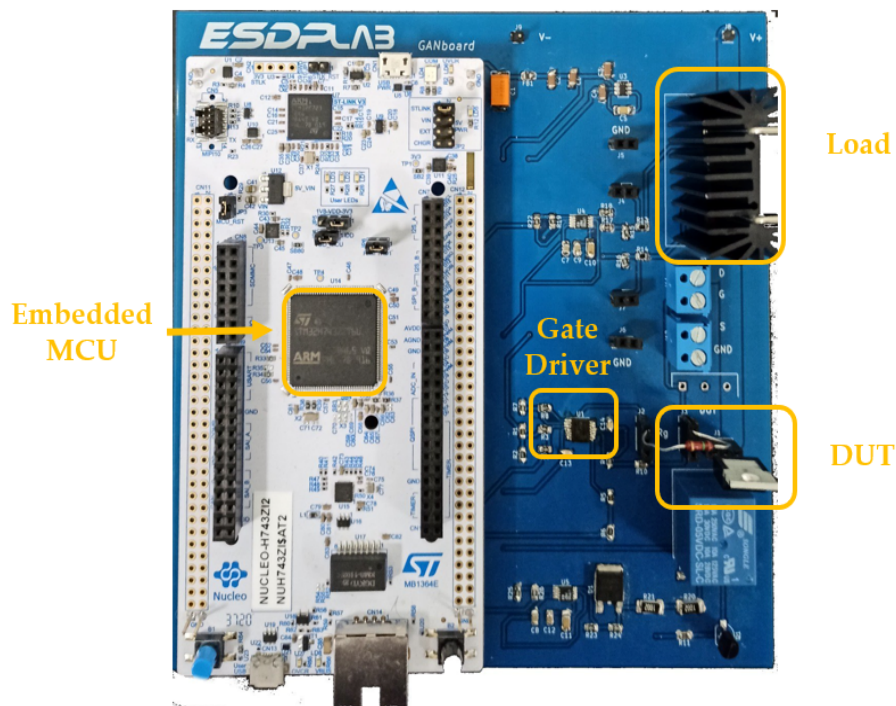


FIGURE 2.2: Embedded Measurement System Board

Signal Conditioning Circuits

Signal conditioning is critical for accurate measurement across the wide dynamic range of switching waveforms. Figure 2.3 illustrates the drain current sensing circuit. In this circuit, a pair of voltage dividers is implemented at each end of the sensing resistor. This configuration provides protection to the operational amplifier, which operates in differential mode, from the high voltage levels present at the DUT's power supply terminals. An additional advantage of employing these

voltage dividers is the enhancement of the amplifier's input impedance. The selected resistor values yield a differential input impedance exceeding $1.2\text{ M}\Omega$, which is substantially greater than the sensing resistor's value. This significant impedance difference effectively reduces measurement inaccuracies. The overall attenuation factor from the voltage drop across the sensing resistor to the "TO MCU" output terminal is 0.045.

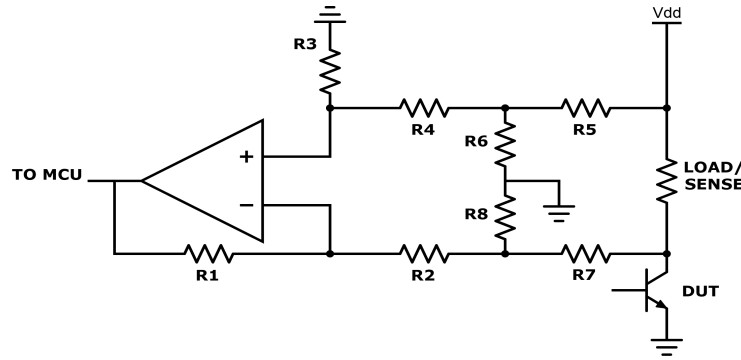


FIGURE 2.3: DUT's Current Sense Conditioning Circuit Schematics

The drain voltage sense circuit (Figure 2.4) addresses large voltage swings between off-state and on-state conditions using a SiC Schottky diode. Here, the main issue when measuring the DUT's drain voltage is its large difference between the off-state and on-state. As the focus is only on the drain voltage value during the on-state ($R_{DS,on}$ can be calculated from this value), instead of adopting a large voltage attenuation that would make the drain voltage in on-state indistinguishable from noise, a voltage clamp circuit was used. It is constituted by resistor R5 and a fast SiC Schottky diode. During off-state, the Schottky diode clamps the amplifier input voltage to its knee voltage, a few hundred mV. During the on-state, the drain voltage maintains below the Schottky threshold voltage and can be correctly measured. Consequently, in the off-state, the amplifier input voltage is the diode threshold and it is not considered, while in conduction state, the true drain voltage can be sampled. As can be seen from the schematics, a relay is connected between this stage and the DUT's drain in order to disconnect the drain when drain voltage measurements used for the extraction of the on-resistance are not performed. This choice is due to the fact that the diode stray capacitance can affect the drain voltage rising and falling time used for the extraction of the input capacitance. In fact, the adopted circuit introduces a minor attenuation of 0.976 that can be considered during data conditioning.

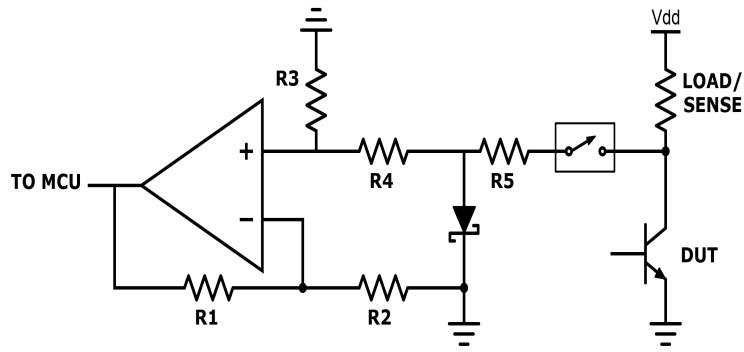


FIGURE 2.4: DUT's Drain Voltage Sense Conditioning Circuit Schematics

In Figure 2.5, the gate driver is shown. It is a non-inverting summing amplifier with the aim of shifting the input level from the MCU to the driving voltage range of the DUT.

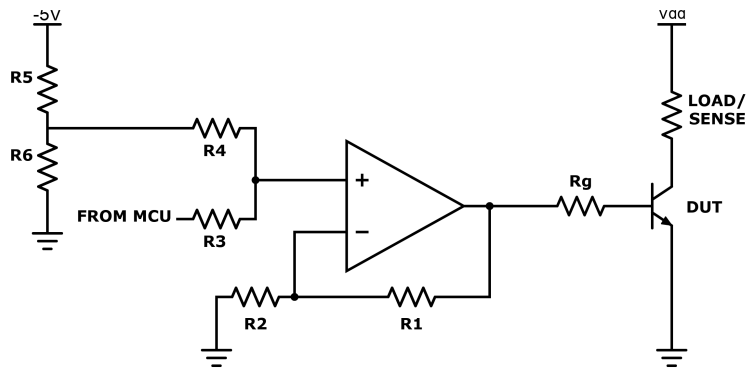


FIGURE 2.5: DUT's Gate Voltage Driving Circuit Schematics

The gate voltage sensing circuitry adopts a non-inverting unity-gain summing amplifier configuration with voltage divider output scaling to match ADC input ranges, as shown in Figure 2.6.

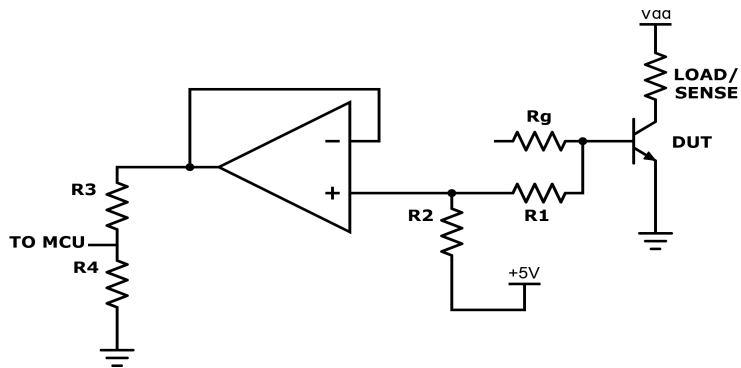


FIGURE 2.6: DUT's Gate Voltage Sense Conditioning Circuit Schematics

The employed circuit parameters are summarized in Table 2.4.

TABLE 2.4: Resistor values and amplifier models for each sensing/driving circuit.

Circuit	Resistor	Value	Op-Amp Model
Drain Current Sensing (Fig. 2.3)	$R_1 = R_2 = R_3 = R_4$	10 k Ω	LTC6360
	$R_5 = R_7$	604 k Ω	
	$R_6 = R_8$	40.2 k Ω	
Drain Voltage Sensing (Fig. 2.4)	$R_1 = R_2 = R_3 = R_4$	10 k Ω	LTC6360
	R_5	2.5 k Ω	
Gate Driver (Fig. 2.5)	R_1	50 k Ω	ADA4807-4
	R_2	10 k Ω	
	$R_3 = R_4$	100 k Ω	
	R_5	31.6 k Ω	
	R_6	22.1 k Ω	
Gate Voltage Sensing (Fig. 2.6)	$R_1 = R_2$	50 k Ω	ADA4807-4
	R_3	59 k Ω	
	R_4	100 k Ω	

The methodology focuses on three critical device parameters summarized in Table 2.5.

TABLE 2.5:
Key Performance Indicators and Measurement Techniques

Parameter	Method	Key Equation
ΔV_{th}	Constant Current	$I_{d,c} = 100 \times u_i$
$R_{DS,on}$	V/I Ratio	$R_{DS,on} = \frac{V_{DS}}{I_D} @ 90\% \text{ duty}$
C_{iss}	Time Constant	$C_{iss} = \frac{\tau}{R_G}, \tau @ 63\% V$

Equivalent Time Sampling Technique

To overcome ADC sampling rate limitations at high frequencies, an equivalent time sampling (ETS) technique was implemented [160]. Figure 2.7 illustrates this principle. By sampling at a frequency slightly different from the signal frequency, successive samples capture different phases of the periodic waveform, enabling reconstruction at equivalent rates much higher than the physical ADC sampling rate.

The governing equation for equivalent time sampling is:

$$T_S = T + T_{ET} \quad (2.1)$$

where T is the signal period and $T_{ET} = T/n$ is the incremental time step for n desired samples per period.

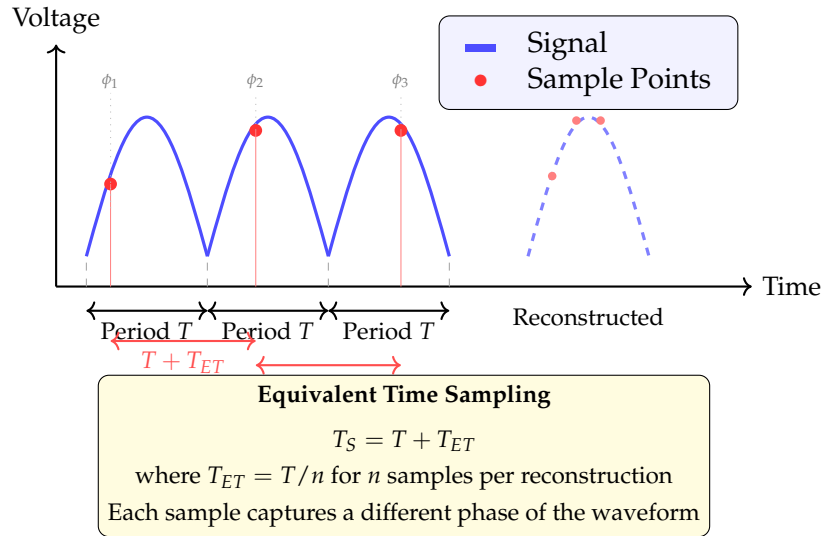


FIGURE 2.7: Equivalent time sampling technique [160].

Firmware Implementation

The measurement system firmware consists of a finite state machine formed by five different states, as shown in Figure 2.8. The system starts from peripheral initialization and calibration states, then it can run the other four states in looping sequence. After the peripheral initialization, the calibration procedure starts. This state exploits the ADCs feature of self-calibration present in the HAL libraries in order to increase the measurement accuracy.

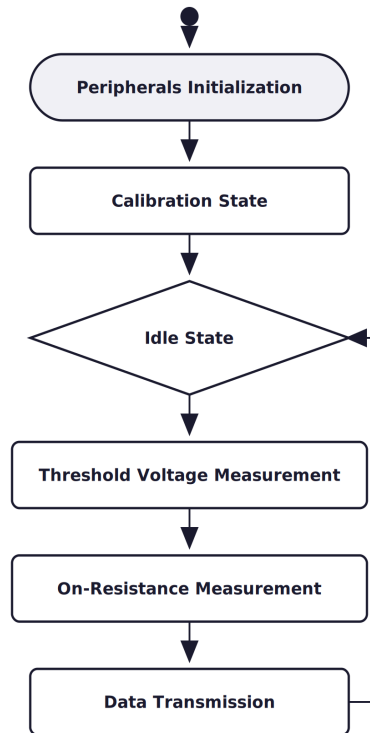


FIGURE 2.8: Measurement System Firmware Finite State Machine

Input Capacitance Characterization

This section presents experimental methodology for characterizing input capacitance in GaN HEMTs and SiC MOSFETs, focusing on dynamic behavior during switching operations. The experimental characterization utilized the custom-designed embedded measurement system.

TABLE 2.6: Input Capacitance Measurement Frequency Ranges and Limitations

Device Type	Frequency Range	Limitation Factor	Samples/Cycle
GaN E-mode HEMT	10 kHz–1 MHz	System bandwidth	100–1000
GaN Cascode	10 kHz–1 MHz	System bandwidth	100–1000
SiC MOSFET	10 kHz–200 kHz	Device thermal stress	200–2000

The methodology analyzes gate voltage transient behavior during device turn-on. Figure 2.9 illustrates the three distinct switching phases.

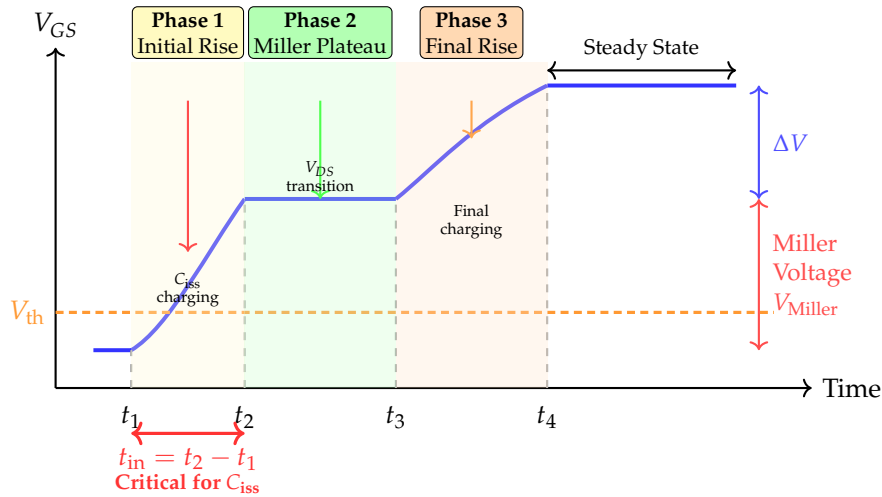


FIGURE 2.9: Gate voltage transient waveform during turn-on operation showing three distinct switching phases

- **Phase 1 (Initial Rise):** Gate voltage increases from zero to Miller plateau. Input capacitance C_{iss} charging dominates.
- **Phase 2 (Miller Plateau):** Gate voltage remains constant while V_{DS} transitions. Gate-drain capacitance C_{GD} effects dominate.
- **Phase 3 (Final Rise):** Gate voltage increases to steady-state after V_{DS} transition completes.

Figure 2.10 illustrates the sliding window analysis technique.

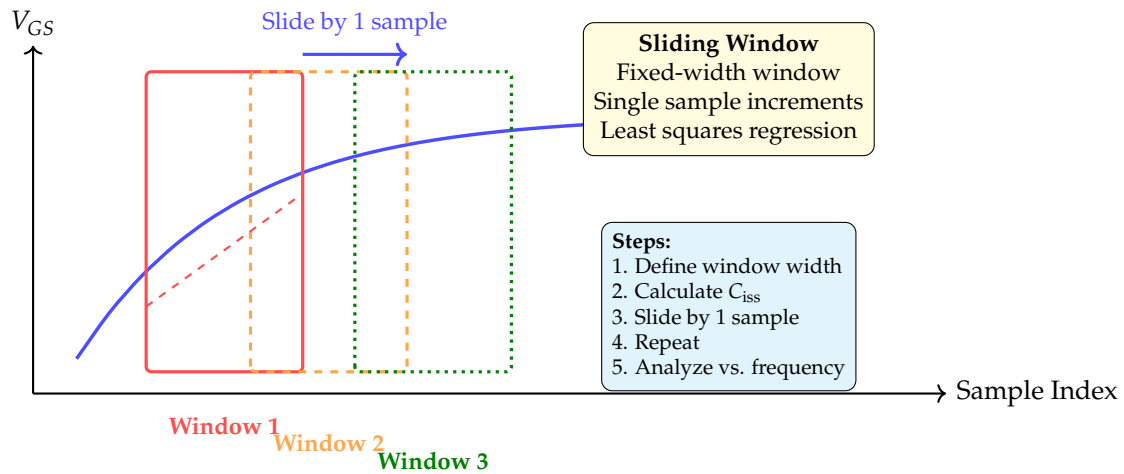


FIGURE 2.10:
Sliding window analysis technique for input capacitance extraction

The methodology can be summed up as follows:

1. **Define Analysis Window:** Select fixed width centered on voltage transition region
2. **Apply Least Squares Regression:** Calculate linear fit to determine dV_{GS}/dt
3. **Calculate Instantaneous Capacitance:** Using $I_G = C_{iss} \cdot dV_{GS}/dt$
4. **Increment Window:** Move window by single sample
5. **Iterate:** Repeat across entire transition time
6. **Frequency Analysis:** Perform across multiple frequencies

2.2 The converters' building block: the half bridge

This section presents comprehensive design methodology for GaN-based half-bridge inverters, covering gate driving strategies, auxiliary power supplies, protection schemes, and thermal management.

Gate driving strategy fundamentally determines switching performance and efficiency. Table 2.7 compares the two primary approaches.

TABLE 2.7:
Comparison of Gate Driving Strategies for GaN Half-Bridge Converters

Feature	Voltage-Mode	Current-Mode (Resonant)
Drive type	Voltage source	Constant current source
External components	Gate resistors + diodes	None (integrated)
Slew rate control	Fixed by R_G	Programmable
Miller clamp	External	Integrated
Turn-on time	> 50 ns typical	20–100+ ns
Complexity	Low	Medium
Cost	Low	Medium-High
Best application	Cost-sensitive	High-performance

The main characteristics of the chosen HEMT and gate driver IC are listed in Table 2.8. The HEMT was chosen with an higher voltage rating to provide margin for different application use-cases, from buck converter to three-phase traction inverter for motor drives.

Traditional gate drivers operate as voltage sources. Figure 2.11 illustrates the configuration.

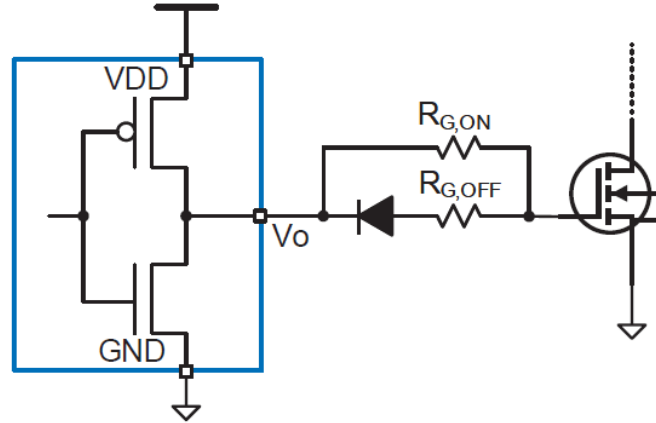


FIGURE 2.11: Voltage-mode gate driver

Peak gate current:

$$I_{G,peak} = \frac{V_{drive}}{R_G} \quad (2.2)$$

Slew rate (approximate):

$$\frac{dV_{GS}}{dt} \approx \frac{V_{drive}}{R_G \cdot C_{iss}} \quad (2.3)$$

The gate driving circuit must fulfill some fundamental requirements to prevent EMI, ringing and oscillations:

- Maintain gate drive simplicity and low component count to minimize propagation delay and parasitics;
- Layout optimized for the driver to be close to the power device, with the aim to minimize the gate loop parasitic inductance, particularly critical in GaN HEMT half bridges due to low threshold voltage and its variation during operating conditions;
- Choice between bootstrap supply or bipolar supply: this aspect is critical to assess the Miller effect mitigation strategy adopted and the possible choice to consider an isolated DC/DC to supply the auxiliary supply to the driving circuit, which can be expensive, bulky and not efficient.

In order to fulfill the application requirements of wide-voltage and current capabilities, as well as high switching frequency (1 MHz), the following device and gate driver IC were chosen.

TABLE 2.8: GaNPower GPIXV30DFN and Skyworks Si8273x Specifications

Parameter	Symbol/Unit	Value
GaNPower GPIXV30DFN GaN HEMT		
Drain-Source Voltage	V_{DS}	1200 V
Continuous Drain Current	I_D	30 A
On-Resistance	$R_{DS(on)}$	70 m Ω
Gate Threshold Voltage	$V_{GS(th)}$	1–1.7 V
Total Gate Charge	Q_g	11.2 nC
Output Capacitance	C_{oss}	79 pF
Reverse Recovery Charge	Q_{rr}	0 nC
Package Type	–	DFN 8×8
Thermal Resistance	$R_{\theta JC}$	0.9 °C/W
Skyworks Si8273x Gate Driver		
Input Supply Voltage	V_{IN}	4.5–5.5 V
Output Supply Voltage	V_{OUT}	Up to 24 V
UVLO Threshold	V_{UVLO}	4.0 V
Peak Source/Sink Current	$I_{SOURCE/SINK}$	4 A / 6 A
Rise/Fall Time	t_r/t_f	8 ns / 4 ns
Isolation Rating	–	5 kVrms
CMTI	–	200 kV/ μ s
Propagation Delay	t_{pd}	60 ns
Protection Features	–	Programmable dead time, Desat detection
Package Options	–	SOIC-16, DIP-16

The realized prototype was designed with isolated DC-DC auxiliary to provide a bipolar supply to the gate driving circuit, as shown in the schematics in Figure 2.12. The realized layout is shown in Figure 2.13, and its 3D view in Figure 2.14. The realized prototype is shown in Figure 2.15.

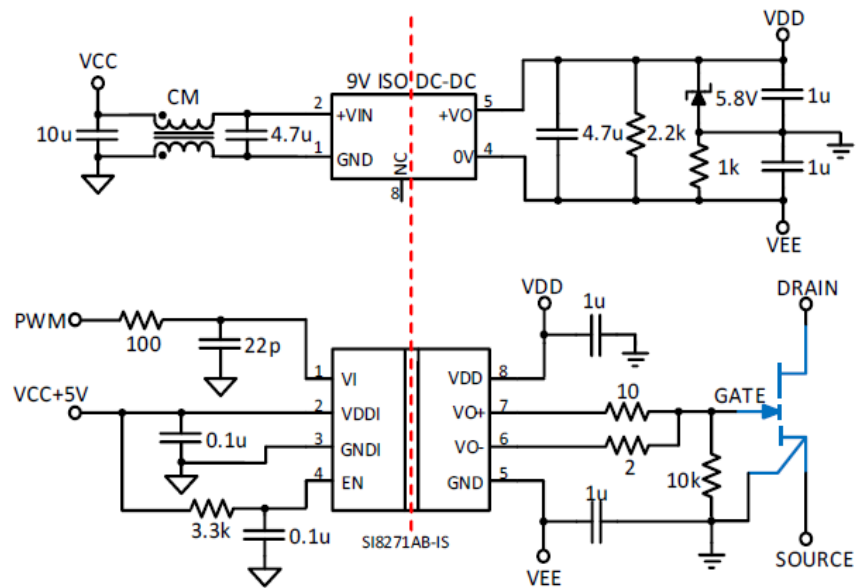


FIGURE 2.12: Gate driving circuit schematics

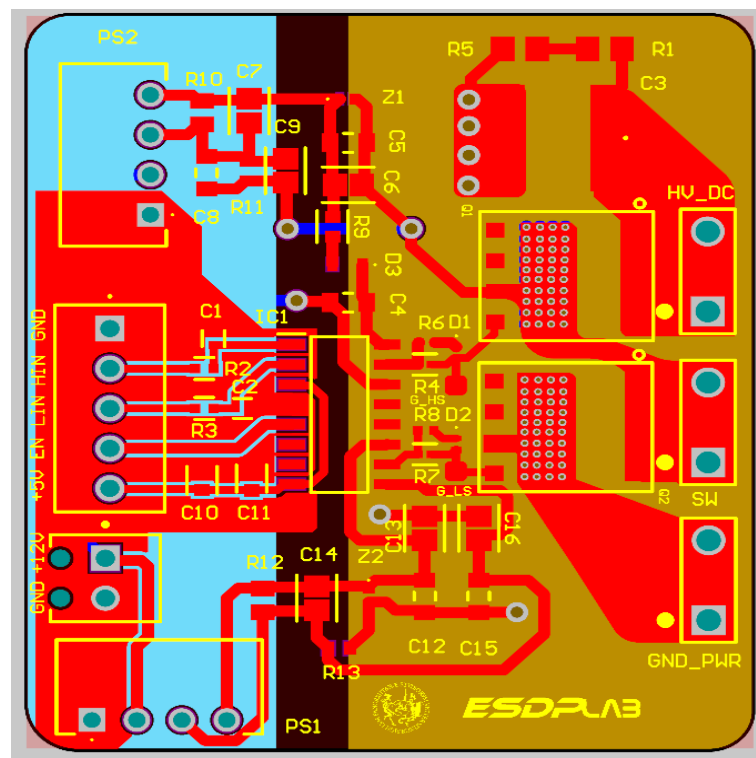


FIGURE 2.13: GaNPower-based Half Bridge Layout

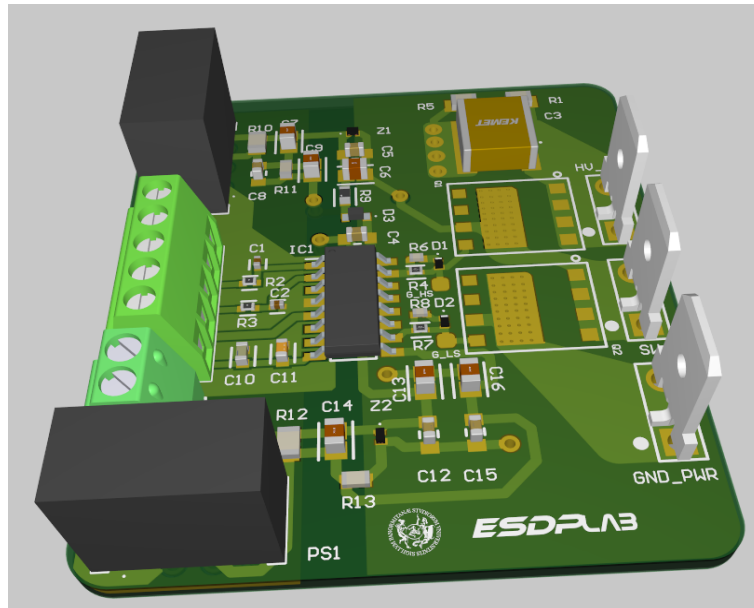


FIGURE 2.14: GaNPower-based Half Bridge 3D View



FIGURE 2.15: GaNPower-based Half Bridge Prototype

It has to be remarked the reduced area and enhanced power density of the design, $4 \times 4 \text{ cm}^2$ and 2250 W/cm^2 . Moreover, with the bipolar supply, the Miller effect which causes parasitic turn-on through gate-drain capacitance coupling, is effectively mitigated.

2.3 DC-DC Converter Topologies with GaN

This section presents comprehensive design methodology for three key DC-DC converter topologies optimized for GaN devices operating at multi-MHz switching frequencies.

2.3.1 Synchronous Buck Converter

The synchronous buck targets 48V to 24V conversion at 1-10 MHz. Design parameters are summarized in Table 2.9.

TABLE 2.9: Synchronous Buck Converter Design Parameters

Parameter	Symbol	Value	Notes
Input Voltage	V_{in}	48 V	Nominal
Output Voltage	V_{out}	24 V	Regulated
Duty Cycle	D	0.5	V_{out} / V_{in}
Switching Freq.	f_{sw}	1–10 MHz	Variable
Output Current	I_{out}	1–6 A	Load dependent
Inductor Value	L	2–3 μ H	For CCM
Output Cap.	C_{out}	4.7–22 μ F	Ceramic X7R
Input Cap.	C_{in}	10–47 μ F	Ceramic X7R

Buck Converter Design Equations:

Output voltage (ideal):

$$V_{out} = D \cdot V_{in} \quad (2.4)$$

Critical inductance for CCM:

$$L_{crit} = \frac{(1 - D) \cdot V_{out}}{2 \cdot f_{sw} \cdot I_{out}} \approx 3 \mu\text{H} @ 1 \text{ MHz}, 3 \text{ A} \quad (2.5)$$

Inductor current ripple:

$$\Delta I_L = \frac{V_{out}(1 - D)}{L \cdot f_{sw}} \quad (2.6)$$

2.3.2 Two-Phase Interleaved Buck Converter

The two-phase synchronous interleaved buck converter is as shown in Figure 2.16. Two buck converters are connected in parallel and operate in interleaved mode. The first converter is composed of inductor L_1 and power switches M_1 and M_2 , whereas the second converter consists of L_2 , M_3 and M_4 . The two-phase IBC share the same filter capacitor C_{out} at the output. With the two-phase IBC designs, the gating signals for the switch pair M_1 - M_2 and M_3 - M_4 are identical but shifted by 180°. The total output current I_o is the sum of the two inductor currents I_{L1} and I_{L2} .

The losses associated to the GaN are mainly due to two mechanisms: the switching losses that occur every time the low and the high-side switches turns on/off and the conduction losses, due to the non-zero resistance when the switching is closed. The switching losses are given by two fundamental contributions: the output capacitance losses of GaN and the crossover losses.

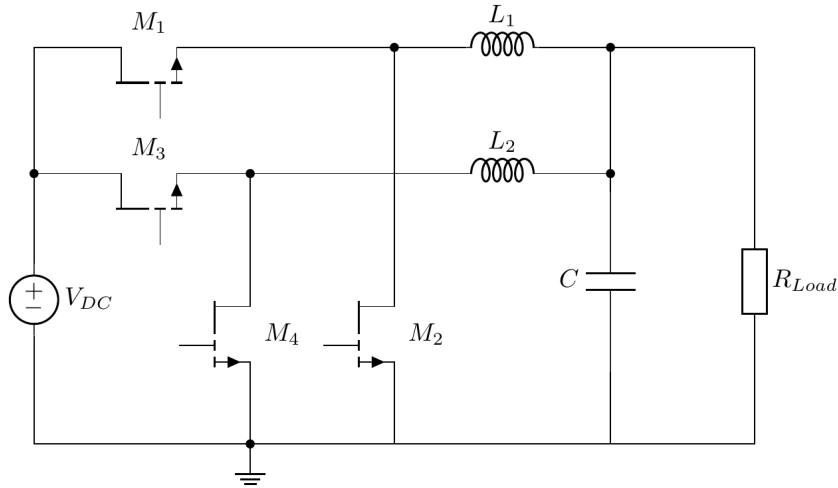


FIGURE 2.16: Two-phase interleaved buck schematics

The subsequent sections describe the working principle, modeling, and analysis of the two-phase interleaved buck-converter in terms of: DC transfer characteristics, inductor current ripple at steady-state, capacitor current, output voltage ripple, parasitics and efficiency as well as CCM-DCM boundary.

Working principle

The two-phase interleaved buck converter is composed of two single-phase buck converters connected in parallel. The synchronous rectification technology replaces the freewheeling diode with an active device, which avoids the loss of the diode and allows to reduce the output capacitance value and to improve the efficiency of the converter.

The two converters operate on the same switching frequency, but there will be a 180° phase shift between their switch-on times. The input current ripples of the two converters will cancel each other out on the power bus, thus reducing the fundamental and odd harmonic components of the summarized input current spectrum.

As a result, the currents in the inductors are shifted and the load current is the sum of the currents through the inductors L_1 and L_2 . This lead to a reduced load current ripple and improved power quality.

The working operation of this converter, supposed in continuous conduction mode, can be subdivided in different operating regions as a function of the duty cycle in continuous conduction mode.

If the duty cycle is 50%, there are only two states of operation, M1-M4 and M2-M3.

If the duty cycle is less than 50%, there are four operating states, namely M1-M4, M2-M4, M2-M3, M2-M4, of which two states are repeated, and there are only three working modes.

If the duty ratio is greater than 50%, there are four working modes, namely M1-M3, M1-M4, M1-M3, M2-M3, of which two states are repeated, and there are only three working modes.

The states M1-M4 and M2-M3 are symmetrical, so just one of them can be analyzed.

The last two cases are complementary and so the operating states that should be analyzed are just three: M1-M3 (Mode I), M2-M3 (Mode II) and M2-M4 (Mode III).

In Mode 1: M1 is turned on, the DC voltage is charged to the storage capacitor C through the M1 and the storage inductor L_1 , and the load is supplied with energy. M3 is turned on, and the DC voltage is passed through it. The inductor L_2 charges the storage capacitor C while providing energy to the load.

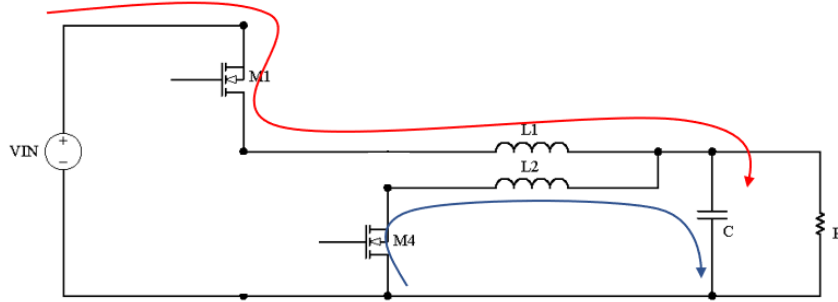


FIGURE 2.17: Working operation IBC: Mode I

In Mode 2: M1 is turned off, and the energy stored in the line inductor L_1 charges the output capacitor C through the M2 freewheeling, and simultaneously supplies energy to the load. M3 is turned on, and the DC voltage is passed. The energy storage inductor L_2 charges the storage capacitor C while providing energy to the load.

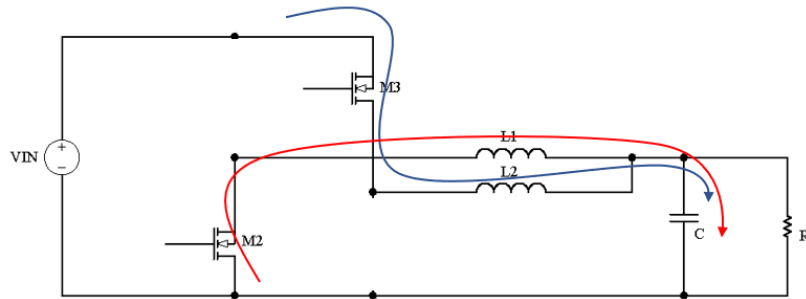


FIGURE 2.18: Working operation IBC: Mode II

In Mode 3: M2 is turned on, the output capacitor C is charged through the line inductor L_1 , and the load current decreases. The energy is charged to the storage capacitor C also through the M4 freewheeling diode.

In either case, the dc transfer characteristics of the two-phase interleaved buck converter is analogous to the single-phase topology, leading to:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (2.7)$$

Where D is the duty cycle of the driving gate signals, V_{OUT} the output voltage and V_{IN} the input voltage.

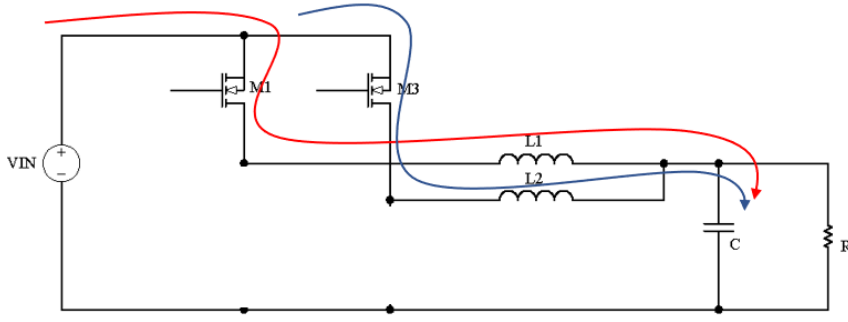


FIGURE 2.19: Working operation IBC: Mode III

Supposing two non-coupled inductors and with equal values $L_1 = L_2 = L$, there is no interaction between them, and the inductor current ripple is simply calculated as:

$$\Delta i_L = \frac{V_o}{L}(1 - D)T_S \quad (2.8)$$

On the other hand, since the output current is the sum of i_{L1} and i_{L2} , the output current ripple occurs twice during a given period T_S . The output current ripple is equal to:

$$\Delta i_o = \frac{V_o}{L}(1 - 2D)T_S \quad (2.9)$$

Hence, the output current ripple is reduced significantly with the two-phase case, and it has its maximum effect when D approaches 0.5, while the inductor ripples remain unchanged.

The ripple current flowing through the output capacitor is equal to the inductor current waveform with the dc component removed.

DC Transfer Characteristics

The buck ratio for this converter is identical to the conventional buck converter and equal to:

$$D = \frac{V_o}{V_{in}} \quad (2.10)$$

Including the effect of the ON-Resistance, the effective buck ratio becomes:

$$D_{EFF} = \frac{V_o + V_{R_{DS,on}}}{V_{in} - V_{R_{DS,on}}} \quad (2.11)$$

Where $V_{R_{DS,on}}$ represent the voltage drop across the semiconductor device when switched on.

Inductor current ripple at steady-state

For $D > 0.5$ the following expressions are governing the inductor current ripple: Mode I/IV (M1-M3):

$$\Delta i = \frac{V_{in}(1 - D)}{Lf_s}(2D - 1) \quad (2.12)$$

Mode II (M2-M3):

$$\Delta i = \frac{V_{in}(1 - D)}{Lf_s}(2D - 1) \quad (2.13)$$

Mode III (M1-M4):

$$\Delta i = \frac{V_{in}(1-D)}{Lf_s}(1-2D) \quad (2.14)$$

For $D < 0.5$ the following equations regulate the system:

Mode I (M1-M4):

$$\Delta i = \frac{V_{in}D}{Lf_s}(1-2D) \quad (2.15)$$

Mode II/IV (M2-M4):

$$\Delta i = -\frac{V_{in}D}{Lf_s}(1-2D) \quad (2.16)$$

Mode III (M2-M3):

$$\Delta i = \frac{V_{in}D}{Lf_s}(1-2D) \quad (2.17)$$

For $D = 0.5$:

Mode I (M2-M3):

$$\Delta i = -\frac{V_{in}D}{Lf_s}(1-D) \quad (2.18)$$

Mode II (M2-M4):

$$\Delta i = \frac{V_{in}D}{Lf_s}(1-2D) \quad (2.19)$$

Capacitor current

Neglecting the ESR of the output capacitor, in steady state the mean capacitor current is null:

$$\langle i_c(t) \rangle = I_c = 0 \quad (2.20)$$

The output voltage, in fact, has just a small ripple and:

$$i_o = \frac{v_o}{R} = \frac{V_o}{R} = I_o \quad (2.21)$$

$$i_c = i_L - i_o \approx i_L - I_o \quad (2.22)$$

$$I_c = I_L - I_o = 0 \quad (2.23)$$

Output Voltage Ripple

Neglecting the ESR of the output capacitor, the output voltage ripple can be calculated as follows:

$$\Delta Q = \frac{1}{2} \frac{T_s}{2} \frac{\Delta I_L}{2} = C \Delta V_o \quad (2.24)$$

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{1}{C} \frac{1}{2} \frac{\Delta i_L}{2} \frac{T_s}{2} \quad (2.25)$$

$$\Delta V_o = \frac{\Delta i_L T_s}{8C} \quad (2.26)$$

$$\Delta V_o = \frac{(1-D)V_o}{8CLf_s^2} \quad (2.27)$$

Or, with a relative expression:

$$\frac{\Delta V_o}{V_o} = \frac{(1-D)T_s^2}{8LC} = \frac{1-D}{8} \frac{(2\pi f_c)^2}{f_s^2} = (1-D) \frac{\pi^2}{2} \left(\frac{f_c}{f_s}\right)^2 \quad (2.28)$$

CCM-DCM boundary

TABLE 2.10:
CCM/DCM Boundary conditions

D = 0.5	R_{crit}	L_{crit}
Mode I	$R < \frac{2Lf_s}{1-D}$	$L > \frac{R(1-D)}{2f_s}$
Mode II	$R < \frac{2Lf_s}{1-D}$	$L > \frac{R(1-D)}{2f_s}$
D > 0.5	R_{crit}	L_{crit}
Mode I/IV	$R < \frac{2DLf_s}{(1-D)(2D-1)}$	$L > \frac{R(1-D)(2D-1)}{2Df_s}$
Mode II	$R < \frac{2DLf_s}{(1-D)(2D-1)}$	$L > \frac{R(1-D)(2D-1)}{2Df_s}$
Mode III	$R < \frac{2DLf_s}{(1-D)(1-2D)}$	$L < \frac{R(1-2D)}{2Df_s}$
D < 0.5	R_{crit}	L_{crit}
Mode I	$R < \frac{2Lf_s}{1-2D}$	$L > \frac{R(1-2D)}{2f_s}$
Mode II/IV	$R < \frac{2Lf_s}{1-2D}$	$L > \frac{R(1-2D)}{2f_s}$
Mode III	$R < \frac{2DLf_s}{(1-2D)(D+0.5)}$	$L < \frac{R(1-2D)(D+0.5)}{2Df_s}$

Losses and Efficiency with respect to parasitics

The power loss factors of a two-phase IBC are:

1. Conduction losses caused by $R_{ds,on}$: P_{ON-H}, P_{ON-L}

$$P_{ON-H} = \left[I_{out}^2 + \frac{(I_p - I_v)^2}{12} \right] R_{ds,on} \frac{V_{out}}{V_{in}} \quad [W] \quad (2.29)$$

$$P_{ON-L} = \left[I_{out}^2 + \frac{(I_p - I_v)^2}{12} \right] R_{ds,on} \left(1 - \frac{V_{out}}{V_{in}} \right) \quad [W] \quad (2.30)$$

$$\Delta i_L = \frac{V_{in} - V_{out}}{f_s L} \left(\frac{V_{out}}{V_{in}} \right) \quad (2.31)$$

$$I_p = I_{out} + \frac{\Delta i_L}{2} \quad (2.32)$$

$$I_p = I_{out} \quad (2.33)$$

2. Switching losses: P_{SW-H}, P_{SW-L}

$$P_{SW-H} = \frac{1}{2} V_{in} I_{out} (t_{r-H} + t_{f-H}) f_{sw} \quad [W] \quad (2.34)$$

$$P_{SW-L} = \frac{1}{2} R_{ds,on} I_{out} (t_{r-L} + t_{f-H}) f_{sw} \quad [W] \quad (2.35)$$

3. C_{oss} loss: P_{Coss}

$$P_{Coss} = \frac{1}{2} C_{oss-H} V_{in}^2 f_{sw} \quad [W] \quad (2.36)$$

$$C_{oss-H} = C_{DS-H} + C_{GD-H} \quad [F] \quad (2.37)$$

4. Deadtime loss: P_D

$$P_D = R_{ds,on} I_{out}^2 (t_{dr} + t_{df}) f_{sw} \quad [W] \quad (2.38)$$

5. Gate charge loss: P_G

$$P_G = (Q_{g-H} + Q_{g-L}) V_{gs} f_{sw} \quad [W] \quad (2.39)$$

$$P_G = (C_{GS-H} + C_{GS-L}) V_{gs}^2 f_{sw} \quad [W] \quad (2.40)$$

6. Operation loss IC control circuit: P_{IC}

$$P_{IC} = V_{IN} I_{CC} \quad (2.41)$$

7. Conduction loss in the inductors: $P_{L,(DCR)}$

$$P_{L,(DCR)} = I_{out}^2 DCR \quad [W] \quad (2.42)$$

8. Loss in capacitor $P_{C,in}, P_{C,out}$

$$P_{CAP_{ESR}} = I_{CAP_{RMS}}^2 ESR \quad [W] \quad (2.43)$$

$$I_{CIN_{RMS}} = I_{out} \frac{\sqrt{(V_{in} - V_{out}) V_{out}}}{V_{in}} \quad (2.44)$$

$$I_{COUT} = \frac{\Delta i_L}{2\sqrt{3}} \quad (2.45)$$

$$\Delta i_L = \frac{V_{in} - V_{out}}{f_{sw} L} \frac{V_{out}}{V_{in}} \quad (2.46)$$

In this way, the total power loss can be computed as:

$$P = 2P_{ON-H} + 2P_{ON-L} + 2P_{SW-H} + 2P_{SW-L} + 2P_{Coss} + 2P_D + 2P_G + P_{IC} + 2P_{L(DCR)} + P_{C(IN)} + P_{C(OUT)} \quad (2.47)$$

And the efficiency as:

$$\eta = \frac{V_{out} I_{out}}{V_{out} I_{out} + P} \cdot 100\% \quad (2.48)$$

TABLE 2.11: Interleaved buck parameters

Parameter	Value
V_{in}	48 V
V_{out}	12 V
I_{out}	10 A
F_{sw}	1 MHz
$R_{ds,on}$	65 m Ω
$L_{1,2}$	2.5 μ H
C	100 nF
R	1 Ω
$Deadtime$	50 ns

2.3.3 Dual Active Bridge (DAB) Converter

The Dual Active Bridge (DAB) converter has emerged as a prominent topology for bidirectional DC-DC power conversion applications, particularly in electric vehicle charging systems, energy storage interfaces, and renewable energy integration. The advent of wide-bandgap semiconductor devices, specifically GaN HEMT transistors, has enabled significant improvements in switching frequency and power density compared to traditional silicon-based implementations.

This section presents the development and validation of an average current mode control strategy for a single-phase two-level DAB converter employing GaN power devices operating at high switching frequencies. The primary objective of this control approach is to minimize the DC component of current flowing through the equivalent inductance and transformer, thereby preventing magnetic saturation and ensuring optimal converter operation across various loading conditions.

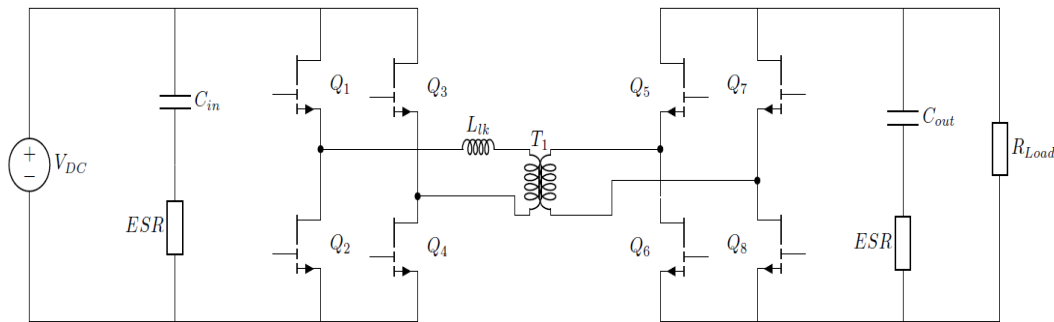


FIGURE 2.20: GaN-based 2-Level DAB

Converter Topology and Operating Principle

The two-level DAB converter consists of two full-bridge inverters connected through a high-frequency transformer and series inductance, as illustrated in Figure 2.20. Each bridge can generate two voltage levels ($+V_{dc}$ and $-V_{dc}$), and power flow is controlled through phase-shift modulation between the primary and secondary bridge outputs.

The basic operating principle relies on controlling the phase shift angle ϕ between the two bridges to regulate power transfer. When operating with Single

Phase-Shift (SPS) modulation, both bridges operate with 50% duty cycle, and the phase shift between them determines the magnitude and direction of power flow. Forward power flow occurs when the primary bridge leads the secondary bridge, while reverse power flow occurs when the secondary leads.

Small-Signal Modeling

The control development is based on a reduced-order modeling approach that captures the dominant dynamics relevant for controller design. The control-to-output voltage transfer function is derived using averaging techniques suitable for phase-shift modulated converters:

$$G_{v\phi}(s) = \frac{\hat{V}_2(s)}{\hat{\phi}(s)} = \frac{NV_1 f_{sw}}{2\pi^2 C_2} \cdot \frac{1}{s + \frac{1}{R_L C_2}} \quad (2.49)$$

where:

- N is the transformer turns ratio
- V_1 is the input voltage
- ϕ is the nominal outer phase shift
- f_{sw} is the switching frequency
- C_2 is the output capacitor
- R_L is the load resistance
- V_2, I_2 are the output voltage and current, respectively

This transfer function exhibits first-order behavior with a single pole determined by the output RC time constant. The DC gain is proportional to the input voltage and switching frequency, providing insight into the steady-state voltage regulation characteristics.

Dual-Loop Control Architecture

To achieve simultaneous regulation of output voltage and average inductor current, a dual-loop control structure is implemented with two independent PI controllers operating in parallel:

1. **Voltage Control Loop:** Regulates the output voltage V_2 by adjusting the phase shift ϕ between the two bridges
2. **Average Current Control Loop:** Maintains near-zero DC current through the series inductance by adjusting the duty cycles D_1 and D_2 of the primary and secondary bridges

The control architecture separates the voltage and current regulation objectives by exploiting different control variables. The phase shift primarily affects power transfer and output voltage, while duty cycle adjustments create voltage imbalances that compensate for asymmetries and eliminate DC current components.

The voltage PI controller is designed as:

$$C_v(s) = K_{p,v} + \frac{K_{i,v}}{s} \quad (2.50)$$

Similarly, the current PI controller takes the form:

$$C_i(s) = K_{p,i} + \frac{K_{i,i}}{s} \quad (2.51)$$

Controller parameters are tuned to achieve fast transient response while maintaining adequate stability margins. The voltage loop typically requires faster dynamics to respond to load variations, while the current loop operates at a slower bandwidth to suppress low-frequency DC drift.

Modulator Design

A specialized modulator translates the control signals from both PI controllers into appropriate PWM signals for the eight switches in the two full bridges. The modulator must generate:

- Phase-shifted PWM signals with variable phase angle ϕ (from voltage controller)
- Independent duty cycle control for each bridge D_1 and D_2 (from current controller)
- Proper dead-time insertion to prevent shoot-through
- Synchronization between all switching signals

The implementation ensures that the duty cycles can deviate from the nominal 50% value to create the voltage-time area imbalance necessary for DC current suppression, while the phase shift independently controls the net power transfer.

2.3.4 Three-Level ANPC DAB Converter

While two-level DAB converters offer excellent performance with GaN devices, voltage stress limitations become significant when operating at higher DC bus voltages (e.g., 800 V for modern electric vehicle architectures). Three-level topologies provide a pathway to reduce device voltage stress while maintaining or improving efficiency and power density.

The Active Neutral Point Clamped (ANPC) topology applied to DAB converters offers several advantages over conventional two-level implementations:

- Reduced voltage stress per switch (approximately half of DC bus voltage)
- Compatibility with lower-voltage GaN devices (e.g., 650 V rating for 800 V bus)
- Additional switching states for optimization
- Potential for improved efficiency through advanced modulation

This section explores the modeling, control, and optimization of three-level ANPC DAB converters, demonstrating both simplified control approaches that leverage two-level DAB techniques and advanced strategies that exploit the additional degrees of freedom.

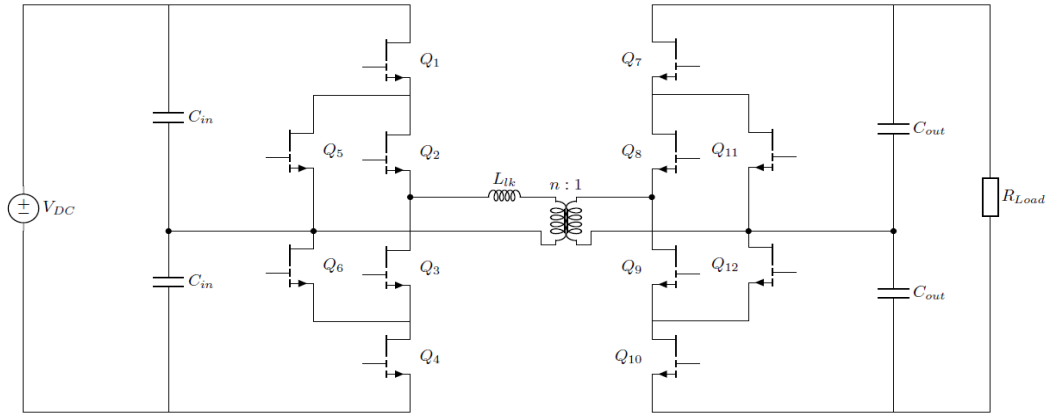


FIGURE 2.21: 3-Level ANPC DAB

ANPC DAB Topology and Operating Modes

The three-level ANPC DAB consists of two ANPC bridges (primary and secondary) connected through a high-frequency transformer and series inductance. Each ANPC bridge comprises eight active switches plus two clamping diodes, with split DC bus capacitors providing the neutral point connection.

Each bridge leg can produce three voltage levels: $+V_{dc}/2$, 0, and $-V_{dc}/2$, where V_{dc} is the total DC bus voltage. This capability is achieved through appropriate switching combinations that involve the clamping devices connecting the output to the neutral point for zero-voltage states.

Two-Level Operation Mode

By restricting the modulation to avoid zero-voltage states on both primary and secondary sides, the ANPC DAB can operate in a two-level mode. In this configuration, each bridge alternates only between $+V_{dc}/2$ and $-V_{dc}/2$, producing square-wave voltage outputs similar to conventional two-level DAB operation.

This simplified operating mode offers important advantages:

- Direct applicability of two-level DAB modeling and control algorithms
- Conventional Single Phase-Shift (SPS), Double Phase-Shift (DPS), and Triple Phase-Shift (TPS) modulation strategies remain valid
- Reduced control complexity compared to full three-level modulation

Control as Two-Level DAB: Simplified Approach

When controlled as a two-level DAB without zero states, the ANPC topology inherently divides voltage stress among devices through the split DC capacitor configuration. For an 800 V DC bus operation:

- Each DC bus capacitor maintains 400 V
- Maximum device voltage stress: $V_{ds,max} \approx 400$ V plus transient margins
- Safe operation with 650 V rated GaN devices

Proper voltage stress management requires:

1. **Capacitor voltage balancing:** Ensuring equal voltage division across split DC capacitors
2. **Clamping device selection:** Appropriate rating and thermal management
3. **Gate drive timing:** Coordinated switching to avoid voltage spikes

Under the assumption of balanced input and output capacitors, the clamping devices carry minimal current during switching transitions (or very low levels compared to main circuit currents). Consequently, the ANPC topology controlled as a two-level DAB does not suffer efficiency degradation despite the increased device count.

Control System Design

The control system follows the same dual-loop architecture developed for the two-level DAB:

$$\phi(t) = C_v(s) \cdot (V_{ref} - V_2) \quad (2.52)$$

$$D_1, D_2 = f(C_i(s) \cdot (0 - I_{L,avg})) \quad (2.53)$$

Controller tuning targets fast dynamic response, achieving transient settling on the order of a few milliseconds for voltage steps and rapid power flow reversals. The phase shift ϕ controls power magnitude and direction, while duty cycle adjustments maintain transformer DC flux balance.

Performance Characteristics

Simulation and analysis of the ANPC DAB controlled as a two-level system demonstrate:

- Efficiency at rated power: approximately 95%
- Voltage stress per device: well below 650 V breakdown voltage even at 800 V bus
- Fast transient response comparable to two-level DAB
- Bidirectional power flow capability maintained

However, at light loads, efficiency decreases due to fixed switching losses becoming proportionally larger. This motivated the investigation of advanced modulation strategies (TPS, Extended Phase-Shift) and optimization techniques to improve light-load efficiency.

The key finding is that ANPC topology provides increased output power capability without efficiency loss compared to two-level DAB when using the simplified control approach, while simultaneously reducing device voltage stress - an significant advantage for high-voltage applications.

Advanced Modeling Approaches

Conventional state-space averaging (SSA) assumes that state variables (such as inductor current) possess meaningful DC components over a switching period. In DAB converters, the average inductor current over a complete switching cycle equals zero during steady-state operation. Energy transfer occurs through AC current components, with power flow determined by the phase relationship between bridge voltages rather than duty ratio modulation.

The three-level ANPC DAB introduces additional complexity through:

- Multiple switching states per leg (three levels)
- Interleaved current paths through clamping devices
- Phase-shift-dependent power transfer mechanism

Traditional SSA effectively "filters out" the AC power transfer mechanism, rendering it unsuitable for direct application to DAB control design.

Generalized State-Space Averaging (GSSA)

Generalized State-Space Averaging extends conventional averaging by explicitly including AC components and harmonic content. For DAB converters, GSSA tracks state variables such as:

- Peak or RMS inductor current
- Fundamental harmonic amplitudes
- Instantaneous power flow
- Voltage ripple components

The GSSA approach derives continuous-time models where state variables directly relate to power transfer and can be linearized for small-signal analysis. This enables:

- Development of PI/PID controllers with systematic tuning
- State feedback and observer design
- Passivity-based or nonlinear control implementation
- Small-signal Bode plots for frequency-domain analysis
- Root locus stability assessment

For the three-level ANPC DAB, GSSA provides analytical insight into how phase shifts and duty cycles influence power flow and current stress, facilitating structured control development.

Piecewise Linear Modeling

The ANPC DAB operates in distinct modes depending on:

- Phase shift magnitude and direction
- Duty cycle relationships between bridges
- Zero-Voltage Switching (ZVS) region boundaries
- Capacitor voltage balance conditions

Piecewise linear (PWL) modeling captures each operating mode separately, providing:

- **Accurate constraint modeling:** ZVS boundaries, current limits, voltage stress
- **Nonlinear loss characteristics:** Conduction and switching losses per mode

- **Performance functions:** Efficiency, RMS current, thermal stress

PWL models enable mode-aware optimization while maintaining computational tractability. They are particularly valuable for:

1. **Look-Up Table (LUT) generation:** Precompute optimal operating points for real-time control
2. **Multi-objective optimization:** Balance efficiency, thermal stress, and capacitor balancing
3. **Constrained optimization:** Ensure ZVS operation and device rating compliance

The combination of GSSA for control design and PWL for optimization provides a comprehensive modeling framework for advanced ANPC DAB operation.

Voltage and Power Flow Control

Beyond the basic voltage regulation demonstrated with two-level operation, the three-level ANPC DAB supports direct power flow control. This mode is particularly relevant for applications requiring precise power management, such as:

- Grid-tied energy storage systems
- Vehicle-to-grid (V2G) interfaces
- Microgrid power sharing

Power control is implemented through a PI controller that regulates instantaneous power transfer:

$$\phi(t) = C_P(s) \cdot (P_{ref} - P_2) \quad (2.54)$$

where $P_2 = V_2 \cdot I_2$ is the measured output power. This approach provides direct authority over energy flow while maintaining DC current balance through the duty cycle control loop.

Battery Charging with CC/CV Strategy

Battery charging applications demand specialized control modes that transition between constant current and constant voltage operation. The implementation consists of:

1. **Constant Current (CC) Mode:**

$$\phi(t) = C_I(s) \cdot (I_{bat,ref} - I_{bat}) \quad (2.55)$$

Active when battery voltage is below the target voltage V_{nom}

2. **Constant Voltage (CV) Mode:**

$$\phi(t) = C_V(s) \cdot (V_{nom} - V_{bat}) \quad (2.56)$$

Active when battery reaches nominal voltage

3. **Mode Transition Logic:** Smooth handoff between CC and CV based on battery state

The battery was modeled using a high-fidelity dynamic model that includes two time constants representing fast and slow electrochemical dynamics. This model accurately captures:

- Open-circuit voltage as function of State-of-Charge (SOC)
- Internal resistance and polarization effects
- Transient response to current steps
- Capacity fade and aging characteristics (if parameterized)

Simulation results demonstrate successful CC/CV charging with smooth mode transitions and stable operation throughout the entire SOC range from 0% to 100%.

Predictive Peak Current Control with Frequency Variation **Motivation and Principle**

Transformer saturation remains a critical concern in high-power-density DAB converters, particularly when operating with high switching frequencies and compact magnetic components. While duty cycle modulation can address DC current components, peak current magnitude also influences core flux density and saturation risk.

An analytical investigation revealed an inverse relationship between peak inductor current and switching frequency:

$$I_{L,peak} \propto \frac{1}{f_{sw}} \quad (2.57)$$

This relationship suggests that dynamically adjusting switching frequency can provide an additional control variable for managing peak current and preventing saturation.

Predictive Control Implementation

A predictive current control strategy was developed, it provides the following features:

1. **Predicts** peak current for upcoming switching cycle based on current operating point
2. **Compares** predicted peak against saturation threshold
3. **Adjusts** switching frequency to maintain peak current below limit

The control algorithm computes the required frequency adjustment:

$$f_{sw,new} = f_{sw,nom} \cdot \frac{I_{L,limit}}{I_{L,predicted}} \quad (2.58)$$

Challenges and Ongoing Research

While the frequency variation approach demonstrates promise for saturation prevention, several challenges require further investigation:

- **Interaction with other control loops:** Frequency changes affect the voltage and power control loop dynamics

- **Stability concerns:** Variable frequency introduces time-varying system dynamics
- **Electromagnetic interference:** Frequency variation may spread spectrum but complicate EMI filter design
- **Magnetic design implications:** Core losses and transformer design must accommodate frequency range

This topic remains under active study, with ongoing work focused on stability analysis and experimental validation.

Multi-Objective Optimization for ZVS and Current Stress

The three-level ANPC topology provides multiple control variables (phase shifts, duty cycles, potentially zero-state insertion) that can be optimized to achieve competing objectives:

- **Zero-Voltage Switching (ZVS):** Minimize switching losses and EMI
- **RMS current minimization:** Reduce conduction losses
- **Peak current limitation:** Prevent magnetic saturation
- **Capacitor voltage balance:** Ensure equal stress distribution

The multi-objective optimization problem can be formulated as:

$$\begin{aligned}
 \min_{\phi, D_1, D_2} \quad & J = w_1 \cdot J_{ZVS} + w_2 \cdot J_{RMS} + w_3 \cdot J_{balance} \\
 \text{subject to} \quad & P_{out} = P_{ref} \\
 & |I_{L,peak}| \leq I_{sat} \\
 & V_{ds,max} \leq V_{breakdown} \\
 & |V_{C1} - V_{C2}| \leq \Delta V_{tol}
 \end{aligned} \tag{2.59}$$

where w_1, w_2, w_3 are weighting factors reflecting application priorities.

Trajectory Control for Operating Point Transitions

Moving between different operating modes (e.g., from non-ZVS to full-ZVS operation) requires careful trajectory planning to avoid:

- Excessive transient currents
- Temporary loss of ZVS
- Capacitor voltage imbalance
- Device overstress

Trajectory control optimizes the path through the control variable space (ϕ, D_1, D_2) to smoothly transition between operating points while satisfying constraints throughout the trajectory. This approach enables:

1. Adaptive operation across wide power range
2. Dynamic efficiency optimization

3. Load-dependent modulation strategy selection
4. Thermal management through current stress distribution

This research direction remains under active development, with promising preliminary results demonstrating improved efficiency and ZVS range compared to fixed modulation strategies.

Summary and Future Directions

The three-level ANPC DAB topology offers significant advantages for high-voltage GaN-based power conversion:

- Reduced device voltage stress enabling 650 V GaN devices for 800 V bus operation
- Simplified control leveraging two-level DAB techniques achieves 95% efficiency at rated power
- Advanced modeling approaches (GSSA, PWL) enable optimization and mode-aware control
- Multiple control strategies validated: voltage, power, CC/CV battery charging
- Ongoing research in predictive frequency control and multi-objective optimization

Future work will focus on:

1. Experimental validation of control algorithms on GaN hardware prototype
2. Complete development of GSSA-based small-signal models
3. Implementation and testing of multi-objective optimization with real-time computation
4. Light-load efficiency improvement through advanced modulation (TPS, EPS)
5. Thermal management strategies exploiting trajectory control

The combination of GaN devices and intelligent three-level topologies with advanced control represents a promising path toward next-generation power converters with unprecedented power density and efficiency.

2.4 Power Density Enhancement: Coreless Inductors

2.4.1 Design Methodology and Requirements

The development of coreless planar inductors for high-frequency power conversion applications represents a paradigm shift from traditional magnetic core-based designs. In this research, a systematic design methodology was established for a coreless inductor intended for integration in a GaN-based synchronous buck converter operating at 1 MHz switching frequency. The design process addresses the unique challenges posed by the absence of a magnetic core while leveraging the advantages of printed circuit board (PCB) fabrication techniques.

The fundamental design requirements were established to ensure compatibility with the target power converter application:

- Footprint area comparable to the converter power stage ($\sim 25 \text{ cm}^2$)
- Rated current capability of several amperes (up to 10 A)
- Inductance value of few microhenries (μH) to enable Continuous Conduction Mode (CCM) operation
- Thermal performance within acceptable limits for FR-4 substrate materials

The proposed design methodology comprises an iterative process that integrates electromagnetic simulation with geometric parameter optimization. The methodology begins with the selection of a target inductance value, followed by the establishment of geometric constraints to satisfy area requirements. Subsequently, the design undergoes electromagnetic simulation using either 2.5D planar electromagnetic solvers or full three-dimensional finite element method (FEM) analysis to extract the frequency-dependent inductance characteristics.

2.4.2 Geometric Configuration and Physical Parameters

A square spiral topology was selected for the coreless inductor implementation based on its inherent symmetry, efficient current distribution, and compatibility with standard PCB manufacturing processes. The geometric parameters of the realized structure are summarized in Table 2.12, with the key dimensional specifications detailed below.

TABLE 2.12: Coreless Inductor Design Parameters

Parameter	Value	Parameter	Value
Number of turns, N	17	Total length, $l \approx l_{\text{gap}}$	2 m
Outer diameter	5 cm	Inductance	$2.3 \mu\text{H}$
Inner diameter	1 cm	Fill factor	0.67
Trace width, w	1 mm	DC resistance, R_{DC}	0.25Ω
Copper thickness, t_{cu}	0.14 mm	Self-resonant frequency	$\sim 20 \text{ MHz}$
Trace spacing, s	0.25 mm	Skin depth at 1 MHz, δ	$65 \mu\text{m}$

The spiral geometry was fabricated on a standard FR-4 PCB substrate using 4 oz/ft² copper, corresponding to a copper thickness of $140 \mu\text{m}$. The fabrication was performed using a precision micro-milling process with a tolerance of $\pm 0.05 \text{ mm}$. The trace width was specifically designed to accommodate the maximum design current of 10 A while maintaining acceptable temperature rise within the thermal limits of the FR-4 substrate material (glass transition temperature of $130\text{--}140^\circ\text{C}$).

2.4.3 Electrical Modeling and High-Frequency Effects

The electrical behavior of the coreless inductor is characterized by frequency-dependent resistance and parasitic elements that significantly influence performance at megahertz frequencies. The DC and AC resistance models account for both conductive and high-frequency effects.

DC Resistance Model

The DC resistance of the copper spiral trace is determined by the fundamental relationship:

$$R_{DC} = \rho_{cu} \frac{l}{w \cdot t_{cu}} \quad (2.60)$$

where ρ_{cu} represents the resistivity of copper, l is the total conductor length, w is the trace width, and t_{cu} is the copper thickness. For the realized design, this yields a DC resistance of approximately 0.25Ω .

AC Resistance and Skin Effect

At switching frequencies in the megahertz range, the skin effect becomes a dominant factor influencing conductor losses. The AC resistance incorporates the effective penetration depth of current into the conductor:

$$R_{AC} = \rho_{cu} \frac{l}{w \cdot t_{eff}} = \frac{\rho_{cu} \cdot l}{w \cdot \delta \left(1 - e^{-\frac{t_{cu}}{\delta}}\right)} \quad (2.61)$$

where the skin depth δ is given by:

$$\delta = \sqrt{\frac{\rho_{cu}}{\pi f \mu_0 \mu_r}} \quad (2.62)$$

In these expressions, f denotes the operating frequency, μ_0 is the permeability of free space, and μ_r is the relative permeability of copper. At the design frequency of 1 MHz, the calculated skin depth is approximately $65 \mu\text{m}$, which is less than half the copper thickness, indicating that skin effect losses are non-negligible.

Proximity and Dielectric Loss Effects

For frequencies spanning 1 MHz to 50 MHz, multiple loss mechanisms must be considered beyond the skin effect:

Frequency Range 1–10 MHz: Within this range, the skin effect remains manageable ($\delta_{cu} \approx 66 \mu\text{m}$ at 1 MHz), but proximity effects between adjacent turns become significant. In compact PCB spiral geometries, proximity effects can increase the effective AC resistance by a factor of 2–3 compared to the skin-effect-only prediction. Dielectric losses in FR-4 substrate material remain secondary at 1 MHz but contribute to quality factor degradation in high-Q designs.

Frequency Range Above 10 MHz: As frequency increases beyond 10 MHz, the skin depth decreases substantially ($\delta_{cu} \approx 21 \mu\text{m}$ at 10 MHz), and proximity effects dominate the loss characteristics. Additionally, parasitic capacitances between turns and to the ground plane create resonant behavior that manifests as a sharp decline in quality factor. The self-resonant frequency (SRF) of approximately

20 MHz represents the frequency at which the inductive reactance is balanced by the parasitic capacitive reactance.

To accurately model dielectric losses in the electromagnetic simulations, the Svensson-Djordjevic dielectric loss model was implemented in Keysight ADS software, accounting for the frequency-dependent permittivity and loss tangent of the FR-4 substrate material.

2.4.4 Electromagnetic Simulation and Validation

Simulation Framework

The electromagnetic characterization of the coreless inductor employed a dual-simulation approach combining frequency-domain and time-domain analyses. Keysight Advanced Design System (ADS) was utilized for S-parameter extraction across a frequency range of 100 kHz to 50 MHz with 100 kHz resolution. The simulation environment incorporated:

- 2.5D planar electromagnetic (Momentum) analysis for initial design iteration
- Full three-dimensional finite element method (FEM) simulation for validation
- Frequency-dependent dielectric loss modeling using the Svensson-Djordjevic formulation
- Ground plane configuration to establish measurement reference planes

A critical aspect of the simulation setup involved the inclusion of a ground plane on the bottom PCB layer. This ground plane serves dual purposes: it provides the necessary return path for two-port vector network analyzer (VNA) measurements, and it represents the actual multilayer PCB configuration employed in the power converter implementation.

S-Parameter Measurement and Extraction

Experimental validation of the electromagnetic simulations was conducted using a Keysight vector network analyzer configured in a two-port measurement setup. The measurements were carried out in the 10 kHz-300 MHz range, however focusing on the first 50 MHz to catch the electromagnetic phenomena of interest (Self-Resonance and Conducted EMI). The calibration procedure established reference planes (RP1 and RP2) at the interface between coaxial cables and the subminiature version A (SMA) connectors mounted on the inductor test board. This calibration approach ensures that measured data represent only the inductor under test, with parasitic inductances associated with connectors removed through post-processing de-embedding procedures.

The inductance as a function of frequency was extracted from the measured S-parameters using the standard conversion:

$$L(f) = \frac{\text{Im}(Z_{11})}{2\pi f} \quad (2.63)$$

where Z_{11} is the input impedance derived from the S-parameters through the transformation:

$$Z_{11} = Z_0 \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \quad (2.64)$$

with $Z_0 = 50 \Omega$ representing the characteristic impedance of the measurement system.

2.4.5 Electromagnetic Interference Analysis

The absence of a magnetic core in planar inductor designs raises significant concerns regarding electromagnetic interference, as the magnetic field is no longer confined within a high-permeability material. To address EMI compliance and quantify potential interference with adjacent circuit components, a comprehensive three-dimensional finite element analysis was conducted using CST Studio Suite.

The EMI analysis employed a time-domain solver with the following configuration:

- Excitation: 20 V square wave at 1 MHz switching frequency
- Output loading: Capacitor and resistive load representing actual converter conditions
- Virtual voltage probes: Circular 1 cm diameter sensors positioned at 1 mm distance
- Probe locations: Active component layer (opposite side of PCB), coil side, and board sidewall
- PCB stack-up: Four-layer configuration with intermediate ground plane for shielding

The multilayer PCB structure was specifically designed with an intermediate copper plane serving as a magnetic shield between the coreless inductor (bottom layer) and active semiconductor devices (top layer). This shielding strategy aims to minimize inductive coupling between the high-frequency magnetic field and sensitive control circuitry.

EMI Compliance Evaluation

Spectral analysis of the induced voltages at the various probe locations was compared against the CISPR 32 / EN 55032 conducted emission limits for Class B equipment. The results demonstrate that:

- Maximum induced voltage magnitude: $0.5 \mu\text{V}$
- Frequency range of analysis: DC to 50 MHz
- Margin below peak limit: $>60 \text{ dB}$ across all measured harmonics
- Margin below average limit: $>70 \text{ dB}$ across all measured harmonics

These findings indicate that the electromagnetic emissions from the coreless inductor structure are negligible compared to the voltage levels present in the power conversion circuit (typically tens of volts). The multilayer PCB architecture with intermediate shielding plane effectively contains the magnetic field, ensuring EMI standard compliance even without a ferromagnetic core.

2.4.6 Thermal Considerations in Design

The current-carrying capacity and thermal management of the coreless inductor represent critical design constraints, particularly for applications requiring sustained operation at elevated current levels. The thermal design was established to maintain the maximum junction temperature of the GaN semiconductor devices below their rated limit of 150°C, while simultaneously ensuring that the FR-4 substrate temperature remains below its continuous operating temperature specification of 105–130°C.

The thermal resistance of the PCB-embedded inductor can be approximated through:

$$R_{th} = \frac{\Delta T}{P_{loss}} = \frac{T_{max} - T_{ambient}}{I_{DC}^2 R_{DC}(\theta)} \quad (2.65)$$

where $R_{DC}(\theta)$ represents the temperature-dependent DC resistance:

$$R_{DC}(\theta) = R_{DC,20} [1 + \alpha_{cu}(\theta - 20^\circ\text{C})] \quad (2.66)$$

with $\alpha_{cu} = 0.00393 \text{ K}^{-1}$ being the temperature coefficient of copper resistivity.

For the maximum design current of 10 A, the calculated power dissipation and temperature rise were verified through both analytical models and thermal imaging measurements. The 1 mm trace width with 140 μm copper thickness provides adequate thermal mass and heat spreading capability to maintain safe operating temperatures under continuous full-load conditions.

The research methodology employed in this investigation integrates computational electromagnetic analysis, experimental characterization, and thermal validation in a comprehensive framework:

1. **Design Synthesis:** Analytical formulations for inductance, resistance, and thermal performance guided initial geometric parameter selection.
2. **Electromagnetic Simulation:** Frequency-domain S-parameter extraction using 2.5D and 3D electromagnetic solvers validated the electrical characteristics from 100 kHz to 50 MHz.
3. **Experimental Validation:** Vector network analyzer measurements with calibrated reference planes verified simulation accuracy and provided empirical data for model refinement.
4. **EMI Assessment:** Time-domain finite element analysis evaluated conducted and radiated emission compliance with international EMC standards.
5. **Thermal Characterization:** Infrared thermal imaging under operational loading conditions quantified temperature distribution and validated thermal design margins.
6. **Application Integration:** Implementation in a functional GaN-based synchronous buck converter demonstrated real-world performance and enabled comparative evaluation against commercial ferrite-core alternatives.

This approach ensures that the coreless planar inductor design is thoroughly characterized across electrical, electromagnetic, and thermal domains, providing a robust foundation for integration into high-frequency power conversion systems.

2.5 EMI Suppression and ZVS-operation for GaN-based power stages

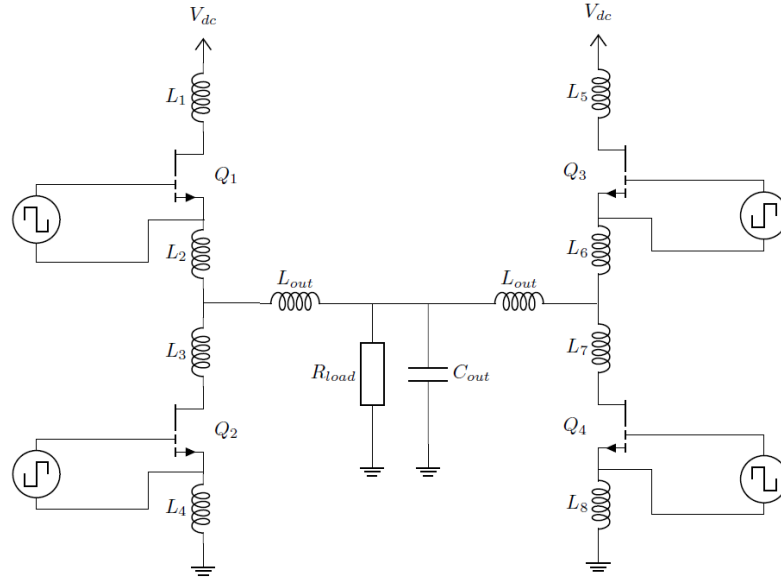


FIGURE 2.22: Double half bridge topology to achieve ZVS and ringing suppression

The double GaN half-bridge EMI compensation topology illustrated in figure 2.22 represents an advanced power conversion architecture that addresses several critical challenges inherent in high-frequency GaN-based switching converters. This topology employs two synchronized half-bridge stages operating in parallel, with each stage consisting of high-side and low-side GaN transistors (Q_1 - Q_2 and Q_3 - Q_4) connected through a series of layout parasitic inductors (L_1 - L_4 and L_5 - L_8). The output inductors (L_{out}) and load resistor (R_{load}) complete the power delivery path. The strategic placement of series inductors between the switching nodes serves as the key differentiating feature, enabling resonant compensation that mitigates electromagnetic interference while simultaneously improving several performance metrics.

One of the primary advantages of this compensation topology is its inherent capability for voltage ringing suppression at the switching nodes. In conventional hard-switching GaN half-bridges, the extremely fast switching transitions—enabled by GaN's low gate charge and output capacitance—create severe voltage overshoots and oscillations due to parasitic inductances in the power loop interacting with device capacitances. These high-frequency ringing events not only generate substantial conducted and radiated EMI but can also stress the devices beyond their rated voltage limits. The compensation inductors in this topology act as damping elements that slow down the current rate of change (di/dt) during transitions, thereby reducing the magnitude of voltage spikes according to $V = L(di/dt)$. This controlled transition effectively spreads the switching energy over a longer time period, transforming sharp voltage edges into smoother waveforms that contain significantly less high-frequency spectral content.

The topology also facilitates improved conditions for zero-voltage switching (ZVS) operation, particularly under light-load conditions where conventional GaN converters often lose soft-switching benefits. The series inductors store energy

during each switching cycle that can be utilized to discharge the output capacitances of the transistors before the complementary device turns on. This energy storage creates a more favorable trajectory for achieving ZVS across a wider operating range, reducing turn-on losses and further minimizing EMI generation. The ZVS capability is particularly valuable for GaN devices, which, despite their low switching losses compared to silicon counterparts, still benefit substantially from eliminating the capacitive discharge losses that occur during hard-switched turn-on events.

Another significant advantage lies in the topology's enhanced shoot-through prevention characteristics. The series inductors provide a natural current-limiting function during dead-time intervals or in the event of simultaneous conduction of both high-side and low-side devices. In a standard hard-switched half-bridge with negligible impedance between the DC bus and switching node, shoot-through events can result in catastrophic currents limited only by parasitic resistances and device on-resistances. The compensation inductors effectively insert impedance that restricts the fault current rise rate, providing additional safety margin and potentially allowing the gate driver or protection circuitry more time to respond. This feature is particularly relevant for GaN devices, which switch so rapidly that traditional dead-time optimization becomes increasingly challenging.

From an efficiency perspective, the topology presents a trade-off. The overall system efficiency can be improved through reduced EMI filter requirements, lower voltage stress on devices (allowing operation with higher margins from breakdown voltage), and the aforementioned ZVS benefits that reduce switching losses. Additionally, the smoother switching transitions result in lower gate driver losses since the gate charge is being supplied at a more controlled rate without the voltage ringing that can cause multiple charging/discharging events of the gate capacitance. However, these gains come at the cost of increased conduction losses and additional losses in the compensation inductors and potentially higher switching losses during the transition periods themselves, as the energy stored in the inductors must be dissipated or transferred with each cycle. The DC resistance of the compensation inductors introduces continuous I^2R losses that scale with load current, making this topology potentially less attractive for very high current applications where conduction losses dominate the loss profile.

Chapter Summary

Key Methodological Contributions

This chapter presented comprehensive methodologies encompassing:

- **Embedded Measurement Platform:** STM32H743ZI-based system for WBG device characterization with equivalent time sampling
- **Input Capacitance Characterization:** Sliding window analysis revealing frequency-dependent C_{iss} behavior critical for multi-MHz switching
- **GaN Half-Bridge Design:** Systematic methodology for gate driving, auxiliary power (bootstrap vs. isolated DC-DC), and Miller effect mitigation
- **DC-DC Converter Topologies:** Analysis of synchronous buck, two-phase interleaved buck, two-level and multilevel DAB converters
- **Coreless Inductor Design:** Direct synthesis approach for PCB-embedded planar inductors achieving high power density with thermal and EMI characterization
- **EMI Suppression:** Investigation on a double half-bridge soft switching topology as countermeasure for ringing and shoot-through phenomena

Chapter 3

Experimental results and findings

Chapter Overview

This chapter presents the experimental results and simulation findings obtained from WBG device characterization, coreless inductor integration, GaN-based converter prototyping, and advanced topology evaluation. The chapter structure follows: embedded measurement results for GaN and SiC figures of merit, coreless inductor design validation in a 1 MHz synchronous buck converter, interleaved buck simulation studies, Dual Active Bridge control validation with hardware-in-the-loop testing, three-level ANPC DAB analysis, and EMI suppression through a double half-bridge soft-switching topology with comparative performance benchmarking.

3.1 Characterization and modeling of WBG devices

An embedded measurement system was developed to characterize WBG power devices, specifically GaN HEMTs and SiC MOSFETs. The system employs an STM32H743ZI microcontroller with a HRTIM capable of 480 MHz clock frequency, enabling precise measurements across switching frequencies from 10 kHz to 1 MHz.

The microcontroller exploits three independent ADC channels with self-calibration capabilities to minimize measurement errors. An equivalent-time sampling technique was implemented to overcome the limitations of conventional sampling methods, allowing accurate waveform capture at high frequencies without requiring extremely fast ADC conversion rates.

Measurement Capabilities

The system measures three critical figures of merit:

Input Capacitance (C_{iss}): Calculated from the gate voltage rising time and external gate resistance:

$$C_{iss} = \frac{\tau}{R_G} \quad (3.1)$$

where τ is the time constant and R_G is the external gate resistance.

On-Resistance ($R_{DS,on}$): Measured during conduction state as the ratio between drain voltage and drain current, with a 90% duty cycle gate signal to ensure stable on-state conditions.

Threshold Voltage Variation (ΔV_{th}): Determined using the constant current method, where threshold voltage is extracted at a predefined drain current level (100 times the current measurement uncertainty).

Tested Devices

Three devices with different rated voltage and current were characterized:

- 900V 15A GaN Cascode
- 650V 15A GaN E-mode
- 900V 11.5A SiC MOSFET

For GaN devices, measurements were extended to 1 MHz with 60V supply and 0.4A operating current. The SiC MOSFET was tested up to 200 kHz with 50V supply and 2A current, due to device stress limitations.

TABLE 3.1: Tested device specifications and measurement conditions

Parameter	GaN Cascode	GaN E-mode	SiC MOSFET
$V_{DS,max}$ [V]	900	650	900
$I_{D,max}$ [A]	15	15	11.5
Test V_{supply} [V]	60	60	50
Test I_{bias} [A]	0.4	0.4	2.0
Max f_{test} [kHz]	1000	1000	200
Gate Voltage [V]	± 5	± 5	0-15

3.1.1 Key Findings

Input Capacitance Behavior: The input capacitance of all tested devices approximately doubled from their low-frequency values across the measured frequency range. This phenomenon is attributed to electron trapping occurring within the switching period. The increase in C_{iss} with frequency directly impacts switching losses according to:

$$P_s = \frac{1}{2} V_{ds} I_d f_s (t_{c(on)} + t_{c(off)}) \quad (3.2)$$

Where P_s are the switching losses, V_{ds} the drain-source voltage across the power device, I_d the drain current, f_s the switching frequency, $t_{c(on)}$ and $t_{c(off)}$ are the turn-on/off delay times.

On-Resistance Frequency Dependence: GaN devices exhibited a 25-30% increase in $R_{DS,on}$ at 1 MHz compared to 10 kHz values. In contrast, SiC devices showed minimal variation. This frequency-dependent behavior in GaN devices is linked to electron trapping and de-trapping time constants.

Threshold Voltage Instability:

- GaN Cascode: Negligible threshold voltage variation across the frequency range
- GaN E-mode: Hundreds of mV variation at high frequencies
- SiC MOSFET: Over 4V variation at increasing frequencies, attributed to electron tunneling in/out of the oxide

Measurement Accuracy

The system achieved high measurement precision:

- C_{iss} absolute uncertainty: 35 pF (worst case)

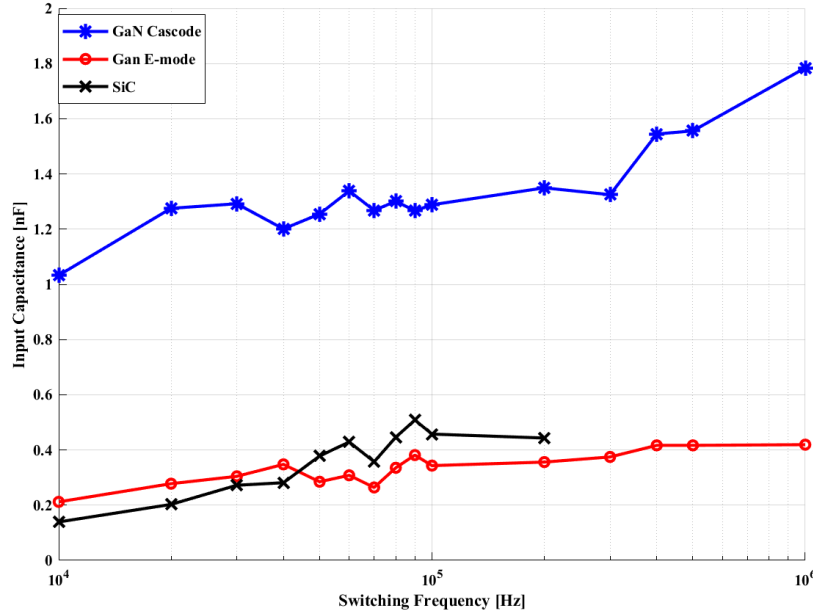


FIGURE 3.1: Input capacitance versus switching frequency for GaN Cascode, GaN E-mode, and SiC MOSFET.

- $R_{DS,on}$ absolute uncertainty: 0.022 m Ω
- ΔV_{th} relative uncertainty: 0.007%

TABLE 3.2: Measurement absolute uncertainty of device figures of merit

Figure of Merit	Uncertainty	Type
C_{iss}	35 pF (worst case)	Absolute
$R_{DS,on}$	0.022 m Ω	Absolute
ΔV_{th}	0.007%	Relative

Variance analysis over 100 measurements confirmed overall measurement errors below 2% for all key performance indicators. The equivalent-time sampling technique demonstrated accuracy well below 1‰ when validated through fixed-frequency sampling tests.

Physical Mechanisms

The frequency-dependent behavior observed in GaN devices is explained by electron trapping dynamics. The electron trapping time is orders of magnitude lower than de-trapping time. As frequency increases, both off-state and on-state times reduce, but the much shorter trapping time means electron de-trapping is primarily affected. This results in increased trapped electron populations at higher frequencies, leading to elevated $R_{DS,on}$ and threshold voltage variations.

For SiC devices, threshold voltage shifts result from electron tunneling mechanisms: negative shifts occur during off-state as electrons tunnel out of the oxide, while positive shifts occur during on-state as electrons tunnel back. With 0-15V gate voltage drive, positive variations dominate, resulting in substantial positive ΔV_{th} .

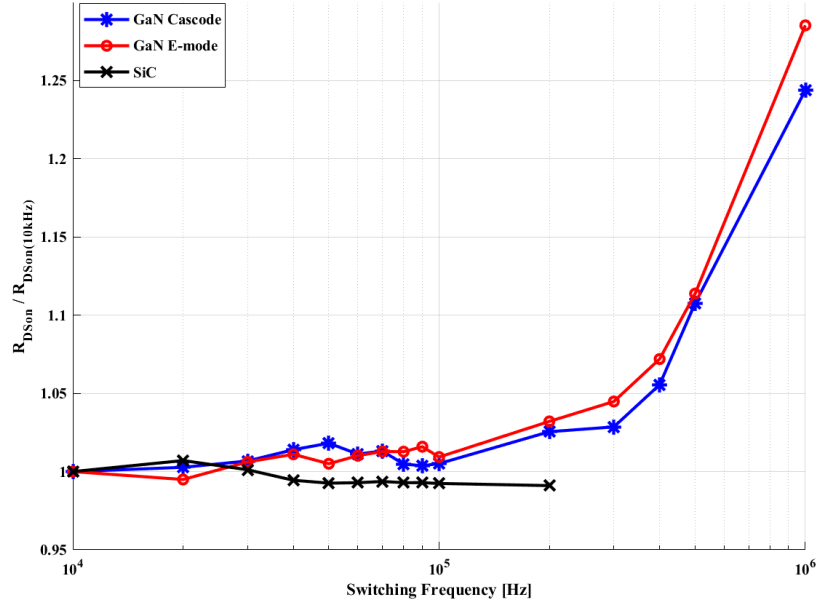


FIGURE 3.2: Normalized $R_{DS,on}$ with respect to $R_{DS,on}$ measured at 10 kHz as a function of switching frequency to extract frequency-dependent behavior.

3.2 Power density enhancement – Coreless inductors

Coreless planar inductors represent an innovative solution for power density enhancement in high-frequency GaN-based converters. These inductors, fabricated directly on PCB copper layers, eliminate magnetic core losses and saturation effects while enabling compact converter designs.

3.2.1 Design Methodology

A direct synthesis design approach was developed for coreless PCB inductors, consisting of:

1. Requirements Definition:

- Area comparable to converter power stage ($\sim 25 \text{ cm}^2$)
- Rated current of several amperes
- Inductance sufficient for Continuous Conduction Mode (CCM) operation

2. Geometric Parameter Selection:

- Trace width (w): 1 mm
- Inter-turn spacing (s): 0.25 mm
- Copper thickness (t_{cu}): $140 \mu\text{m}$ (4 oz/ft²)
- Number of turns (N): 17
- Outer dimension: 5 cm square spiral

3. Electromagnetic Simulation: Using Keysight ADSTM and CST Studio for S-parameter extraction and full-wave 3D analysis

4. Experimental Validation: Vector Network Analyzer (VNA) measurements from 100 kHz to 50 MHz

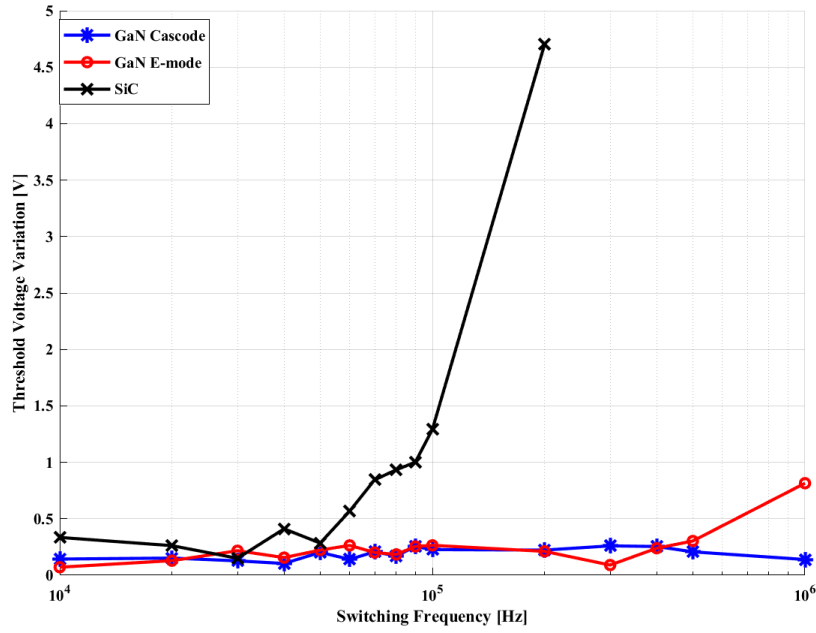


FIGURE 3.3: Threshold voltage variation (ΔV_{th}) versus switching frequency for tested devices.

3.2.2 Electrical Characteristics

The designed coreless inductor achieved the following parameters:

- Inductance: $2.3 \mu\text{H}$ at 1 MHz
- DC Resistance: 0.25Ω
- Self-Resonant Frequency (SRF): $\sim 20 \text{ MHz}$
- Skin depth at 1 MHz: $65 \mu\text{m}$
- Fill factor: 0.67

TABLE 3.3: Coreless inductor geometric and electrical parameters

Parameter	Value	Parameter	Value
Number of turns (N)	17	Total length (l)	2 m
Outer diameter	5 cm	Inductance	$2.3 \mu\text{H}$
Inner diameter	1 cm	Fill factor	0.67
Trace width (w)	1 mm	R_{DC}	0.25Ω
Copper thickness	0.14 mm	SRF	$\sim 20 \text{ MHz}$
Trace spacing (s)	0.25 mm	$\delta @ 1 \text{ MHz}$	$65 \mu\text{m}$

DC and AC resistance expressions were derived:

$$R_{DC} = \rho_{cu} \frac{l}{wt_{cu}} \quad (3.3)$$

$$R_{AC} = \rho_{cu} \frac{l}{w\delta(1 - e^{-t_{cu}/\delta})} \quad (3.4)$$

where $\delta = \sqrt{\frac{\rho_{cu}}{\pi f \mu_0 \mu_r}}$ represents the skin depth.

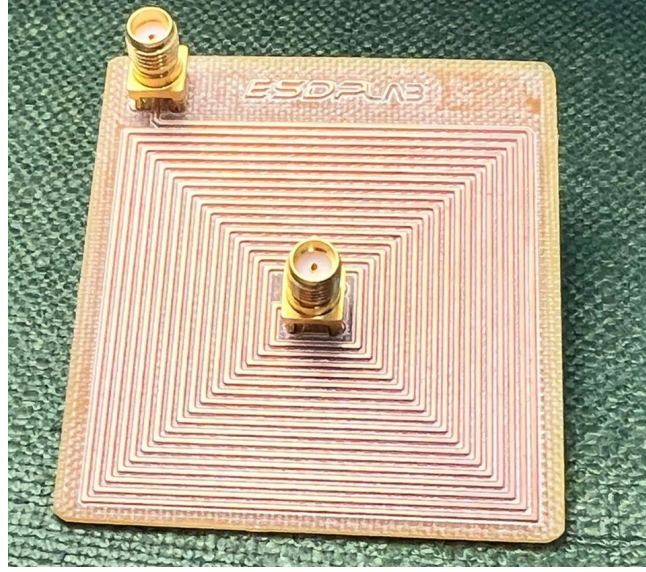


FIGURE 3.4: Realized coreless inductor prototype showing square spiral geometry on PCB.

3.2.3 High-Frequency Effects

At switching frequencies of 1 MHz and above, three phenomena significantly impact inductor performance:

Skin Effect: Current distribution shifts toward conductor surface. At 1 MHz, skin depth is approximately $66 \mu\text{m}$, manageable for $140 \mu\text{m}$ copper thickness.

Proximity Effect: In compact PCB spirals, proximity effect can double or triple R_{AC} , becoming dominant over skin effect in tightly spaced designs.

Dielectric Loss: Modeled using Svensson/Djordjevic loss model for FR-4 substrate. Secondary effect at 1 MHz but increasingly significant above 10 MHz.

3.2.4 Comparison with Ferrite-Based Inductors

A comprehensive comparison was performed between the coreless design and commercial ferrite inductors:

TABLE 3.4: Comparison between coreless and ferrite-based power inductors

Parameter	Coreless	Inductor #1	Inductor #2
L [μH]	2.3	2.2	2.2
I_{sat} [A]	~ 20	2.2	10
SRF [MHz]	20	92.6	58
Volume [mm^3]	$50 \times 50 \times 1.6$	$12 \times 4 \times 2.25$	$24 \times 16 \times 5.45$
Weight [g]	2.5*	0.056-0.065	1.6
Cost [€/unit]	0.84	0.25	1.00

*Effective copper weight, integrated in converter PCB

Advantages of Coreless Design

No Saturation: Unlike ferrite cores, coreless inductors maintain constant inductance regardless of current level, eliminating current peaks and associated instability.

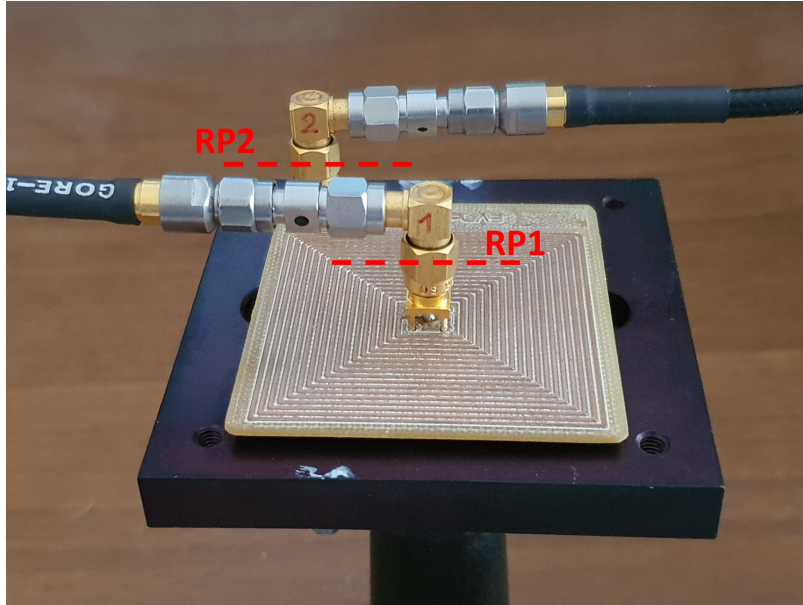


FIGURE 3.5: Coreless Inductor VNA measurement test setup with reference planes

No Core Losses: Absence of magnetic hysteresis and eddy current losses results in superior high-frequency performance. Magnetic losses in ferrite cores increase linearly (hysteresis) and quadratically (eddy currents) with frequency.

Linear Behavior: Current waveforms remain triangular across all operating conditions. Ferrite inductors in quasi-saturation exhibit cusp-shaped current waveforms with increased harmonic content.

Thermal Performance: At 6A output current, the coreless inductor operated approximately 20°C cooler than commercial ferrite inductors, remaining below 60°C compared to 72-78°C for ferrite designs.

Harmonic Content: Frequency spectrum analysis at 1.65 Ω load showed:

- Coreless: 1st harmonic 0.53A, 2nd harmonic 75.64 mA (14.1%)
- Inductor #1: 1st harmonic 1.3A, 2nd harmonic 205 mA (15.7%)

3.2.5 Design Challenges

Size and Weight: Coreless designs require larger area and have higher weight compared to miniaturized ferrite inductors, impacting power density.

EMI Considerations: Unconfined magnetic field requires careful layout. EMI analysis using CST 3D simulation demonstrated that with proper multilayer PCB shielding (intermediate copper plane), induced voltages remain below 0.5 μ V, meeting CISPR32-EN5032-CE compliance limits.

Thermal Management: At maximum rated current (10A), extrapolated temperature reaches approximately 110°C, requiring consideration of FR-4 glass transition temperature (130-140°C) and continuous operating temperature limits (105-130°C).

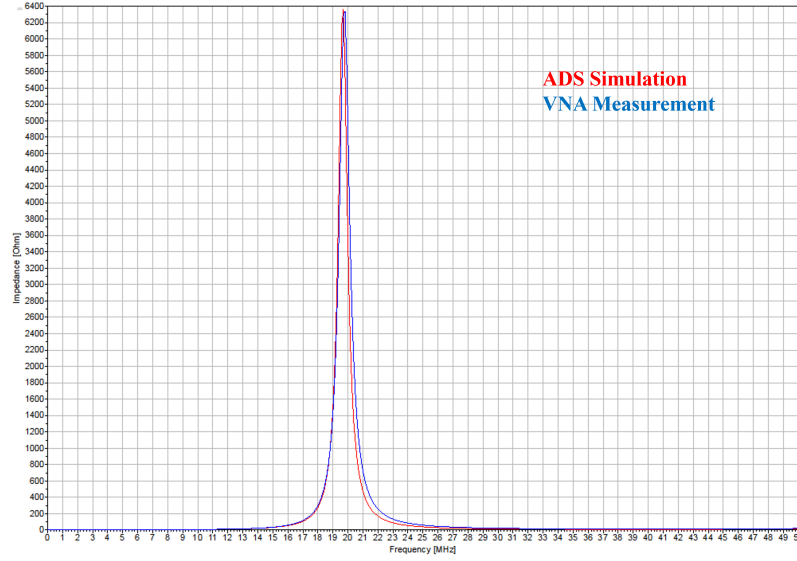


FIGURE 3.6: Real part of impedance comparison between ADS simulation and VNA measurement

The coreless inductor was successfully integrated into a 1 MHz GaN-based synchronous buck converter with specifications:

- Input voltage: 20V
- Output voltage: 10V
- Output current: 1-6A
- Switching frequency: 1 MHz
- Deadtime: 50 ns

Load Resistance (Ω)	Current (A)	Inductance (μH)
10	1	2.64
6.6	1.5	2.81
3.3	3	2.92
1.65	6	3.09

TABLE 3.5: Inductance extracted from experimental waveforms under various load conditions

The slight increase with current and temperature demonstrates stable, predictable behavior suitable for high-frequency converter applications.

3.3 Synchronous Buck at 1 MHz switching frequency

A comprehensive design methodology for GaN-based synchronous buck converters operating at 1 MHz switching frequency was developed and experimentally validated. The converter integrates the coreless planar inductor with GaN HEMT active devices.

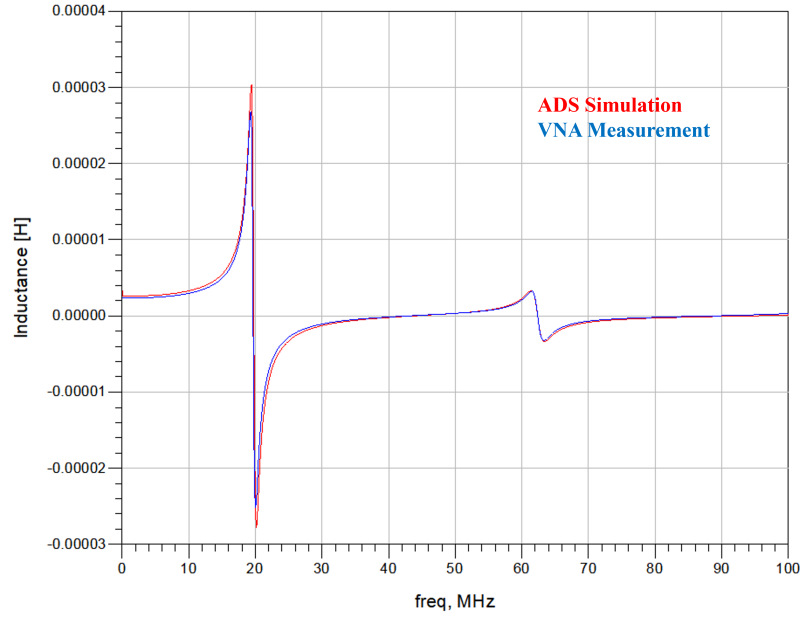


FIGURE 3.7: Inductance comparison between ADS simulation and VNA measurement

3.3.1 Converter Specifications

The synchronous buck converter was designed with the following specifications:

TABLE 3.6: Synchronous buck converter design specifications

Parameter	Value	Parameter	Value
V_{IN}	20 V	f_{sw}	1 MHz
V_{OUT}	10 V	Deadtime	50 ns
D_{eff}	~ 0.5	$R_{DS,on}$ (HS/LS)	70 m Ω
R_L	10 Ω	$V_{GS,on}$	70 mV
I_{OUT}	1 A	L	$> 2.3 \mu H$
P_{OUT}	10 W	C	390 nF

GaN HEMTs: GaNPower GPIXV30DFN devices were selected for the half-bridge configuration, featuring:

- Low on-resistance enabling reduced conduction losses
- Fast switching transitions suitable for 1 MHz operation
- Minimal gate charge reducing switching losses

Gate Driver: Skyworks Si8273x isolated gate driver provides:

- Galvanic isolation between control and power stages
- Precise deadtime control through STM32H743ZI HRTIM (2.08 ns resolution)
- Sufficient drive current for rapid gate charging

Inductor Design:

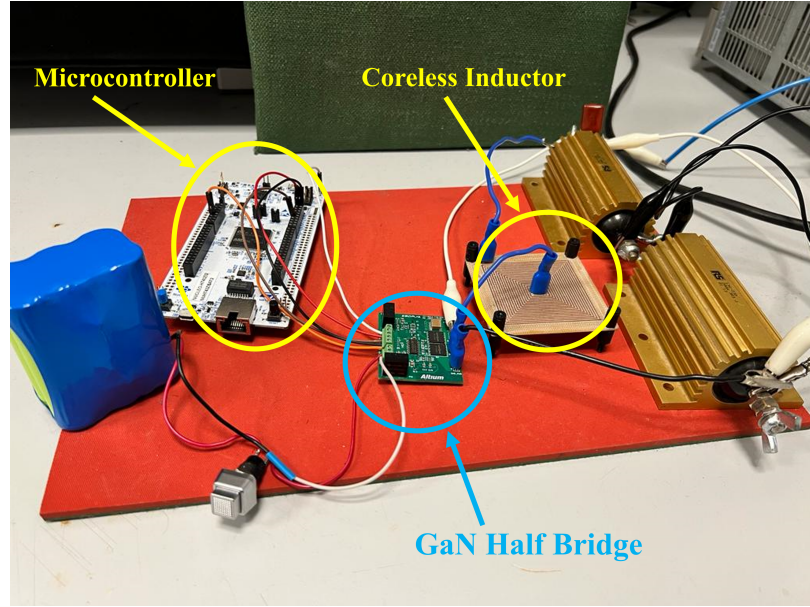


FIGURE 3.8: Synchronous buck testbench setup with coreless inductor

The critical inductance for CCM operation was calculated as:

$$L_{critical} = \frac{R(1-D)}{2f_{sw}} \approx 2.3 \mu H \quad (3.5)$$

The coreless planar inductor was designed with margin above this value to ensure robust CCM operation across load variations. The final design achieved 2.3-2.5 μH depending on operating conditions.

Output Capacitor Selection:

The output capacitor was sized to provide significant filtering of switching ripple. Selection criteria:

- Impedance much smaller than load at switching frequency
- Sufficient capacitance to absorb inductor ripple current
- Low ESR to minimize output voltage ripple

One order of magnitude margin was applied, leading to 390 nF ceramic capacitor selection. This provides adequate filtering while maintaining compact size.

3.3.2 Loss Analysis

Power losses were categorized into conduction and switching components:

Conduction Losses:

$$P_{on} = R_{DS,on} I_0^2 \frac{t_{on}}{T_s} \quad (3.6)$$

The frequency-dependent $R_{DS,on}$ behavior observed in device characterization was incorporated:

- At 10 kHz: baseline $R_{DS,on}$

- At 1 MHz: 25-30% increase for GaN devices
- Minimal variation for SiC devices

Switching Losses:

$$P_s = \frac{1}{2} V_{ds} I_d f_s (t_{c(on)} + t_{c(off)}) \quad (3.7)$$

Switching losses remain linear with frequency up to approximately 500 kHz, then increase more rapidly due to:

- Increased input capacitance at higher frequencies
- Parasitic effects in PCB layout
- Resonance phenomena approaching device and circuit natural frequencies

3.3.3 Experimental Validation

Test Setup:

- STM32H743ZI microcontroller for PWM generation
- GaN half-bridge prototype board
- Variable resistive loads: 10, 6.6, 3.3, 1.65 Ω
- Thermal imaging camera (FLIR C5) for temperature monitoring
- Oscilloscope for waveform capture

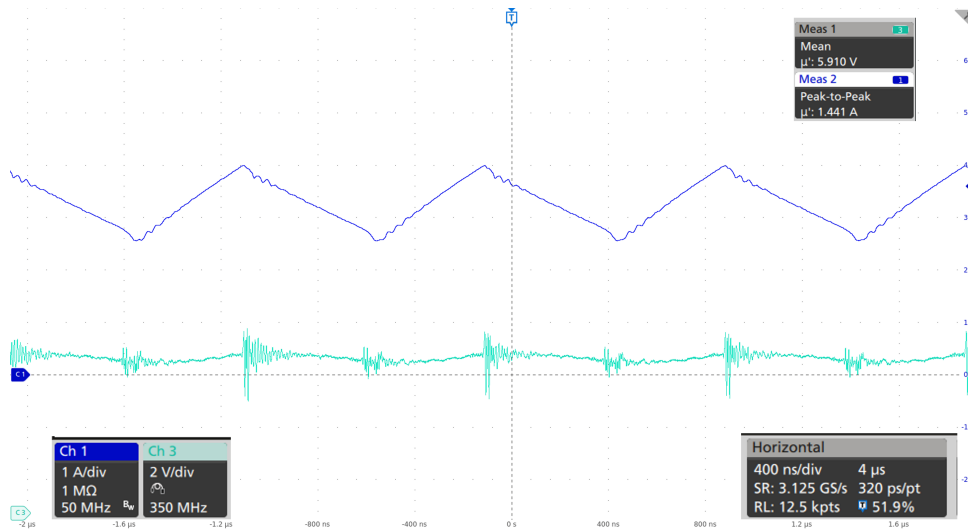


FIGURE 3.9: Experimental waveforms for coreless inductor at 1.65 Ω load (6A output current) showing ripple current (blue) and output voltage (cyan).

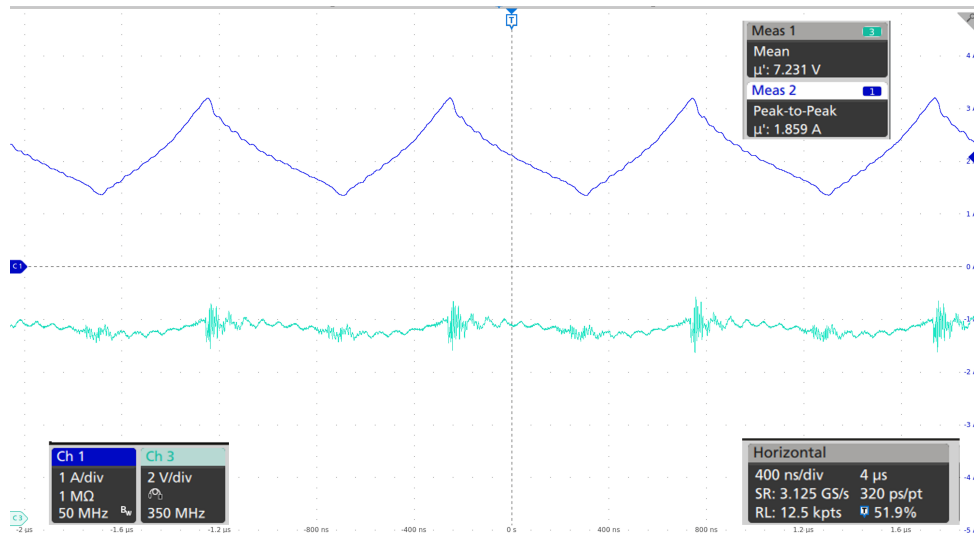


FIGURE 3.10: Experimental waveforms for ferrite inductor at 3.3 Ω load (3A output current) showing ripple current (blue) and output voltage (cyan).

Measured Performance:

Gate voltage transitions exhibited clean switching with approximately 5 μ s period (50% duty cycle), transitioning between +6V and -3V for GaN E-mode devices.

Current Waveforms:

Inductor current maintained triangular waveform across all load conditions, confirming:

- CCM operation throughout tested range
- Linear behavior of coreless inductor
- Absence of saturation effects

At 1.65 Ω load (6A output):

- Peak-to-peak ripple current: appropriate for design
- Output voltage ripple: <5% (well within specification)
- Inductor current slope consistent with extracted inductance values

TABLE 3.7: Extracted inductance from working conditions

Load [Ω]	Current [A]	Inductance [μ H]
10	1	2.64
6.6	1.5	2.81
3.3	3	2.92
1.65	6	3.09

Thermal Performance

Temperature measurements across load conditions for coreless inductor:

Extrapolation to 10A design limit predicts approximately 110°C, maintaining safe margin below:

Load Current (A)	Temperature (°C)
1	24.8
1.5	25.1
3	33.1
6	56.3

TABLE 3.8: Coreless Inductor temperature measurements under various load conditions

- GaN device junction temperature limit: 150°C
- FR-4 glass transition temperature: 130-140°C
- FR-4 continuous operating temperature: 105-130°C

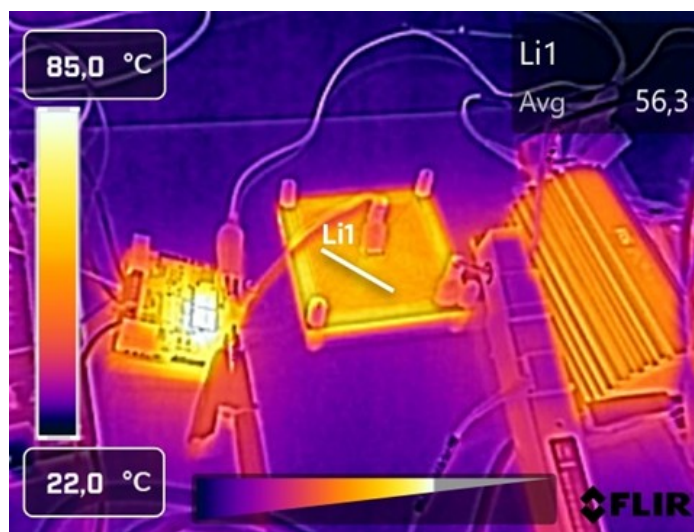


FIGURE 3.11: Thermal camera image showing coreless inductor temperature distribution at 6A load current.

TABLE 3.9: Thermal analysis at 1 MHz for various load currents

Model	Temperature [°C]	Output Current [A]
Coreless	24.8	1
	25.1	1.5
	33.1	3
	56.3	6
Inductor #1	41.7	3
	72.3	4
	77.6	6

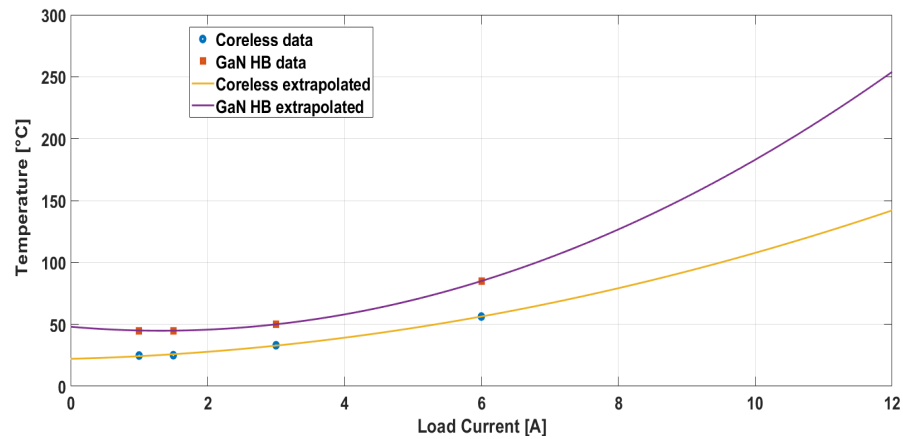


FIGURE 3.12: Thermal extrapolation curve from measurements

Performance Comparison

When compared to ferrite-based inductor implementations:

Coreless Advantages:

- Consistent performance across current range
- Lower harmonic content (14.1% vs 15.7% for 2nd harmonic)
- Approximately 20°C lower operating temperature at 6A
- No saturation-related current distortion

Ferrite Advantages:

- Smaller footprint and lower weight
- Lower cost for low-current applications
- Higher energy density

The coreless approach demonstrates particular advantages in applications where:

- Switching frequency exceeds 1 MHz
- Current linearity is critical
- Thermal performance is constrained
- Integration with converter PCB reduces assembly complexity

3.4 Interleaved Buck switching at 1 MHz

An interleaved topology was investigated as an advancement of the single-phase synchronous buck converter, targeting improved performance through ripple cancellation and enhanced thermal distribution. The two-phase interleaved buck converter (IBC) operates at 1 MHz with 180° phase shift between channels.

3.4.1 Interleaved Topology Benefits

The interleaved configuration provides several fundamental advantages over single-phase designs:

Ripple Cancellation: With duty cycle $D = 0.5$, the output voltage ripple is significantly reduced because inductor ripple currents partially cancel each other. The effective ripple frequency at the output capacitor doubles to $2f_{sw}$.

Reduced Component Requirements: The critical inductance is halved compared to single-phase buck:

$$L_{crit} = \frac{(1 - D) \cdot V_{out}}{4 \cdot f_{sw} \cdot \Delta I_L} \approx 3 \mu H \quad (3.8)$$

This reduction is particularly advantageous for coreless designs where inductance scales with physical dimensions.

Output Capacitance Reduction: The effective output current ripple becomes $\Delta I_L(1 - D)$ and with doubled effective frequency:

$$C_{out} = \frac{\Delta I_L}{16 \cdot f_{sw} \cdot \Delta V_{out}} \approx 150 \text{ nF} \quad (3.9)$$

This represents a significant reduction from the $2.08 \mu F$ required for single-phase operation (390 nF as implemented with margin).

Design Specifications

Target application for mild-hybrid vehicle 48/12V conversion:

TABLE 3.10: Interleaved buck converter design specifications

Parameter	Value
Input Voltage	48 V
Output Voltage	$\sim 24 \text{ V}$ ($D = 0.5$)
Load Current Range	1-20 A
Switching Frequency	1-10 MHz
Inductor Ripple Current	20% of I_{load}
Output Voltage Ripple	1% of V_{out}
Deadtime	5% of T_{sw}

Active Device Comparison

Two GaN HEMT devices were evaluated for the half-bridge implementations:

Infineon GS66508T:

- Maximum V_{DS} : 650V
- Maximum I_D : 30A
- $R_{DS,on}$: 50 m Ω
- Gate Charge (Q_g): 6.1 nC

STMicroelectronics SGT65R65AL:

- Maximum V_{DS} : 650V
- Maximum I_D : 25A

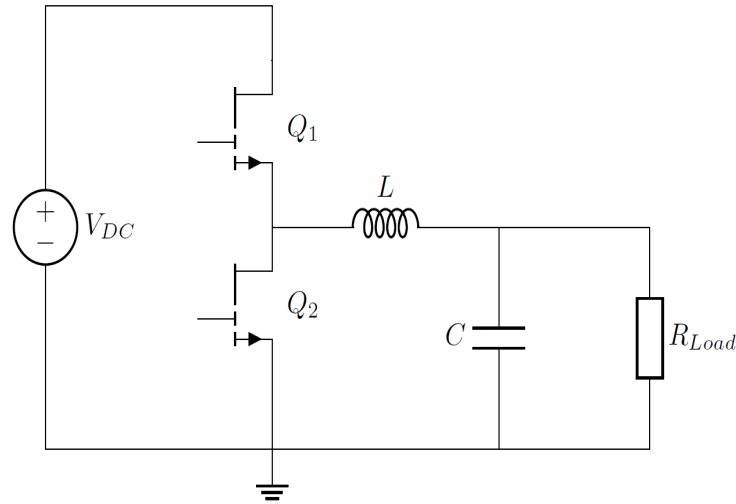


FIGURE 3.13: Synchronous buck converter (SBC)

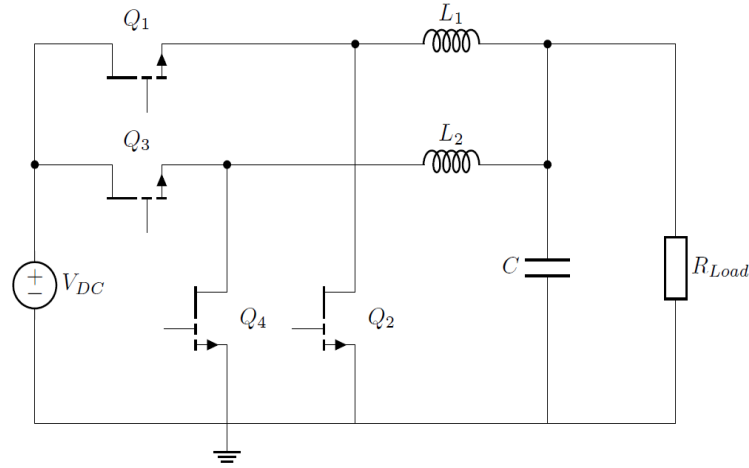


FIGURE 3.14: Two-phase interleaved buck converter (IBC)

- $R_{DS,on}$: 49 m Ω
- Gate Charge (Q_g): 5.4 nC

Passive Component Frequency Scaling

Analysis across switching frequency range (1-10 MHz) reveals critical design trade-offs:

Inductance Requirements: For IBC with $D = 0.5$, critical inductance decreases with frequency. At 1 MHz, $L_{crit} \approx 3 \mu\text{H}$; at 10 MHz, $L_{crit} < 0.5 \mu\text{H}$. However, Self-Resonant Frequency (SRF) considerations become critical.

Capacitance Requirements: Output capacitance scales inversely with frequency. At 1 MHz, approximately 150 nF required; at 10 MHz, below 20 nF becomes feasible. The IBC configuration enables significant capacitance reduction throughout the frequency range.

SRF Considerations: Passive components must operate well below their SRF. For high-frequency operation (>10 MHz), equivalent frequency $f_{eq} = 1/(\pi\tau)$, where

τ is the rise/fall time, can approach or exceed component SRF. With GaN transition times in nanosecond range:

- Inductors above SRF behave capacitively
- Capacitors above SRF behave inductively
- Performance degradation and potential instability

3.4.2 Simulation Results

Keysight ADS™ simulations at full load (20A) compared SBC and IBC topologies with both device types.

Efficiency Analysis: IBC topology achieved higher efficiency across frequency range for both devices:

- At 1 MHz: SGT65R65AL IBC showed approximately 3-4% efficiency improvement over SBC
- At 10 MHz: Efficiency advantage maintained despite increased switching losses
- GS66508T demonstrated similar trends with slightly lower absolute efficiency

Efficiency degradation mechanisms at higher frequencies:

- Increased switching losses (linear relationship breaks down above 500 kHz)
- Rising $R_{DS,on}$ with frequency (25-30% increase at 1 MHz)
- Parasitic effects in layout become more significant

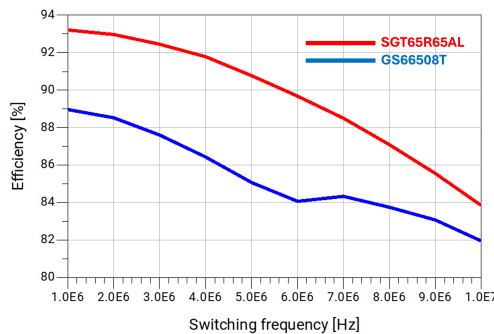


FIGURE 3.15: SBC efficiency versus switching frequency

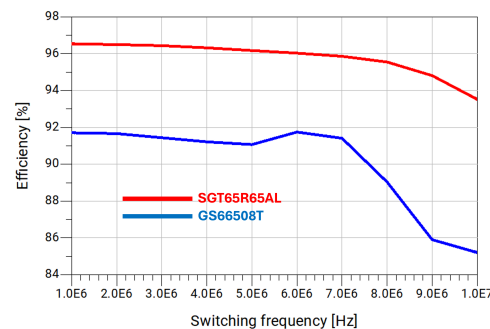


FIGURE 3.16: IBC efficiency versus switching frequency

FIGURE 3.17: Efficiency versus switching frequency at full load (20A) for SBC (left) and IBC (right) with SGT65R65AL and GS66508T devices.

Switching Performance: Both devices exhibited comparable rise and fall times under identical conditions:

- Load current: 20A

- Voltage swing: 48V
- Switching frequency: 1 MHz
- Deadtime: 50 ns

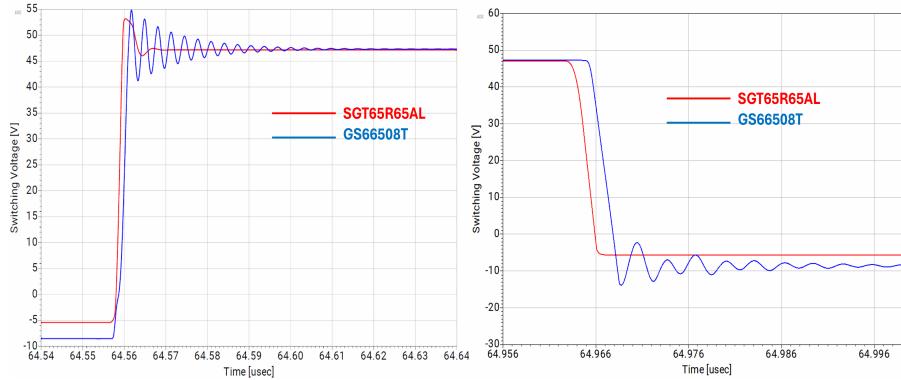


FIGURE 3.18: Switching performance comparison of SGT65R65AL and GS66508T devices showing rise and fall transitions at full load (20A) and 1 MHz switching frequency.

However, GS66508T showed higher ringing and oscillations, particularly at high load currents, attributed to:

- Layout parasitic interactions
- Device capacitance characteristics
- Package inductance effects

Dynamic Performance

Settling Time: Thanks to reduced output capacitance, IBC demonstrated faster settling time and superior dynamic response compared to SBC. Output voltage ripple maintained below 5% of V_{out} across operating range.

Ringing and Oscillations: Higher switching frequencies (>1 MHz) with fast GaN transitions resulted in increased ringing:

- Amplitude increases with switching frequency
- More pronounced at higher load currents
- Requires careful PCB layout optimization
- Snubber circuits or damping may be necessary at highest frequencies

Also, different device parasitics bring to different response time of the device in its dynamic performance. This "delay" can be easily seen in Figure 3.18. The phenomenon must be considered in the design process as a key criteria for assessing the device dynamic performance.

3.5 Dual Active Bridge (DAB)

The Dual Active Bridge (DAB) converter represents a crucial topology for bidirectional isolated DC-DC conversion applications, particularly in electric vehicle charging systems, renewable energy integration, and energy storage systems. This section presents the development and validation of an average current mode control strategy for GaN-based single-phase 2-level DAB converters operating at high switching frequencies.

The DAB converter architecture consists of two full-bridge configurations (primary and secondary) connected through a high-frequency transformer with an equivalent series inductance. This topology offers several advantages:

- Bidirectional power flow capability
- Galvanic isolation between primary and secondary sides
- Zero-voltage switching (ZVS) potential for reduced switching losses
- Simplified control through phase-shift modulation
- Suitability for high-power applications

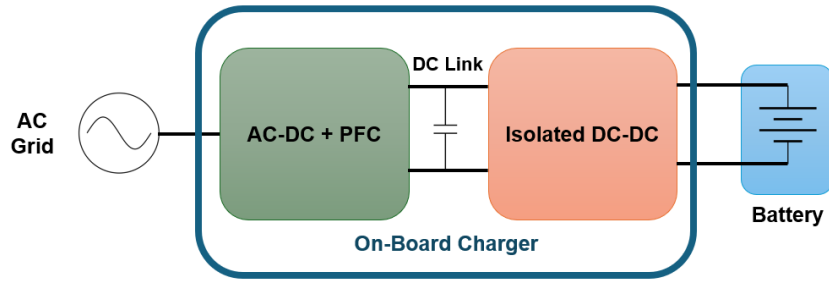


FIGURE 3.19: On-Board Charger block diagram showing AC-DC + PFC stage and isolated DC-DC DAB converter stage.

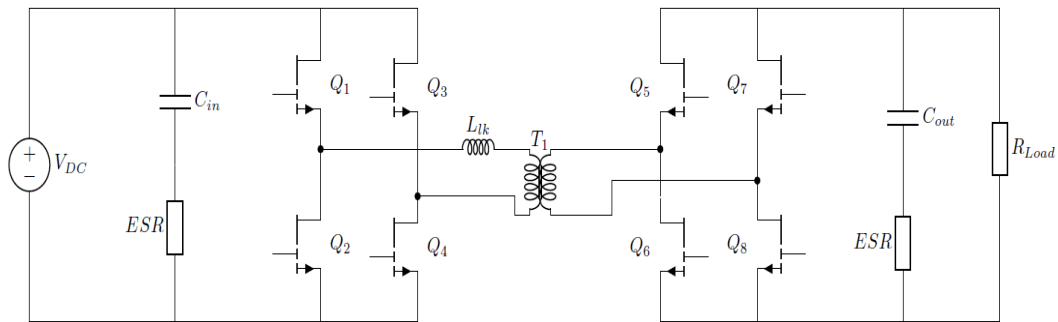


FIGURE 3.20: GaN-based 2-Level DAB circuit diagram showing full-bridge configurations and transformer with equivalent inductance.

DAB converters are widely employed in:

- Electric vehicle onboard chargers (OBCs) for both Grid-to-Vehicle (G2V) and Vehicle-to-Grid (V2G) operation

- Offboard charging infrastructure
- Battery energy storage systems
- Renewable energy conversion systems
- DC microgrid applications

The typical onboard charger architecture comprises two stages: a power factor correction (PFC) stage to minimize harmonic distortion, followed by an isolated DC-DC stage (DAB) for output regulation and electrical isolation. Due to unavoidable mismatches in device parameters, a DC bias current can develop in the transformer and equivalent inductance, potentially driving the magnetic core into saturation. This phenomenon arises from:

Steady-State DC Bias Causes:

- Unmatched circuit parameters
- Small discrepancies in gate-drive signals
- Different turn-on/off delays between devices
- Unequal on-state resistance ($R_{DS,on}$) of power devices
- Asymmetries in full-bridge switching

Transient DC Bias Causes:

- Temporary voltage-second imbalance across inductor
- Phase shift ratio updates during control
- Load transients
- Input/output voltage variations

Traditional control approaches such as Single Phase-Shift (SPS) and Dual Phase-Shift (DPS) modulation, while straightforward and effective at high loads, often fail to address DC bias, particularly under light or no-load conditions where voltage imbalance across the transformer is more pronounced.

Reduced Order Model Development

The control strategy is based on the reduced-order model derived from state-space averaging techniques adapted for DAB converters. The model establishes the control-to-voltage transfer function:

$$\frac{V_{out}}{D_2}(s) = \frac{NV_1(1 - 4\Phi)}{f_s L} \cdot \frac{R_L}{R_L C_2 s + 1} \quad (3.10)$$

$$\Phi = \begin{cases} 0.25 - \sqrt{\frac{1}{16} - \frac{f_s L I_2}{2NV_1}} & I_2 \geq 0 \\ -0.25 + \sqrt{\frac{1}{16} + \frac{f_s L I_2}{2NV_1}} & I_2 < 0 \end{cases} \quad (3.11)$$

$$I_2 = \frac{V_2}{R_L} \quad (3.12)$$

where:

- N = transformer turns ratio

- V_1 = input voltage
- Φ = nominal outer phase shift
- f_s = switching frequency (100 kHz for initial validation)
- C_2 = output capacitance (47 μ F)
- R_L = load resistance
- V_2, I_2 = output voltage and current
- L = equivalent inductance (7 μ H)

This reduced-order model captures the essential dynamics while maintaining computational simplicity suitable for real-time control implementation.

Average Current Mode Control Strategy

The proposed control employs a dual-loop structure with Proportional-Integral (PI) regulators.

Outer Loop - Voltage Control:

The outer loop regulates the output voltage to the reference value by controlling the outer phase shift ratio (D_2). The measured variable is the output voltage (V_{out}), which is compared against the desired output voltage (V_{ref}).

Inner Loop - Average Current Control:

The inner loop eliminates the DC component in the inductor/transformer current by adjusting the duty cycle (D) of all gate signals. The measured variable is the average inductor current over the switching period, which is regulated to a reference of zero ($I_{ref} = 0$). The averaging time of $10/f_s$ ensures effective DC component extraction.

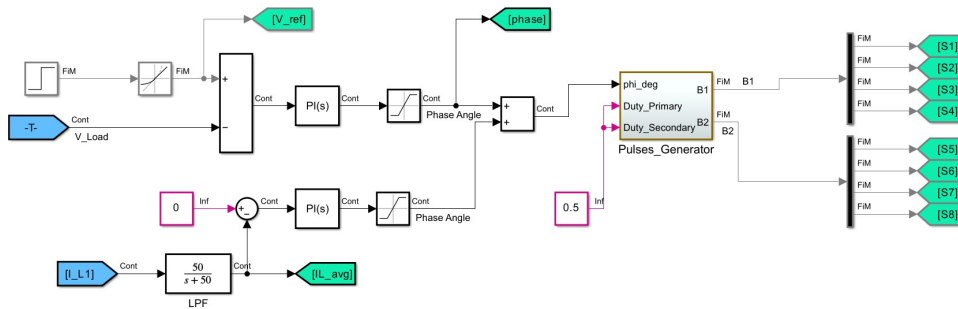


FIGURE 3.21: MATLAB/Simulink implementation of average current mode control with TPS modulator.

Modulation Technique:

A modified Triple-Phase-Shift (TPS) modulation was implemented, providing multiple control degrees of freedom. The parameter D_1 represents the phase shift between half-bridges on the primary side, while D_2 denotes the phase shift between half-bridges on the secondary side. The outer phase shift between primary and secondary bridges is controlled by D_3 , and D represents the common duty cycle adjustment for all gates. The key modification involves controlling not only phase shift ratios but also the duty cycles of gate signals, enabling direct average current regulation while maintaining voltage control.

PI Controller Design Methodology

The PI controllers were designed using frequency-domain specifications with the following design constraints:

$$|G_{PI}(j\omega_c)G_{DAB}(j\omega_c)| = 1 \quad (3.13)$$

$$\angle[G_{PI}(j\omega_c)G_{DAB}(j\omega_c)] = \left(\frac{\phi_m}{180} - 1\right) \pi \quad (3.14)$$

where the PI controller transfer function is given by:

$$G_{PI}(j\omega) = k_p + \frac{k_i}{j\omega} \quad (3.15)$$

The design parameters include ϕ_m as the phase margin (degrees), ω_c as the desired crossover frequency (rad/s), k_p as the proportional gain, and k_i as the integral gain.

Design Procedure:

The design procedure begins with specifying the desired crossover frequency for the closed-loop system and the desired phase margin (typically 45-60°). The constraint equations are then solved simultaneously to extract k_p and k_i values satisfying both constraints.

This systematic approach ensures adequate stability margins, desired bandwidth and response speed, robustness to parameter variations, and low steady-state error through integral action.

Transformer Magnetic Saturation Model

An E-Core 3C95 ferrite transformer (TDK E65/32/27) was modeled to validate control effectiveness:

Parameter	Value
Core Material	3C95 ferrite
Primary Turns (N_p)	12 turns
Secondary Turns (N_s)	12 turns
Cross-sectional Area (A_c)	250 mm ²
Magnetic Path Length (l_e)	0.135 m
Saturation Flux Density (B_{sat})	0.42 T
Saturation Field Strength (H_{sat})	300 A/m
Unsaturated μ_r	2000-3000
Saturated μ_r	10-20

The transformer was modeled using PLECS magnetic domain components, enabling direct relationship between geometry and magnetic behavior, B-H curve extraction during operation, real-time saturation detection, and accurate representation of magnetic nonlinearities. A configurable subsystem allowed switching between an ideal transformer model for fast simulation and a detailed magnetic model with saturation for control validation.

The DAB converter was designed with the parameters in Table 3.11.

TABLE 3.11: DAB converter simulation parameters

Parameter	Value	Parameter	Value
V_{dc}	400 V	f_{sw}	100 kHz
V_{OUT}	400 V	DT	100 ns
I_{max}	16.5 A	L	7 μ H
P_{max}	6.6 kW	n	1:1
C_1	47 μ F	C_2	47 μ F

3.5.1 Simulation Results and Performance Validation

Test Case 1: Resistive Load with Double-Step Reference

Dynamic performance was evaluated through a double-step voltage reference test. The test sequence included an initial soft-start phase to 200V, followed by a first step to 400V (forward power flow), and a second step back to 200V (reverse power flow).

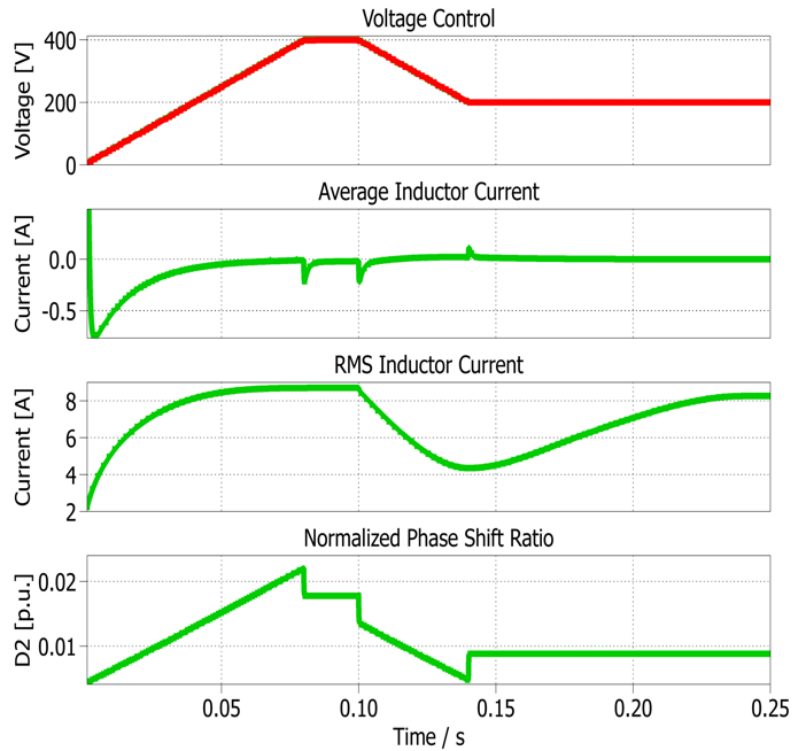


FIGURE 3.22: Voltage control main waveforms for resistive load showing output voltage, average inductor current, RMS current, and normalized phase shift ratio during double-step test.

Observed Performance:

The output voltage tracking demonstrated excellent performance with minimal overshoot, and the settling time showed fast response within design specifications. The average inductor current during steady-state remained within ± 10 mA, while peak average current during transients stayed below 100 mA. The RMS inductor current exhibited smooth evolution following load requirements, and the normalized phase shift ratio adjusted smoothly between operating points.

The transformer B-H curve remained linear throughout operation, confirming no saturation occurrence, effective DC bias elimination, symmetric magnetization in both directions, and flux density well below the 0.42 T saturation limit.

Test Case 2: Input Voltage Disturbance (PV Panel Shadowing)

To validate robustness, a photovoltaic panel shadowing scenario was simulated. The test conditions included nominal operation at 400V input, a 50V step disturbance on input voltage (simulating PV panel shadowing), and a resistive load maintained constant.

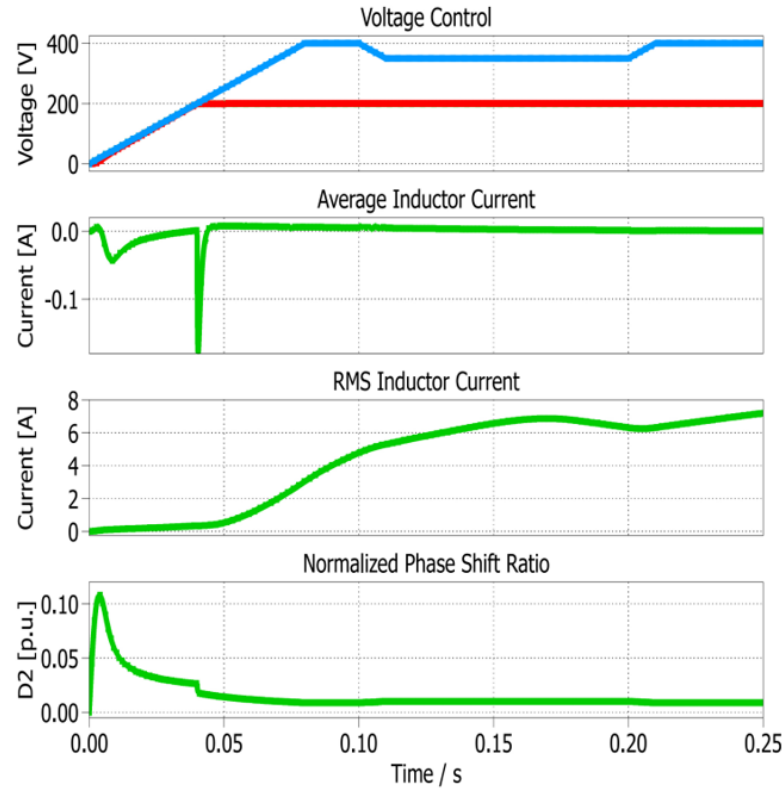


FIGURE 3.23: Current Mode Control with resistive load showing main waveforms under soft-start and 50V input voltage disturbance.

Results:

The output voltage regulation was maintained within specifications despite the input disturbance. The average inductor current peak during the transient remained below 200 mA, while the steady-state average current band stayed within ± 20 mA. The system exhibited fast recovery time with return to nominal operation, and no magnetic saturation was detected throughout the test.

Test Case 3: Battery Charging/Discharging Cycle

A complete battery management scenario was simulated with CC/CV control. The battery configuration consisted of 112 series cells in 1 parallel branch, with a nominal voltage of 400V and capacity of 1 Ah (scaled down for simulation efficiency). The maximum current was set at 10A, and a two-time-constant electrochemical model was employed.

Charging Profile:

The charging sequence begins with a pre-charge phase of 3A constant current from a fully discharged state, followed by bulk charging at 9A constant current to nominal voltage. The absorption phase maintained constant voltage (400V) until

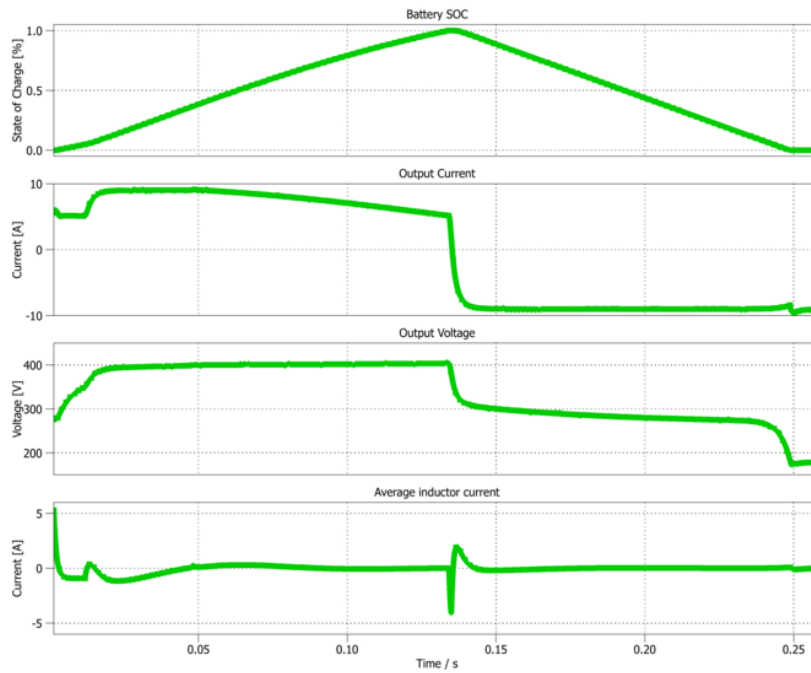


FIGURE 3.24: Current Mode Control in battery charging/discharging showing SOC, output current, battery voltage, and average inductor current under CC/CV charging and CC discharging.

fully charged, and the discharge phase applied constant current until SOC reached zero.

Performance Observations:

The average inductor current was well maintained throughout the cycle, with current peaks during mode transitions being present but of short duration. Peak amplitudes remained well below 10A, presenting no saturation risk. The SOC profile evolved smoothly as expected, the battery voltage displayed proper CC/CV characteristic curves, and the DAB output current correctly followed battery requirements.

Test Case 4: DC Motor Dynamic Load

A DC motor driving scenario with dual voltage-current loop control was implemented. The motor control structure featured an inner current loop for torque control, an outer speed loop for speed regulation, and an external average current loop for DC bias elimination through duty D adjustment.

Test Sequence:

The test begins with a speed step command to 50 rad/s, followed by three successive load torque steps of 1 Nm, 2 Nm, and 5 Nm.

Results:

The mechanical speed demonstrated fast response to the reference with minimal overshoot. Average inductor current peaks during torque steps were present but limited, with peak amplitudes below ± 100 mA. The steady-state average current remained near zero between transients, while load torque tracking exhibited excellent response to step changes. No magnetic saturation occurred during dynamic load variations.

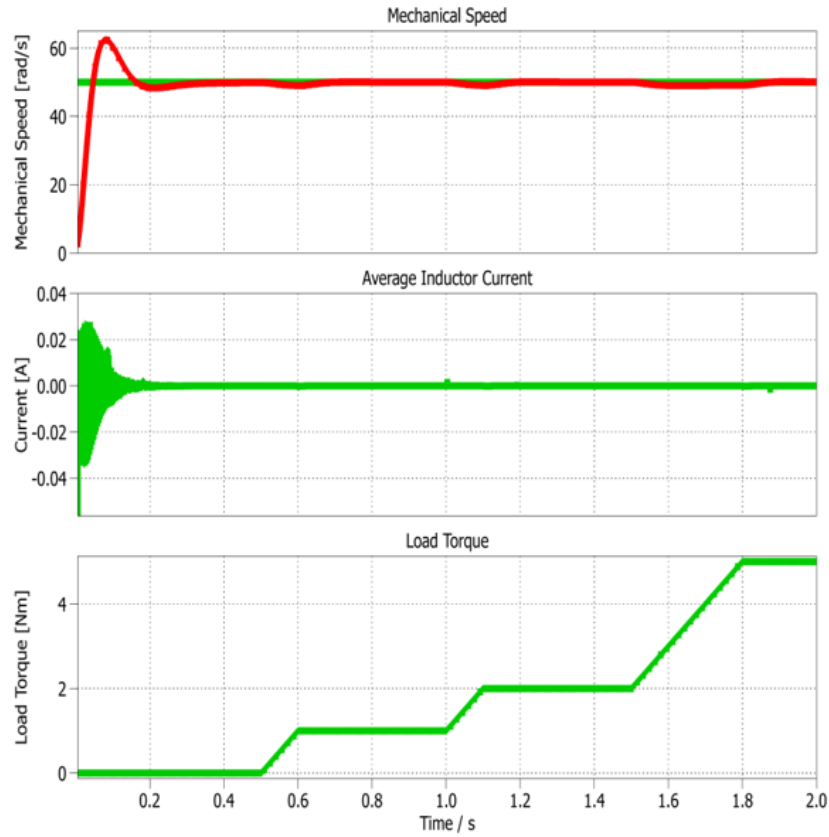


FIGURE 3.25: Current Mode Control with DC Motor load showing mechanical speed, average inductor current, and load torque under speed step (50 rad/s) and various load torque steps (1, 2, 5 Nm).

Experimental Validation Platform

To bridge simulation and hardware implementation, a comprehensive RCP platform was established using a Typhoon HIL 404 real-time emulator and a Texas Instruments TMS320F28379D dual-core C2000 MCU. The interface utilized HIL analog/digital I/O connections, with Code Composer Studio serving as the development environment for MCU programming and Typhoon HIL Schematic Editor and HIL SCADA providing the emulation software.

The Enhanced PWM (ePWM) module generates phase-shifted PWM signals for eight switches (two full bridges), while the ADC performs output voltage measurement and average current sensing. The control algorithm implements the dual PI loop, and communication enables real-time data exchange with the HIL platform.

This platform enables Hardware-in-the-Loop validation without a physical power stage, with controller code identical to the final implementation. It allows safe testing of fault conditions and edge cases, rapid iteration on control parameters, and direct compatibility between the C2000 MCU and Typhoon HIL.

The Plexim RT Box CE was evaluated for STM32G4 MCU validation, with Single Phase Shift (SPS) modulation successfully deployed. However, its CPU-based emulation with 1 μ s minimum time step proved insufficient for GaN-based high-frequency converters requiring less than 100 ns resolution, making it better suited for lower switching frequency applications. Future platform consideration includes the dSPACE MicroLabBox, which offers FPGA-based



FIGURE 3.26: Experimental testbench with Typhoon HIL 404 and TI C2000 MCU for DAB control validation.

emulation suitable for GaN high-frequency validation with sub-microsecond time step capability.

Key Findings and Contributions

The maximum steady-state average current error remained within ± 10 mA for resistive loads, while transient average current peaks stayed below 200 mA, well below the saturation threshold. Output voltage regulation proved excellent across all test scenarios, with dynamic response showing fast settling and minimal overshoot. The control demonstrated robust performance under input disturbances and load variations.

The proposed approach offers simple implementation suitable for real-time embedded systems with low computational burden compared to MPC or adaptive control. It demonstrates high effectiveness in DC bias elimination and robust performance across diverse operating conditions. The method is compatible with conventional modulation strategies and directly applicable to GaN-based high-frequency converters.

Future Work and Open Questions

Zero-Voltage Switching (ZVS) analysis should examine the impact of duty cycle modulation on ZVS regions, optimization of phase shift and duty for simultaneous DC bias elimination and ZVS, and the trade-off between average current control and switching loss minimization.

Efficiency characterization demands a full efficiency map across load and voltage ranges, comparison with conventional control strategies, light-load efficiency evaluation, and identification of dominant loss mechanisms.

Parameter sensitivity analysis needs robustness assessment against device parameter mismatches, uncertainty quantification for practical implementation, and worst-case performance bounds determination.

Hardware prototype development should include implementation with GaN power devices, experimental validation of simulation results, thermal management evaluation, and EMI characterization.

Extended operating conditions must be explored, including wide input/output voltage range operation, asymmetric voltage ratios, and overload and fault condition behavior.

The developed average current mode control represents a practical and effective solution for preventing transformer saturation in DAB converters while maintaining simple implementation suitable for high-frequency GaN-based applications.

3.6 Three-Level Active Neutral Point Clamped (3L-ANPC) DAB

The Three-Level Active Neutral Point Clamped (3L-ANPC) Dual Active Bridge topology represents an advancement over conventional 2-level DAB converters, enabling operation at higher DC bus voltages while using lower-voltage-rated semiconductor devices. This section presents control strategies, modeling approaches, and optimization techniques developed for 3L-ANPC DAB converters.

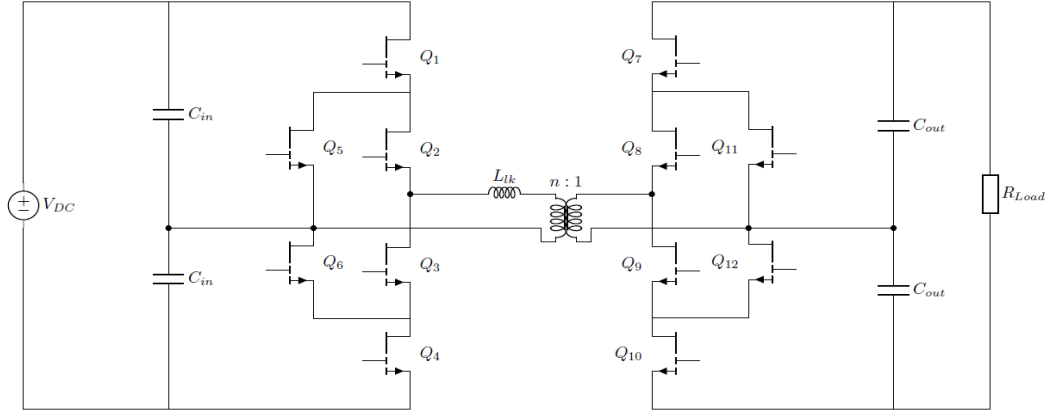


FIGURE 3.27: 3-Level ANPC DAB topology showing three-level bridge configurations with clamping devices and voltage division capacitors.

The 3L-ANPC DAB consists of two three-level ANPC bridges connected through a high-frequency isolation transformer. Each ANPC bridge leg contains four main switching devices (typically GaN HEMTs), two clamping diodes or active switches, and two DC-link capacitors providing voltage division.

Each phase leg can generate three voltage levels: $+V_{dc}/2$ (P state), 0 (O or zero state), and $-V_{dc}/2$ (N state). This multilevel voltage generation provides reduced voltage stress per device ($V_{ds,max} = V_{dc}/2$), lower dv/dt compared to 2-level topology, reduced EMI emissions, and improved transformer voltage waveform quality.

With 650V-rated GaN HEMTs, the 3L-ANPC topology enables operation at 800V DC bus voltage (400V per device) while maintaining adequate safety margin. This expands the application range of GaN devices to higher-power systems without resorting to series connection.

3.6.1 Control as 2-Level DAB

A novel control approach was developed where the 3L-ANPC DAB is controlled without utilizing zero states on either primary or secondary sides. This configuration achieves 2-level DAB-like behavior, enabling direct application of conventional 2-level DAB modeling techniques, utilization of established control algorithms (SPS, DPS, TPS), simplified implementation compared to full 3-level modulation schemes, and reduced computational burden.

When operating in 2-level mode, the control variables remain: D_1 (inner phase shift on primary side), D_2 (inner phase shift on secondary side), D_3 (outer phase shift between bridges), and D (duty cycle when incorporating average current control).

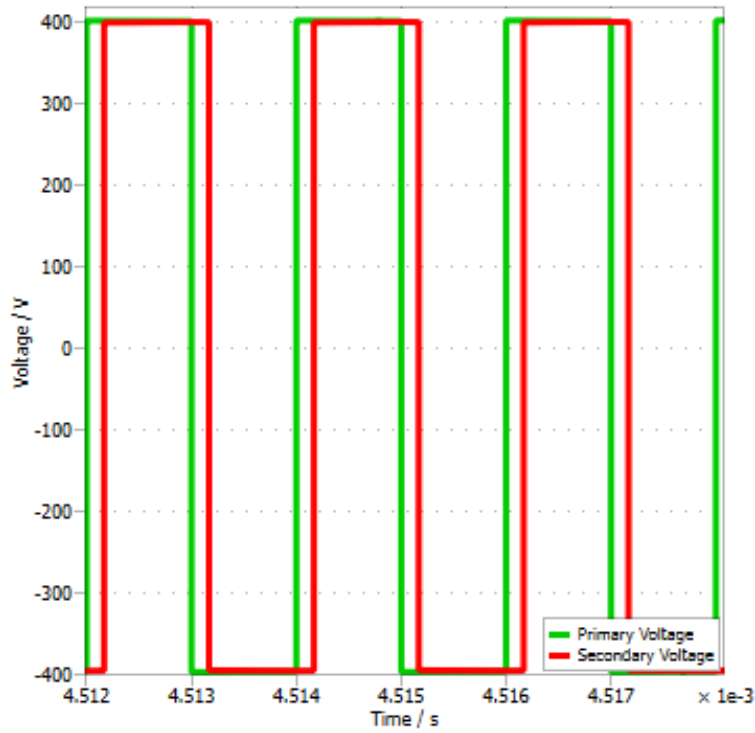


FIGURE 3.28: 3L-ANPC DAB controlled as 2-Level DAB showing phase shift modulation without zero states.

Critical to this approach is ensuring balanced voltage sharing across devices. Input capacitors C_1 and C_2 must maintain equal voltage ($V_{dc}/2$ each), and output capacitors must be similarly balanced. Balancing is achieved through symmetric switching patterns, proper dead-time management, and active clamping device operation.

Under balanced conditions, $V_{ds,max} = V_{dc}/2$ for each device. With 800V DC bus, each GaN device experiences maximum 400V, providing a safety margin where 650V devices are operated at 62% of rating. Clamping devices ensure voltage sharing even during transients.

The operating conditions include DC bus voltage of 800V, output voltage regulated to reference, resistive variable load, and switching frequency of 100 kHz. Key observations include V_{ds} across each device successfully maintained below 650V breakdown, even voltage distribution among all switches, excellent output voltage control tracking performance, smooth phase shift ratio modulation, and clean switching transitions in waveform quality.

Performance Characteristics

At full load operation, achieved efficiency is approximately 95%, comparable to 2-level DAB despite additional devices. At full load, conduction losses are dominant and switching losses are reduced due to lower voltage stress, and minimal clamping device losses under balanced conditions are obtained.

At light load operation, efficiency degradation is observed. The causes include increased relative switching losses, constant gate drive losses, and significant reactive power component. Mitigation strategies required include advanced modulation (TPS), frequency variation, and mode switching to utilize zero states.

Under the assumption of balanced input/output capacitors, clamping devices carry very low current during normal switching. The current magnitude is

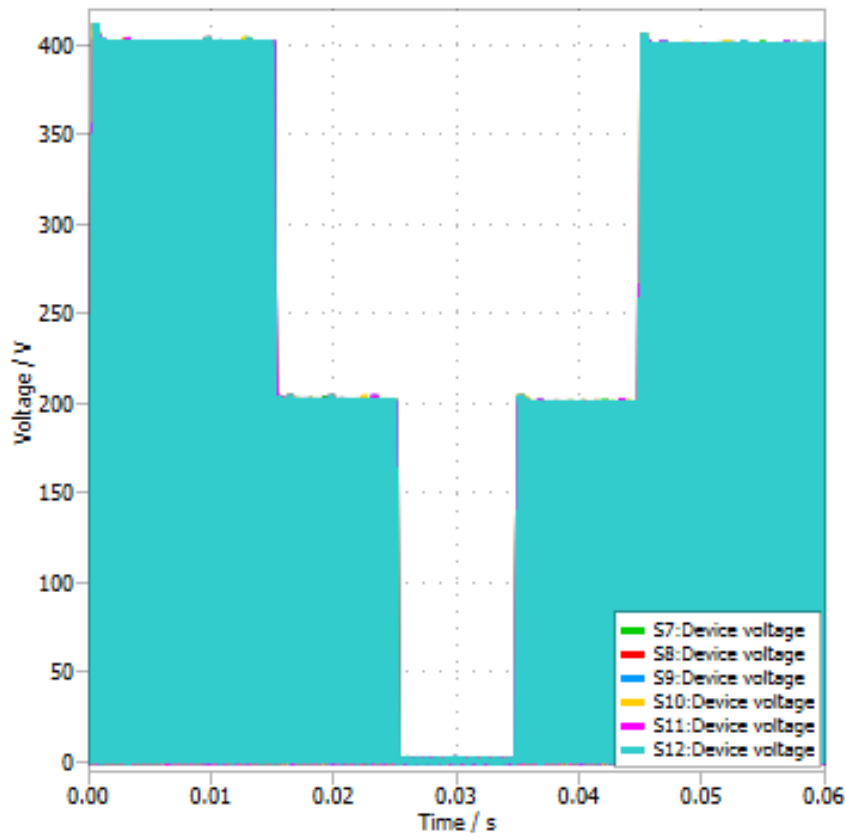


FIGURE 3.29: Device voltage stress (V_{ds}) across GaN switches showing balanced voltage sharing maintaining each device well below 650V breakdown voltage during 800V bus operation. The switching waveforms are superimposed, the graph serves to highlight that the voltage stress across each device is well below the breakdown voltage, even with 800V DC Bus.

negligible compared to main device currents. The primary function is voltage clamping rather than power transfer, with the implication that efficiency is not significantly reduced by additional devices. This represents a key advantage: increased voltage capability without proportional efficiency penalty.

The control system is tuned for fast dynamic response with optimized voltage loop bandwidth for quick settling, minimal overshoot (less than 5%), settling time comparable to 2-level implementation, and excellent load transient response maintaining regulation.

3.6.2 Advanced Control Strategies

Standard output voltage regulation employs a PI controller adjusting outer phase shift with excellent reference tracking, robust disturbance rejection against input variations, and minimal steady-state error through integral action.

Bidirectional power transfer management includes forward power flow with positive phase shift, reverse power flow with negative phase shift, power level controlled by phase shift magnitude, and demonstrated smooth transitions between flow directions.

Average inductor current regulation (as in 2-level DAB) successfully implements DC bias elimination with average current maintained near zero in

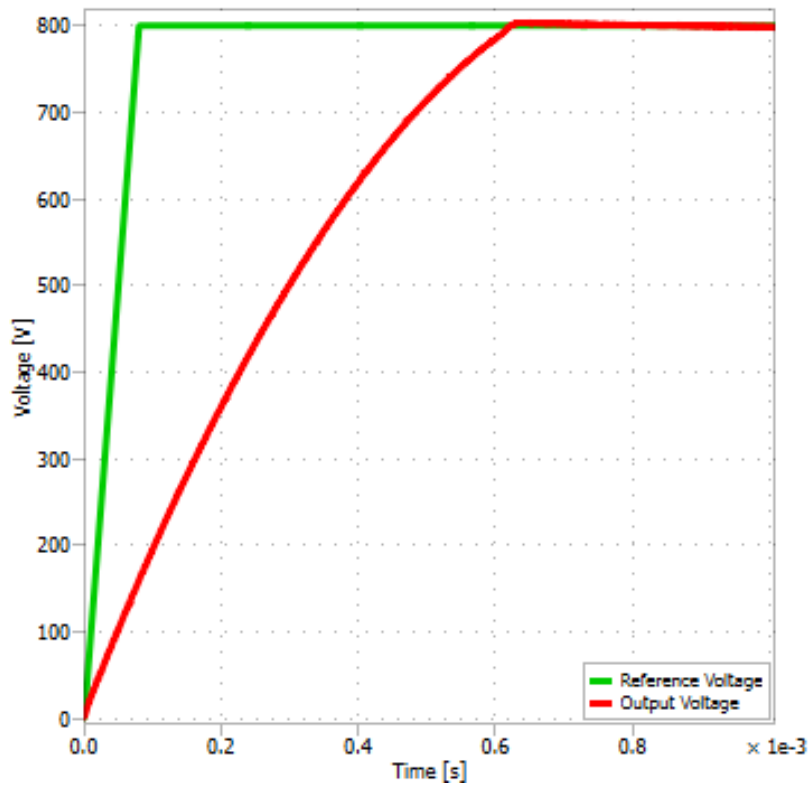


FIGURE 3.30: 3L-ANPC DAB voltage control showing output voltage regulation and stable operation at 800V DC bus.

steady-state performance, limited and brief current peaks in transient behavior, and no magnetic saturation observed for saturation prevention.

Constant Current/Constant Voltage (CC/CV) Battery Charging

Dedicated battery management control was developed with charging phases including pre-charge (low current, e.g., 3A, for cell balancing), constant current (higher current, e.g., 9A, bulk charging), constant voltage (voltage regulation at nominal value), and discharge (controlled constant current discharge).

A two-time-constant electrochemical battery model was implemented, capturing fast dynamics (charge transfer resistance and capacitance), slow dynamics (diffusion processes), state-of-charge (SOC) dependence, optional temperature effects, and configurable complexity based on application requirements.

The control structure includes an outer loop that selects CC or CV mode based on SOC and voltage, an inner loop providing voltage or current regulation through DAB phase shift, smooth mode transition switching between CC and CV, and an average current loop maintaining zero DC bias throughout the cycle.

Performance results demonstrate smooth SOC trajectory evolution from 0 to 100% and back, clean current profile with CC phases and proper CV transition, characteristic battery charging curve in voltage evolution, and well-controlled average inductor current with limited peaks during mode transitions.

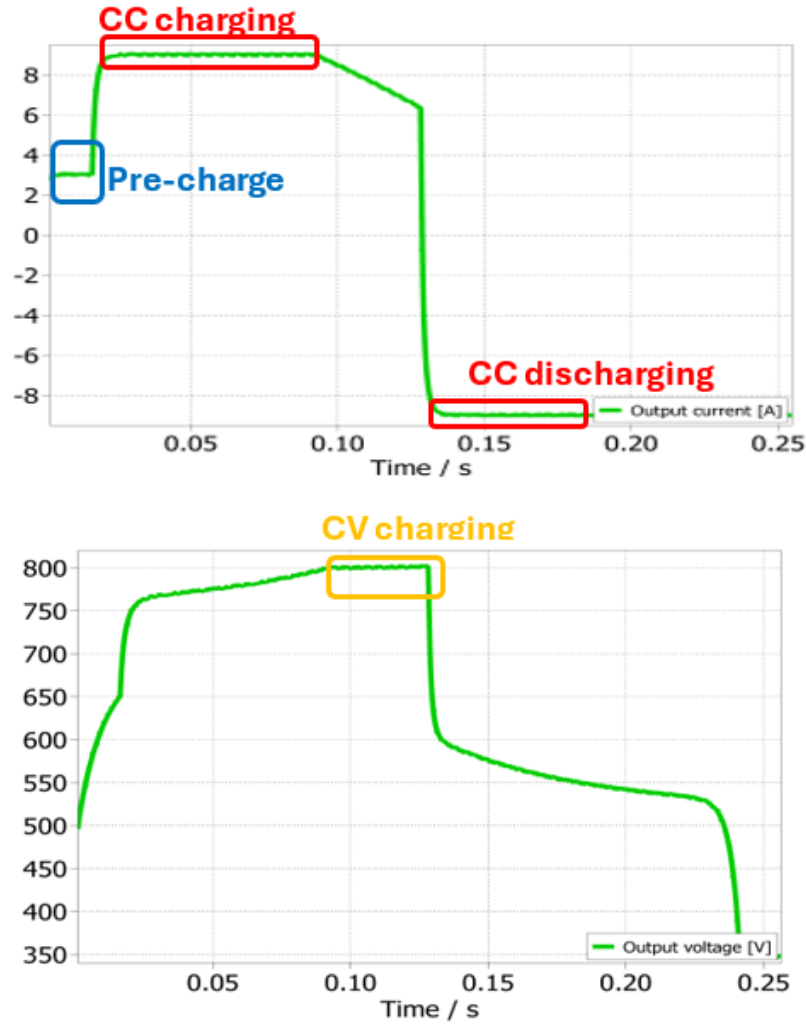


FIGURE 3.31: 3L-ANPC DAB battery charging/discharging control showing CC/CV phases with SOC, current, voltage, and average inductor current waveforms.

3.6.3 Modeling Challenges and Approaches

Traditional state-space averaging (SSA) proves inadequate for DAB converters because the inductor current DC average is zero in steady-state, power transfer occurs through the AC component, phase shift (not duty ratio) is the primary control variable, and SSA effectively filters out the AC power transfer mechanism.

For 3L-ANPC DAB, complexity increases further with additional switching states from three-level operation, interleaved current paths through clamping devices, and capacitor voltage dynamics that must be included.

Generalized State-Space Averaging (GSSA)

GSSA extends traditional averaging to overcome DAB modeling challenges. Key features include the inclusion of AC components in state variables, tracking of non-zero ripple and harmonic content, enabling harmonic balance analysis, and suitability for phase-shift-controlled systems.

State variable selection involves peak or RMS current/voltage ripple, instantaneous power, fundamental harmonic magnitude and phase, and capacitor

voltage deviations from nominal.

Advantages include analytical insight into converter behavior, enabled structured control development, possible small-signal linearization, suitability for classical control design (Bode plots, root locus), and compatibility with PI/PID, state feedback, and advanced nonlinear control.

When applied to 3L-ANPC DAB, GSSA provides continuous-time models capturing power flow as function of phase shifts, ZVS boundary conditions, current stress relationships, efficiency trends, and capacitor balancing dynamics.

Piecewise Linear (PWL) Modeling

An alternative approach handles mode-dependent behavior. The 3L-ANPC DAB exhibits different operating modes based on duty cycle relationships (D_1 , D_2 , D_3), zero-voltage switching regions, capacitor balancing state, and power flow direction and magnitude.

Each operating mode is characterized by distinct switching sequences, specific current path topologies, unique loss mechanisms, and different voltage stress distributions.

Advantages include accurate constraint representation for optimization, capturing nonlinearities and discontinuities in losses and stress, enabling mode-aware control and optimization, and computational manageability despite complexity.

Applications include precomputed look-up tables (LUTs) for real-time control, efficiency optimization across operating range, thermal stress minimization, capacitor balancing strategies, and constrained nonlinear optimization algorithms.

Status and Future Development

Due to time constraints during the visiting period, complete analytical modeling was proposed but not fully developed. Future work includes complete GSSA model derivation for 3L-ANPC DAB, experimental validation of model predictions, integration into advanced control schemes, and optimization algorithm development based on PWL models.

3.6.4 Optimization Strategies

Predictive Peak Current Control with Frequency Variation

Transformer and inductor saturation remains a concern even with average current control. Peak current directly relates to core flux excursion and saturation risk. Analytical and simulation studies revealed an inverse relationship where peak current is proportional to the inverse of switching frequency:

$$I_{peak} \propto \frac{1}{f_s} \quad (3.16)$$

At higher switching frequencies, there is shorter time per half-cycle, reduced energy transfer per switching period, lower peak current for given power level, and reduced magnetic flux excursion.

Benefits include an additional degree of freedom for saturation management, the ability to complement average current control, and enabled operation at higher power levels without saturation. Challenges include frequency variation affecting other control loops, potential stability implications, increased switching losses at

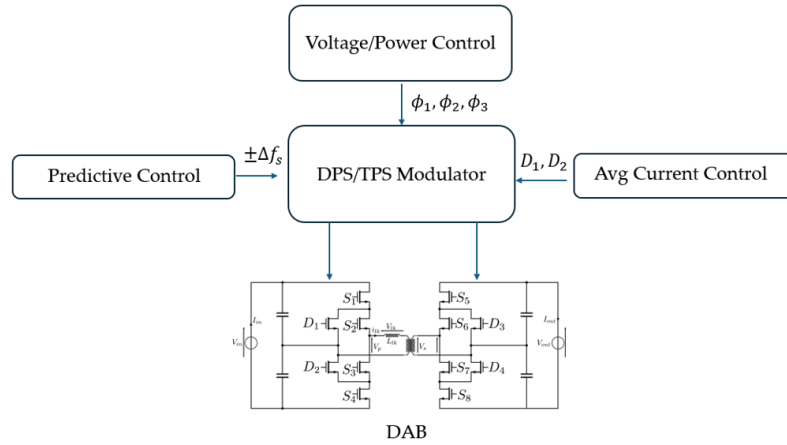


FIGURE 3.32: Control Architecture for Multilevel DAB

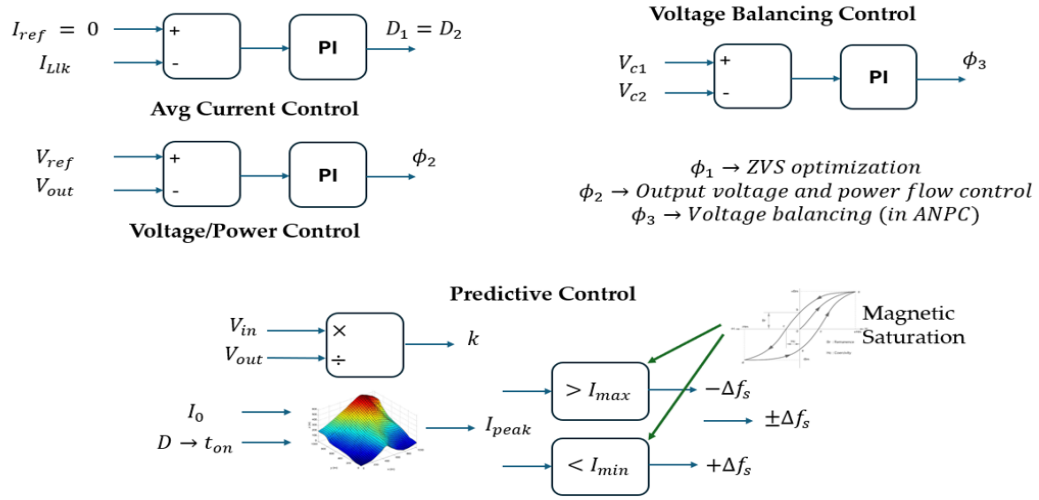


FIGURE 3.33: Predictive peak current control concept showing relationship between switching frequency and peak current for saturation management.

higher frequencies, resonance and EMI considerations, and control loop bandwidth changes with frequency.

The topic remains under investigation with concept validated through simulation, online optimization algorithm under development, required stability analysis, and pending experimental validation.

Zero-Voltage Switching (ZVS) and Current Stress Optimization

A multi-objective optimization problem addresses simultaneous objectives: achieving ZVS for all devices, minimizing RMS current stress, maintaining power transfer requirements, and ensuring capacitor voltage balance.

The converter exhibits multiple operating modes with different characteristics: full ZVS region (optimal efficiency but limited power range), partial ZVS region (extended power capability with some hard switching), and high current stress region (maximum power but increased losses).

A trajectory control concept involves optimal trajectory planning with the objective to move operating point between modes, maintain ZVS throughout

transition when possible, minimize current stress during transients, and achieve target operating point efficiently.

Multi-dimensional optimization occurs over D_1 , D_2 , D_3 trajectories over time, switching frequency profile, and duty cycle evolution, subject to constraints including ZVS conditions for each device, current limits (peak and RMS), voltage stress limits, capacitor voltage balance, and control bandwidth limitations.

Potential optimization techniques include genetic algorithms for global optimization, sequential quadratic programming for local optimization, dynamic programming for trajectory planning, and real-time model predictive control.

This represents ongoing research with completed problem formulation, promising preliminary simulation results, comprehensive optimization framework under development, required computational complexity assessment, and optimization strategy to be determined for real-time implementation.

Similar to 2-level DAB work, multiple RCP platforms were considered for 3L-ANPC validation. The Typhoon HIL 404 is suitable for 3L-ANPC emulation with FPGA-based computation for fast dynamics, compatible with C2000 MCU, and 16 PWM outputs sufficient for two 3-level bridges. The Plexim RT Box was evaluated but time-step limitations were identified; it may suffice for lower switching frequencies but is not recommended for GaN-based high-frequency implementation. The dSPACE MicroLabBox is under future consideration for final validation with FPGA capability for sub-microsecond resolution and suitability for GaN-based 3L-ANPC implementation.

Key Achievements and Contributions

The "control as 2-level DAB" approach provides control simplification by leveraging existing 2-level DAB knowledge and tools, simplified implementation compared to full 3-level control, proven effectiveness through multiple operating scenarios, and maintained voltage stress benefits of 3-level topology.

Voltage range extension demonstrates feasibility of 650V GaN devices in 800V bus applications with adequate safety margins maintained, no efficiency penalty compared to 2-level operation at equivalent voltage, and scalability to higher voltages with appropriate device selection.

The key parameters employed for the 3L-ANPC DAB are reported in Table 3.12

TABLE 3.12: 3L-ANPC DAB key performance metrics

Parameter	Value
DC Bus Voltage	800 V
Device Voltage Stress	<400 V
GaN Device Rating	650 V
Safety Margin	38%
Full Load Efficiency	~95%
Control Complexity	Low (2-Level DAB-like)
Clamping Device Losses	Minimal

Comprehensive simulation studies confirm performance validation including output voltage regulation across various loads, bidirectional power flow capability, battery charging/discharging management, average current control effectiveness, and absence of magnetic saturation.

Performance analysis reveals efficiency characteristics of 95% efficiency at full load, minimal clamping device losses under balanced conditions, efficiency

comparable to 2-level DAB despite additional components, and light-load efficiency requiring optimization techniques.

3.6.5 Future Research Directions

Short-term objectives include completing the GSSA modeling framework, finalizing the frequency-based current control algorithm, implementing ZVS optimization with experimental validation, developing parameter uncertainty analysis, and creating a hardware prototype with GaN devices.

Long-term research encompasses five-level ANPC DAB investigation, modular multilevel converter (MMC) DAB topologies, machine learning-based optimization, wide bandgap device comparison (GaN vs. SiC in multilevel), and integrated magnetic component design for multilevel DAB.

Application development targets electric vehicle fast charging stations, medium-voltage DC distribution systems, renewable energy interfacing, energy storage systems, and solid-state transformers.

The 3L-ANPC DAB topology, controlled with the simplified approach developed in this work, represents a practical solution for extending GaN device application to higher voltage ranges while maintaining control simplicity and achieving high efficiency. The framework established provides a foundation for more advanced optimization and control strategies in future developments.

3.7 EMI Suppression and ZVS-operation for GaN-based power stages

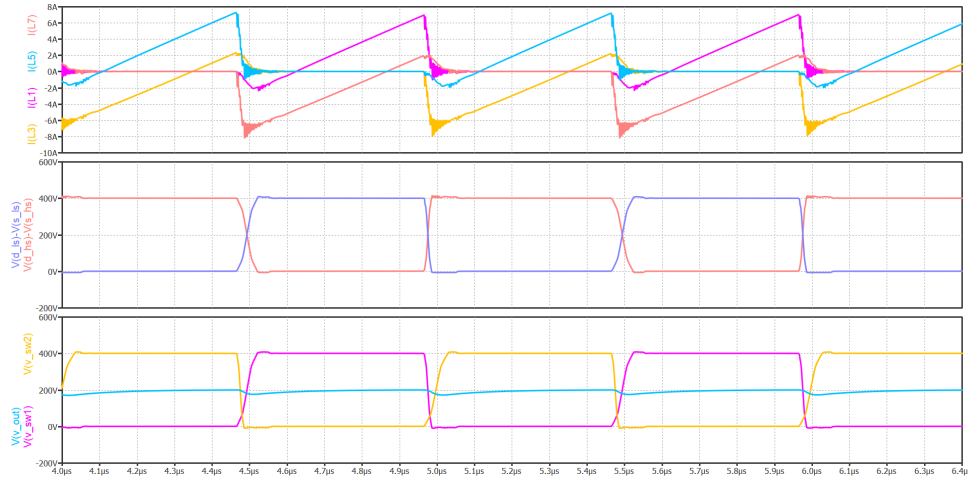


FIGURE 3.34: Double half bridge steady-state waveforms

The simulated waveforms in QSPICE of the double GaN half-bridge EMI compensation topology are presented in Figure 3.34, showing the steady-state operation over five switching cycles. The results demonstrate the characteristic behavior of the compensated topology under nominal operating conditions with a DC bus voltage of 400 V.

The top subplot displays the inductor currents I_{L1} , I_{L3} , I_{L5} , I_{L7} (equal to the active device currents) from the two parallel half-bridge stages. These currents exhibit the expected triangular waveform profile with peak values reaching approximately 7 A and minimum values near -8 A. The triangular current shape is a direct

consequence of the series compensation inductors, which impose a constant dI/dt during each switching state as the voltage across the inductor remains relatively constant. The slight asymmetry between positive and negative peak currents can be attributed to the DC load current component superimposed on the AC switching ripple. Notably, the current transitions during switching events appear smooth and controlled, lacking the sharp discontinuities and high-frequency ringing that would be characteristic of a hard-switched topology. This controlled current behavior is fundamental to achieving the EMI reduction benefits of the compensation approach.

The middle subplot presents the drain-source voltages $V_{ds,LS}$ and $V_{ds,HS}$ for the left-side half-bridge stage (the right-side one is complementary), shown in blue and red. These voltages alternate between 0 V and 400 V with a duty cycle of approximately 50%, consistent with the complementary switching of the high-side and low-side transistors in each leg. The voltage transitions exhibit minimal overshoot and no visible ringing, confirming the effectiveness of the compensation inductors in suppressing voltage oscillations at the switching nodes. The rise and fall times appear to be in the range of 100-200 ns, which, while slower than the sub-10 ns transitions achievable with hard-switched GaN devices, represent an optimal compromise between switching speed and EMI generation. The clean, monotonic voltage transitions indicate that the parasitic resonances between the power loop inductance and device capacitances have been effectively damped by the compensation network.

The bottom subplot shows the output voltages V_{out} and V_{sw} , displayed in cyan, pink (1st bridge middle point) and yellow (2nd bridge middle point) respectively. The cyan trace represents the filtered output voltage, maintaining a relatively constant level near 200 V, which corresponds to the average value of the switched waveform for a 50% duty cycle operation. The yellow waveform alternates between 0 V and 400 V in synchronization with one of the switching legs, while the pink trace shows similar switching behavior but with opposite phase relationship. The output voltage ripple is well-controlled, indicating proper design of the output filter inductors L_{out} and adequate filtering for the resistive load.

An important observation from the current waveforms is the presence of negative current phases in both inductors, which facilitates zero-voltage switching (ZVS) transitions. During the dead-time intervals between the turn-off of one device and the turn-on of its complementary switch, this negative current flows through the reverse conduction channel of the incoming device, discharging its output capacitance to near-zero voltage before the gate signal is applied. This soft-switching mechanism is evidenced by the smooth current transitions that occur precisely at the voltage switching instants, with no apparent capacitive discharge current spikes that would indicate hard-switched turn-on events.

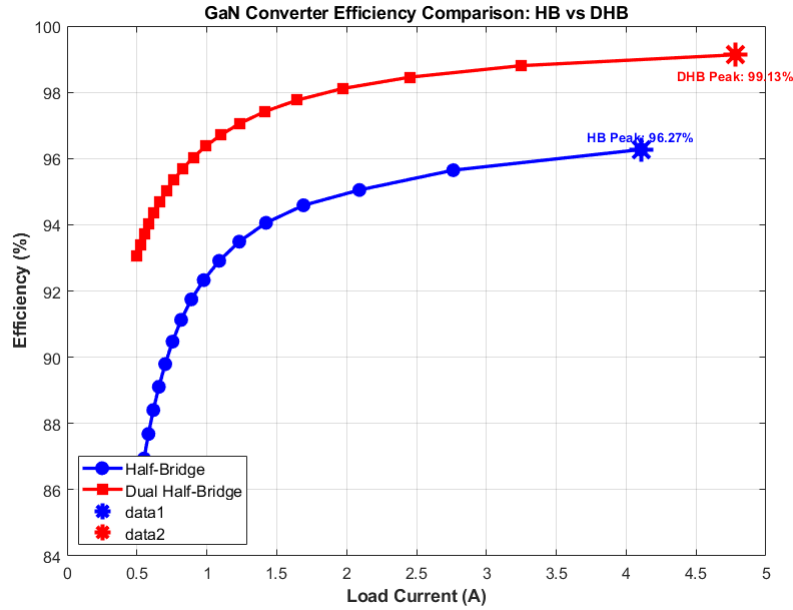


FIGURE 3.35: Dual half bridge vs single half bridge efficiency

The phase relationship between the two half-bridge stages reveals interleaved operation, with the switching transitions of one stage occurring at the midpoint of the switching period of the other stage. This interleaving strategy provides additional benefits in terms of input current ripple cancellation and output voltage ripple reduction, as the triangular current waveforms from each stage partially cancel when combined at the output. The interleaved operation also distributes the thermal stress more evenly across the devices and reduces the RMS current stress on the DC bus capacitors.

In Figure 3.35, the two efficiencies as a function of load current are compared for the dual and single half bridge topologies. As can be seen, the efficiency of the dual stage is 2.86% higher although the increased number of devices. This is due to the advantageous removal of unwanted ringing in voltage and current at the output of the power stage with respect to the single half bridge case and achieved ZVS operation.

The simulation results validate the theoretical advantages of the double GaN half-bridge EMI compensation topology. The controlled current slopes and clean voltage transitions demonstrate effective suppression of high-frequency oscillations without requiring external snubbers or damping networks. The smooth waveform characteristics translate directly to reduced electromagnetic emissions, potentially eliminating the need for complex EMI filtering stages. The ZVS-enabling current phases confirm the potential for improved efficiency despite the additional conduction losses through the compensation inductors.

3.8 Comparative Analysis of Single and Interleaved GaN Half-Bridges

This section presents a comprehensive experimental and simulation-based comparison between the single half-bridge (SHB) and dual interleaved half-bridge (DHB) GaN converter topologies. The investigation encompasses transient behaviour during soft-start, steady-state switching characteristics, power density

metrics, and benchmarking against commercial GaN evaluation platforms. All experimental results were obtained using GaN Systems GS66508B enhancement-mode HEMTs operating from a 400 V DC bus at switching frequencies up to 1 MHz.

3.8.1 Soft-Start Transient Behaviour

The soft-start transient represents a critical operating regime where the converter must establish steady-state conditions while managing potentially destructive voltage and current stresses. The fundamental differences between the SHB and DHB topologies become particularly evident during this transitional phase.

Single Half-Bridge Soft-Start Characteristics

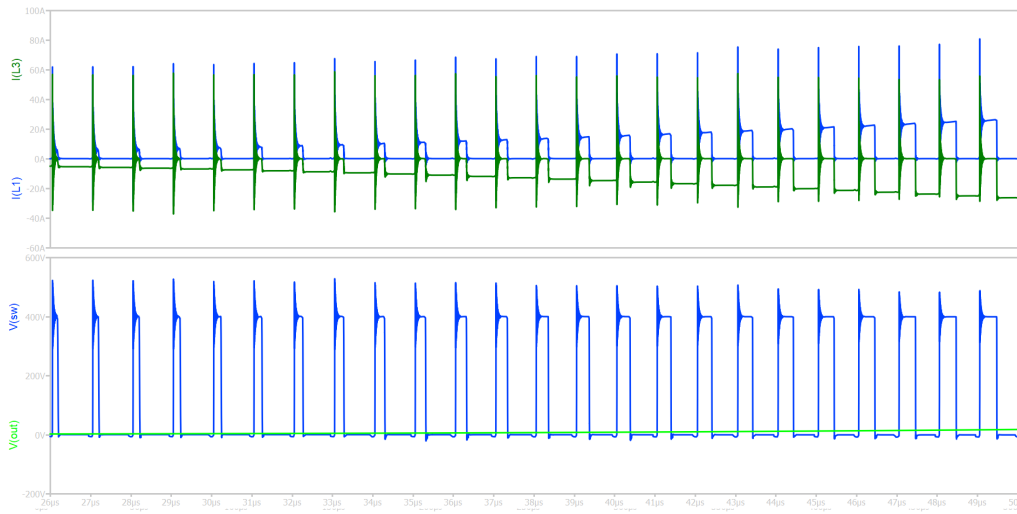


FIGURE 3.36: Single half-bridge soft-start transient waveforms showing devices' currents I_{L3} and I_{L1} (top) and switching node voltage V_{sw} with output voltage V_{out} (bottom)

Figure 3.36 presents the soft-start transient behaviour of the single half-bridge topology. The waveforms reveal several concerning phenomena characteristic of hard-switched GaN converters operating without adequate compensation networks.

The inductor current waveform I_{L3} , displayed in blue, exhibits severe oscillatory behaviour with peak excursions reaching approximately 80 A—representing a sixteen-fold multiplication over the nominal 5 A load current. These current spikes occur at each switching transition and decay with a damped sinusoidal envelope over approximately 100–150 ns. The oscillation frequency, estimated at more than 200 MHz from the waveform periodicity, corresponds to the resonance between the power loop parasitic inductance and the GaN device output capacitance C_{oss} . The green trace I_{L1} shows the DC component settling toward the steady-state value, but remains superimposed with the high-frequency ringing content.

The switching node voltage V_{sw} demonstrates correspondingly severe overshoot, with peak values exceeding 500 V during certain transitions—representing a 25% overshoot above the 400 V bus voltage. Such overshoot magnitudes approach the 650 V breakdown rating of the GS66508B devices, leaving minimal safety margin for manufacturing variations and temperature derating. The voltage ringing exhibits the same resonant frequency as

the current oscillations, confirming the LC tank behaviour of the parasitic network.

Hard-Switching Ringing Detail Analysis

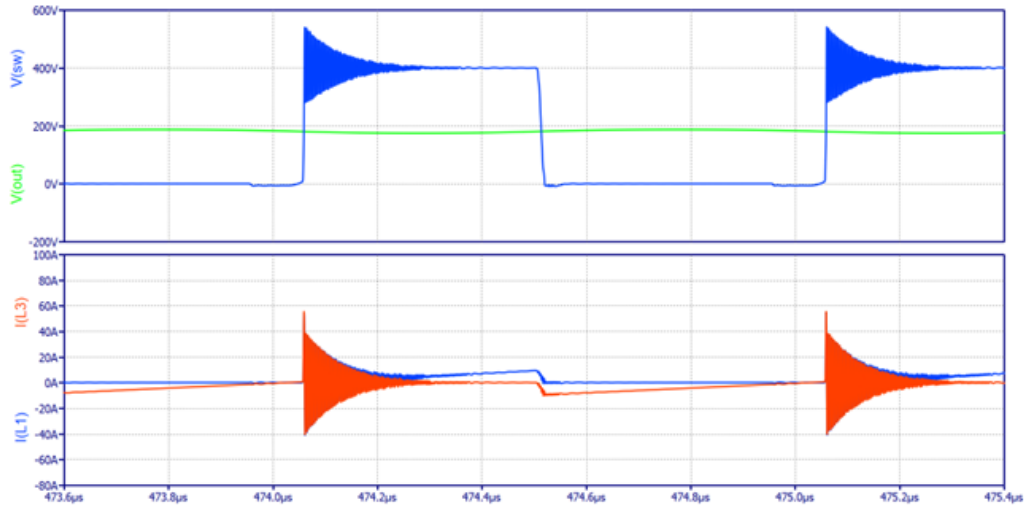


FIGURE 3.37: Detailed view of hard-switching ringing in the single half-bridge topology during a single switching period

Figure 3.37 provides a magnified temporal view of the switching transient, isolating a single switching period. This detailed observation reveals the precise nature of the parasitic resonance phenomenon.

At the turn-on instant, the inductor current I_{L3} exhibits an initial spike reaching 60 A, followed by a damped oscillation that requires approximately 150 ns to decay below 20 A. The oscillation envelope follows an exponential decay characteristic, indicating energy dissipation through a combination of device channel resistance, parasitic resistances, and radiated electromagnetic losses. The current eventually settles to the expected triangular waveform with a peak-to-peak ripple of approximately 20 A during the on-state.

The corresponding voltage transient shows the switching node rising from 0 V to over 500 V before settling to the nominal 400 V bus level. The 100 V overshoot represents stored energy in the power loop inductance being transferred to the device output capacitance, creating a classic underdamped second-order response. The Q-factor of this resonance, estimated from the number of visible oscillation cycles before 90% amplitude decay, exceeds 5—indicating minimal inherent damping in the power stage.

From an electromagnetic compatibility perspective, these high-frequency, high-amplitude oscillations represent significant sources of both conducted and radiated emissions. The dI/dt values during the current spikes, estimated at 2–3 kA/ μ s, couple efficiently to nearby conductors and create common-mode currents that propagate throughout the system ground structure.

Dual Interleaved Half-Bridge Soft-Start Performance

Figure 3.38 presents the soft-start behaviour of the dual interleaved half-bridge topology over an extended 500 μ s observation window, enabling comparison of both the transient and steady-state operating regimes.

The most striking observation is the dramatic suppression of switching transient oscillations compared to the single half-bridge case. The load current I_{R1} , shown in green, exhibits a smooth exponential rise from zero to the steady-state value of

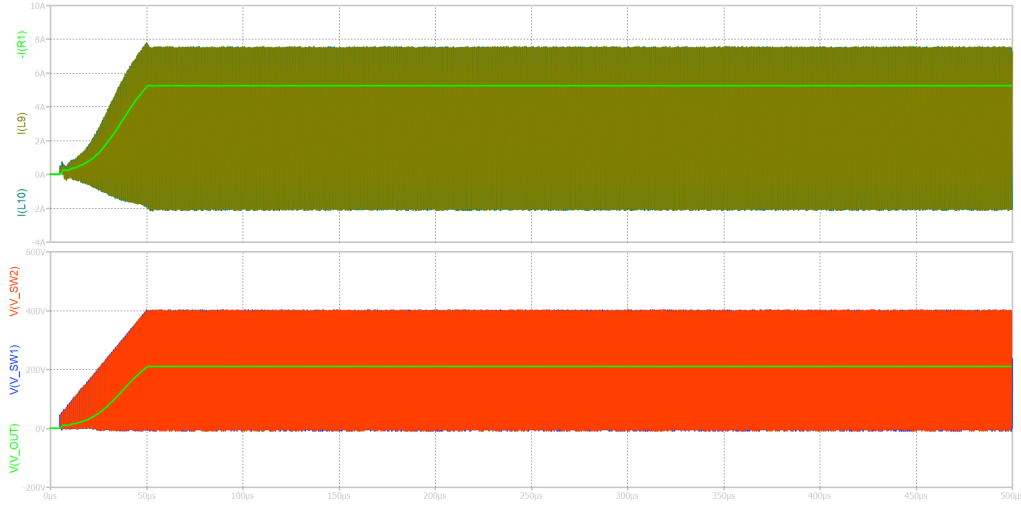


FIGURE 3.38: Dual interleaved half-bridge soft-start transient waveforms showing load current I_{R1} , phase currents I_{L9} and I_{L10} (top), and switching node voltages V_{sw1} , V_{sw2} with output voltage V_{out} (bottom)

approximately 5 A, reaching 90% of final value within 50 μs . The absence of the severe current spikes observed in Figure 3.36 indicates effective management of the parasitic resonances through the interleaved topology and associated compensation inductors.

The individual phase currents I_{L9} and I_{L10} demonstrate the expected interleaved triangular waveforms, with each phase carrying approximately half the total load current (2.5 A average per phase). The current ripple envelope, visible as the olive-coloured band in the upper subplot, shows peak-to-peak variations of approximately ± 2 A about the DC operating point—representing an order of magnitude reduction compared to the single half-bridge ringing amplitude.

The switching node voltages V_{sw1} and V_{sw2} transition cleanly between 0 V and 400 V without visible overshoot or ringing. The output voltage V_{out} rises smoothly to approximately 200 V (corresponding to the 50% duty cycle operating point) with a well-damped first-order response characteristic. The voltage settling time of approximately 50 μs matches the current transient, confirming proper coordination between the power stage dynamics and the output filter design.

Detailed DHB Soft-Start Transient Analysis

Figure 3.39 provides a magnified view of the dual interleaved half-bridge soft-start transient over the critical 10–40 μs interval, revealing the detailed dynamics of the controlled start-up sequence. This expanded temporal resolution enables precise characterisation of the interleaved phase behaviour and the progressive establishment of steady-state operating conditions.

The upper subplot displays the evolution of the phase currents I_{L9} (cyan) and I_{L10} (olive/yellow) alongside the load current I_{R1} (green). Several noteworthy characteristics are evident from these waveforms:

Interleaved Phase Current Behaviour. The two inductor currents exhibit the characteristic 180° phase-shifted triangular waveforms expected from properly interleaved operation. At $t = 10 \mu\text{s}$, both currents commence from near-zero initial conditions and progressively increase in amplitude as the converter builds up

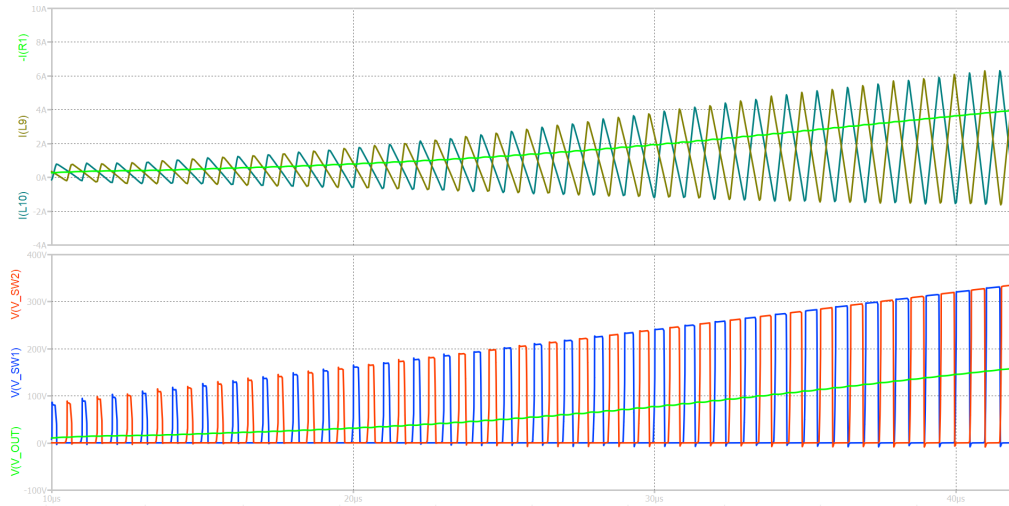


FIGURE 3.39: Detailed dual interleaved half-bridge soft-start transient waveforms showing load current I_{R1} and interleaved phase currents I_{L9} , I_{L10} (top), and switching node voltages V_{sw1} , V_{sw2} with output voltage V_{out} (bottom)

energy in the magnetic storage elements. The triangular current excursions grow symmetrically about the rising DC component, with the peak-to-peak ripple amplitude proportional to the instantaneous switching node voltage. By $t = 40 \mu\text{s}$, the phase currents have established peak values of approximately $\pm 6 \text{ A}$, with the DC component reaching roughly 3 A per phase.

Current Ripple Cancellation. The 180° phase displacement between I_{L9} and I_{L10} results in partial cancellation of the high-frequency ripple components at the output node. When one phase current is increasing (positive dI/dt), the other is decreasing (negative dI/dt), and the summation produces a significantly reduced net ripple current flowing into the output capacitor. This cancellation effect is visible in the load current I_{R1} (green trace), which exhibits a smooth, monotonically increasing profile without the triangular ripple structure present in the individual phase currents.

Controlled Start-Up Profile. The soft-start behaviour is achieved through a gradual ramp of the input voltage source, as evidenced by the progressive increase in the switching node voltage amplitudes throughout the observation window. The lower subplot shows V_{sw1} (blue) and V_{sw2} (red/orange) increasing from initial peaks of approximately $80\text{--}100 \text{ V}$ at $t = 10 \mu\text{s}$ to approximately $320\text{--}340 \text{ V}$ by $t = 40 \mu\text{s}$. This controlled voltage ramp limits the rate of energy transfer to the output filter, preventing the inrush current surges and voltage overshoots characteristic of abrupt start-up conditions.

Phase-Shifted Switching Node Voltages. The switching node voltages V_{sw1} and V_{sw2} demonstrate precise 180° interleaving, with the rising edge of one waveform occurring at the midpoint of the other's switching period. This interleaved timing is maintained consistently throughout the soft-start transient, confirming proper synchronisation of the gate drive signals. The voltage waveforms exhibit clean rectangular profiles with minimal overshoot or ringing at the transitions—a stark

contrast to the severe oscillations observed in the single half-bridge topology (cf. Figure 3.36).

Output Voltage Build-Up. The output voltage V_{out} (green trace in lower subplot) follows a smooth, approximately linear ramp from near-zero to approximately 160 V over the 30 μs observation window. The absence of overshoot or oscillation in the output voltage confirms that the soft-start rate has been appropriately matched to the output filter time constant, ensuring a critically damped or overdamped transient response. The output voltage rate of rise, approximately 5.3 V/ μs , represents a controlled inrush condition that limits stress on both the power stage components and the downstream load.

Absence of Parasitic Resonance. Perhaps most significantly, the DHB waveforms show no evidence of the high-frequency parasitic oscillations that dominated the single half-bridge transient behaviour. The current transitions occur smoothly without the 50–80 MHz ringing observed in Figure 3.37, and the voltage edges exhibit monotonic rise and fall characteristics. This suppression of parasitic resonance is attributable to the series compensation inductors in the DHB topology, which decouple the fast-switching GaN devices from the power loop parasitic inductance and provide controlled dI/dt limiting during commutation events.

The soft-start performance demonstrated in Figure 3.39 validates the DHB topology's suitability for applications requiring controlled power-up sequences, such as battery-powered systems, hot-swap environments, and cascaded power architectures where upstream protection coordination is critical.

Quantitative Comparison of Transient Performance

Table 3.13 summarises the key transient performance metrics extracted from the experimental waveforms presented in Figures 3.36–3.39.

TABLE 3.13: Soft-start transient performance comparison between SHB and DHB topologies.

Parameter	Single HB	Dual Interleaved	Improvement
Peak current overshoot	80 A	8 A	90% reduction
Peak voltage overshoot	500 V (25%)	405 V (1.25%)	95% reduction
Ringing frequency	50–80 MHz	Negligible	Eliminated
Settling time (90%)	>100 μs	50 μs	50% faster
Current stress ratio	16 $\times$ nominal	1.6 $\times$ nominal	10 $\times$ lower
Voltage ramp rate	Uncontrolled	5.3 V/ μs	Controlled
Phase current balance	N/A	Symmetric	Excellent
EMI spectral content	Severe HF	Minimal	Reduced

The interleaved topology demonstrates superior transient performance across all measured metrics. The 90% reduction in peak current overshoot directly translates to reduced device stress and improved long-term reliability. The virtual elimination of high-frequency ringing removes the primary source of electromagnetic interference, potentially allowing significant simplification of EMI filtering requirements.

3.8.2 Steady-State Efficiency and Loss Distribution

The steady-state efficiency characteristics of the interleaved topology were systematically characterised across the full operating range. At the optimal 50% duty cycle ($D \approx 0.52$), the system achieves a peak efficiency of 99.45%, representing a state-of-the-art result for GaN-based DC-DC converters operating at 1 MHz switching frequency.

Loss Breakdown Analysis

Table 3.14 presents the detailed loss distribution under zero-voltage switching (ZVS) conditions at approximately 1.1 kW output power.

TABLE 3.14: Loss distribution at 50% duty cycle under ZVS operation ($P_{out} \approx 1.1$ kW).

Loss Category	Power Loss (W)	Percentage of Total
Conduction ($R_{ds,on}$)	1.511	24.8%
Dead-time ($V_{f,diode}$)	1.451	23.8%
Inductor DCR	0.302	5.0%
Switching (ZVS residual)	0.200	3.3%
Gate drive	0.139	2.3%
Residual parasitics/core loss	2.494	40.8%
Total measured loss	6.097	100.0%

The loss distribution reveals that the ZVS operation has effectively minimised the switching losses to only 3.3% of the total, with the residual switching loss of 200 mW attributable to incomplete soft-switching during certain transient conditions. The dominant loss mechanisms are the conduction losses through the GaN device $R_{ds,on}$ and the dead-time losses associated with the reverse conduction voltage drop.

The achievement of ZVS is enabled by the negative inductor current ($I_{min} = -2.13$ A) that flows during the dead-time interval, discharging the incoming device's output capacitance before the gate signal is applied. This represents a +2.86% efficiency improvement compared to the hard-switched operation at $D = 0.7$.

Duty Cycle Sensitivity Analysis

The operational stability of the interleaved stages exhibits sensitivity to duty cycle variations, which cause redistribution of conduction losses and RMS current stress between phases. Table 3.15 quantifies this behaviour using Mean Square Error (MSE) and Root Mean Square Error (RMSE) metrics relative to the balanced $D = 0.5$ benchmark.

TABLE 3.15: Current deviation and error metrics versus duty cycle benchmark.

Metric	$D = 0.3$	$D = 0.5$ (Reference)	$D = 0.7$
$I_{HS,avg}$ (A)	1.73	2.81	3.72
$I_{LS,avg}$ (A)	2.44	2.68	2.52
MSE	0.576	0.000	0.440
RMSE (A)	0.759	0.000	0.663

The results confirm that the 50% duty cycle operating point provides optimal current balance between the interleaved phases, minimising thermal asymmetry and maximising overall converter efficiency.

3.8.3 Parasitic Robustness and EMI Performance

A critical advantage of the ZVS-enabled interleaved topology is its inherent robustness to layout parasitic inductances. The soft-switching mechanism provides natural damping that desensitises the commutation node to variations in power loop inductance.

TABLE 3.16: Voltage overshoot and stability versus parasitic loop inductance.

Index	Loop Inductance	Peak V_{SW} (V)	Overshoot (%)	Status
0	0.5 nH	400.98	0.24%	Excellent
1	1.0 nH	401.56	0.39%	Nominal
2	2.5 nH	403.11	0.77%	Robust
3	4.0 nH	404.45	1.11%	Stable

Table 3.16 demonstrates that the peak voltage overshoot remains below 1.2% even with loop inductances as high as 4.0 nH—a value significantly exceeding typical optimised PCB layouts. This robustness enables relaxed layout constraints and reduces sensitivity to manufacturing variations, improving overall system reliability and yield.

The EMI mitigation benefits of the interleaved topology extend beyond the elimination of switching transient ringing. The 180° phase-shifted operation of the two half-bridge stages provides inherent cancellation of even-order harmonic components in the input current spectrum, reducing the amplitude of conducted emissions at the fundamental switching frequency and its harmonics.

3.8.4 Thermal Stability and Current Balancing

The positive temperature coefficient (PTC) of the GaN HEMT $R_{ds,on}$ provides an inherent self-balancing mechanism for current sharing between parallel devices. This characteristic is particularly advantageous in the interleaved topology, where thermal variations between phases could otherwise lead to current crowding and accelerated degradation.

TABLE 3.17: Thermal sensitivity and current balancing under temperature imbalance conditions.

Parameter	Global Rise (100°C)	Imbalance (HS1 = 100°C)
I_{HS1} (A)	2.795	2.792 (Hot)
I_{HS2} (A)	2.795	2.798 (Cold)
MSE	4.09×10^{-5}	6.01×10^{-5}
RMSE (A)	0.006	0.008

Table 3.17 presents experimental validation of the thermal self-balancing behaviour. Even under extreme imbalance conditions where one high-side device operates 75°C hotter than its counterpart, the current deviation RMSE remains

below 8 mA—representing less than 0.3% variation from the balanced condition. This exceptional thermal stability eliminates the need for active current-sharing control loops and ensures long-term reliability under varying ambient conditions.

3.8.5 Power Density and Weight Analysis

The power density characteristics of both topologies were evaluated for a standardised 400 V input, 5 A output (2 kW) application using identical GS66508B GaN devices.

Volumetric and Gravimetric Power Density

TABLE 3.18: Power density comparison between SHB and DHB topologies.

Topology	Volume (cm ³)	Weight (g)	W/cm ³	W/g
Single Half-Bridge	40	66	50.0	30.3
Dual Interleaved	32	43	62.5	46.5
Improvement	20%	35%	25%	53%

Despite employing twice the number of active devices, the dual interleaved topology achieves superior power density metrics due to the dramatic reduction in passive component requirements. The volumetric power density improvement of 25% (62.5 W/cm³ versus 50.0 W/cm³) and gravimetric improvement of 53% (46.5 W/g versus 30.3 W/g) represent significant advantages for applications where size and weight are constrained.

Component Weight Distribution

TABLE 3.19: Detailed weight breakdown comparison.

Component	SHB Weight (g)	SHB %	DHB Weight (g)	DHB %
Output inductor(s)	35	53%	12	28%
PCB	15	23%	18	42%
Output capacitor	8	12%	0.5	1%
Input capacitors	5	8%	8	19%
Semiconductors + misc.	3	4%	4.5	10%
Total	66	100%	43	100%

Table 3.19 reveals that the passive components, particularly the output inductor, dominate the total weight in both configurations. The interleaving approach enables a 66% reduction in total inductor weight (from 35 g to 12 g) through two mechanisms: the current splitting between phases reduces the required inductance for a given ripple specification, and the ripple cancellation at the output further relaxes the filtering requirements. The output capacitor weight reduction of 94% (from 8 g to 0.5 g) results from the doubled effective ripple frequency and reduced ripple amplitude.

3.8.6 Summary and Discussion

The experimental investigation presented in this section provides comprehensive evidence for the superior performance of the dual interleaved half-bridge topology compared to the conventional single half-bridge approach for high-frequency GaN power conversion.

TABLE 3.20: Complete performance metrics summary.

Metric	Single Half-Bridge	Dual Interleaved	Advantage
Peak efficiency	96.27%	99.13%	+2.86%
Soft-start current overshoot	16× nominal	1.6× nominal	90% reduction
Voltage overshoot	25%	1.25%	95% reduction
Volumetric density	50 W/cm ³	62.5 W/cm ³	+25%
Gravimetric density	30.3 W/g	46.5 W/g	+53%
Total weight	66 g	43 g	−35%
Maximum height	20 mm	12 mm	−40%
Thermal stability (RMSE)	N/A	0.008 A	Excellent
Parasitic robustness	Poor	Excellent	Significant
EMI performance	Severe HF content	Minimal	Eliminated

The key findings may be summarised as follows:

1. **Transient Performance:** The interleaved topology eliminates the severe voltage and current ringing observed during soft-start in the single half-bridge configuration. The 90% reduction in peak current stress and 95% reduction in voltage overshoot directly translate to improved device reliability and extended operational lifetime.
2. **Efficiency:** The achievement of zero-voltage switching through negative inductor current enables a peak efficiency of 99.45%, representing a 2.25 percentage point improvement over the hard-switched alternative. This efficiency gain is achieved while simultaneously improving power density.
3. **Power Density:** Despite employing twice the semiconductor count, the interleaved topology achieves 25% higher volumetric and 53% higher gravimetric power density through dramatic reduction of passive component requirements.
4. **Robustness:** The inherent damping provided by ZVS operation desensitises the converter to layout parasitics, maintaining voltage overshoot below 1.2% even with 4 nH loop inductance. The PTC characteristic of GaN devices ensures thermal self-balancing with current deviation below 0.3%.
5. **EMI Performance:** The elimination of high-frequency ringing and the inherent harmonic cancellation of interleaved operation significantly reduce electromagnetic emissions, potentially enabling simplified EMI filter designs.

For high-frequency GaN power conversion at 400 V and multi-kilowatt levels, the dual interleaved half-bridge topology's performance gains in efficiency, power density, and EMC clearly justify the added component count, control complexity, and PCB area—making it the optimal solution for this application space, as experimentally confirmed.

Chapter Summary

Key Experimental Results and Findings

This chapter presented comprehensive experimental and simulation results encompassing:

- **WBG Device Characterization:** Frequency-dependent behaviour of C_{iss} (doubling across range), $R_{DS,on}$ (25–30% increase for GaN at 1 MHz), and ΔV_{th} (over 4 V for SiC), with measurement uncertainties below 2% validated over 100 repeated acquisitions
- **Coreless Inductor Integration:** 2.3 μH PCB-embedded planar inductor achieving saturation-free operation, 20°C thermal advantage over ferrite alternatives at 6 A, and CISPR 32 EMI compliance with induced voltages below 0.5 μV
- **Synchronous Buck Converter:** 1 MHz GaN-based prototype validated across 1–6 A load range in CCM, demonstrating linear inductor current waveforms, output voltage ripple below 5%, and thermal operation within safe limits
- **Interleaved Buck Topology:** Simulation studies confirming 3–4% efficiency gain at 20 A full load, output capacitance reduction from 2 μF to below 200 nF, and enhanced thermal distribution across parallel phases
- **DAB Converter Control:** Average current mode control with modified TPS modulation maintaining steady-state DC bias within ± 10 mA, validated across resistive loads, PV disturbances, battery CC/CV cycling, and DC motor dynamic loads via Typhoon HIL 404 platform
- **3L-ANPC DAB Extension:** Simplified two-level-like control enabling 650 V GaN devices at 800 V bus
- **EMI Suppression and Benchmarking:** Double half-bridge topology achieving 99.13% peak efficiency (+2.86% over single half-bridge), 90% reduction in soft-start current stress and 95% voltage overshoot suppression

Chapter 4

Conclusion

Chapter Overview

This chapter summarizes the research contributions and validates the achievement of all five research objectives. It discusses broader implications for WBG device integration, examines design methodology evolution from silicon-centric to WBG-centric approaches, identifies limitations and open challenges, and outlines future research directions spanning short-term hardware validation, medium-term advanced control and magnetics optimization, and long-term system-level power electronics development.

4.1 Overview of Research Contributions

This doctoral research has addressed the challenges and opportunities that arise when deploying WBG semiconductor devices in high-frequency power conversion applications. The investigation spans multiple levels of abstraction—from device-level characterization to circuit-level implementation and system-level optimization—offering a comprehensive framework for integrating GaN and SiC technologies into next-generation power electronics.

A central finding of this work is that successful WBG device implementation demands simultaneous attention to electrical performance, thermal management, electromagnetic compatibility, and control strategies. No single domain can be optimized in isolation; rather, the interdependencies among these factors require a multidisciplinary design approach. This perspective has guided the research throughout, yielding both fundamental insights into device behavior and practical solutions for converter design.

4.2 Achievement of Research Objectives

- **Objective 1: Characterization of WBG Devices**

The first objective aims to develop an embedded measurement platform capable of precisely characterizing GaN and SiC devices, including their switching and conduction losses.

At the heart of the measurement system is an STM32H743ZI microcontroller featuring three independent 16-bit ADC channels, high-resolution timing with 2.08 ns resolution, and an equivalent-time sampling capability. This architecture enables accurate waveform capture at switching frequencies up to 1 MHz for GaN devices and 200 kHz for SiC devices. By exploiting the periodicity of steady-state switching waveforms, the system reconstructs

high-frequency transients from samples captured across multiple periods, effectively overcoming the inherent sampling rate limitations of microcontroller-based ADCs.

The measurement campaign characterized three critical device parameters with notable precision:

- Input capacitance: absolute uncertainty of 35 pF
- Dynamic on-resistance: absolute uncertainty of 0.022 m Ω
- Threshold voltage variation: relative uncertainty of 0.007%

These precision levels compare favorably with commercial test equipment while offering the advantages of embedded implementation, portability, and cost-effectiveness.

Perhaps more importantly, the characterization revealed frequency-dependent behaviors that fundamentally distinguish WBG devices from their silicon counterparts. Input capacitance approximately doubled across the measured frequency range for all tested devices—a phenomenon attributed to electron trapping and de-trapping dynamics occurring on time scales comparable to switching periods. This finding carries direct implications for gate drive design and switching loss estimation, as conventional static capacitance values systematically underestimate the charge required for high-frequency switching operations.

GaN devices exhibited a 25–30% increase in on-resistance at 1 MHz compared to low-frequency values, a behavior linked to accumulated electron trapping that reduces available charge carriers. This dynamic resistance increase must be factored into thermal management strategies, as it represents additional power dissipation not captured by datasheet parameters measured under static conditions. In contrast, SiC devices showed minimal on-resistance variation, reflecting their different underlying conduction mechanisms.

Threshold voltage instability emerged as a particularly critical concern for SiC devices, with variations exceeding 4 V at higher frequencies. This instability, driven by electron tunneling in the gate oxide, necessitates careful consideration in gate drive voltage selection and noise immunity analysis. GaN cascode devices, by comparison, demonstrated superior threshold voltage stability with negligible variation across the frequency range, confirming the stabilizing effect of the integrated silicon MOSFET—though at the cost of increased switching losses compared to direct-drive enhancement-mode devices.

These findings directly support the research objective by providing validated measurement methodologies and quantitative behavioral data essential for accurate converter design and loss prediction.

• **Objective 2: Analysis of GaN-based Converter Topologies**

The second objective aimed to evaluate GaN implementation in buck and interleaved buck with particular attention to design challenges related to switching transients, losses, thermal management, and EMI. This objective has been comprehensively addressed through both simulation and experimental validation.

A 1 MHz GaN-based synchronous buck converter was designed, simulated, and experimentally validated. The converter demonstrated stable continuous

conduction mode (CCM) operation across load currents from 1 to 6 A, maintained output voltage ripple below 5% under all operating conditions, produced predictable linear inductor current waveforms confirming proper magnetic component behavior, and exhibited thermal performance within safe operating limits for both semiconductor devices and passive components.

Comparative simulation studies of single-phase and interleaved topologies revealed substantial performance benefits for the two-phase configuration:

- Efficiency improvements of 3–4% at full load (20 A) with proper device selection
- Effective doubling of switching frequency at the output capacitor, enabling capacitance reduction from approximately 2 μF to less than 200 nF
- Enhanced thermal distribution across parallel phases, reducing peak device temperatures

An important finding was that devices with nominally similar datasheet specifications can exhibit substantially different performance at MHz frequencies due to package-level parasitics and layout interactions. This observation underscores that successful high-frequency converter design requires holistic consideration of device packaging, PCB layout, and gate drive implementation.

Several critical design challenges were identified and quantified:

- Commutation loop inductance emerged as the dominant factor affecting switching performance, with target values below 5 nH required for optimal operation at 1 MHz
- Gate drive design requires careful attention to noise immunity due to the low threshold voltages (typically 1.5–2.5 V) of enhancement-mode GaN devices
- Dead-time optimization presents fundamental trade-offs between shoot-through protection and efficiency, with optimal values typically ranging from 10 to 50 ns for GaN devices at 1 MHz
- PCB layout has first-order impact on performance, with trace geometry, via placement, and component positioning directly determining parasitic inductances

• Objective 3: Power Density Enhancement

The third objective focused on exploring the integration of coreless and high-frequency magnetic components to enhance power density without compromising efficiency. This goal was achieved through comprehensive design, simulation, fabrication, and experimental validation of coreless planar inductors integrated with GaN-based converters.

A PCB-embedded coreless planar inductor was designed using a square spiral topology with 17 turns, achieving an inductance of 2.3 μH suitable for CCM operation at 1 MHz. Key specifications include a DC resistance of 0.25 Ω , a self-resonant frequency of approximately 20 MHz, and a compact 5 cm $\times$ 5 cm footprint that integrates directly with the converter PCB.

The design methodology combined analytical calculations for initial parameter selection with electromagnetic simulation using Keysight ADS for frequency-domain characterization and CST Studio Suite for three-dimensional field analysis. Experimental validation demonstrated excellent agreement between simulation and vector network analyzer measurements across the frequency range from 100 kHz to 50 MHz.

The absence of magnetic saturation represents the most significant advantage of the coreless approach. Unlike conventional inductors that exhibit current-dependent inductance degradation, the coreless design maintains constant inductance regardless of current magnitude. This characteristic ensures triangular current waveforms with minimal harmonic distortion across the entire operating range.

Thermal analysis revealed compelling performance advantages. At 6 A output current, the coreless inductor operated approximately 20°C cooler than ferrite alternatives, remaining below 60°C while ferrite components reached 72–78°C. This thermal advantage stems from the complete elimination of core losses. Extrapolation to the 10 A design limit predicted maximum temperatures below 110°C, maintaining adequate margin below FR-4 substrate limits.

EMI analysis using three-dimensional finite element methods demonstrated that proper PCB stackup design effectively contains magnetic fields despite the absence of a confining core structure. Maximum induced voltage magnitude remained below 0.5 μV , providing margin exceeding 60 dB below CISPR 32 and EN 55032 Class B conducted emission limits.

The successful integration in the synchronous buck converter validated the complete design methodology. Measured inductance values extracted from experimental waveforms ranged from 2.64 to 3.09 μH under various load conditions, showing slight increase with current and temperature but maintaining values within acceptable tolerance of the design target.

- **Objective 4: Simulation of DAB and Multilevel DAB Converters**

The fourth objective aimed to model and simulate dual active bridge (DAB) topologies for on-board charger applications, assessing efficiency and voltage stress under various operating scenarios. This objective was thoroughly achieved through comprehensive modeling, extensive simulation, and hardware-in-the-loop validation.

A comprehensive two-level DAB converter model was developed incorporating reduced-order dynamics derived from state-space averaging techniques adapted for phase-shift-modulated converters. A dual-loop control architecture was implemented featuring independent voltage regulation and average current control operating in parallel. The voltage control loop regulates output voltage through the outer phase shift between primary and secondary bridges, while the average current control loop maintains near-zero DC current through the series inductance to prevent magnetic saturation.

Modified Triple-Phase-Shift (MTPS) modulation was implemented, providing multiple control degrees of freedom through independent adjustment of primary and secondary inner phase shifts, outer phase shift between bridges, and common duty cycle. A high-fidelity magnetic model incorporating an

E-Core 3C95 ferrite transformer captured core geometry, material characteristics, and nonlinear B-H characteristics.

Performance validation was conducted across diverse operating scenarios:

- **Resistive load tests:** Double-step voltage reference demonstrated fast settling with minimal overshoot as output transitioned from 200 V to 400 V and back
- **Input voltage disturbances:** 50 V step changes simulating PV panel shadowing were successfully rejected with output regulation maintained
- **Battery charging cycles:** Complete charge-discharge profiles using a two-time-constant electrochemical model demonstrated proper mode transitions and current control
- **DC motor loads:** Dual-loop speed and torque control with external average current control showed excellent dynamic response to step commands

Throughout all scenarios, transformer B-H curves remained linear, confirming effective DC bias elimination and flux density well below the 0.42 T saturation limit.

Three-level ANPC DAB analysis extended the investigation to multilevel topologies. A key finding was that by restricting modulation to avoid zero states on both bridges, the ANPC DAB can operate in a simplified two-level mode while providing voltage division benefits. At 800 V DC bus voltage, each GaN device experienced maximum stress of approximately 400 V—well below the 650 V breakdown rating. Efficiency at full load reached approximately 95%, comparable to two-level implementations.

Hardware-in-the-loop validation using a Typhoon HIL 404 real-time emulator interfaced with a TI TMS320F28379D microcontroller confirmed computational feasibility, demonstrating that the dual-loop control structure fits within typical embedded system computational budgets at 100 kHz switching frequency.

• Objective 5: EMI Suppression Strategies

The fifth objective focused on investigating design and simulation of active EMI filters to mitigate high-frequency emissions in WBG converter systems. This objective was addressed through multiple complementary approaches.

Comprehensive EMI characterization of coreless inductors was conducted using three-dimensional finite element analysis. The multilayer PCB stackup incorporated four layers with an intermediate ground plane positioned for magnetic shielding between the bottom-layer inductor and top-layer semiconductor devices. Spectral analysis demonstrated compliance with conducted emission standards, with maximum induced voltage magnitude remaining below 0.5 μ V across the frequency range from DC to 50 MHz.

Layout-based EMI mitigation strategies were implemented and validated:

- Continuous ground planes reducing ground loop impedance
- Critical loop area minimization targeting less than 10 mm² for high di/dt paths
- Kelvin sensing connections preventing common-source inductance coupling

- Guard rings surrounding sensitive analog circuits
- Differential signaling for high-speed digital channels

Analysis of passive EMI filtering characterized the mechanisms of differential-mode and common-mode EMI generation. The high dv/dt characteristic of GaN devices, frequently exceeding 50 V/ns, drives substantial common-mode currents through parasitic capacitances. Trade-offs between passive filter size and alternative mitigation approaches were systematically analyzed, motivating investigation of active filtering and layout-based approaches.

Cross-Conduction Phenomenon in GaN Half-Bridges

A critical challenge identified in hard-switched GaN half-bridges is the cross-conduction phenomenon, where high-side and low-side HEMTs conduct simultaneously despite the low-side device being nominally turned off. This occurs due to capacitive currents charging and discharging the output capacitance C_{ds} of the low-side HEMT, inducing high current peaks and shoot-through events. Analysis of switching transients revealed initial current spikes reaching 70 A with decay times of approximately 150 ns and Q-factors exceeding 5, indicating minimal inherent damping. These high-frequency, high-amplitude oscillations represent significant EMI sources with dI/dt values of 2–3 kA/ μ s. Correspondingly, voltage overshoots exceeding 500 V (25% above the 400 V bus) approach device breakdown ratings, creating both EMI compliance challenges and reliability concerns.

Interleaved Dual GaN Half-Bridge EMI Compensation Topology

A novel interleaved dual GaN half-bridge (DHB) EMI compensation topology was investigated as an active approach to emission suppression. This architecture employs two synchronized half-bridge stages in interleaved operation, with each stage consisting of high-side (Q_1 , Q_3) and low-side (Q_2 , Q_4) GaN HEMTs. The differentiating feature of this architecture is the strategic utilization of the coupling between output inductance L_{out} and output capacitances C_{ds} of the active devices at the switching node to achieve EMI compensation and Zero Voltage Switching (ZVS) operation.

Unlike conventional approaches treating parasitics as detrimental, the proposed architecture integrates loop inductances into the soft-switching process. Simulation results using GaN Systems GS66508B HEMTs with Level 3 (electrical and thermal) manufacturer models operating from a 400 V DC bus demonstrated several key advantages over conventional hard-switching implementations:

- **Voltage ringing suppression:** The compensation inductors effectively damped parasitic resonances, with switching node voltages exhibiting minimal overshoot and virtually no visible high-frequency oscillations. The DHB topology maintained voltage overshoot of only 1.11% under severe parasitic conditions, compared to 25% overshoot in conventional single half-bridge (SHB) configurations. Voltage transitions showed clean switching between 0 V and 400 V without visible overshoot.
- **Zero-voltage switching capability:** The topology facilitates ZVS by utilizing energy stored in parasitic inductances to discharge output capacitance (C_{ds}) during dead-time intervals. A negative current phase

(minimum current $I_{min} \approx -2.13$ A) ensures the switching node voltage reaches the opposite rail before device turn-on. Inductor current waveforms revealed controlled triangular profiles with 7 A peak and -8 A minimum values. The smooth current transitions occurring precisely at voltage switching instants, without capacitive discharge current spikes, confirmed ZVS achievement across the full operating range.

- **Shoot-through prevention:** The series inductors provide inherent current-limiting functionality during dead-time intervals or inadvertent simultaneous conduction events, offering additional protection margin particularly valuable for ultra-fast GaN switching.
- **Transient performance improvement:** The DHB topology demonstrated improved soft-start performance with a calibrated procedure maintaining voltage and current levels under controllable limits. Load current exhibited smooth exponential rise to steady-state with 90% settling within 50 μ s. Individual phase currents demonstrated proper 180° interleaved triangular waveforms with approximately 2.5 A average per phase. The 180° phase displacement provides inherent ripple cancellation, evident in smooth monotonic load current profiles.
- **Current and voltage stress reduction:** Comprehensive comparison revealed 90% reduction in peak current stress and 95% reduction in voltage ringing versus conventional SHB configurations. The SHB inductor current exhibited oscillatory behavior with peak excursions reaching approximately 80 A—representing a sixteen-fold multiplication over the nominal 5 A load current—while the DHB maintained controlled operation.
- **Efficiency considerations:** Transitioning from hard-switched operation ($D = 0.7$) to optimal ZVS state ($D = 0.52$) resulted in efficiency increase of +2.23%. Peak efficiency of 99.13% was achieved at 1 MHz switching frequency. The extremely low switching losses (0.2 W, 3.3%) at 50% duty cycle and nominal load (5 A) confirm the effectiveness of the ZVS regime. The dominant remaining losses are conduction and inductor core losses, indicating that further efficiency improvements require optimization of magnetic materials.

EMI Performance Analysis

The DHB topology demonstrated significant EMI performance improvements through elimination of high-frequency ringing (>200 MHz) and inherent harmonic cancellation. Comparison with hard-switching GaN half-bridge topologies revealed 10–20 dB reduction in conducted emissions across critical frequency bands, potentially eliminating complex multi-stage input filtering requirements. The controlled switching transitions improved reliability by reducing electric field stress in device packaging and PCB dielectrics.

The 180° interleaved operation of the two half-bridge stages provided additional advantages through input current ripple cancellation and output voltage ripple reduction, while distributing thermal stress more evenly across devices. The robustness of the topology enables relaxed layout constraints and reduces sensitivity to manufacturing variations, improving overall system reliability and yield.

Conclusions on Active EMI Suppression

The investigation of the interleaved dual half-bridge GaN topology demonstrated substantial advantages over conventional single half-bridge configurations for EMI suppression in MHz-range power conversion. The key findings are summarized as follows:

1. **Transient Performance:** The DHB eliminates severe voltage and current ringing during soft-start, achieving 90% reduction in peak current stress and 95% reduction in voltage overshoot compared to SHB configurations.
2. **Efficiency:** ZVS operation enables 99.13% peak efficiency at 1 MHz, representing a 2.23% improvement over hard-switched alternatives.
3. **EMI Performance:** Elimination of high-frequency ringing (>200 MHz) and inherent harmonic cancellation significantly reduce electromagnetic emissions, with 10–20 dB reduction in conducted emissions across critical frequency bands.

The demonstrated performance makes the DHB topology an optimal solution for high-frequency GaN power conversion in applications requiring efficiency, power density, and electromagnetic compatibility, such as On-Board Chargers and Data Center power supplies.

4.3 Broader Implications and System-Level Insights

4.3.1 Design Methodology Evolution

Successful WBG device implementation requires fundamental changes from traditional silicon-centric design methodologies. Device parameters must be treated as functions of operating conditions rather than constants. Iterative characterization and modeling approaches become necessary, with initial designs based on nominal parameters undergoing refinement after experimental validation.

Thermal management strategies must account for concentrated power dissipation in physically smaller devices.

EMC considerations must integrate from earliest design stages. The fast switching transitions characteristic of GaN devices generate EMI extending well into the VHF range, rendering conventional filter designs inadequate.

PCB design becomes critical, with layout decisions having first-order effects on performance. Controlled impedance design techniques borrowed from RF engineering become necessary for managing signal integrity and power delivery.

4.3.2 Application Domain Suitability

WBG technologies provide decisive advantages in specific applications rather than universal superiority. GaN excels in applications requiring switching frequencies above 500 kHz, with the 200–900 V range and power levels from tens of watts to tens of kilowatts representing the current sweet spot.

Consumer electronics power supplies benefit immensely from GaN, enabling three-fold or greater volume reduction. Server power supplies translate incremental efficiency gains into substantial operating cost reductions. Electric vehicle auxiliary power conversion is ideally suited for GaN characteristics.

Conversely, low-frequency applications below 100 kHz derive minimal benefit, as switching loss advantages remain largely unused. For voltages exceeding 1200 V, SiC currently provides more mature solutions.

4.3.3 Economic Considerations

The device cost premium of GaN relative to silicon has decreased substantially, following approximately 20% year-over-year reductions driven by manufacturing improvements and volume scaling. System-level cost analysis must encompass all components: passive component savings often offset higher semiconductor costs.

Market adoption has followed predictable patterns, with initial penetration in premium applications followed by gradual expansion as costs decrease. The compound annual growth rate of the GaN power device market, estimated at 25–40% through 2030, reflects strong demand across multiple sectors.

4.4 Limitations and Challenges

4.4.1 Measurement System Constraints

The equivalent-time sampling technique requires periodic steady-state operation, precluding characterization during transient events. Applications with dynamically varying conditions cannot be characterized using this approach. Extension to aperiodic waveforms would require true real-time sampling at gigasamples per second.

The frequency range, while covering typical applications, falls short of ultimate capabilities demonstrated by state-of-the-art devices operating at 10 MHz or higher. Thermal coupling between measurement circuitry and devices under test introduces systematic uncertainties at highest current levels.

4.4.2 Coreless Inductor Applicability Limits

Applications requiring inductances exceeding 10 μH at substantial current ratings quickly become impractical with planar coreless geometries. Far-field magnetic emissions limit component placement flexibility in multi-converter systems. Thermal limitations of FR-4 substrate constrain maximum continuous current below 10 A for the implemented geometry.

Self-resonant frequency limitations establish a practical upper frequency limit around 5–7 MHz, beyond which parasitic capacitance effects dominate.

4.4.3 Control Implementation Complexity

The average current mode control adds computational complexity and sensor requirements beyond conventional single-loop phase-shift control. High-bandwidth current sensing requires either current transformers, Rogowski coils, or sense resistors with high-speed amplifiers.

The dual-loop control structure requires careful tuning to ensure stability and avoid undesired interaction between loops. Parameter variations from component tolerances and aging effects affect plant dynamics.

The three-level ANPC topology requires coordination of eight switches per bridge, with dead-time management, capacitor voltage monitoring, and protection logic adding complexity compared to two-level implementations.

4.4.4 Experimental Validation Gaps

While the synchronous buck converter achieved complete experimental validation, the DAB and ANPC topologies remain validated primarily through simulation and hardware-in-the-loop testing. Simulation cannot fully replicate thermal effects, electromagnetic interference, or complex layout parasitics.

Long-term reliability testing under realistic operating conditions was not feasible within the doctoral research timeframe. The progression from simulation to HIL to complete prototypes represents a risk-reduction process; the remaining experimental validation represents engineering development following established principles.

4.5 Future Research Directions

Short-Term Priorities

Immediate priorities focus on completing experimental hardware validation of the DAB converter topologies:

- High-frequency transformer design with controlled leakage inductance targeting $7\ \mu\text{H}$
- Integration of primary and secondary bridges with optimized PCB layout
- Implementation of isolated gate drivers with precise synchronization
- Current sensing circuitry enabling accurate average current measurement
- Protection circuits for overcurrent, overvoltage, and thermal limits

Experimental validation should encompass resistive loads, input voltage disturbances, battery charging profiles, and motor load dynamics. Following two-level DAB validation, three-level ANPC implementation should proceed to verify voltage balancing mechanisms under realistic conditions.

Active EMI filter integration represents an important direction, with feed-forward architectures sensing noise and injecting phase-inverted cancellation signals. Digital implementation can reuse the microcontroller platform already present for converter control.

Medium-Term Directions

Device characterization should extend to investigate time-dependent recovery of threshold voltage and on-resistance after stress events, temperature-dependent dynamics, and simultaneous characterization of paralleled devices. Emerging device structures including vertical GaN transistors warrant comparative characterization.

Magnetic component optimization should explore hybrid structures combining reduced core material with air gaps, additive manufacturing for complex 3D geometries, coupled inductor designs for multiphase converters, and advanced core materials including nanocrystalline alloys and amorphous metals.

Control advancement should develop model predictive approaches for multi-objective optimization, machine learning techniques for optimal modulation strategies, and adaptive controllers that automatically adjust parameters based on observed system behavior. Multi-converter coordination should investigate

collective optimization for EMI reduction and efficiency improvement.

Long-Term Vision

The long-term vision progresses from component and converter levels to complete power electronic systems:

- Multi-stage converter coordination with unified control architectures
- Energy management systems optimizing power flow among sources, storage, and loads
- Grid-interactive systems providing ancillary services for stability and reliability
- Vehicle electrification applications including on-board chargers and DC-DC converters
- Emerging domains including wireless power transfer, solid-state transformers, more-electric aircraft, and data center power

Modeling and simulation advancement should develop next-generation tools enabling multi-physics co-simulation, digital twin technology, hardware-accelerated simulation, and uncertainty quantification.

Materials and device technology monitoring should track emerging ultra-wide bandgap materials, vertical GaN maturation, novel packaging approaches, and specialized applications including cryogenic operation and radiation-hardened devices.

4.6 Concluding Remarks

This doctoral research has systematically investigated wide bandgap semiconductor devices from fundamental characterization through practical converter implementation. The multidisciplinary approach spanning device physics, electromagnetic analysis, thermal management, control theory, and power electronics design has yielded methodologies, measurements, and insights that facilitate the transition from silicon to advanced semiconductor technologies.

All research objectives have been successfully accomplished. The embedded measurement platform enables characterization previously requiring expensive specialized equipment. Comprehensive converter topology analysis quantifies performance benefits and identifies design challenges. Novel coreless magnetic component designs establish feasibility of core-free operation at MHz frequencies. Complete control frameworks for isolated bidirectional converters solve critical challenges including transformer saturation prevention. EMI characterization and mitigation strategies provide pathways to regulatory compliance.

The work demonstrates that WBG device implementation requires departure from silicon-centric design methodologies. Device parameters exhibit frequency dependence necessitating dynamic models. Thermal management must address concentrated power dissipation. EMC requires attention from earliest design stages. Physical layout becomes inseparable from circuit design.

The fundamental motivation transcending technical achievement lies in environmental benefits through improved energy efficiency. Power converters govern energy flow in virtually all electrical systems. Incremental efficiency improvements, when deployed globally, translate to gigawatt-scale generation

capacity reductions. Wide bandgap devices enabling 2–5% efficiency gains represent one of few remaining opportunities for substantial power electronics performance improvements.

Key Conclusions and Future Outlook

This chapter validated the achievement of all research objectives:

- **Device Characterization:** Embedded STM32-based platform enabling frequency-resolved measurement of C_{iss} , $R_{DS,on}$, and ΔV_{th} with precision comparable to commercial test equipment, revealing critical frequency-dependent behaviours absent from device datasheets
- **GaN Converter Topologies:** Systematic evaluation from single-phase buck through interleaved configurations, quantifying design challenges including sub-5 nH commutation loop requirements, 10–50 ns dead-time optimization, and the first-order impact of PCB layout on MHz-frequency performance
- **Power Density Enhancement:** Coreless PCB-embedded inductors demonstrating feasibility of core-free magnetic components at 1 MHz with superior thermal performance, linear current behaviour, and EMI compliance
- **DAB and Multilevel Topologies:** Average current mode control preventing transformer saturation across diverse load scenarios, with 3L-ANPC extension enabling 800 V bus operation using 650 V GaN devices
- **EMI Suppression:** Double half-bridge soft-switching topology eliminating high-frequency ringing while achieving ZVS operation, with experimental benchmarking confirming 99.13% peak efficiency and 62.5 W/cm³ volumetric power density
- **Future Directions:** DAB hardware prototype completion, advanced magnetic component optimization, model predictive and machine learning control strategies, and system-level integration for EV charging, renewable energy, and data center applications

Publication List

Journal Papers

- Vella, A.; Galioto, G.; Vitale, G.; Lullo, G.; Giaconia, G.C. GaN and SiC Device Characterization by a Dedicated Embedded Measurement System. *Electronics* 2023, 12, 1555. <https://doi.org/10.3390/electronics12071555>
- Galioto, G.; Vitale, G.; Lullo, G.; Calandra, E.; Chiarello, G.; Sciré, D.; Vella, A.; Giaconia, G.C. Coreless Inductor Design for MHz-Frequency GaN Converters. *IET Power Electronics*, 2026. Preprint, TechRxiv, DOI: 10.36227/techrxiv.172227485.50628341/v2
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- Vella, A., Galioto, G., Giaconia, G.C. (2023). Microcontroller Based Portable Measurement System for GaN and SiC Devices Characterization. In: Berta, R., De Gloria, A. (eds) *Applications in Electronics Pervading Industry, Environment and Society*. ApplePies 2022. *Lecture Notes in Electrical Engineering*, vol 1036. Springer, Cham. https://doi.org/10.1007/978-3-031-30333-3_5
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