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TECHNOLOGIES AND METRICS FOR METROLOGICAL CHARACTERISTICS IMPROVEMENT OF LOW-COST DEVICES FOR SMART GRIDS MEASUREMENTS

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ABSTRACT

In recent years, rapid changes have occurred in electric grids. This includes the significant integration of renewable energy sources into the grid, alongside the liberalization of the electricity market. Additionally, there has been a rise in the number of "prosumers" – users who transit from passive consumers to active producers, generating their own energy, primarily through domestic photovoltaic systems. Although mini and micro wind generators are less common, they also contribute to this trend. These transformations have not only altered the traditional concept of the grid, which previously involved a unidirectional power flow from generation sites to users, but have also transformed it from a passive into an active and intelligent network – known as a *smart grid*.

In smart grids, the measurement of voltage and current parameters, as well as the amount of energy exchanged between users and producers, takes on a fundamental role. For example, the load flow problem, that needs to know the active and reactive power in the different nodes of the network, for a correct application of dispatching, or the frequency and voltage regulation, key features to provide an efficient energy service. The increased complexity of the electricity grid, combined with the new needs related to remote control, communication and interconnection, has made it necessary to use distributed measurement systems, which require a greater number of instruments capable of carrying out different activities. For this reason, the possibility of using low-cost devices for measurements, and in particular for power quality measurements, has become increasingly important. The use of programmable devices also allows great flexibility in adapting to the required measures. One of the main aspects taken into account in the management of the network is "*power quality*", a term that includes the main characteristics of voltage and current, and that requires continuous and different measurement techniques. Among the various aspects related to power quality, the evaluation of the harmonic content of the voltage is one of those that attracts the greatest interest both from users, who are increasingly informed and attentive to the management and economic aspects of domestic utilities, that by energy producers and managers, in order to maximize profits.

The Ph.D. project involved the participation and financial support of the University of Palermo, the National Research Council (CNR) and the company STMicroelectronics. The goal of this thesis is to investigate the feasibility of the development of a measuring instrument, based on a low-cost microcontroller and AFE device, able to perform a harmonic analysis of the power system voltage respecting the requirements of the standard (to reach the highest accuracy class).

Specifically, the project started with standard review to establish the requirements from current legislation, for a device within the highest accuracy class. Different technological solutions and metrics have been developed and compared in order to ensure compliance with the standard while using low-level hardware, optimizing the software component. For the validation, different tests have been conducted using an existing microcontroller board, with typical specifications of a low-cost device.

This thesis is the conclusion of this project, in which this possibility was evaluated defining which specifications this device should have.

The thesis consists of five chapters: in the first one, an in-depth analysis of power quality measurements for smart grids is reported, with a focus on current standards (in particular the IEC 61000-4-7 and 61000-4-30). In the second chapter the studies concerning the techniques of harmonic analysis and the aspects related to the possibility of realizing a harmonics measurement instrument using a low-cost device, with all the consequent difficulties, are reported. The third chapter includes simulation tests to assess the feasibility of implementing the necessary metrics, in order to narrow the field to workable solutions and to be able to define some minimum specifications. The simulated metrics were then implemented on a real device, which was appropriately characterized, and tested under different conditions, described in chapter four. The last chapter contains the conclusions.

1. MEASUREMENTS IN SMART GRIDS

1.1 Smart grid

Electric grids have undergone rapid changes in the last decades, including the significant integration of non-programmable power generation sites from renewable sources into the grid and the liberalization of the electricity market [1, 2]. The number of so-called prosumers has also increased; they are users who, from passive, turn into active, generating energy themselves (mainly with domestic photovoltaic systems; mini and micro wind generators are less spread) and exchanging it with the network [3–5]. These transformations have not only reshaped the network concept, that until the first decade of the century was a unidirectional power flow line, from generation sites to users, but have also shifted it from being perceived as a passive system, as an active and intelligent network— a *smart grid*.

The term "smart grid" is used to describe an advanced and modern electric grid with digital technology, communication systems and automation to enhance the efficiency, reliability, and sustainability of electricity generation, distribution, and consumption [1]. It is a more interconnected grid, with bidirectional power flow and a strong presence of measure and communication systems. The term "smart" in this context refers to the novelty of intelligent features, spread into the grid. In particular, a smart grid is characterized by:

- Advanced communication and distributed metering: Smart grids use two-way communication systems that allow devices, such as smart meters and sensors, to communicate with each other and with the central control systems [6, 7]. This enables real-time monitoring and control of the grid and of the power flow. In fact, the existence of prosumers leads to the need to measure and exchange information not only on the energy used, but also on the energy produced, which is added to that already produced by large plants and therefore requires accurate management [8]. Moreover, the large variety of production plants and the strong interconnection of the grids require a dense network of sensors and smart meters, distributed all over the grid and not and not concentrated in a few important nodes of the grid.

- Automation and control: Using the enormous quantity of information taken from the distributed measurement systems, a smart grid uses automation to efficiently manage the flow of electricity [4]. Automation allows a quick identification and isolation of electric faults, rerouting of power to minimize disruptions, and optimal management of energy sources. Through real-time monitoring and automated responses, a smart grid can improve the reliability of the electrical grid. This is crucial in preventing and minimizing power outages. Thanks to this, smart grids are designed to be more resilient to various challenges, including natural disasters and cyber-attacks [9]. The system can quickly adapt and recover from disruptions, ensuring a more robust and secure electrical infrastructure.

- Integration of renewable energy sources: with the increasing integration of renewable sources power plant, a smart grid can dynamically adapt the power flow to the variations in renewable generation. It allows a better integration of intermittent energy sources, like solar and wind power [3, 10].

- Demand response: smart grids enable demand response programs, where consumers can adjust their electricity usage based on real-time pricing or signals (thanks to communication

system and real time control) from the grid [11]. This helps balance supply and demand, improving overall grid stability.

- Efficient resource management: the intelligence embedded in smart grids allows to optimized resource management [10]. This includes efficient use of electricity, better load balancing, and reduced energy losses during transmission and distribution.

- Data analytics: smart grids generate a significant amount of data from various sensors and devices. Advanced analytics can be applied to this data to gain information of grid performances, predict potential issues and optimize overall grid operations [12].

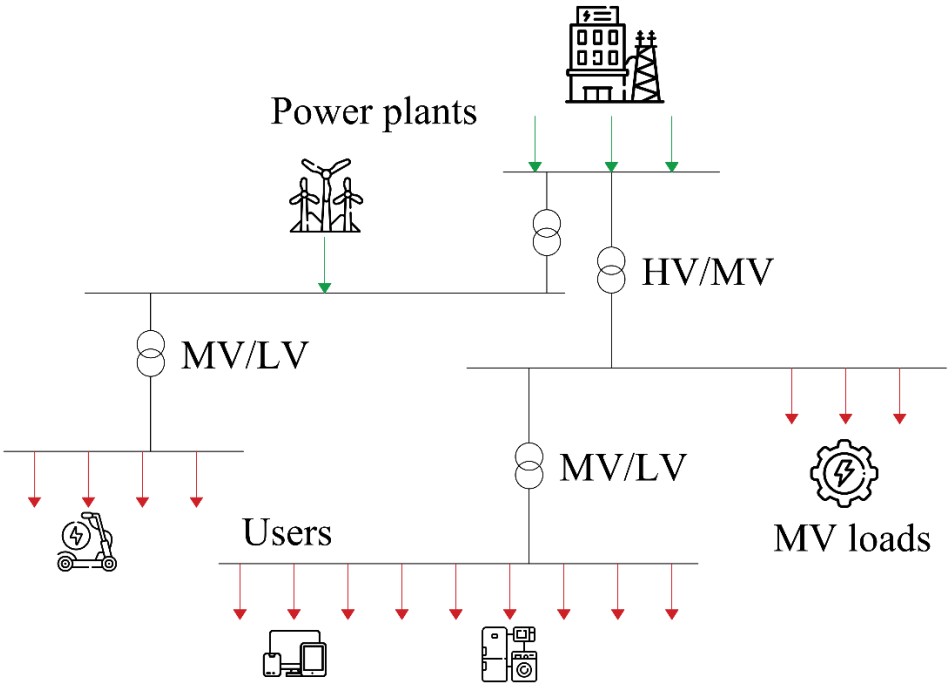

Fig. 1. 1 - Traditional electric grid (unidirectional power flow)

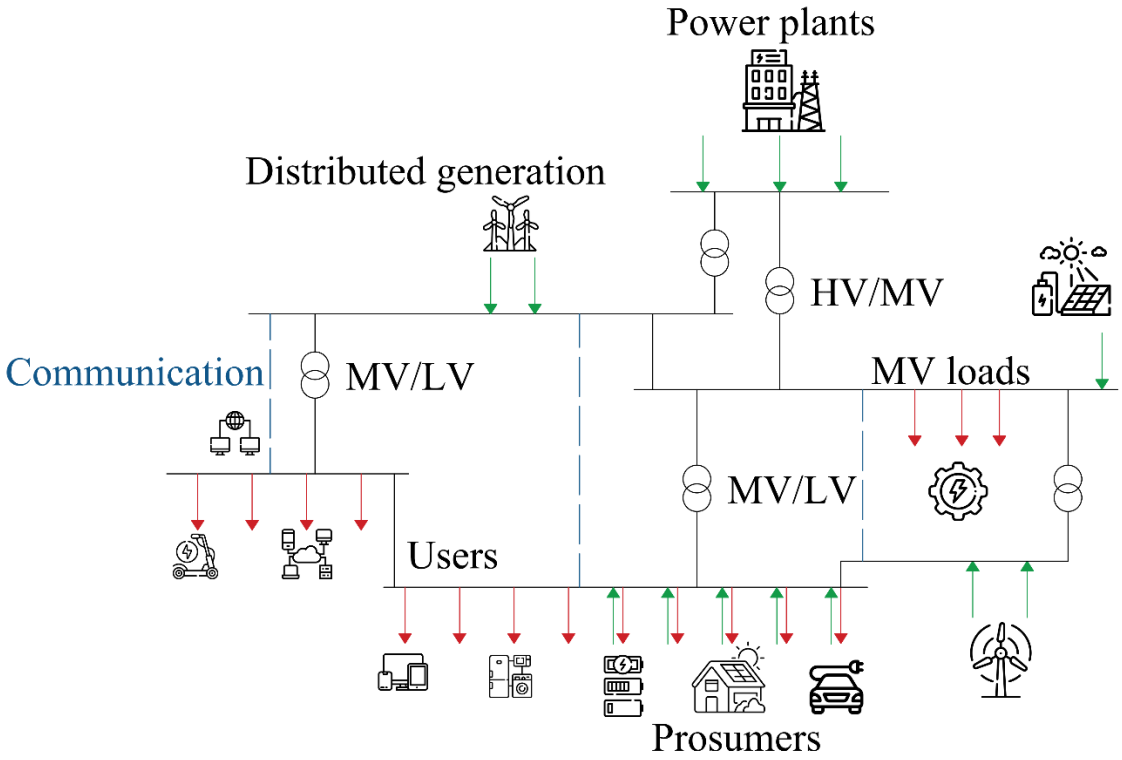

Fig. 1. 2 - Smart grid (bidirectional power flow and smart features)

In this context, as already mentioned, the measurements of the characteristic parameters of the electric quantities have assumed an increasing role. In fact, not only there has been an increase of the actors involved in the network, but also the simultaneous increase of sources that cause disturbances, of different magnitude, to the energy present in the network [8, 13] [14].

In smart grids, information and communication technologies are used to create integrated *data&electricity* networks, with new functionalities that guarantee the maintenance of high efficiency both in generation and in usage [15–17]. For example, an intelligent regulation of loads balances the production of electricity from non-controlled renewable sources with electricity consumption. This concept is named DSM – Demand side management and is just one of many aspects that differentiates smart grids from traditional networks [2].

To be defined "intelligent", the electricity grid must be characterised by the presence of technologies and devices that allow data exchange between all relevant users of the energy; only then, new and profitable demand management strategies can be implemented. In this scenario, energy measuring devices, called Smart Meters (SM) [18, 19], play a key role and must be able to:

- ensure two-way communication of data to and from the Network Manager;
- help consumers with information to monitor, manage and control their energy consumption (active user role);

In many cases, DSM techniques require smart meters to be also able to remotely disconnect loads with commands from the system operator. The expected final result should be a participatory network in which all actors in the energy market share both the responsibilities and the benefits achievable.

In order to ensure the maximum functionality of the measuring system, smart meters cannot be considered as a stand-alone system but must be inserted within a network, known in literature as AMI, Advanced Metering Infrastructure [20]. AMI is defined as a set of devices, protocols and rules for interconnection that will modify the current power grid, until it becomes able to determine its state by means of measurements made by smart meters distributed along the network and not only at the

customers/loads nodes [11, 21]. The information on the quantities of interest, collected by the SMs, are sent to the automatic network control devices. The latter shall process the required data previously, extrapolating the information that allows the implementation of the regulation to keep the network in the desired operating conditions while ensuring adequate reliability, continuity and efficiency. The accuracy of the metrological part and the synchronization between the instruments represent, therefore, important aspects that impact on the operation of the entire network and not only on the metering system.

Moreover, in order for this to happen, it is essential to ensure efficient communication between the devices located along the network and the operators. Communication can take place, if a suitable support network is set up, through wireless technologies, with the great advantage of being able to connect to the "network" from any point and at any time [22]. Nowadays, main negative aspects are the cost and the cyber security of the data. The electric grid is one of the potential communication media, thanks to the possibility of using energy transport cables, also for the exchange of information; through PLC technology (Power Line Communication) [15, 16] it is, in fact, possible to transmit data in a different frequency band than that used for energy transport, both in low voltage systems and in medium voltage systems. The advantages of this method are linked to two aspects: the first is the intrinsic security of the system, so that the data can only be accessed by the sending and receiving concentrator, a concept not to be underestimated in the "free access" data era available online. The second is the possibility of use the existing electrical infrastructure, which especially in the rural context or small islands, where ether systems are not widespread, presents both practical and economic aspects [10].

1.2 Power quality measurements for smart grids

In smart grids, the measurement of voltage and current parameters, as well as the amount of energy exchanged between users and producers, takes on a fundamental role [8, 11]. For example, the load flow problem, that needs to know the active and reactive power in the different nodes of the network, for a correct application of dispatching, or the frequency and voltage regulation, key features to provide an efficient energy service. The increased complexity of the electricity grid, combined with the new needs related to remote control, communication and interconnection, has made it necessary to use distributed measurement systems, which require a greater number of instruments capable of carrying out different activities [18]. For what concern the metrological aspects, energy quality is measured not only in terms of interruption (total or partial), but also by quality of the electric "quantities"; in fact, to ensure all the reported features of the smart grid system, it is necessary to start from the measurement and monitoring of the most important parameters of voltage and current, other than the consumption of power [23]. Those parameters represent the core of the Power Quality (PQ) [24–26] theme and the related standards.

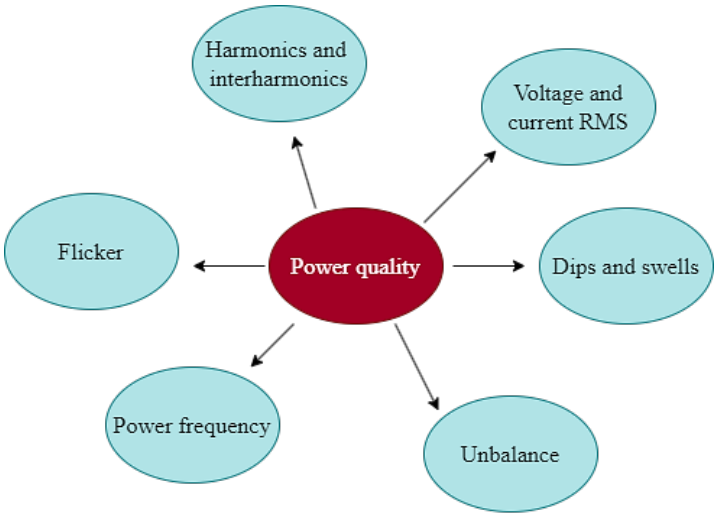

Fig. 1. 3 - Power quality quantities

Both electric utility providers and consumers are becoming more apprehensive about the quality of electric power. There are many primary factors contributing to the increasing concern:

- Advanced load equipment in smart grids, incorporating microprocessor-based controls and power electronic devices, are more sensitivity to variations in voltage and current parameters compared to older equipment.
- The increasing focus on overall power system efficiency has led to the continued proliferation of devices like high-efficiency control systems, adjustable-speed motor drives and shunt capacitors for power factor correction, aimed at reducing losses. On the other hand, this trend is elevating harmonic levels on power systems, prompting widespread concern regarding its potential future impact on system capabilities.
- Users are increasingly informed of power quality issues. Utility customers are becoming more knowledgeable about disruptions, voltage sags, and switching transients, thereby urging utilities to enhance the quality of power delivered [27].

- The interconnected nature of many components within networks has intensified. Integrated processes mean that the failure of a single component can have significantly more significant consequences.

The underlying theme across all these reasons for heightened concern about electric power quality is the ongoing drive for increased productivity among all utility customers.

The term commonly used to describe the subject of these evaluations is "*power quality*," although in most cases, it specifically addresses the quality of the voltage. From a physic point of view, power refers to the rate of energy delivery, which is proportional to the product of voltage and current. Defining the *quality* of this quantity would be challenging. The power supply system can only regulate the quality of the voltage, because it lacks control over the currents drawn by specific loads. Therefore, standards in the power quality domain focus on maintaining the supply voltage within certain limits.

Of course a close relationship exists between voltage and current in any practical power system. Despite generators producing near-perfect sine-wave voltage, the current flowing through the system's impedance can induce various disturbances to the voltage [8, 28]. This phenomenon is amplified by the fact that, in electrical power plants, both in industry and in the tertiary sector, non-linear electrical loads are increasingly common. Typical examples of distorting loads are those related to power electronics: diode rectifiers, inverters and UPS [28]. And even in the domestic environment there is a growing presence of distorting utilities: LED lights, electronic devices, etc.

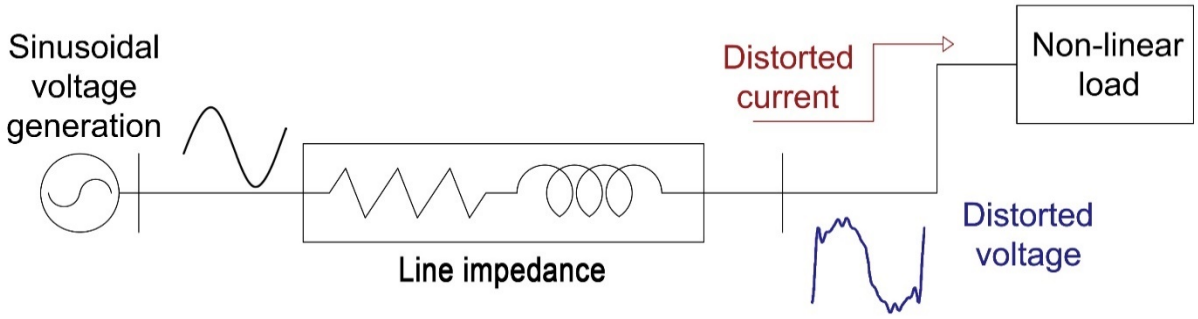

Fig. 1. 4 - Non-linear load and line impedance effects on sinusoidal voltage

Harmonic disturbances primarily arise from equipment with non-linear voltage/current characteristics. Currently, a significant portion of industrial, commercial, and residential loads are non-linear, resulting in distortion levels on the low voltage power supply network, significant enough to impact the quality of energy delivered to nearby devices [29, 30].

On one hand, the number of devices generating harmonics on the power supply continues to rise. Conversely, there is a growing number of devices, even among consumers, sensitive to any spurious harmonics that may be present on the power supply. Computers, communication equipment, and other electronic systems are all susceptible to malfunctions or reduced efficiency due to harmonic effects; in electric motors, current harmonics can lead to losses in windings and the core, potentially causing core and winding overheating, torque fluctuations, and overall motor inefficiency.

Voltage and current harmonics can also cause unjustified interference in fault protection circuits. Spurious harmonics, in general, can disrupt electronic instruments and relay transformers, and may even result in improper disconnections by protective devices such as switches [31].

Due to the increasing issue of harmonic pollution in power systems and the necessity to guarantee appropriate PQ standards, there has been a growing interest among distribution network operators, electricity users, producers and prosumers in integrating harmonic distortion measurement into smart

grids and related measuring systems [31–34]. This integration allows a widespread monitoring of the network without increment the costs, especially if low-cost solutions are used matched with existent measure devices. Regarding the implementation of metrics, numerous studies in recent years have explored various approaches to PQ monitoring and harmonic evaluation [13, 24, 26, 35, 36]. The aim is to have reliable solutions capable of meeting the standards requirements for instrumentation in power systems without increasing the costs and also the management complexity of the system itself [37].

Measurement methods for harmonic content evaluation are based on digital signal processing algorithms and can be grouped into two major classes:

- Data decomposition methods: DFT, FFT, CZT, based on Fourier analysis;
- Parametric methods: MUSIC (Multiple Signal Classification) based on self-regressive methodology.

Between these two main categories, the suitable measurement methods are determined. However, the selection of instruments depends on the type of measurement required, centralized or distributed.

The subsequent step involves defining the uncertainty introduced by the instruments during the measurement process. If this value falls within acceptable parameters for the specific measurement, the instruments can be installed, and measurement data can then be collected.

For this Project it was decided to focus on techniques based on the Fourier transform, since the reference standard [38] (as seen below) indicates the DFT algorithm (Discrete Fourier Transform) and its derivatives, as a choice to be preferred for harmonic analysis.

1.3 Analysis of current standards

The first part of this Ph.D. project was devoted to an in-depth study of the legislation on PQ measures [39]. In particular, IEEE 1459 “Standard Definitions for the Measurement of Electric Power Quantities Under Sinusoidal, Nonsinusoidal, Balanced, or Unbalanced Conditions” [40], IEC 61000-4-30 “Electromagnetic compatibility (EMC) Part 4-30: Testing and measurement techniques - Power quality measurement methods” [41] and IEC 61000-4-7 “Electromagnetic compatibility (EMC) Part 4-7: Testing and measurement techniques - General guide on harmonics and interharmonics measurements and instrumentation, for power supply systems and equipment connected thereto” [38] were first analysed. These have been identified as the main references for the realization of a device for the measurement, specifically, of harmonic distortion in the grids [42].

For a more overall and complete point of view, other standards regarding grid specifications have been studied. In particular, for the Italian network, the CEI 0-21 – “Reference technical rules for the connection of active and passive users to the LV electrical Utilities” [43] and IEC 0-16 – “Reference technical rules for the connection of active and passive consumers to the HV and MV electrical networks of distribution Company” [44] were analysed; for the European situation, the standards VDE-AR-N 4105 “Generators connected to the low-voltage distribution network – Technical requirements for the connection to and parallel operation with low-voltage distribution networks” [45] and VDE-AR-N 4110 “Technical requirements for the connection and operation of customer installations to the medium voltage network (TCR medium voltage)”[46] were also analysed.

The regulatory overview was essential to contextualize the studies and tests conducted, in order to maintain consistency between the specifications to be developed and the real situations in which any measuring device would work.

It is essential to underline that scientific progress and the regulatory situation must necessarily go hand in hand, so as not to fall into the problem of having in one case techniques that are perfect on paper but not practically usable on the other hand, the not-possibility technologically progress because the regulatory framework does not take account of the latest developments [42, 47, 48].

In this thesis, not all the details regarding the standard will be reported, although these have served as a preliminary step for the development of the work. Instead, the focus will be on legislation concerning the main object of the work, namely power quality measures, the IEC 61000-4-30 and IEC 61000-4-7 standards.

1.3.1 Technical Standard for Power Quality - IEC 61000-4-30

The standard IEC 61000-4-30 “Electromagnetic compatibility (EMC) Part 4-30: Testing and measurement techniques - Power quality measurement methods”[41] is the main reference for PQ measurements; This Standard defines “the methods of in situ measurement and interpretation of the various parameters that define the quality of the electrical power in supply systems in alternative current with a fundamental frequency of 50 Hz or 60 Hz. The parameters that define the quality of the electrical power considered are limited to those of phenomena conducted in power systems such as frequency, amplitude voltage, flicker, holes and voltage variations, interruptions and transients, harmonics and interharmonics, rapid voltage changes, signalling on power lines, current measurements, etc “.

Annex A is provided as an informative complement to the normative part of this standard and regards “Power quality measurements – Issues and guidelines”. It reports for example installation precautions, informations about transducers and transient voltages and currents. Annex B includes contractual applications of power quality measurements and provides guidance on the measurement of PQ for contractual purposes. Emissions in the frequency range from 2 kHz to 150 kHz are considered in Annex C and over/under deviations are considered in Annex D.

In Annex E, specifications about Class B instrumentation are reported.

The standard also provides significant technical changes with respect to the previous edition:

- The measurement method for current, previously informative, is now normative with some changes;
- The measurement method for RVC (rapid voltage change) has been added;
- The measurement method for conducted emissions in the 2 kHz to 150 kHz range has been added in informative Annex C;
- Underdeviation and overdeviation parameters are moved to informative Annex D;

Class A and Class S measurement methods are defined and clarified, while Class B is moved to informative Annex E and considered for future removal; measurement methods are described for each relevant parameter in terms that give “reliable and repeatable results, regardless of the method’s implementation”.

1.3.1.1 Accuracy classes – A-Class and S-Class

One of the main aspects of the standard is the definition of three classes of measurement and, for each class, measurement methods and appropriate performance requirements are included. The definition, directly reported in the standard, is:

- Class A

This class is used where precise measurements are necessary, for example, for contractual applications that may require resolving disputes, verifying compliance with standards, etc. Any measurements of a parameter carried out with two different instruments complying with the requirements of Class A, when measuring the same signals, will produce matching results within the specified uncertainty for that parameter.

- Class S

This class is used for statistical applications such as surveys or power quality assessment, possibly with a limited subset of parameters. Although it uses equivalent intervals of measurement as Class A, the Class S processing requirements are much lower. Some surveys may assess power quality parameters of several measurement sites on a network; other surveys assess power quality parameters at a single site over a period of time, or at locations within a building or even within a single large piece of equipment.

- Class B

Class B methods shall not be employed for new instruments. Class B is moved to Annex E on the basis that all new instrument designs will comply with either Class A or Class S. Class B may be relevant for legacy instruments that are still in use. Class B may be removed in the next edition of this standard.

The standard considers that the electrical quantity to be measured may be either directly accessible, as is generally the case in low-voltage systems, or accessible via measurement transducers. An "instrument" may include the whole measurement chain (Figure). In this standard, the normative part does not consider any possible measurement transducers external to the instrument and their associated uncertainty, but Annex A gives guidance.

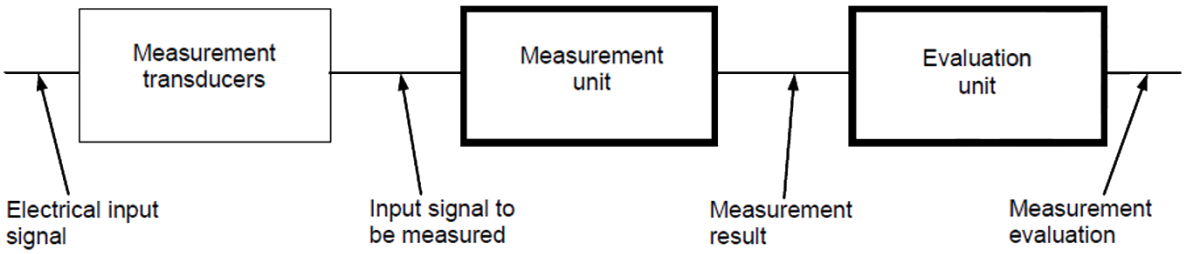

Fig. 1. 5 - Measurement chain scheme according to Standard IEC 61000-4-30

Regarding the quantities to be measured for power quality evaluations, the standard considers:

- Power frequency
- Magnitude of the supply voltage
- Flicker
- Supply dips and swells
- Voltage interruptions
- Voltage unbalance
- Voltage harmonics
- Voltage interharmonics
- Mains signalling voltage on the supply voltage
- Rapid voltage change
- Current parameters (magnitude, harmonics, unbalance)
- Conducted emission in the 2 kHz to 150 kHz range

For every quantity it declares measurement method, uncertainty and measuring range, measurement evaluation and, when required, aggregation of data.

About data aggregation, the standard reports the aggregation over time[1] intervals and related requirements.

[1] Standard imposes, for Class A instruments, to collect 10 or 12 cycles time intervals; it imposes also to aggregate the data in 3 additional intervals: 150/180 cycles, 10-min and 2-hour (only for flicker).

1.3.1.2 Harmonic measurements

For voltage harmonic measurement assessment, the standard first declare that main reference is the standard IEC 61000-4-7. For what concern measurement methods, the standard defines that, for class A instruments, "IEC 61000-4-7 shall be used to determine a 10/12-cycles[2] *gapless* harmonic subgroup measurement; […] Measurements shall be made at least up to the *50th order*".

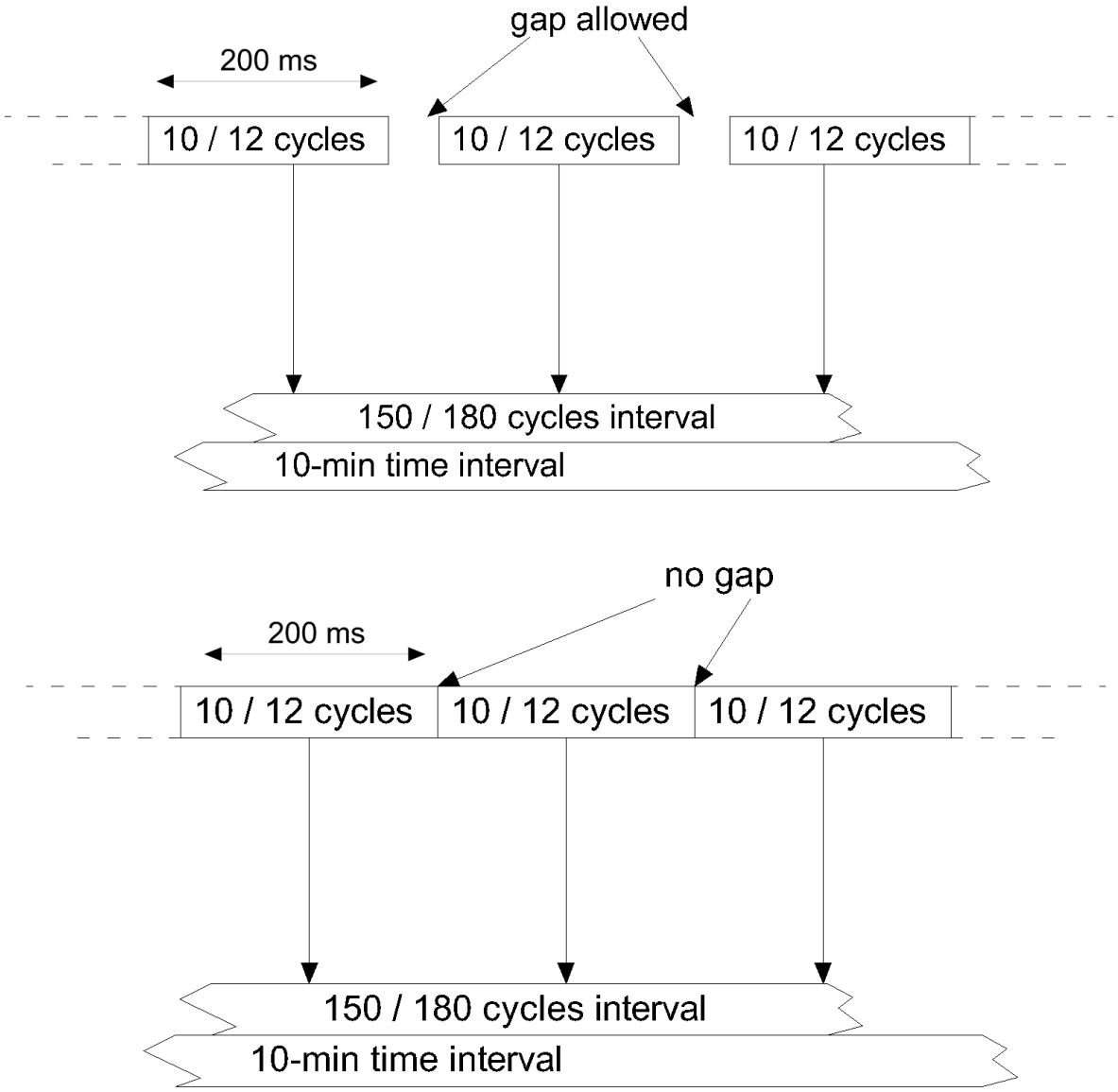

Fig. 1. 6 - On top: Gap sampling. Bottom: Gapless sampling

In this sentence, main aspects of a class A instrument are reported, i.e. the gapless sampling and elaboration of data with 200 ms time windows[2] and the requirement of accuracy to be respected up to 50th order harmonic component.

For measurement accuracy, the standard refers to the standard IEC 61000-4-7.

[2] The standard defines "cycle" the entire period of the signal; it is equal to 10 for the electrical system with power frequency equal to 50 Hz and 12 for the ones with power frequency equal to 60 Hz. In this way, the time length of the observation window is 200 ms for both cases. The definition is the same for IEC 61000-4-7.

1.3.2 Technical Standard for harmonic analysis - IEC 61000-4-7

The standard IEC 61000-4-7 "Electromagnetic compatibility (EMC) – Part 4-7: Testing and measurement techniques – General guide on harmonics and interharmonics measurements and instrumentation, for power supply systems and equipment connected thereto"[38] is the international reference standard for harmonic assessment.

This section of IEC 61000 relates instruments designed for measuring spectral components within the frequency range up to 9 kHz. These components are overlaid on the fundamental frequencies of power supply systems at 50 Hz and 60 Hz. For practical purposes, the standard categorizes between harmonics, interharmonics, and other components beyond the harmonic frequency range, extending up to 9 kHz.

This standard outlines the specifications for measurement instruments used to test specific equipment items in compliance with emission limits. Additionally, it covers instrumentation for measuring harmonic currents and voltages within operational supply systems.

In the standard, definitions related to frequency analysis are reported; it is possible to find definition of a signal transformed with Fourier series development, Total Harmonic Distortion (THD), etc.

In chapter 4 "General concepts and common requirements for all types of instrumentation", the standard first characterize the measurement chain, whose scheme is reproduced in Fig. 1. 7

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The standard declares that DFT is not mandatory if equivalent algorithm are used; FFT is mainly recommended if DFT is not used.

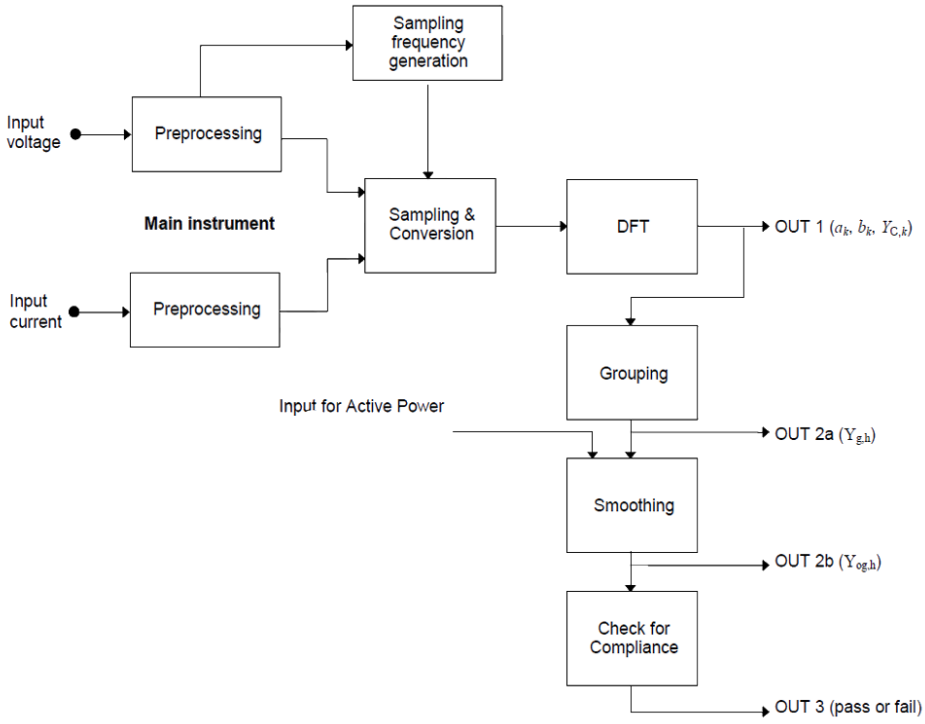

Fig. 1. 7 - Harmonic analysis scheme according to Standard IEC 61000-4-7

It is important to notice that the scheme also considers current and power measurement, that are not an object of this study.

1.3.2.1 Synchronization of the sampling window

As mentioned in previous chapters, the standard imposes that "The [observation] window width shall be 10 (50 Hz systems) or 12 (60 Hz systems) fundamental periods (T_w = [10 or 12] × T1 ≈ 200ms) with rectangular weighting, synchronized to the fundamental frequency of the power system. Hanning weighting is allowed only in the case of loss of synchronisation". Moreover, the window must be synchronized with each set of 10 or 12 cycles, corresponding to the power system frequency of 50 Hz or 60 Hz, with a maximum allowable error $e_{\%}$ of ±0.03% of the entire duration of the set of cycles.

The synchronization error $e_{\%}$ can be defined, starting from the maximum error E on the observation window. In detail, for a given observation window, the number of samples N to be acquired can be obtained by multiplying the desired observation window by the sampling frequency. If the obtained value of N is not integer, the nearest integer value is assumed, leading to a maximum error E of half a sample, i.e. $0.5 \cdot Ts$ in terms of time interval. In this way, the synchronization error can be expressed as follows:

$$e_{\%} = 100 \cdot \frac{E}{T_w} \qquad [1.\ 1]$$

where:
E = 0,5·Ts ;
Ts = Sampling period [s] = 1/ f_S;
f_S = sampling frequency [Hz];
T_w = observation window [s] = 10 x T_1[3]≈ 200 ms (in the case of $f_1 = 50\ Hz$);
T_1 = fundamental period [s] = $1/f_1$;
f_1 = fundamental frequency [Hz];

More considerations about synchronization error are carried out in next chapter.

1.3.2.2 Harmonics measurement accuracy

For instrumentation measuring harmonic components classification, two classes of accuracy are suggested; the A-Class and the S-Class mentioned in IEC 6100-4-30 refer to Class I and Class II of the standard IEC 6100-4-7 respectively. In Table 1. 1 the maximum allowable errors for voltage, current and power are reported. The measurement refers to single-frequency and steady-state signals, in the operating frequency range, applied to the instrument under rated operating conditions to be indicated by the manufacturer (temperature range, humidity range, instrument supply voltage, etc.).

The error e is defined as the difference between the measured value of the single harmonic component and the reference value.

[3] The symbol " ≈ " is used instead of " = " because, in real operating condition, the frequency can be different than the nominal value.

Table 1. 1 - Accuracy requirement for voltage, current and power harmonic analysis according to Standard IEC 61000-4-7

Class	Measurement	Conditions	Maximum error
I	Voltage	Um ≥ 1% Unom	±5% Um
		Um < 1% Unom	±0,05% Unom
	Current	Im ≥ 3% Inom	±5% Im
		Im < 3% Inom	±0,15% Inom
	Power	Pm ≥ 150 W	±1% Pm
		Pm < 150 W	±1,5 W
II	Voltage	Um ≥ 3% Unom	±5% Um
		Um < 3% Unom	±0,15% Unom
	Current	Im ≥ 10 % Inom	±5% Im
		Im < 10 % Inom	±0,5% Inom
Inom: Nominal current range of the measurement instrument; Unom: Nominal voltage range of the measurement instrument; Um, Im and Pm: Measured values.			

Class I instruments are advised for situations requiring precise measurements, such as verifying compliance with standards or resolving disputes. They are particularly recommended for emission measurements.

Class II instruments, on the other hand, are suitable for general surveys but can also be used for emission measurements if the values indicate that, even with the increased uncertainty, the limits are not exceeded. In practice, this implies that the measured values of harmonics should be less than 90% of the allowed limits.

1.3.2.3 Grouping and smoothing

According to IEC 6100-4-7 standard, the FFT (or DFT) result must be processed to perform a grouping operation firstly and then smoothing using a first order filter.

The single harmonic component value Y_C is grouped to be "the sum of squared intermediate components between two adjacent harmonics", defined in the standard. The equation that describes this process is:

$$Y_{grouped,h} = \sqrt{\frac{1}{2}Y^2_{C,(N\cdot h)-\frac{N}{2}} + \frac{1}{2}Y^2_{C,(N\cdot h)+\frac{N}{2}} + \sum_{k=-\frac{N}{2}+1}^{\frac{N}{2}-1} Y^2_{C,(N\cdot h)+k}}$$

[1. 2]

$Y_{grouped,h}$ is the RMS value of the harmonic group, N is the number of fundamental periods sampled in the observation window, $Y_{C,(N\cdot h)+k}$ is the RMS value of the spectral component of a given bin, output of the DFT, and $(N \cdot h) + k$ is the order of the spectral components.

From this definition, we can observe that sampling a higher number of periods produce a higher $Y_{grouped,h}$ value and a more constrict relation between distant spectral component (the order depends on N).

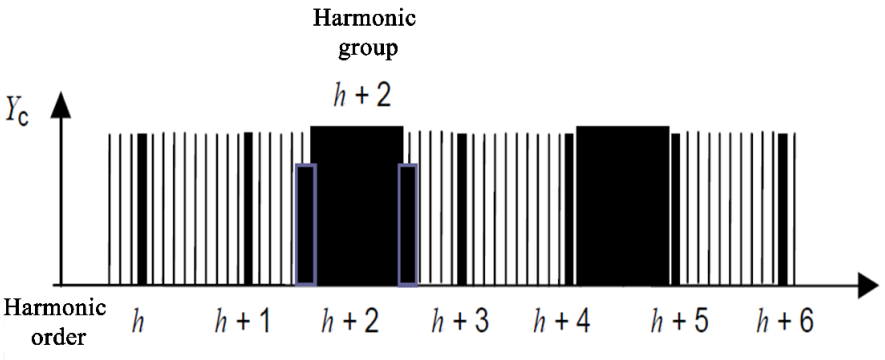

Fig. 1. 8 - Grouping scheme - Standard IEC 61000-4-7

For the output of the grouping block the standard imposes to use a smooth digital filter, equivalent of a first order low-pass filter. Filter time constant is equal to 1.5 s. The input of the filter is the grouped value $Y_{grouped,h}$. Coefficients α and β of the filter are reported in Table 1. 2 and depend on the fundamental frequency of the signal f_1 and the number of fundamental periods in the observation window *N*. For this application, $N = 10$ and $f_1 = 50\ Hz$ is set, so the values of the coefficients are $\alpha = 8.012$ and $\beta = 7.012$.

The scheme of the filter is reported in

Fig. 1. 9.

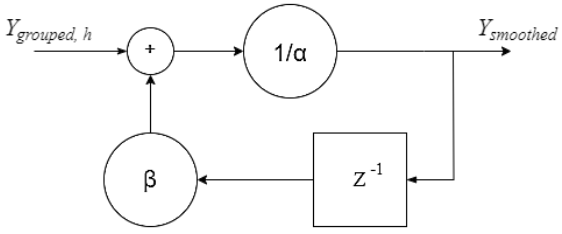

Fig. 1. 9 - Smooth filter scheme - Standard IEC 61000-4-7

The filter has been realized using the transfer function *G*:

$$G = \frac{Y_{smoothed,h}}{Y_{grouped,h}} = \frac{1}{\alpha - \beta z^{-1}} \quad [1.\ 3]$$

Table 1. 2 - Smooth filter coefficient - Standard IEC 61000-4-7

Power frequency [Hz]	Cycles N in observation window	Sampling rate (of the digital low-pass filter) [ms]	α	β
50	10	>> 1/200	8,012	7,012
60	12	>> 1/200	8,12	7,012
50	16	>> 1/320	5,206	4,206
60	18	>> 1/267	6,14	5,14

2. HARMONIC ANALYSIS WITH LOW-COST COMMERCIAL DEVICES FOR SMART GRID APPLICATIONS

2.1 Harmonic analysis of analog signals

A sinusoidal voltage is generated by an ideal AC generator, equipped with finely distributed stator and field windings, and functioning in an idealized uniform magnetic field—a condition that doesn't occur in practical applications. In real AC machines, both the winding distribution and magnetic field inherently lack uniformity. While the distortion of the generator voltage remains quite small (typically around 1–1.5%), this distortion increases notably in transformers and when nonlinear loads are involved, such as electronic equipment. Furthermore, distortion in the waveform arises due to network impedance between the power source and nonlinear load, which, in turn, distorts the voltage waveform at the point where they are connected, as described in previous chapter. Harmonics are generated by a range of components within the electrical system, including generators, transformers, nonlinear loads, and switching devices [49]. These harmonics represent multiples of the fundamental frequency. It's important to note that interharmonics can also be observed in distribution systems. Harmonic orders may vary from 2 to 100 even more yet harmonic studies usually analyse first 25 or 50 orders, due to their significant magnitudes compared to higher order harmonics [37, 49].

The mathematical study of the components of a periodic signal is called harmonic analysis. This analysis is commonly applied in various fields, including mathematics, physics, engineering, and signal processing. The analysis of the signal is based on the studies of the French mathematician Jean Baptiste Joseph Fourier, who stated that every periodic function could be decomposed into a series of sinusoidal components, linearly combined, characterized by different amplitudes and frequencies. This representation is called the Fourier series [50].

The Fourier series decomposition allows to express a function in the time domain $f(t)$ (with period T) as composition of sinusoidal components, with a given amplitude and a frequency that is an integer multiple of the frequency of the signal; the expression of the Fourier series is:

$$f(t) = F_0 + \sum_{h=1}^{\infty} f(t)_h = \frac{a_0}{2} + \sum_{h=1}^{\infty} [a_h \cos(h\omega t) + b_h \sin(h\omega t)] \quad [2.\ 1]$$

$F_0 = \frac{a_0}{2}$ is the mean value and is 0 for alternate functions; $F_0 = \frac{1}{T}\int_0^T f(t)\ d(t)$

$a_h = \frac{1}{\pi}\int_0^{2\pi} f(t)\cos(h\omega t)\ \ d(\omega t)$

$b_h = \frac{1}{\pi}\int_0^{2\pi} f(t)\sin\ (h\omega t)\ d(\omega t)$

Starting from *[2. 1]* is it possible to obtain relevant simplifications if the signal presents particular characteristics of symmetry. For example, for an odd signal $\big(f(-t) = -f(t)\big)$, the value of a_h is always zero, for an even signal $\big(f(-t) = f(t)\big)$ the value of b_h is always zero.

Naturally in practical applications it is not possible to sum infinite components and it is necessary to stop the sum at a defined order. This implies an approximation of the original signal, that is less relevant the more the number of harmonic components is. In FIGURA the example of the Fourier decomposition of a square wave (that only has odd harmonics) until the 7th order and its reconstruction is reported.

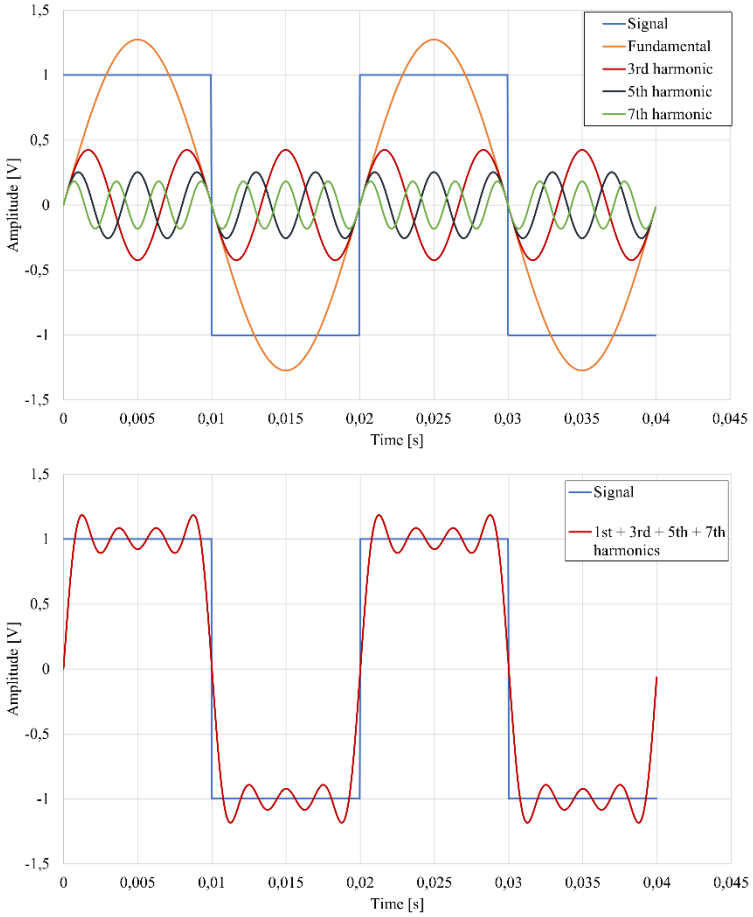

Fig. 2. 1 - Harmonic decomposition of a square signal

If the signal is not periodic, a transformation is necessary. The Fourier transform F of a signal allows to decompose a non-periodic function in a infinite linear combination of basic functions $e^{j\omega t}$:

$$F(\omega) = \int_{-\infty}^{\infty} f(t) e^{-j\omega t} dt$$

[2. 2]

Function F is called "integral Fourier function" and develops a non-periodic function in its components in the frequency domain. The inverse process allows to recreate a signal in the time domain starting from its component in the frequency domain:

$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} e^{j\omega t} F(\omega)\, d\omega$$

[2. 3]

Some examples of the Fourier transform application of non-periodic signals are reported below.

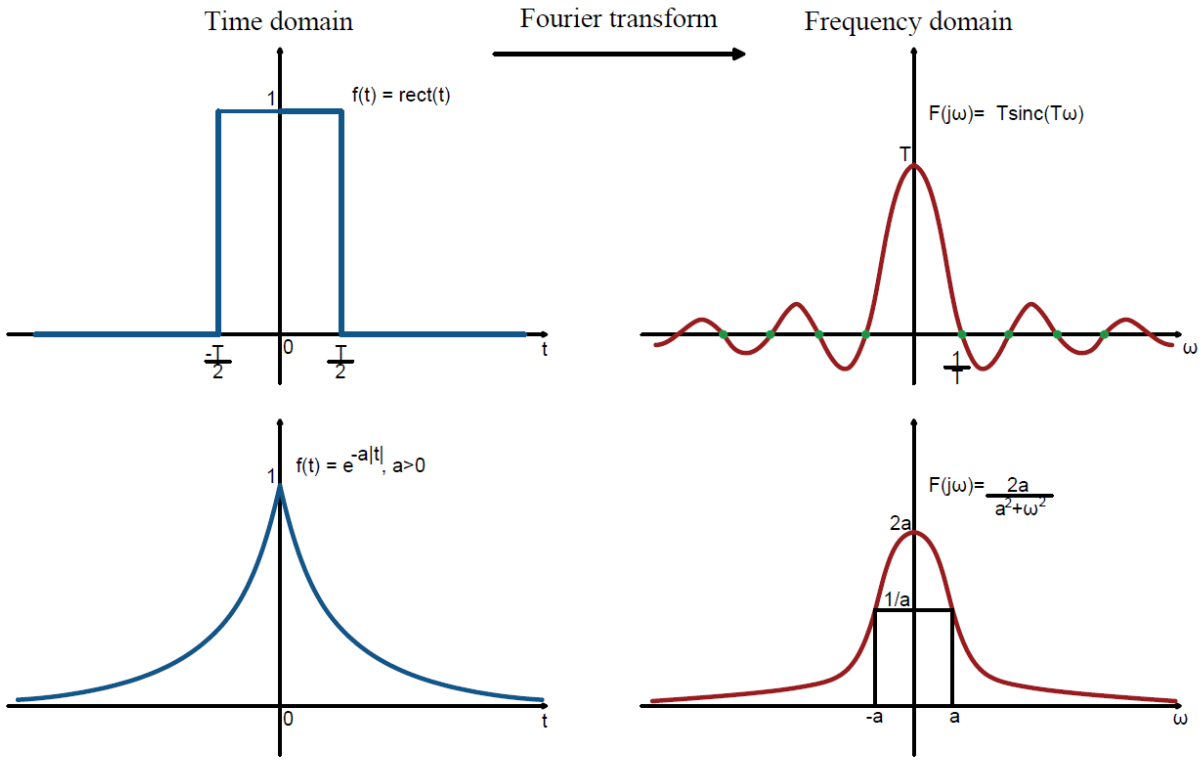

Fig. 2. 2 - Fourier transform application of non-periodic signals

A real signal is called analog and it is continuous in both time and value. For its elaboration using electronic system is necessary to convert (discretize) the analogue signal into a digital signal, that is a discrete-time signal. This conversion is done by the ADC – analog to digital converter and is made of different actions. It is important to underline that the discretization of the signal concerns both the amplitude and the time.

The first step is the sampling and consist of a conversion a continuous signal into a sequence of points at regular time intervals. The distance between two consecutive points is the sampling period T_s; the lower is T_s and the closest are the points, making signal reconstruction more accurate.

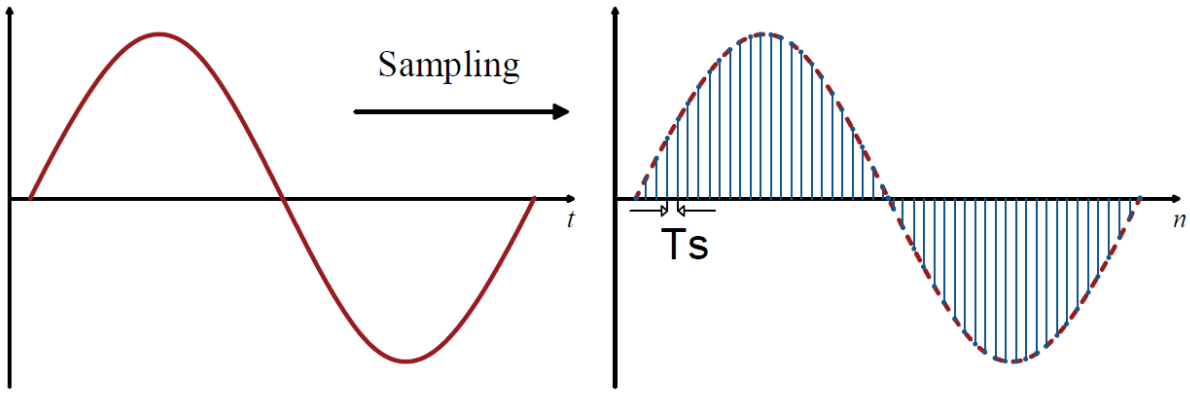

Fig. 2. 3 - Sampling process

The value of the samples is then obtained by the process of quantization and depends on the number of bits B of the digital converter. In each interval of durationT_s, the converter approximates the assumed voltage level of the analog signal to the nearest of the output levels, obtained by dividing the full-scale range R of the device into regular intervals of amplitude $Q = \frac{R}{2^B}$ (the quantization interval). It is therefore evident that, with the same range, a converter that use of a greater number of bits will have available smaller quantization intervals, being able to discriminate with more accuracy the amplitude values of two consecutive samples, as visible in

Fig. 2. 4. The difference between the original and digital signals is called quantisation error. The quantised signal is then coded to obtain the numeric value of the set of samples.

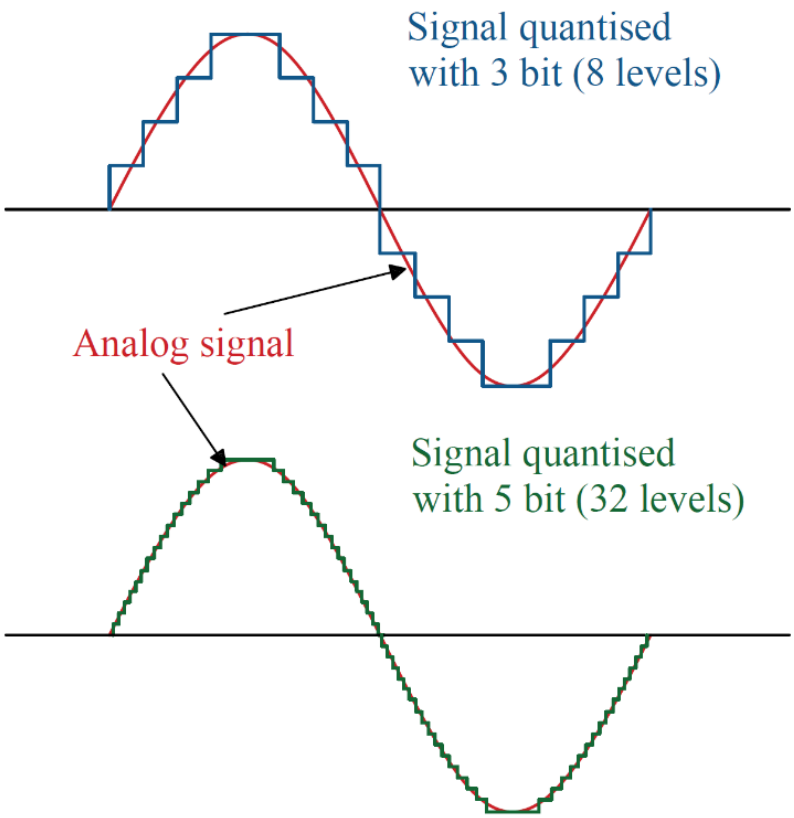

Fig. 2. 4 - Signal quantisation with different number of bit

Once the representative samples of the signal have been obtained, it is passed from having a signal in the time domain, making possible to perform a harmonic analysis using the Fourier transform, to a discrete signal. It is therefore necessary to resort to other techniques, or rather algorithm, that allow to carry out the desired analyses on the digital signal.

2.1.1 Discrete Fourier Transform

The Discrete Fourier Transform (DFT), commonly known in the literature by the acronym DFT (Digital Fourier Transform) [51] responds to the need to perform the Fourier transform of a discrete periodic signal. Simple results are obtained by sampling in frequency at regular intervals. The DFT algorithm converts a finite number of samples (of a signal) having the same time distance into a set of coefficients of a finite linear combination of complex sinusoids, ordered as the frequency increases, that are function of the same input samples. It can therefore be said that the sampled signal is transformed from its own source domain, the time, to the frequency domain.

Being the function $x(t)$ now transformed into a set of N samples $x(n)$, the DFT therefore consists of a numerical algorithm that discretizes the Fourier Transform, whose expression is reported in *[2. 3]*, in the form:

$$X(k) = \sum_{n=0}^{N-1} x(n) \cdot e^{-j\left(\frac{2\pi}{N}\right)\cdot k\cdot n},$$

[2. 4]

with $k = 0,1,2, \dots N-1$

where k is the index of output values, n is the index of input values.

The algorithm thus described requires the execution of N sums and N multiplications, that produce a computational cost equal to N^2. This is a quite large amount of operation, if it is considered that the set of points have no limitations and depend on the sampling frequency and the frequency of the signal.

2.1.2 Fast Fourier Transform

The possibility to carry out the DFT was a milestone in the history of the study of signals, at a time when operations had to be carried out by hand. Main limitation stated in the computational cost, so every possibility that allowed to reduce the amount of operations was investigated. Most techniques investigated to improve the efficiency of the DFT exploit its symmetry and periodicity properties; with appropriate precautions, a variant of the DFT was proposed by J. Cooley or J. Turkey [52], that allowed to lower the computational cost from N^2 to $Nlog_2\ (N)$ [50, 53]. This algorithm was named Fast Fourier Transform (FFT). The fundamental principle on which all these algorithms are based is the decomposition of the calculation of the DFT in a sequence of DFT of size gradually smaller. To optimize the FFT calculation, main aspect is the need of a number of input points that is a power of 2 [54, 55]. A comparison of the amount of operations of DFT and FFT, for the same number of samples, is reported in Table 2. 1 and showed in Fig. 2. 5.

Table 2. 1 - Computational cost comparison of DFT and FFT

Number of points N	Computational cost for DFT (N*N)	Computational cost for FFT (N*log(N)
4	16	2
8	64	7
16	256	19
32	1024	48
64	4096	116
128	16384	270
256	65536	617
512	262144	1387
1024	1048576	3083
2048	4194304	6782
4096	16777216	14796

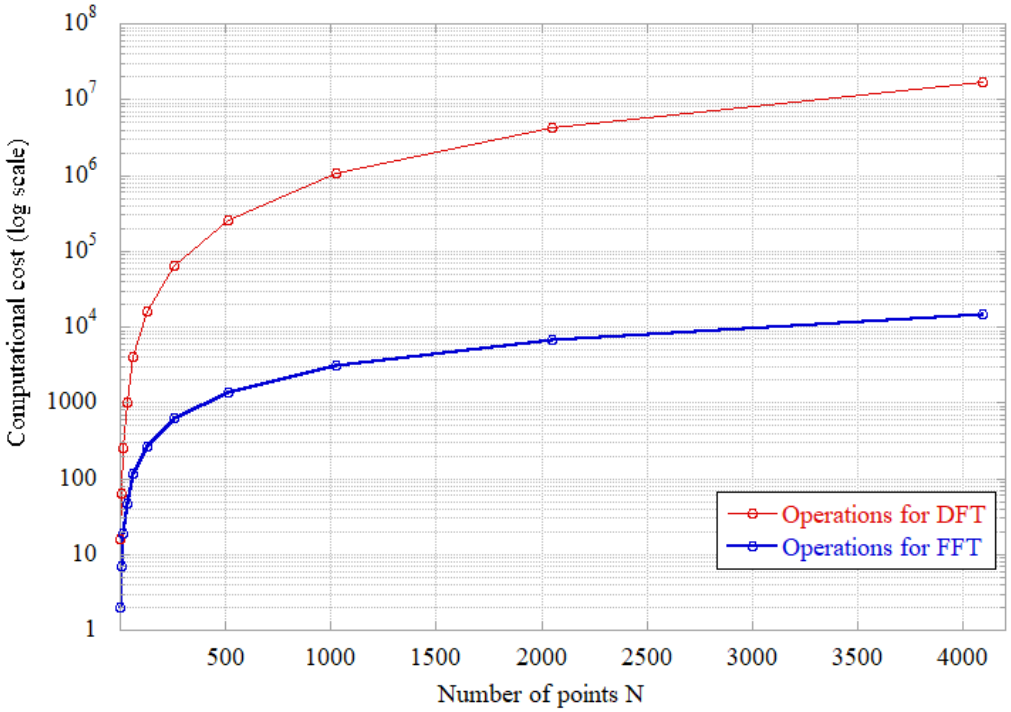

Fig. 2. 5 - Computational cost comparison of DFT and FFT in log10 scale

Comparing the number of operations reported in Table 2. 1 is clear that, for a device with discrete hardware, the main solution to carry on a harmonic analysis is the FFT.

For what concern the need of a number of points that is power of 2, this implies some adjustments that will be deepened successively.

2.2 Problems related to sampling

When an analog signal $f(t)$ is sampled and converted in a discrete signal$f(x)$, the spectrum of the digital signal obtained performing the DFT (or the FFT[4]) is made of repetitions of the spectrum of *f(t)*. The period of repetitions is equal to the sampling period *Ts* and is the invers of the sampling frequency f_s. With the proper precautions, the DFT can be seen as a sampling, in the frequency domain, of the Fourier transform, with a sampling period of f_s/N, being N the number of samples. This ratio also represents the frequency resolution of the harmonic spectrum Δf. Since the sampling is a finite (in term of time) operation, the total time of the sampling is called Observation Window (T_w) and can be determined multiplying the number of points per the sampling period. This is equal to the ratio N/f_s and, consequently, to the inverse of Δf. This means that the only possibility to improve the frequency resolution, for a more detailed spectrum, is to enlarge the observation window.

For an analog signal, the sampling can be seen as taking only a part of it, i.e. mathematically as a product between the signal and a rectangular window function $w(t)$. The DFT algorithm is based on the assumption that the signal is stationary, so the acquired N samples are repeated throughout time; if discontinuities occur between subsequent repetitions, for examples because a non-integer number of periods of the signal is sampled, this might lead to some distortions of the frequency spectrum (even when the input signal is periodic).

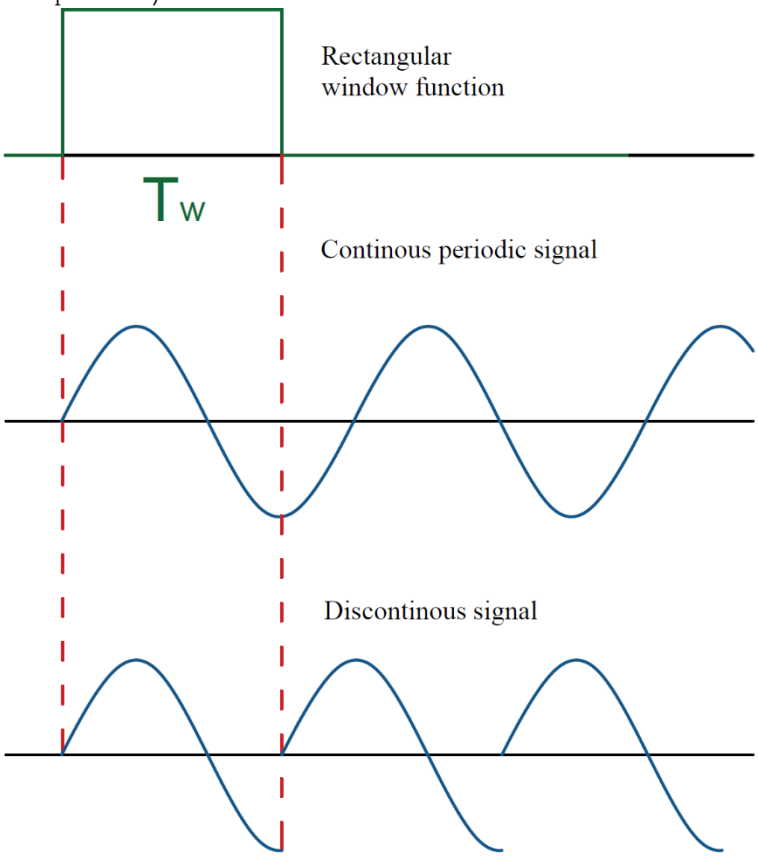

Fig. 2. 6 - Asynchronous sampling

As seen before, the equivalent of the rectangular function in the frequency domain is the sinc. The product in the time domain corresponds to the convolution in the frequency domain. In the general

[4] DFT and FFT algorithms produce the same results, in term of harmonic spectrum components. For this reason, in those paragraphs, the chose of the algorithm will be postponed and, referring to the discrete application of the Fourier transform, the term DFT will be used.

case of signals comprising several harmonics, the sinc functions will superimpose to all harmonics (tones) and the resulting spectrum is then a distorted version of the "true" spectrum.

Because of the windowing, the spectrum of the acquired signal is distorted into a sequence of lobes (one main lobe, centered on frequency *f*, and secondary decreasing side lobes), due to the sinc spectrum. This phenomenon is the so-called spectral leakage.

\

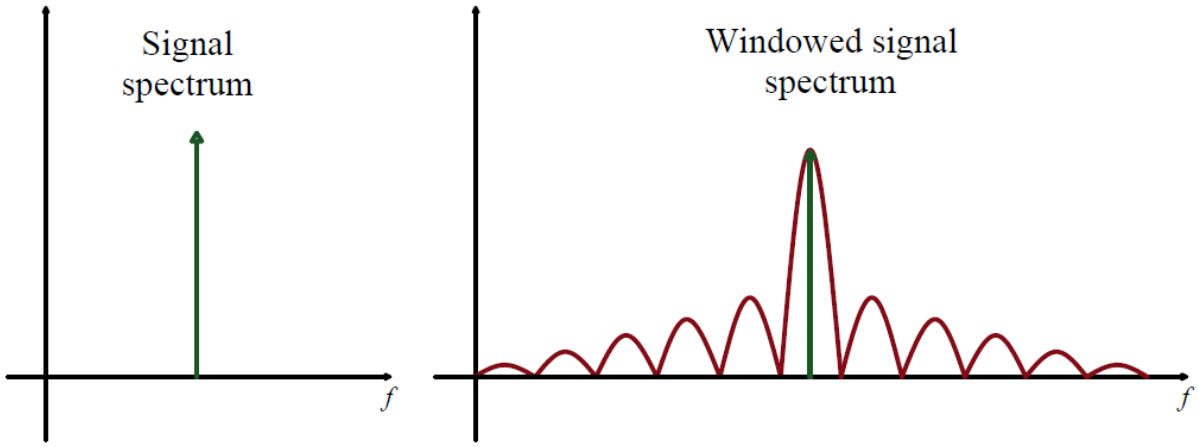

Fig. 2. 7 - Leakage phenomenon

The condition above described is defined as asynchronous sampling. Although this is an unfavourable condition, it is often impossible to avoid it, since, in order to define sampling not asynchronous but synchronous, several conditions must be met:

- the observation window must be an integer multiple of the period of the signal; this implies that:
- the frequency of the signal must be exactly known and
- the sampling frequency must be adjustable to modify T_w amplitude according to the main frequency.

Those condition are not easy to be met and the condition of asynchronous sampling is quite common.

In the case of asynchronous sampling, when the spectrum of the windowed signal is "sampled" (by means of the DFT), the DFT samples are different from the peak of the main lobe and the zero crossing of the side lobes. This results in the fact that the spectral leakage is visible in the DFT spectrum. It leads to errors in the measurement of both magnitude (Sla) and frequency (SLf), defined scallop loss errors.

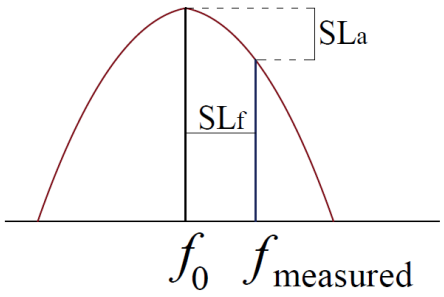

Fig. 2. 8 - Scallop Loss error in amplitude (SLa) and frequency (SLf) measurement

Scallop loss errors can be reduced with some adjustments:

- increase of number N of acquired samples; this implies a large memory buffer and/or the possibility to increase the sampling frequency of the device.
- use of smoothed windows (this technic is called windowing and different window function can be used; mathematically, the sampling is a generic use of a rectangular function for the windowing of the signal);
- other techniques to synchronize the observation window with the signal or to adjust the number of points in input for the DFT (interpolation, zero padding)

For the case of synchronous sampling, when the spectrum of the windowed signal is "sampled" (by means the DFT), the following DFT samples are obtained:

- the peak is in correspondence of the main lobe, which corresponds to the spectral line of the signal (in the case of the figure a sinusoid at frequency f_0);
- the zero crossing of the side lobes correspond to the zeros of the spectrum;
-

This results in the fact that the spectral leakage is not visible in the DFT spectrum, and no errors occur in magnitude and frequency measurements. Mathematically, this is obtained when the fundamental frequency is an integer multiple of the frequency resolution:

$$f_0 = k \cdot \Delta f = k \cdot \frac{1}{T_w} = k \cdot \frac{f_s}{N}$$

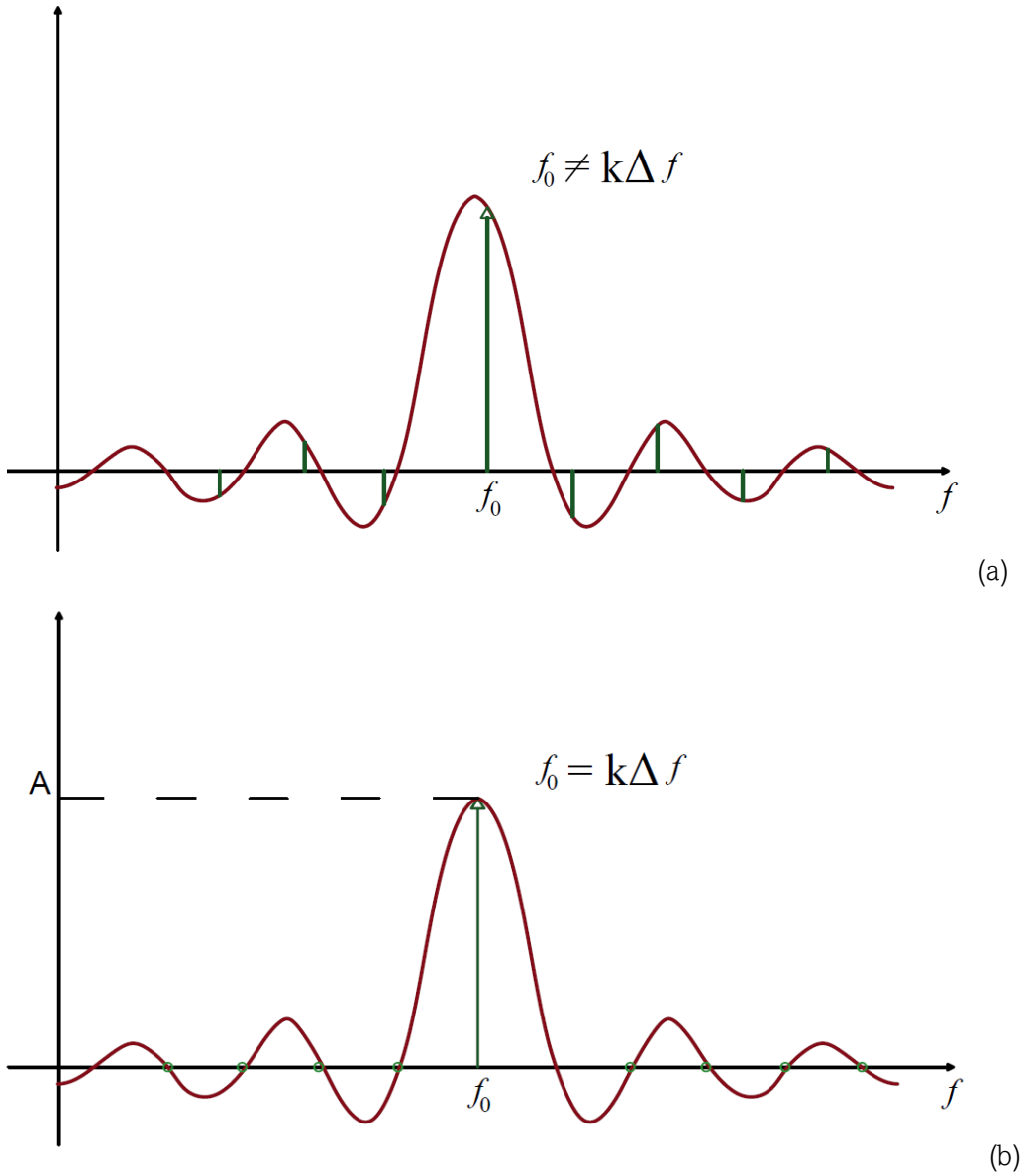

Fig. 2. 9 - Sampling with spectral leakage (a) and without (b)

The synchronization of the signal is an important aspect also for the standard and not just for a theoretical examination of the sampling phenomenon, as described in paragraph 1.3.2.

2.3 Problems for the implementation of harmonic analysis techniques on low cost devices

The implementation of harmonic analysis algorithms on a microcontroller device requires precautions that depend on two main factors:

- The level of accuracy and/or reliability you want to achieve;
- The hardware and software features of the available device.

The first condition, for this work, is to be intended as compliance with current legislation (Standard IEC 61000-4-7 and 61000-4-30) for devices for power quality measurements and specifically for harmonics. The standard analysis, in fact, has brought out some aspects that require specific conditions that must be met (for example the need, for a device for harmonic analysis, to discriminate harmonics up to 50th, implies a minimum (theoretical) sampling frequency of 5000 Hz, to comply with the theorem of Shannon[5]). For the second condition, it is important take into account device specifications because, if certain conditions cannot be physically reached due to the hardware component, it is necessary to act on the software part or vice versa [33]. This is the case for this project, which aims to evaluate the possibility of creating a device that is, simultaneously, compliance with the A-Class of the standard, but with a low-budget hardware.

One of the main aspects to be considered is the gapless sampling of a 200 ms observation window. A gapless sampling implies that the device must be able to perform every operation without losing samples, maintaining a synchronization error under the 0.03% (see Chapter 1.3.2). This means that, according to standard, following the scheme reported in Fig. 1. 7, the instrument must complete the harmonic analysis, the grouping operations and the smoothing of the output values in a 200 time window, while contemporary sampling the actual signal.

In terms of number operation, the groping and the smoothing algorithm have a really lower weight than the harmonic analysis algorithm. For this reason, the main focus has been on the possibility to implement an efficient harmonic analysis algorithm that allows to respect the time restriction.

FFT computational cost, equal to $O(N \cdot log(N))$, is really lower than DFT $O(N^2)$, being N the number of points to be processed. A comparison of the number of operations for different cases is reported in Table 2. 2 and Fig. 2. 10. For the test, the points have been processed on a microcontroller device; the board is a NUCLEO STM32F767ZI, with a maximum CPU frequency of 216 MHz. It's clear that to process the same number of points, the two algorithms require really different times.

Table 2. 2 - DFT and Interpolation + FFT calculation time comparison

Points	Time required [s]	
	DFT	Interpolation + FFT
128	0,132	0,0030
256	0,528	0,0062
512	2,088	0,0123
1024	8,273	0,0249
1667	22,790	
2048	33,171	0,0466

[5] The Shannon theorem states that a signal can be correctly reconstructed if sampling is carried out at a frequency equal to at least twice the maximum frequency (called Nyquist frequency). In the case of a signal with harmonics, the maximum frequency is that of the major order harmonic. For a 50 Hz signal with 50 harmonics, the higher frequency will be 50 50=2500 Hz and the minimum frequency is therefore 5000 Hz.

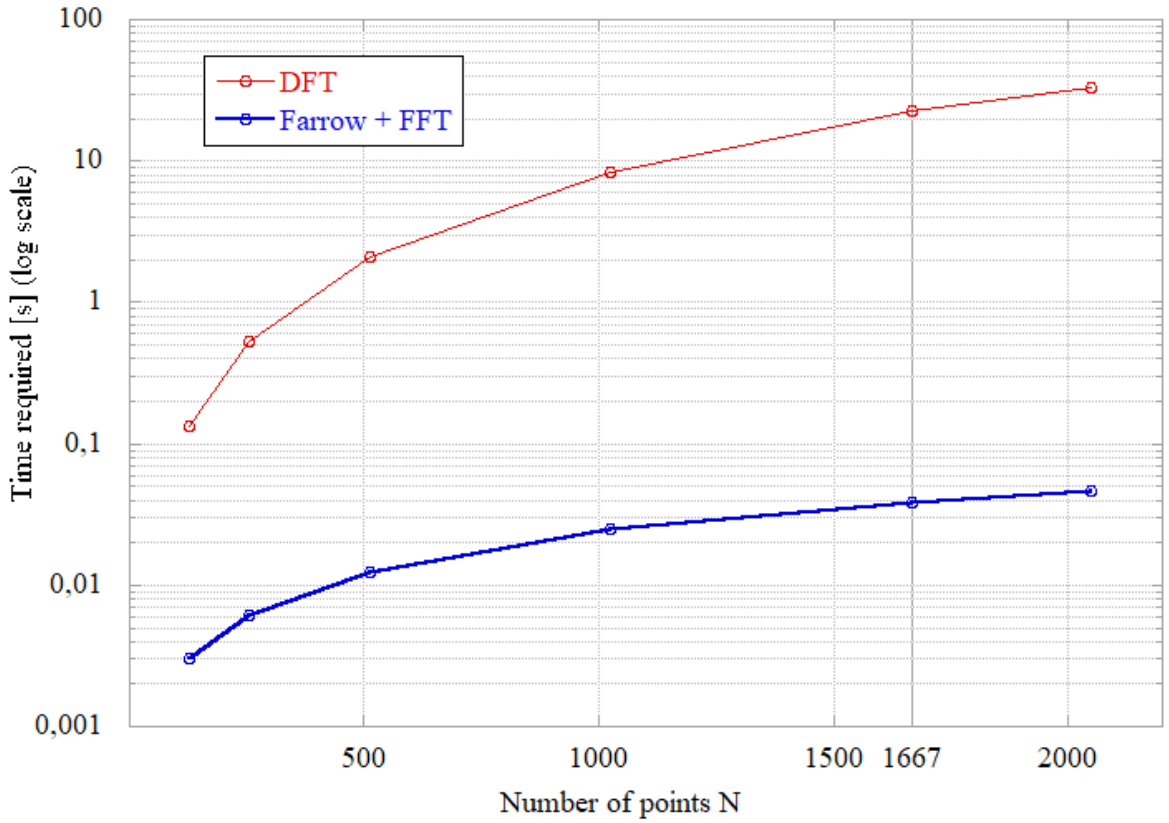

Fig. 2. 10 - DFT and Interpolation + FFT calculation time comparison - log10 scale

As reported in previous chapters, the efficient execution of the Fast Fourier Transform (FFT) algorithm requires the number of samples to be a power of two [54]. In practical implementations, to be compliance with standard requirements of synchronizing the observation window, this imposes limitations on the sampling frequency for data acquisition. For instance, to synchronously sample a 50 Hz signal within a 200 ms observation window and acquire 512 samples, a sampling rate of 2560 Sa/s second would be necessary. Low-cost devices often have fixed sampling frequencies or offer discrete values based on the microcontroller's reference clock, making it challenging to obtain the optimal sampling frequency.

The Discrete Fourier Transform (DFT) algorithm can be employed instead of FFT to alleviate these constraints, as it doesn't impose restrictions on the sampling frequency or the number of samples required within the desired observation window. However, due to its higher computational complexity ($O(N^2)$ opposed to $O(NlogN)$ for the FFT), the execution time of the algorithm may not meet Class A requirements in terms of processing time for gapless signal acquisition and analysis, unless very high-performance systems are utilized.

To reach a number of points that is a power of 2, after the sampling, different techniques are available. Main known are interpolation and zero-padding (ZP) [56]. The second one is really faster than every interpolation algorithm, but it has different malus.

First one is the possibility of only increase the number of points. For the tested sampling frequency, 16, 24 and 32 kHz, for an observation window of 200 ms, a number of points equal to 3200, 4800 and 6400 respectively is acquired. This implies that a number of points equal to 4096 for the first case and 8192 for the others is required. For those cases, a higher computational cost is required for the FFT. Second and most critical aspects of ZP technique is the loss of synchronization of the “padded” signal and the consecutive scallop loss error, that worsen the harmonic measurement accuracy. In fact, even acquiring am integer number of periods, adding zeros the signal is not synchronized and an equivalent not-integer number of periods is considered. Different tests have been conducted using LabVIEW software with different sampling frequencies (so different number of zeros added) to measure the error

committed using ZP compared to interpolation algorithm signal reconstruction. The voltage signal used is made of a 50 Hz fundamental frequency and 50 harmonics, as request in Chapter 1.3.2.

In Fig. 2. 11 – top side the harmonic spectrum is reported. A portion of the spectrum is showed in Fig. 2. 11 – bottom side, where an evident scallop effect is visible. In Fig. 2. 12 the results of one of the tests proposed for harmonic measurement error evaluation is reported; FFT of the signal with zero-padding and interpolated have been implemented and the results have been compared with original spectrum of the signal. For the interpolation, a third order algorithm has been used.

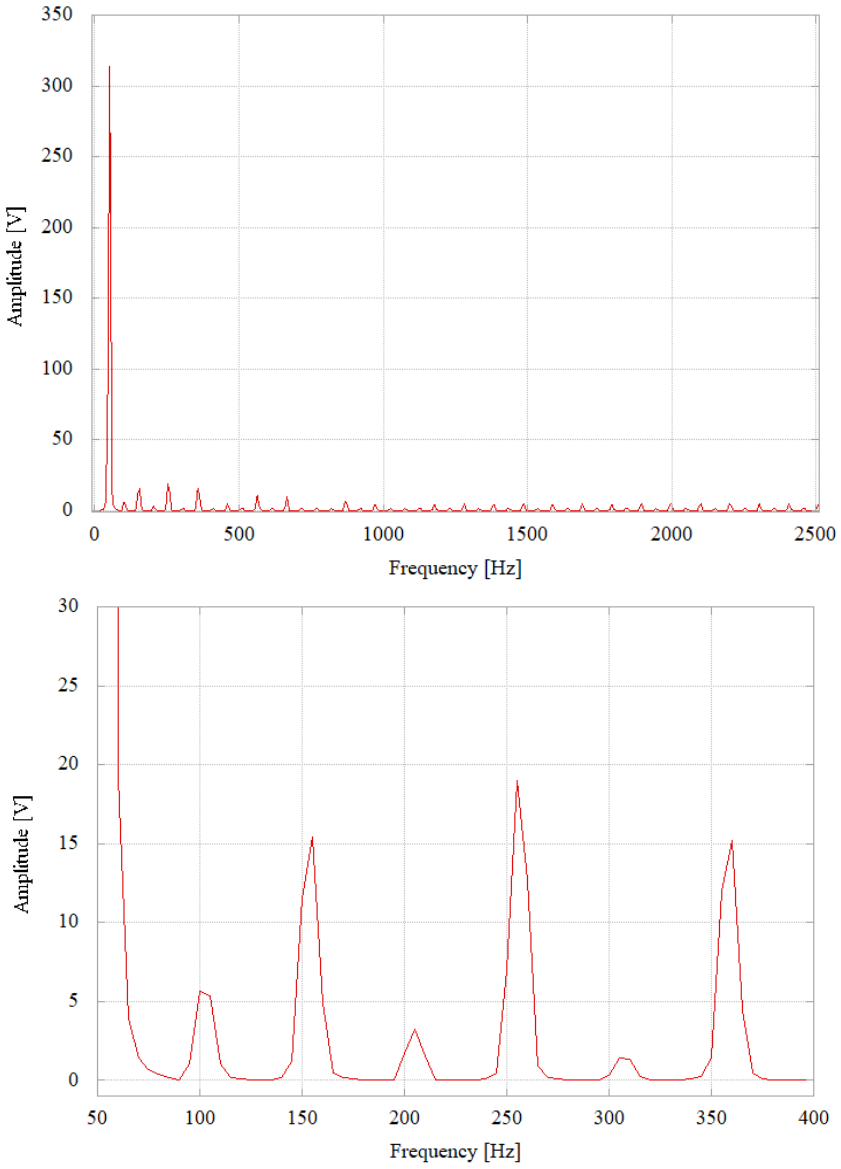

Fig. 2. 11 -On top: Harmonic spectrum of a signal with scallop error.

Bottom: zoom on the firsts 7 harmonic components of the signal

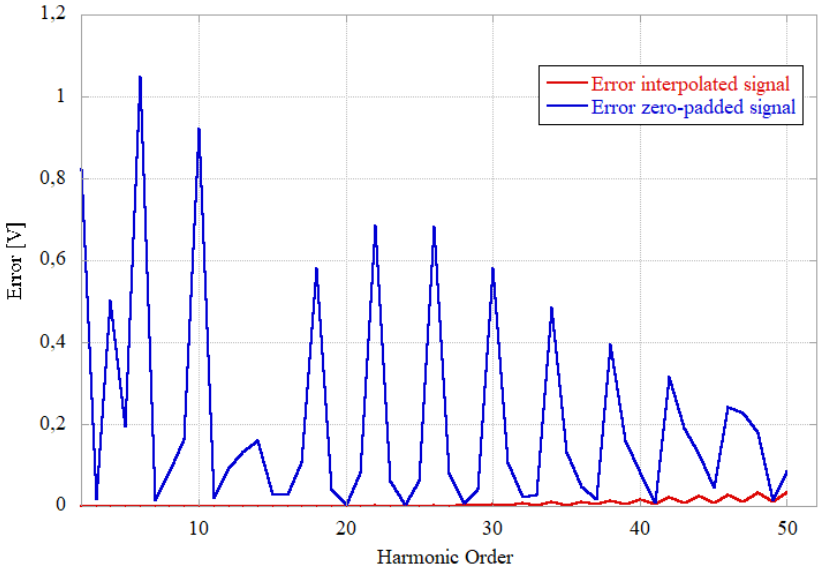

Fig. 2. 12 - Error comparison of harmonic analysis of signal after zero padding and after interpolation

2.3.1 Interpolation algorithms

For the implementation on low-cost devices, the most concrete and flexible possibility is to use an interpolation algorithm to perform an efficient FFT calculation, regardless of the value of f_s [57–59]. However, when pursuing this method, it's crucial to carefully consider the choice of the interpolation algorithm. Using a low-order function may not be suitable for accurately reconstructing the signal. Interpolation algorithms, in fact, works approximating the segment of the signal between consecutive samples using a designated function (linear, polynomial, sinusoidal, etc.). The precision of signal reconstruction and the computational workload are contingent on the sampling frequency and the type and order of the selected interpolating function; the accuracy of the reconstruction improves with a higher order of the approximation function and an increased number of samples N within the observation window Tw. To increase the sampling frequency request on the other hand a greater memory requirement for storing the acquired data. As for the computational cost, the number of operations necessary for implementing the algorithm escalates with both the order of the interpolation function and the number of samples needed for spectral analysis. Consequently, this leads to an increase of the time required to execute these operations.

From this perspective, it is essential to balance the quantity of available samples for interpolation and the adoption of a lower-order function, for signal reconstruction. More in detail, with a fixed number of samples, enhancing the interpolation function's order leads to improved reconstruction accuracy. For instance, as demonstrated in Fig. 2. 13, a comparison between two interpolation functions with an equal number of interpolated points illustrates this effect. When using a particular interpolation function, increasing the number of collected samples it is possible to reconstruct the signal with a lower approximation. So, the use of a low-order interpolation function, such as linear interpolation, becomes practical only when a substantial number of data points are available within the given time window.

2.3.1.1 Lagrange interpolation algorithm

Lagrange polynomial interpolation is a mathematical technique used to approximate a function by constructing a polynomial that passes through a set of given data points [59, 60]. The goal is to find a polynomial that matches the function's values at specific data points and can be used to estimate the function's values at other points within the same range.

For a giver function $f(x)$, in the x variable, the N order interpolator polynomial of Lagrange $p_n(x)$ is defined starting from $n+1$ samples $(x_0, x_1, x_2, \dots x_n)$ and the related values $[f(x_0), f(x_1), f(x_2) \dots . f(\mathrm{x})]$, as:

$$p_n(x) = \sum_{i=0}^{n} f(x_i) \cdot \prod_{k=0, k\neq i}^{n} \frac{x - x_j}{x_i - x_j}$$

[2. 5]

If we define:

$$L_k(x) = \prod_{\mathrm{k}=0,\mathrm{k}\neq i}^{n} \frac{x - \mathrm{x}_j}{\mathrm{x}_i - \mathrm{x}_j}$$

[2. 6]

It is possible to express the Lagrange polynomial in the most known form:

$$p_n(x) = f(x_0)L_0(x) + f(x_1)L_1(x) + \cdots + f(x_n)L_n(x)$$

[2. 7]

Lagrange polynomial interpolation has some advantages, such as the possibility to easily change the order of the function, but it can also be sensitive to the distribution of data points, leading to issues like Runge's phenomenon if data points are unevenly spaced. The use of Lagrange algorithm is widely known and widespread in the literature, so that the main data processing software are already provided with tools for the use of Lagrange functions. An example of interpolation of a signal using Lagrange functions is reported in Fig. 2. 13, starting from Matlab default function for 1st and 3rd order interpolation of a signal.

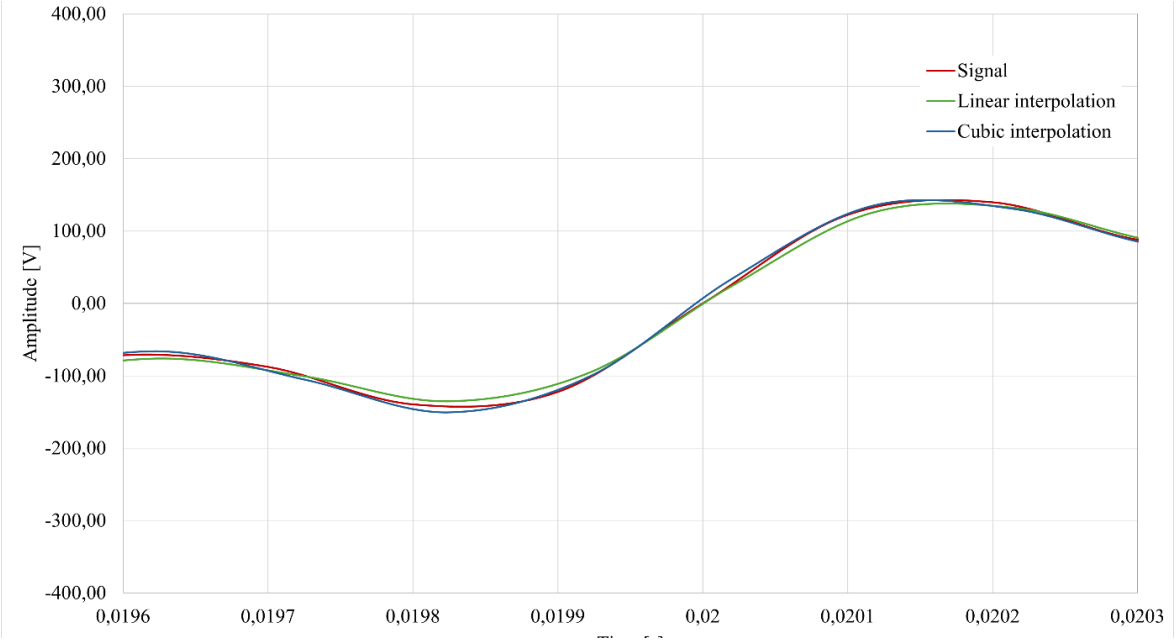

Fig. 2. 13- Detail of the comparison of different interpolation functions (linear and cubic). Example with a non-sinusoidal signal (fundamental 50 Hz component and 5th harmonic)

2.3.1.2 Farrow interpolation algorithm

The use of Lagrange algorithm has the potential to use a lower sampling frequency for the acquisition of the samples, in the way to reduce the memory required for samples storage, using a higher order function. The problem related to this solution consists of the time required for the interpolation operations due to computational cost of the algorithm. Even if this is not a problem using LabVIEW software and a pc-based instrument, for the implementation of the metrics on a low-cost device this can be relevant, if it is considered to work on gapless sampling condition and respect the 200 ms observation window, to be compliance with higher accuracy class of the standard.

Different solutions have been investigated; the best solution founded is the implementation of an interpolator starting from the Farrow filter structure, really common for Fractional-delay digital filter (FD-DF) implementation [61–63].

Farrow interpolator (FI) can be seen as a particular case of the Lagrange interpolator [64, 65]. It can be implemented in different h order functions and use the same coefficient calculation to generate a function that try to approximate the original signal every $h + 1$ points. In Lagrange, every time a new point is considered, the entire polynomial must be recalculated, as reported in [2. 5]. For Farrow implementation, it is assumed that the samples are equidistant, which is a plausible assumption if we consider a regular and fixed sampling frequency, as in this case. Whit this assumption, the calculation time is really reduced even with higher order functions, because the coefficients of the polynomial remain constant.

In continuous time domain, a h order function can be express as:

$$f(t) = k_h t^h + k_{h-1} t^{h-1} + \cdots + k_1 t + k_0 \quad [2.\ 8]$$

With k_i = constant, for $i = h, h-1, h-2 \ldots 0$.

In discrete time domain, according to Farrow hypothesis, we consider a distance between two consecutive samples equal to T_s, so that the samples n and $n + 1$ are placed at the time $n \cdot T_S$ and $(n + 1) \cdot T_s$ respectively. Total observation window T_w will be equal to the total number of samples N multiplied for Ts. The value of the function in discrete time at the time $n \cdot T_s$ is of course the value of the sample n and can be calculated only with n = integer.

The mathematical procedure of interpolate to increase or reduce the number of points from N to P is equivalent to change T_S keeping constant T_w, to have:

$$N \cdot T_s = P \cdot T_{snew} \quad [2.\ 9]$$

The ratio of T_{snew}/T_s is called interpolation ratio and it is a constant.

Instead of use the T_{snew} value, to calculate the placement of the new point, it is assumed that the time pT_{snew} can be expressed as

$$pT_{snew} = (n + \mu) \cdot T_S \quad [2.\ 10]$$

Where p is the index of the points after interpolation (p = 0,1,2…P) and μ is a value between -1 and 1.

After those considerations, it is possible to express the value of the interpolating function z at every time $(p \cdot T_{snew})$, within the observation window, as:

$$z(nT_S + \mu Ts) \approx K_h(nT_S + \mu Ts)^h + K_{h-1}(nT_S + \mu Ts)^{h-1} + \cdots + K_1(nT_S + \mu Ts) + K_0$$

[2. 11]

Just changing the coefficients K and μ.

For a third order function, for examples, the variables are the four coefficients K_3, K_2, K_1 and K_0. They can be calculated using the known values of the function of 4 consecutive samples placed at $(n-1)T_s, nT_s, (n+1)T_s$ and $(n+2)T_s$. With the hypothesis that T_S is constant, the four coefficients will remain constant whatever will be n. With few mathematical passages, it is possible to express the interpolating function in the only variable μ:

In this way, only μ must be calculated, and not the $n+1$ coefficients as for the n-order Lagrange polynomial [61, 65]. This allows decreasing the number of operations needed for the interpolation and the time required for the algorithm execution.

$$\boldsymbol{z(n \cdot Ts + \mu \cdot Ts) = \left(\frac{\mu^3}{6} - \frac{\mu}{6}\right) z\big((n+2)Ts\big) + \left(-\frac{\mu^3}{2} + \frac{\mu^2}{2} + \mu\right) z\big((n+1)Ts\big) +}$$

$$\boldsymbol{+\left(\frac{\mu^3}{2} - \mu^2 - \frac{\mu}{2} + 1\right) z\big((n)Ts\big) + \left(-\frac{\mu^3}{6} + \frac{\mu^2}{2} - \frac{\mu}{3}\right) z\big((n-1)Ts\big)}$$

[2. 12]

To reduce the calculations, in coding programming it is possible to rewrite the expression *[2. 12]* using matrix and vectors, because the coefficients of μ^h are constant. This can be one for every Farrow function order; the example reported is for the third order function.

It is possible to define the vector (column) μ^* as:

$$\mu^* = [\mu^3; \mu^2; \mu; 1]$$

Defining the matrix C as:

i	c_3[i]	c_2[i]	c_1[i]	c_3[i]
-2	1/6	0	- 1/6	0
-1	- 1/2	1/2	1	0
0	1/2	-1	- 1/2	1
1	- 1/6	1/2	- 1/3	0

It is possible to express equation *[2. 12]* as:

$$z(n \cdot Ts + \mu \cdot Ts) = H[-2]z\big((n+2)Ts\big) + H[-1]z\big((n+1)Ts\big) + H[0]z\big((n)Ts\big) + H[+1]z\big((n-1)Ts\big)$$

[2. 13]

Also equal to

$$z(n \cdot Ts + \mu \cdot Ts) = \sum_{i=-2}^{1} H[i]z\big((n-i)T_S\big)$$

[2. 14]

Where

$$H[i] = \sum_{l=0}^{3} C[i]\mu^l$$

[2. 15]

Substituting in *[2. 14]*, it is reached:

$$z(n \cdot Ts + \mu \cdot Ts) = \sum_{i=-2}^{1} \sum_{l=0}^{3} C[i]\mu^l z\big((n-i)T_S\big)\,;(a)$$

$$z(n \cdot Ts + \mu \cdot Ts) = \sum_{l=0}^{3} \mu^l \sum_{i=-2}^{1} C[i] z\big((n-i)T_S\big)\,;(b)$$

[2. 16 a; 16 b]

The term $\sum_{i=-2}^{1} C[i]z\big((n-i)T_S\big)$ will be defined as $Y(l)$; The expression became:

$$z(n \cdot Ts + \mu \cdot Ts) = \sum_{l=0}^{3} Y(l) \cdot \mu^l$$

[2. 17]

The extended form, for this particular case of a third order function, is:

$$z(n \cdot Ts + \mu \cdot Ts) = Y(3)\mu^3 + Y(2)\mu^2 + Y(1)\mu + Y(0)$$

[2. 18]

That can be rewritten for a better implementation as:

$$\boldsymbol{z(n \cdot Ts + \mu \cdot Ts) = \big[\big(Y(3)\mu + Y(2)\big)\mu + Y(1)\big]\mu + Y(0)}$$

[2. 19]

The enormous simplification of this method, if compared to Lagrange implementation, is that $Y(l)$ is just multiplication of a constant value and the sample known. Calculating μ for every new point as defined in [2. 10], starting from the interpolation ratio, the implementation of the interpolation algorithm is really easy even with a third order function.

2.4 Data coding

One aspect to consider when implementing metrics on the microcontroller board is the amount of memory required by the device. The memory required varies depending on the number of samples acquired and the number of points processed by the interpolator and the FFT, even in a not negligible way. In practical terms this translates into a greater expense for the manufacturer, as the materials required for memory components are of high value and increasingly in demand. In addition to the number of points, what affects is also the encoding of the data.

With coding, each ADC output value is represented by a digital code. In binary code, the value is represented by a sequence of n bits (being n the number of bits of the ADC). There are various binary codes (which can be useful for different applications). For our scopes we can refer to the general coding scheme coding represented in the Fig. 2. 14, where the sign bit can be present (for coding both positive and negative values) or not (for only positive values). In this last case we will refer to the natural binary code (or straight binary code).

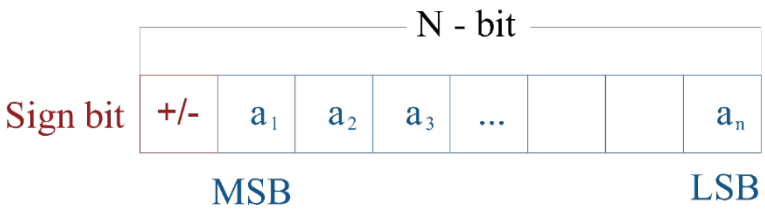

Fig. 2. 14 - Coding bit distribution

With the straight binary coding (n bit) a generic value V_{in} within the range form *0* to V_{FS} can be represented according to the following equation:

$$V_{in} = \left(a_1 \cdot 2^{(n-1)} + a_2 \cdot 2^{(n-2)} + \cdots \ldots a_n \cdot 2^{(n-n)}\right)\frac{V_{FS}}{2^n} \quad [2.\ 20]$$

The coefficients $a_1\ a_2 \ldots a_n$ can assume the values *0* or *1*. The sequence of a_i values represents the binary code for V_{in}. a_1 is the Most Significant Bit MSB; a_n is the Least Significant Bit LSB. The maximum error is equal to half the difference between to subsequent codes (equal to the least significant bit, LSB). Thus the maximum quantization error is equal to LSB/2.

The binary representation (straight or in complement to two) is fine for integer or fractional numbers, but the latter are rounded and then a mistake is made in reporting the data. You can represent "real" numbers (with finite but variable precision) using a type notation:

$$X = (\pm)F \cdot 10^E$$

Where F is the mantissa (significand) and E is the exponent.

Tipically for a 32 bit code, excluded the first for the sign, 8 are used for the exponent and the remaining part for the mantissa.

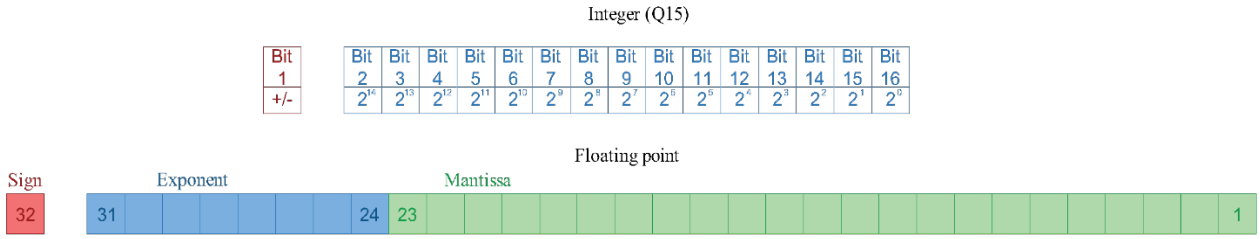

Fig. 2. 15 - Coding bit distribution for integer format and floating point format

The memory required to a device takes into account not only the storage of the points after sampling, but also all the space necessary for the mathematical processing of samples (interpolation, FFT, Smoothing, Grouping). It is therefore estimated the memory that the device should have available for a full harmonic analysis according to the standards, with 16, 32 and 64 bit coding, depending on the device specifications (sampling frequency) and the characteristics of the chosen interpolation algorithm. The results, expressed in kilobytes, are reported in Table 2. 3.

As one of the most stringent requirements for the instrument to be in class A is the one dependent on to time (200 ms time window for gapless sampling), the choice of encoding has been influenced not only by memory, but also by the possibility for a low cost hardware to process data in Fixed point or in Floating point and in which time. Because of for the test a board NUCLEO STM32F767ZI (maximum CPU frequency of 216 MHz) has been chosen (the motivations are reported in Chapter 4), samples are encoded directly from the ADC in fixed point Q15 (the description of the encoding is shown above). The interpolation process, which uses a newly written algorithm, has also been implemented in fixed point, to perform it quickly. The process of FFT instead, which takes advantage of the libraries available to the device, has been carried out in 32-bit floating point, allowing therefore an optimization in terms of time not indifferent, to the detriment of a slightly higher share of memory

Table 2. 3 - Memory required for complete harmonic analysis

Memory required [kbyte] for 200 ms acquisition (10 periods)							
Case tested		Samples	Sampled acquired [kbyte]	Storage of samples after interpolation [kbyte]	FFT array [kbyte]	Grouping and Smoothing [kbyte]	Total [kbyte]
N. bit = 64	fs = 16 kHz (interp. 2048)	3200	25	16	16	0,8	57
	fs = 16 kHz (interp. 4096)	3200	25	32	32	0,8	89
	fs = 24 kHz (interp. 2048)	4800	37,5	16	16	0,8	70
	fs = 24 kHz (interp. 4096)	4800	37,5	32	32	0,8	102
	fs = 32 kHz (interp. 2048)	6400	50	16	16	0,8	82
	fs = 32 kHz (interp. 4096)	6400	50	32	32	0,8	114
N. bit = 32	fs = 16 kHz (interp. 2048)	3200	12,5	8	8	0,4	29
	fs = 16 kHz (interp. 4096)	3200	12,5	16	16	0,4	45
	fs = 24 kHz (interp. 2048)	4800	18,75	8	8	0,4	35
	fs = 24 kHz (interp. 4096)	4800	18,75	16	16	0,4	51
	fs = 32 kHz (interp. 2048)	6400	25	8	8	0,4	41
	fs = 32 kHz (interp. 4096)	6400	25	16	16	0,4	57
N. bit = 16	fs = 16 kHz (interp. 2048)	3200	6,25	4	4	0,2	14
	fs = 16 kHz (interp. 4096)	3200	6,25	8	8	0,2	22
	fs = 24 kHz (interp. 2048)	4800	9,375	4	4	0,2	17
	fs = 24 kHz (interp. 4096)	4800	9,375	8	8	0,2	25
	fs = 32 kHz (interp. 2048)	6400	12,5	4	4	0,2	21
	fs = 32 kHz (interp. 4096)	6400	12,5	8	8	0,2	29

3. SIMULATION STUDY OF METRICS FOR HARMONIC ANALYSIS

In previous chapter it has been investigated if it is possible to realize an instrument for PQ analysis, with a focus on voltage harmonic analysis, using a low cost microcontroller device and, if it is possible, which specification this device should have to reach the A-Class according to IEC Standard [38, 41].

Firstly, an analysis of the requirement of the standard have been conducted. Then the system composed of the chain sampling-elaboration of the samples-Fourier analysis has been implemented in a PC-based instrument to test the pros and the limitations of the solutions provided.

3.1 Synchronization error

As reported in Chapter 1.3.1 and 1.3.2, both in IEC 61000-4-30 and IEC 61000-4-7 Standards, the "maximum permissible error for time between leading edges", i.e. the synchronization error, "…is equal to $\pm 0.03\%$".

The error $e_{\%}$ can be defined as in equation *[1. 1][3. 1]*.

With few passages it is obtained an error defined as

$$e_{\%} = 100 \cdot \frac{1}{2 \cdot f_s} \frac{1}{10 \cdot T1} = 5 \cdot \frac{f_1}{f_s} \qquad [3.1]$$

where:

f_S = sampling frequency [Hz];

T_1 = fundamental period [s] = $1/f_1$;

f_1 = fundamental frequency [Hz];

The error only depends on sampling frequency if power frequency is considered fixed.

If the power frequency is variable, as it happens in real applications, frequency $f_s(f_1)$ must be checked to guarantee an error lower than 0.03 in all the cases:

$$f_s(f_1) > \frac{5 \cdot f1}{0.03} \qquad [3.2]$$

According to standard CEI 0-21 "Reference technical rules for the connection of active and passive users to the LV electrical Utilities" [43], power frequency is reported to be variable in a range of $0.94 f_1 - 1.03 f_1$; in Fig. 3. 1, the error committed in this range, with different sampling frequency, is reported.

A limit value of f_s equal to $8.34\ kHz$ is set to respect the limit of $e_{\%} = 0.03$ for the case of $f_1 = 50\ Hz$. For all the further tests, a minimum limit value of $10\ kHz$ for the sampling frequency has been considered.

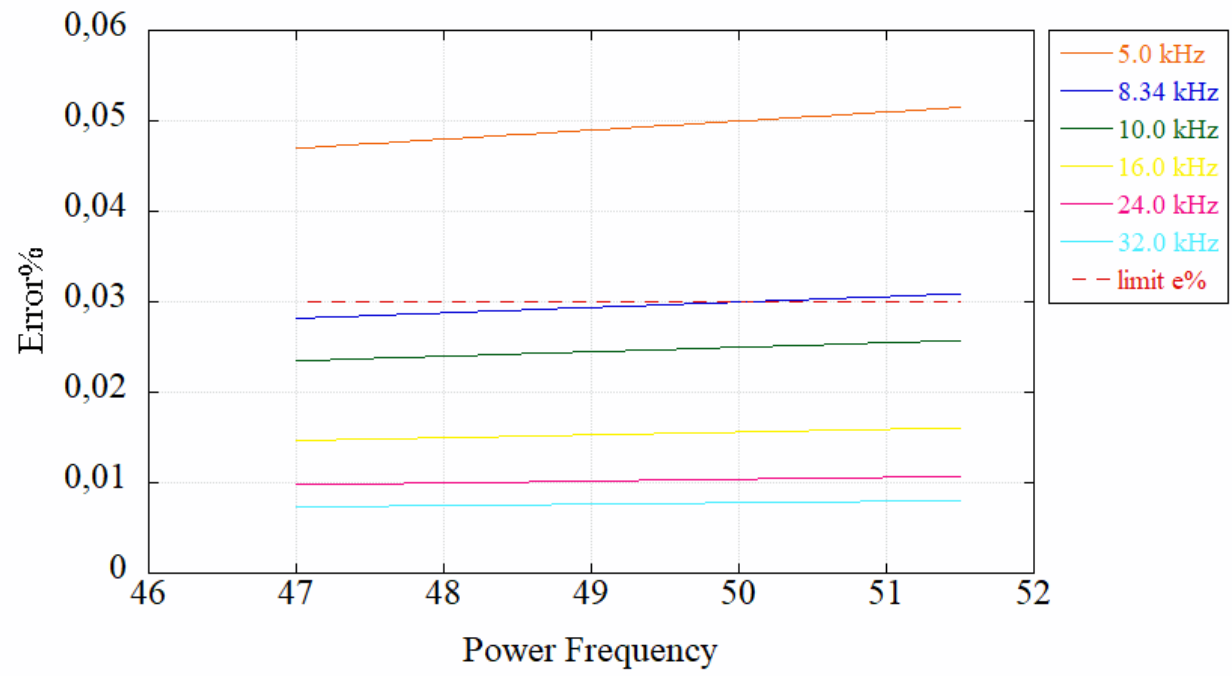

Fig. 3. 1 - Synchronization error for different sampling frequency

3.2 Zero-cross technique

A zero cross (ZC) technique is useful to improve synchronization. Moreover, to respect the limitation of the standard concerning the amplitude of the observation window, the ZC function allowed to acquire 10 periods exactly.

There are different conditions that allowed to detect the passing of the function for the zero. A first possibility is to monitor the difference between two consecutive points. When the difference is zero, the function has passed the zero value. Considering the real behaviour, it is not possible to obtain perfectly zero, so a threshold must be set, according to sample value resolution. This solution only use the difference operation and has a low computational cost, but it is not accurate if the samples are too distant or the resolution isn't enough high.

Another possibility is to multiply the values of two consecutive samples and only when the results is negative the ZC condition has occurred. Multiplication is more complicated to implement for a microcontroller but there is no need of threshold set and the zero crossing is always detected.

Using a ZC function, the samples are taken one per time but only two are memorized; until the crossing for the zero value occurs, the samples are not stored. After ZC detection, the samples are stored and the amplitude of the observation window is only determined by the number of periods counted.

One of the main problems with ZC implementation is the presence of noise and disturbances. To avoid false zero cross detection when the signal moves around the zero value, the ZC algorithm is disabled once the first zero cross is detected and it is enabled again after around 3/4 of the signal period (i.e. around 15 ms for a 50 Hz signal)

3.3 Accuracy Requirements - Simulation Tests

In order to test the accuracy in signal reconstruction of the different algorithms, a test system has been implemented in LabVIEW software. The focus was on single harmonic component detection in the range 2nd – 50th harmonic of a 50 Hz signal, as request in IEC 61000-4-7 standard for S-Class and A-Class instrument for harmonic measurement. More in detail, for these instruments, the error limits for harmonic components measurement are:

For a A-Class instrument:

- $e \leq 5\%\ U_m$, for $U_m \geq 1\%\ U_{nom}$,
- $e \leq 0.05\%\ U_{nom}$, for $U_m < 1\%\ U_{nom}$,

[3. 1]

For a S-Class instrument:

- $e \leq 5\%\ U_m$, for $U_m \geq 3\%\ U_{nom}$,
- $e \leq 0.15\%\ U_{nom}$, for $U_m < 3\%\ U_{nom}$,

[3. 2]

where U_m is the measured amplitude of each harmonic component and $U_{nom}$is the rated voltage. The definition of the error is reported in 1.3.2.2.

The errors introduced by the interpolation algorithm were estimated by comparing the results of the spectral analysis with the harmonic components amplitudes of the simulated reference test signal.

As regards the test signal, the IEC standards don't give any information about the signal for what concerns single harmonics amplitudes or overall THD; thus, the signal used for the simulations was built following the indication of standard EN 50160 "Voltage characteristics of electricity supplied by public distribution systems" [66], which provides amplitudes limits for harmonics up to the 25th, as reading in Table 3. 1. For 25th to 50th order harmonics, amplitudes were set to values similar to those of EN 50160, i.e. 0.5% of the fundamental for even components and 1.5% odd harmonics.

A virtual instrument (VI) has been realized in LabVIEW to implement Lagrange linear, quadratic and cubic interpolation of the test signal, giving back a fixed number of points, power of two. Then FFT is processed and the amplitude of each component are compared to original signal harmonics.

The VI allowed also to check if the IEC 61000-4-7 error limits for harmonic detection were fulfilled.

Table 3. 1 - Harmonics relative amplitude for test signal

Even order harmonics		Odd order harmonics			
Order h	Relative amplitude Uh	Order h (multiple of three, up to 21st)	Relative amplitude Uh	Order h (other, up to 49th)	Relative amplitude Uh
2	2,00%	3	5,00%	5	6,00%
4	1,00%	9	1,50%	7	5,00%
6 ÷ 50	0,50%	15, 21	0,50%	11	3,50%
				13	3,00%
				17	2,00%
				19 ÷ 49	1,50%
uh is the amplitude of the h-order harmonic (percentage of fundamental component)					

Test voltage signal waveform is shown in Fig. 3. 2.

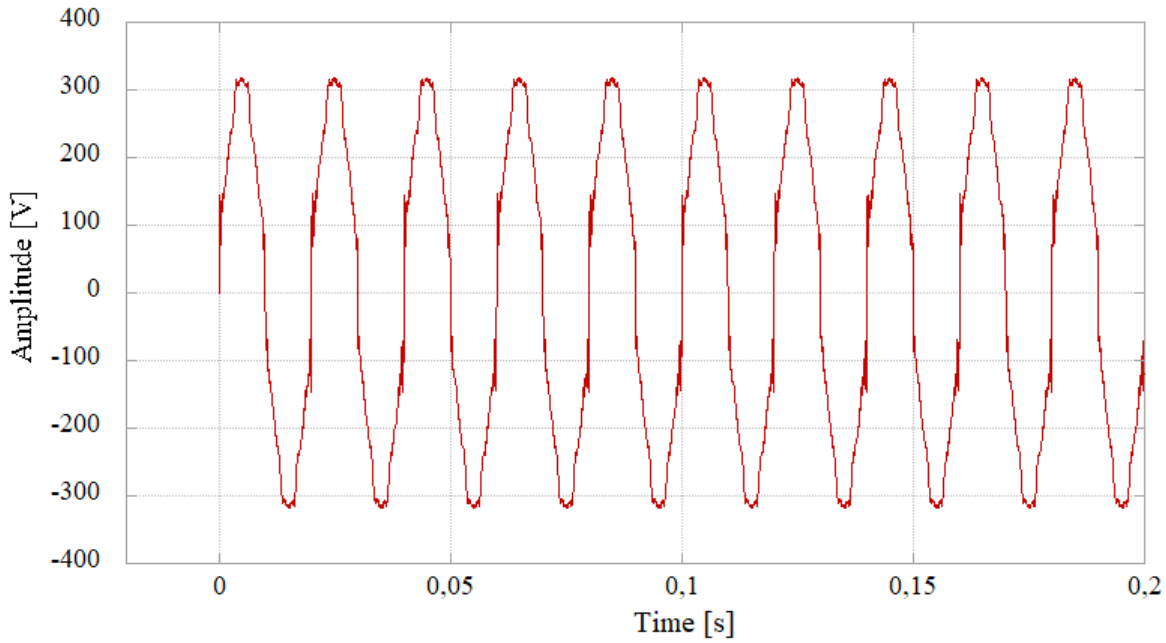

Fig. 3. 2 - Test signal

With the VI different cases, summarized in Table 3. 2, have been simulated, with different value of sampling frequency and number of points after the interpolation. Sampling frequency has been set according to equation [3.2] limitations; the values have been chosen starting from the analysis of commercial devices for harmonic measurement available on market and the indications of industrial

partners, ST Microelectronics s.r.l., for most plausible values of sampling frequency of a new low-cost device to be produced. The points after the interpolation have been set to 2048 and 4096, values close to the number of sampled acquired in the 16-32 kHz sampling frequency range, in accordance with memory required issues and computational cost of operations (see chapter 4).

Table 3. 2 - Simulated cases

Case	fs [kHz]	Points after interpolation
1	16	2048
2	24	
3	32	
4	16	4096
5	24	
6	32	

In Fig. 3. 3 a block diagram of the VI is reported. The results of the simulations are showed in figures from Fig. 3. 4 to Fig. 3. 9. Results show how, in the range of frequencies tested, the quadratic and cubic interpolation algorithms allow to maintain the errors made below the values imposed by the standards. Linear algorithm, on the contrary, it is not usable with a 16 kHz f_s. The results, in terms of standard compliance, are the same for both 2048 and 4096 points after interpolation reached, because the difference between the errors made in the two cases is low-significant.

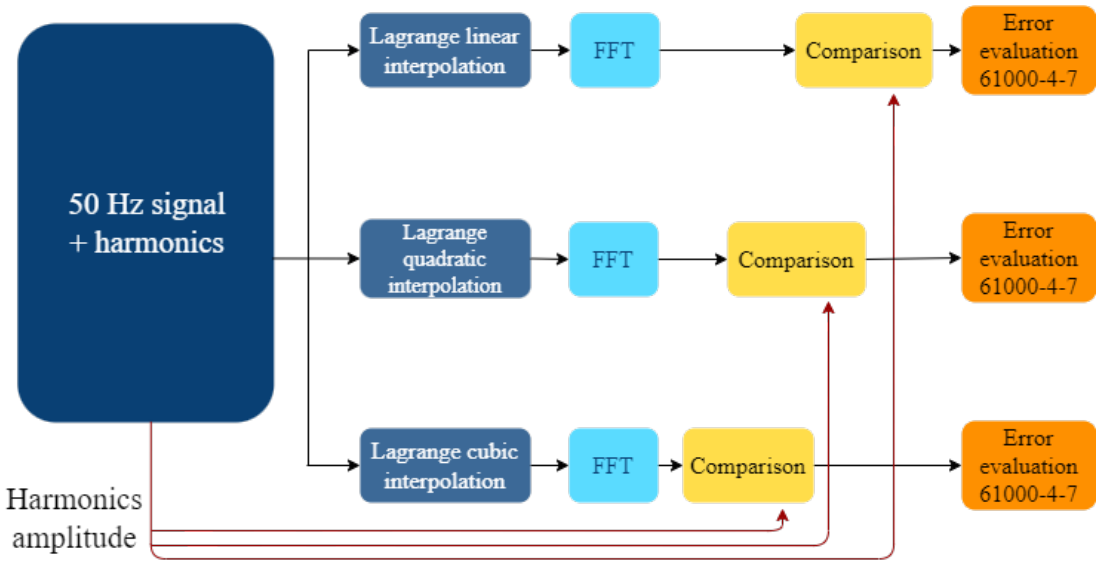

Fig. 3. 3 - Block diagram of LabVIEW VI for interpolation algorithms comparison

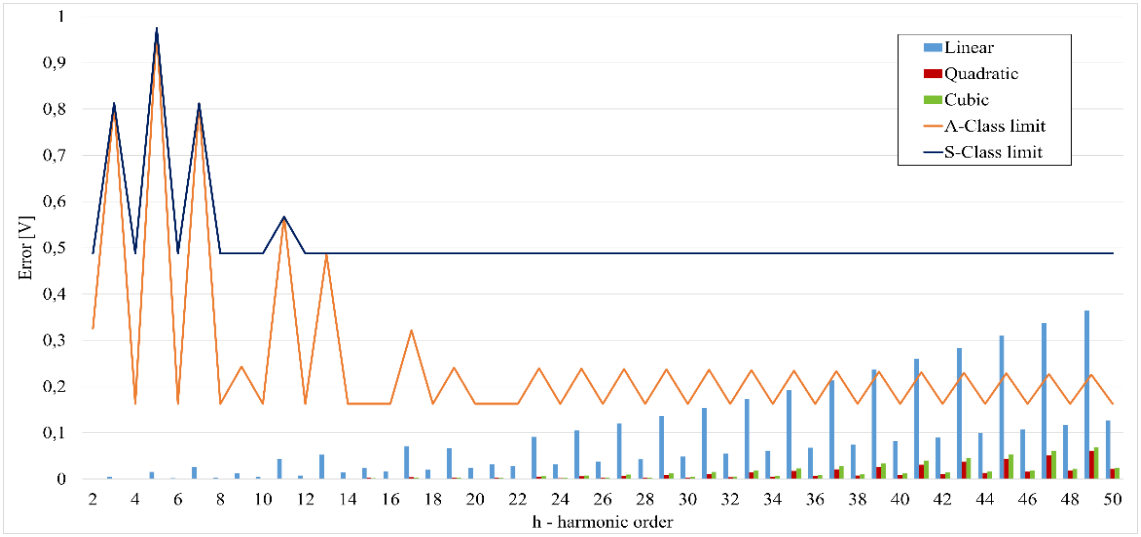

Fig. 3. 4 - Error harmonic components for Case 1: fs = 16 kHz, n. points = 2048

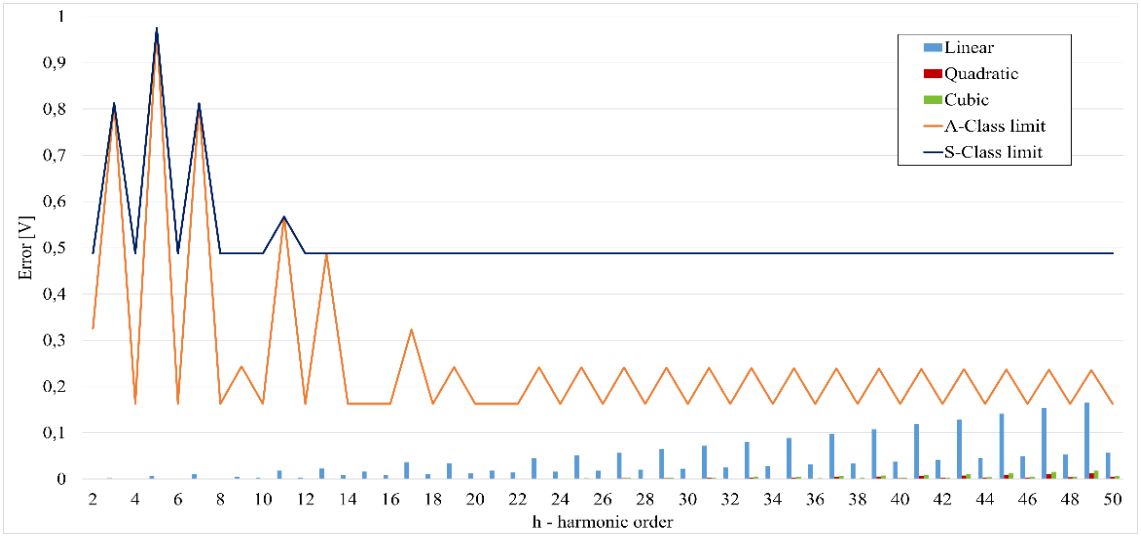

Fig. 3. 5 - Error harmonic components for Case 2: fs = 24 kHz, n. points = 2048

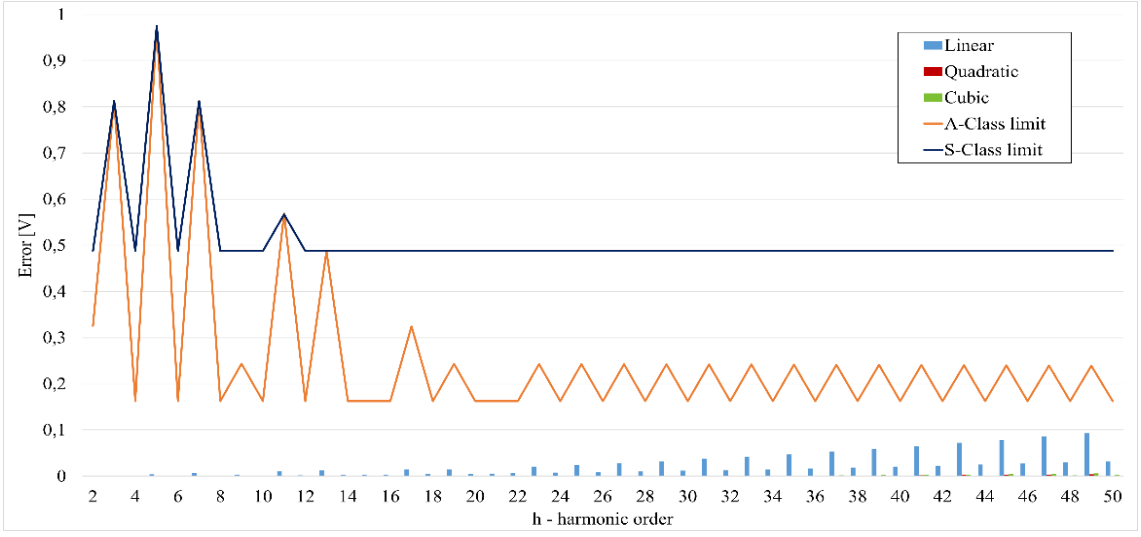

Fig. 3. 6 - Error harmonic components for Case 3: fs = 32 kHz, n. points = 2048

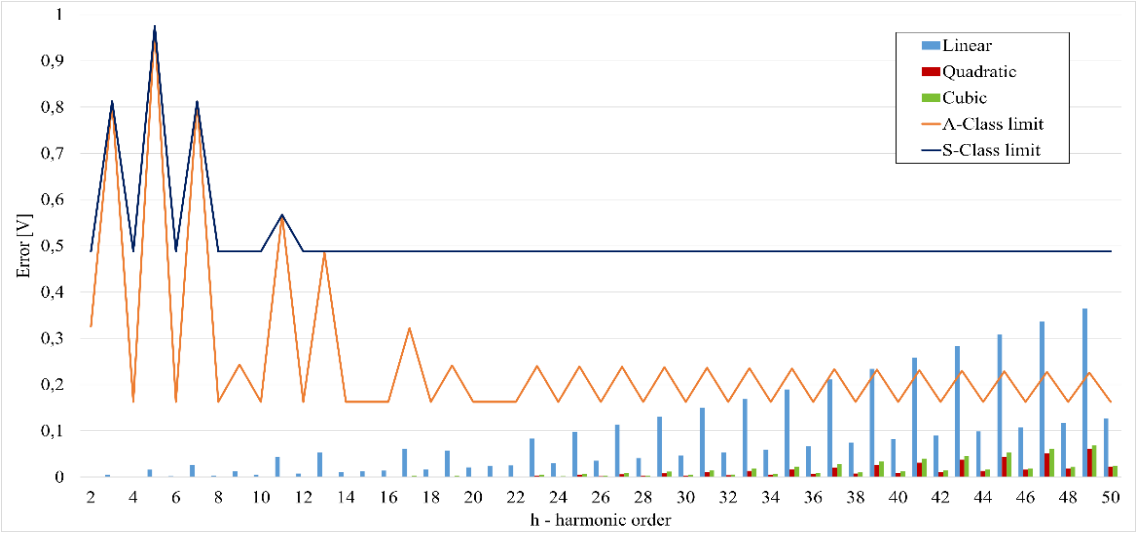

Fig. 3. 7 - Error harmonic components for Case 4: fs = 16 kHz, n. points = 4096

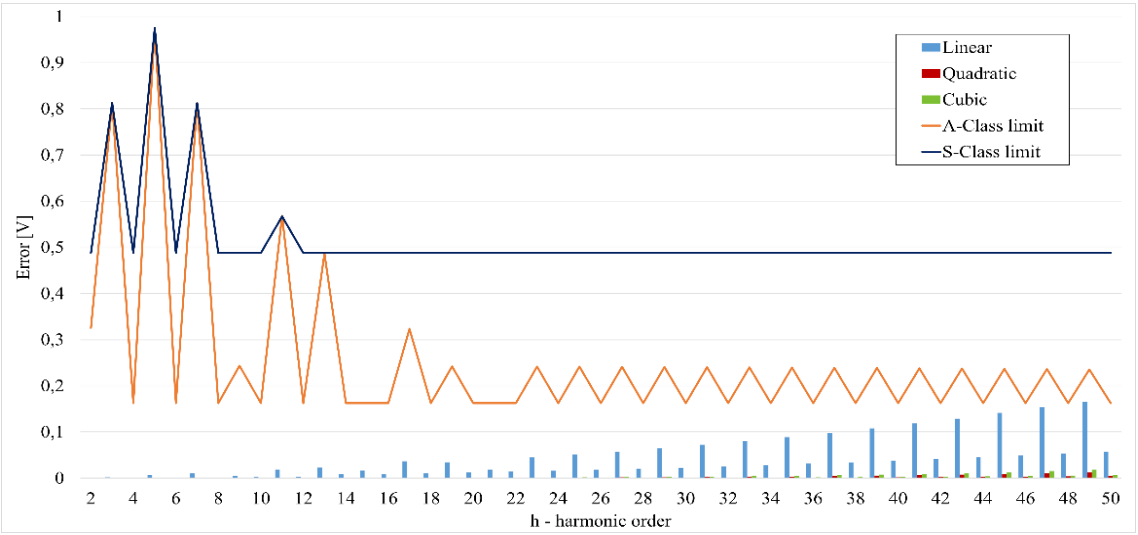

Fig. 3. 8 - Error harmonic components for Case 5: fs = 24 kHz, n. points = 4096

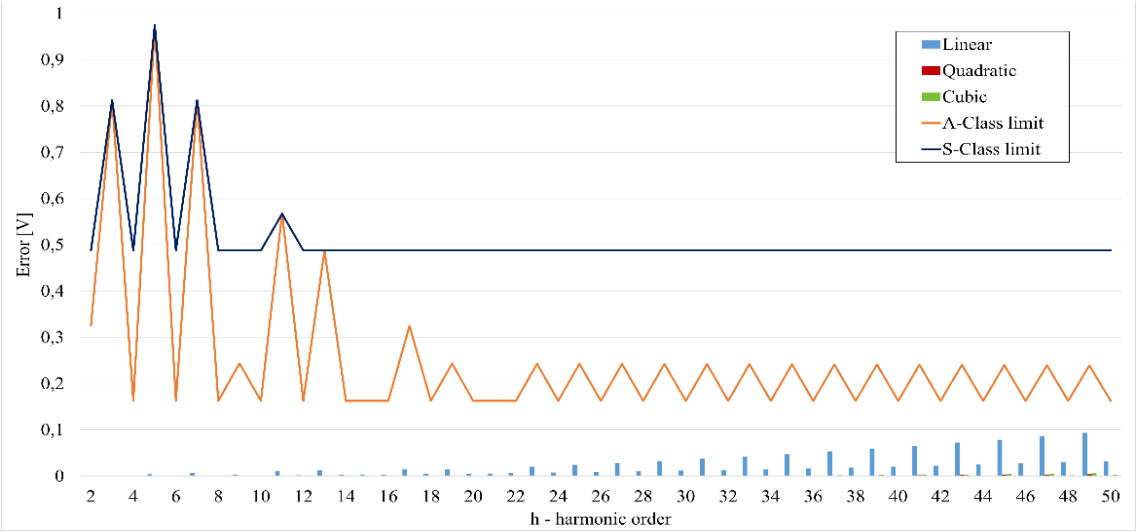

Fig. 3. 9 - Error harmonic components for Case 6: fs = 32 kHz, n. points = 4096

Table 3. 3 - Accuracy limitation compliance

Error limitation on harmonic measurement												
Algorithm used for interpolation	**Sampling frequencies and points after the interpolation**											
	Case 1 fs = 16 kHz; 2048 points		Case 2 fs = 24 kHz; 2048 points		Case 3 fs = 32 kHz; 2048 points		Case 4 fs = 16 kHz; 4096 points		Case 5 fs = 24 kHz; 4096 points		Case 6 fs = 32 kHz; 4096 points	
Reference	S - Class	A - Class	S - Class	A - Class	S - Class	A - Class	S - Class	A - Class	S - Class	A - Class	S - Class	A - Class
Lagrange linear interpolation	Respected	Not respected	Respected		Respected		Respected	Not respected	Respected		Respected	
Lagrange quadratic interpolation	Respected		Respected		Respected		Respected		Respected		Respected	
Lagrange cubic interpolation	Respected		Respected		Respected		Respected		Respected		Respected	

3.4 Simulation results – Farrow Algorithm

The possibility to use the Farrow algorithm instead of Lagrange one, and which order function eventually, has been investigated in simulation using LabVIEW software. The cases reported in Table 3. 2, simulated in LabVIEW using the signal showed in Fig. 3. 2, have been repeated using the Farrow interpolation algorithm of first, second and third order. The results are reported in figures from Fig. 3. 10 to Fig. 3. 15.

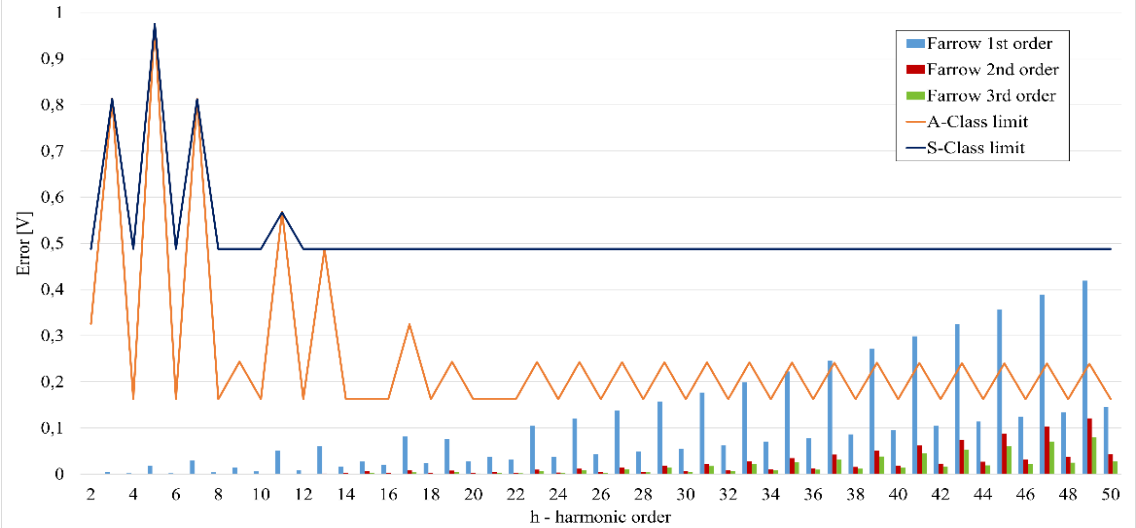

Fig. 3. 10 - Error harmonic components for Case 1 with Farrow Algorithm: fs = 16 kHz, n. points = 2048

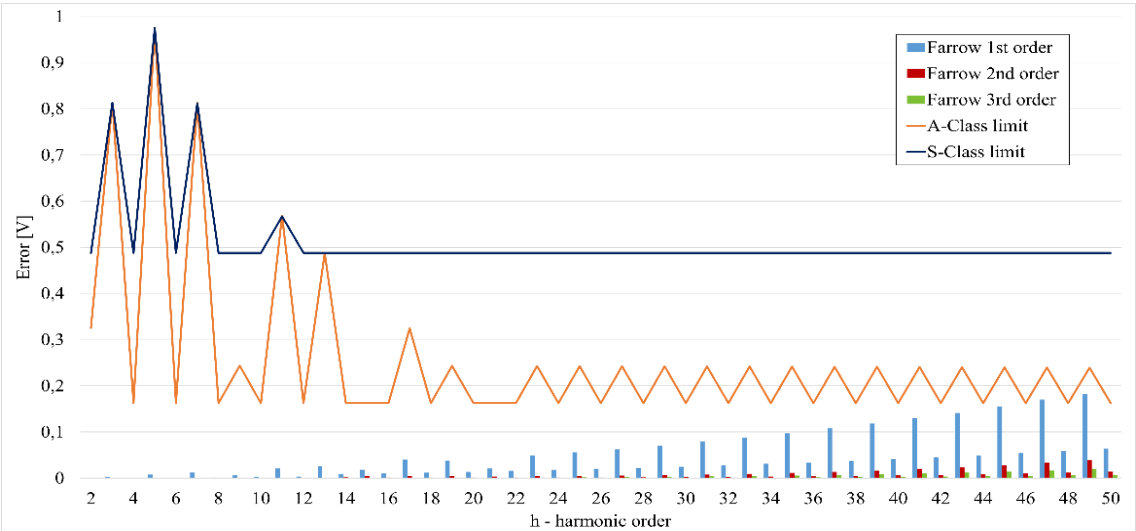

Fig. 3. 11 - Error harmonic components for Case 2 with Farrow Algorithm: fs = 24 kHz, n. points = 2048

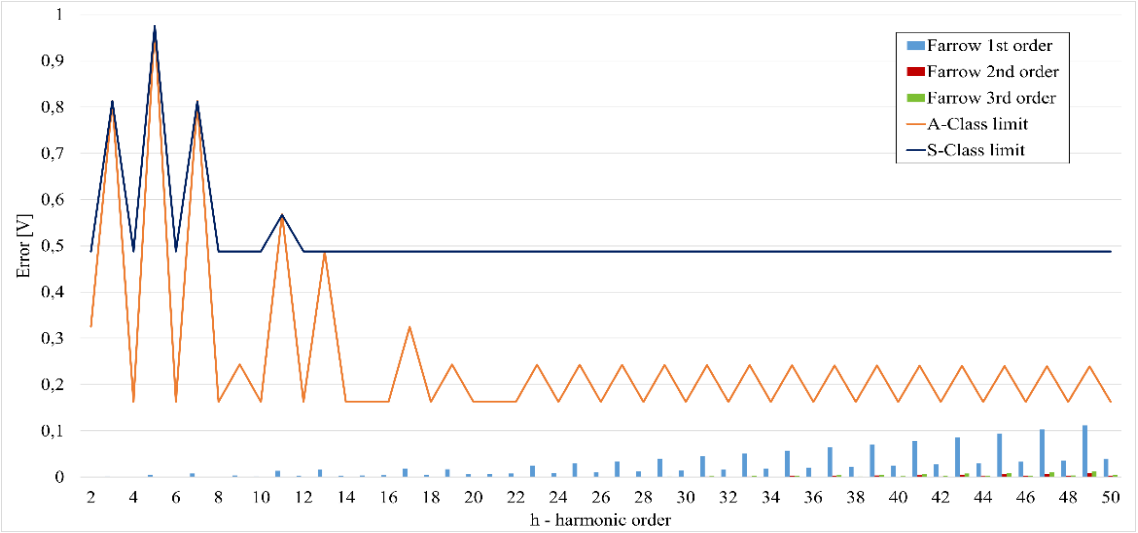

Fig. 3. 12 - Error harmonic components for Case 3 with Farrow Algorithm: fs = 32 kHz, n. points = 2048

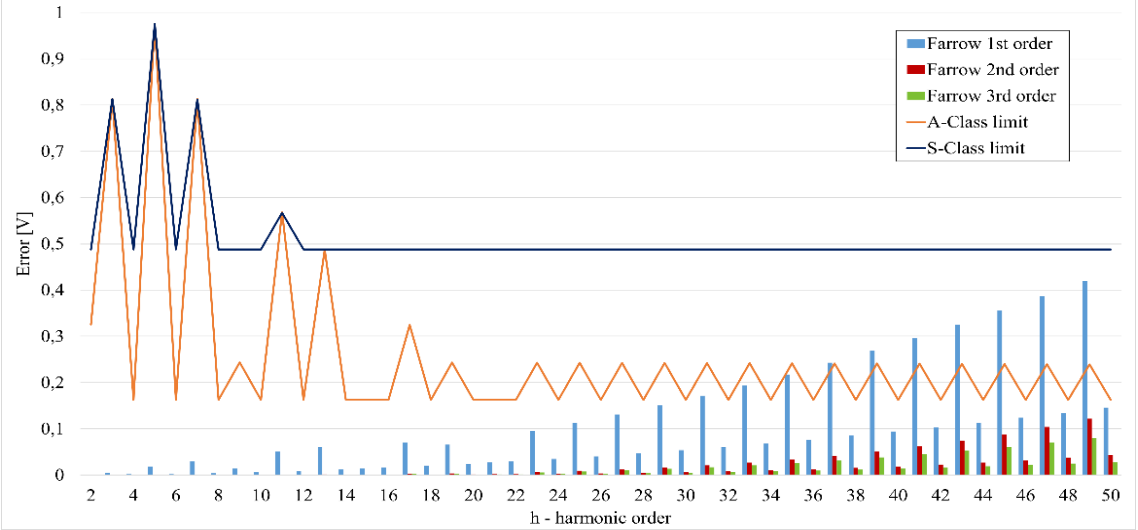

Fig. 3. 13 - Error harmonic components for Case 4 with Farrow Algorithm: fs = 16 kHz, n.points = 4096

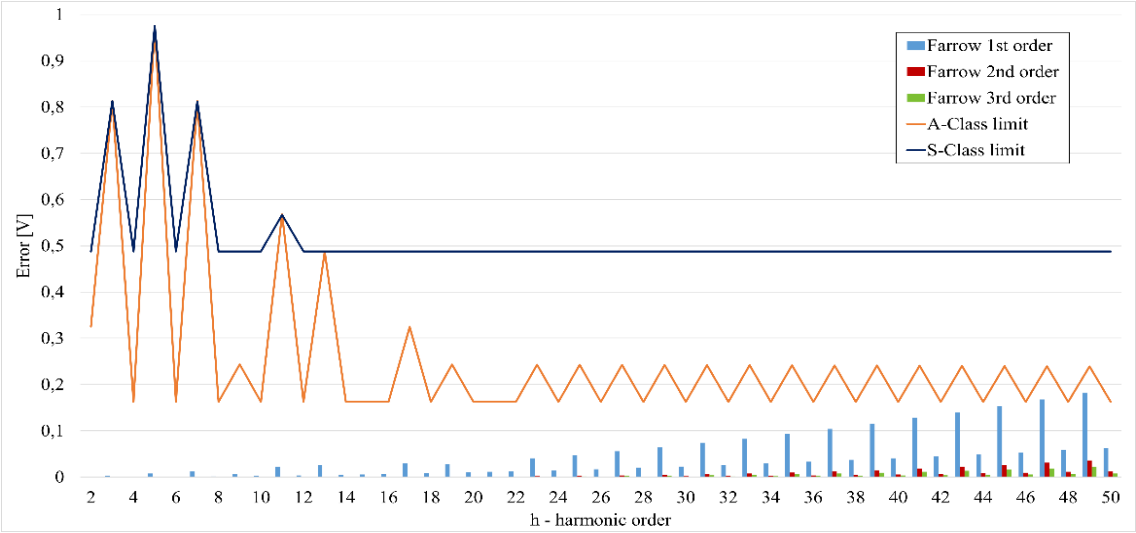

Fig. 3. 14 - Error harmonic components for Case 5 with Farrow Algorithm: fs = 24 kHz, n.points = 4096

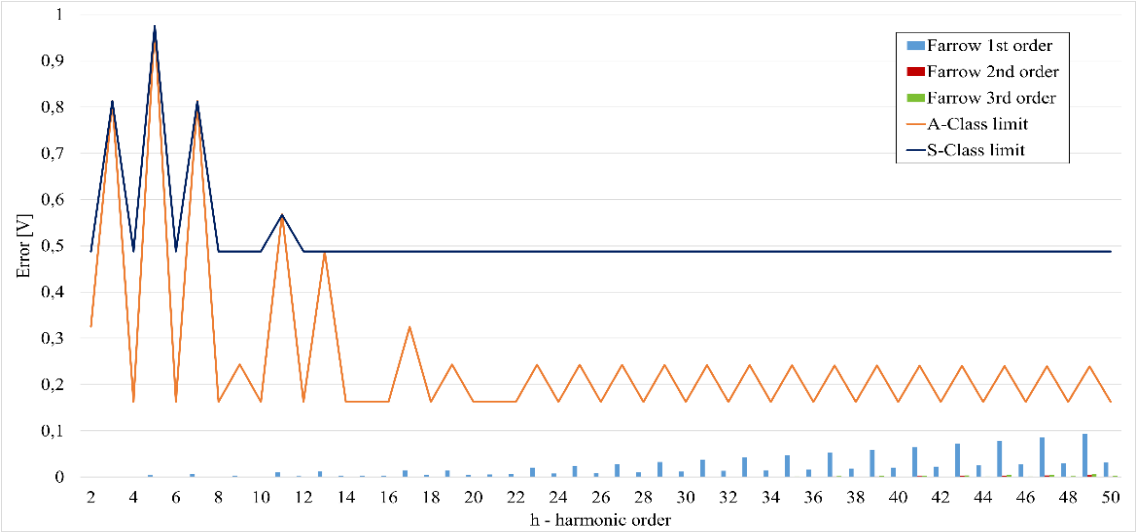

Fig. 3. 15 - Error harmonic components for Case 6 with Farrow Algorithm: fs = 32 kHz, n.points = 4096

Table 3. 4 - Accuracy limitation compliance using Farrow interpolation algorithm

Error limitation on harmonic measurement												
Algorithm used for interpolation	**Sampling frequencies and points after the interpolation**											
	Case 1 fs = 16 kHz; 2048 points		Case 2 fs = 24 kHz; 2048 points		Case 3 fs = 32 kHz; 2048 points		Case 4 fs = 16 kHz; 4096 points		Case 5 fs = 24 kHz; 4096 points		Case 6 fs = 32 kHz; 4096 points	
Reference	S - Class	A - Class	S - Class	A - Class	S - Class	A - Class	S - Class	A - Class	S - Class	A - Class	S - Class	A - Class
Farrow 1st order interpolation	Respected	Not respected	Respected		Respected		Respected	Not respected	Respected		Respected	
Farrow 2nd order interpolation	Respected		Respected		Respected		Respected		Respected		Respected	
Farrow 3rd order interpolation	Respected		Respected		Respected		Respected		Respected		Respected	

Comparing the results obtained in simulation, it is possible to assume that the errors committed using the Farrow interpolation algorithm are comparable, on the basis of function order, number of points after interpolation and sampling frequency, to the errors obtained using the Lagrange algorithm. Because of the computational cost of the Farrow algorithm, that is really lower than the Lagrange one, Farrow algorithm has been chosen for the implementation on the microcontroller device for real test, in order to verify the correspondence between the behaviour of the errors in simulation with a PC-based instrument and in real condition using a low-cost device.

For what concerns the classification of the instrument, the tests provided indications about the possibility of having an A – Class instrument, even with the lower sampling frequency. To verify this possibility, the algorithms have been rewritten for an on-board implementation in a low-cost microcontroller board, to simulate a PQ meter, and tested in different conditions (see Chapter 4).

3.5 Grouping and smoothing

The groping algorithm has been implemented in LabVIEW Virtual Instrument firstly used only for error comparison, refreshing the block diagram reported in Fig. 3. 16 , as showed below.

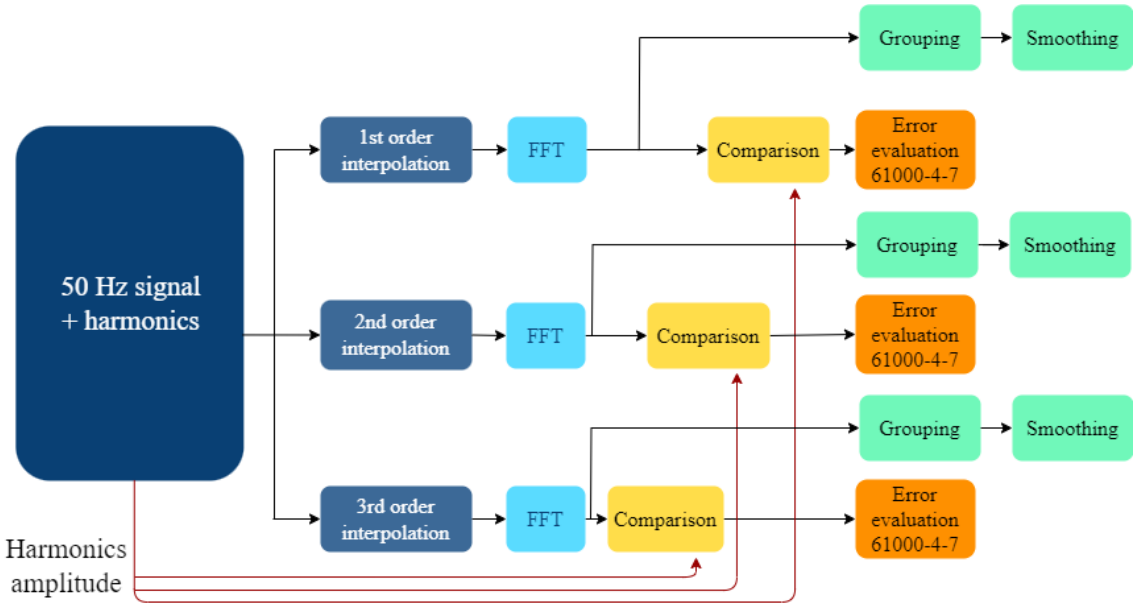

Fig. 3. 17 - Block diagram of LabVIEW VI for interpolation algorithms comparison and grouping/smoothing operation

In Fig. 3. 18 is possible to observe the grouped harmonic components of the signal used for the previous test, for the Case 2 (sampling frequency equal to 24 kSa/s and 2048 points after the interpolation, using in this example the first order Farrow algorithm for the interpolation) compared with the result of the FFT.

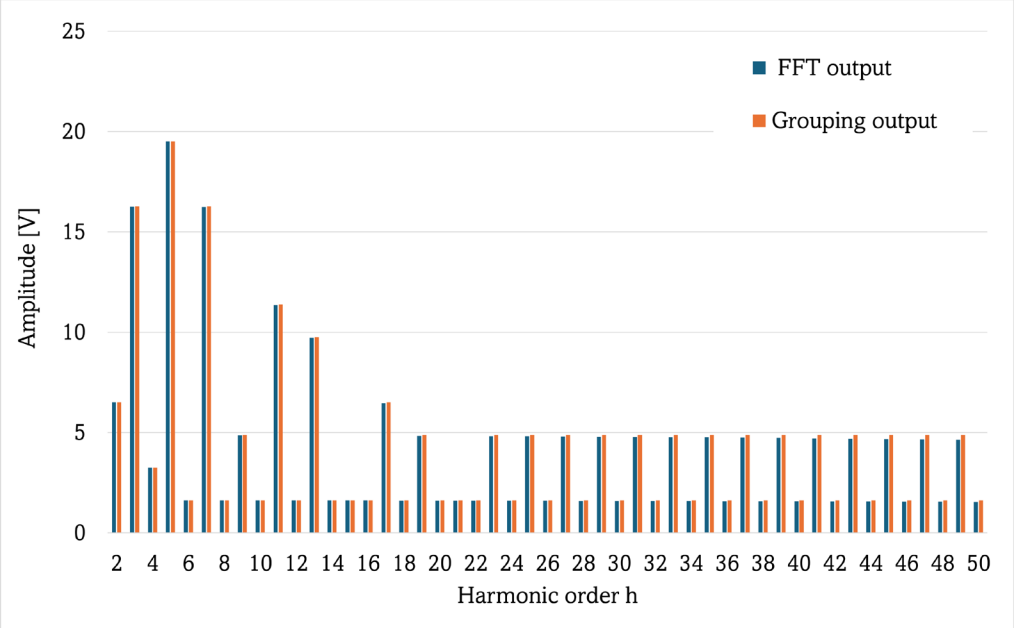

Fig. 3. 18 - RMS value of h-order harmonic component before (Yc,h) and after (Ygrouped,h) grouping

After grouping, the standard imposes to smooth the signal using a smooth digital filter, equivalent of a first order low-pass filter. Typically, the voltage (and current) spectral contents fluctuate during monitoring, causing variations in all groups values. To address this, a smoothing algorithm has been implemented utilizing the histories of groups values.

Filter time constant is equal to 1.5 s. The input of the filter is the grouped value $Y_{grouped,h}$. Coefficients α and β of the filter are reported in Table 1. 2 and depend on the fundamental frequency of the signal f_1 and the number of fundamental periods in the observation window *N*. For this application, $N = 10$ and $f_1 = 50\,Hz$ is set, so the values of the coefficients are $\alpha = 8.012$ and $\beta = 7.012$.

The scheme of the filter is reported in

Fig. 1. 9. The filter has been realized using the transfer function *G*:

$$G = \frac{Y_{smoothed,h}}{Y_{grouped,h}} = \frac{1}{\alpha - \beta z^{-1}} \quad [3.\ 3]$$

This post-processing involves 15 consecutive values, which are updated either with each FFT window (every 200 ms) in a time-aggregation set, with two different possibility, according to standard:

- cycle integration (fifteen 10/12-cycles intervals, respectively for 50/60 Hz systems),
- from cycle to time clock integration (10 min of 10/12-cycles intervals).

In Fig. 3. 19 the third harmonic value before and after smoothing operation is reported as example. For the first series of test, the stationary signal has been considered.

The case considered is Case 1 (sampling frequency equal to 16 kSa/s and 2048 points after the interpolation; first order Farrow algorithm for the interpolation). The input consists of 3 set of 15 observation windows with a total number of 45, to permit the filter to stabilize (time constant is 1.5 seconds; the filter is at steady state condition after 5 times the time constant i.e. 7.5 s; 45 observation windows are equal to 9 s). After that, to simulate the fluctuations of the signal, a variable value (lower than 1%) has been added to the stationary signal. The results are reported in Fig. 3. 19 and Fig. 3. 20 respectively.

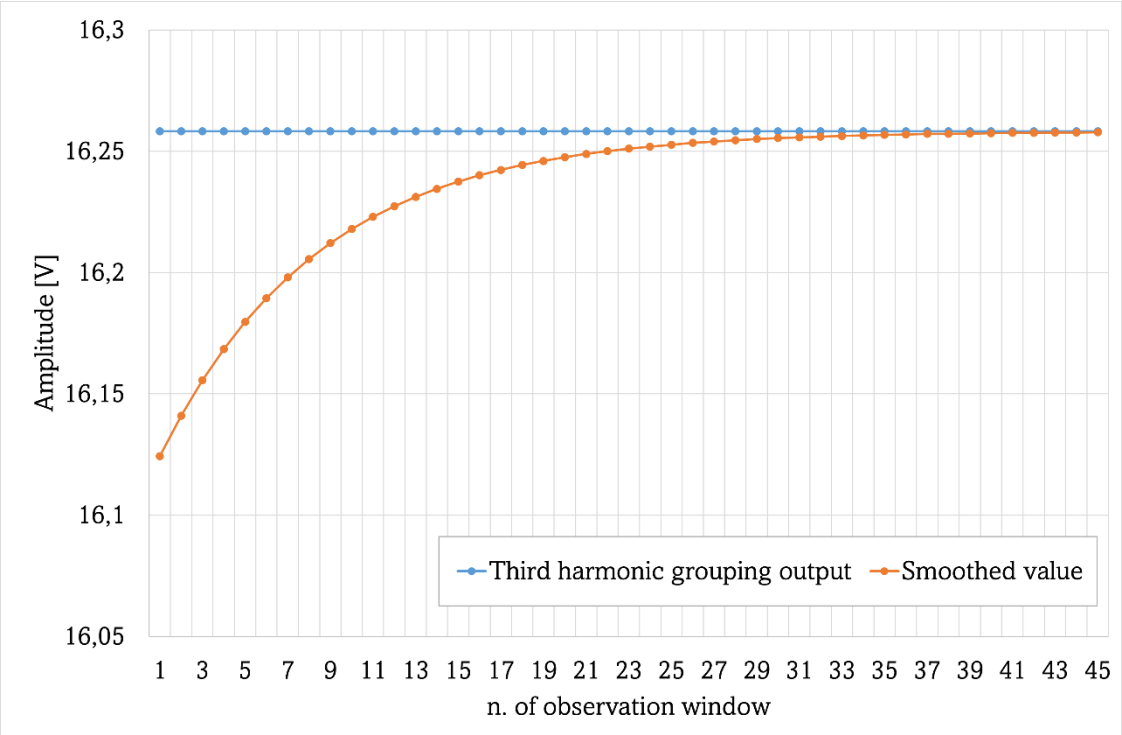

Fig. 3. 19 - Case 1 results (fs= 24 kSa/s and 2048 points after the interpolation; interpolation with first order Farrow algorithm); Grouping output and smoothing output for the third harmonic component. Stationary signal.

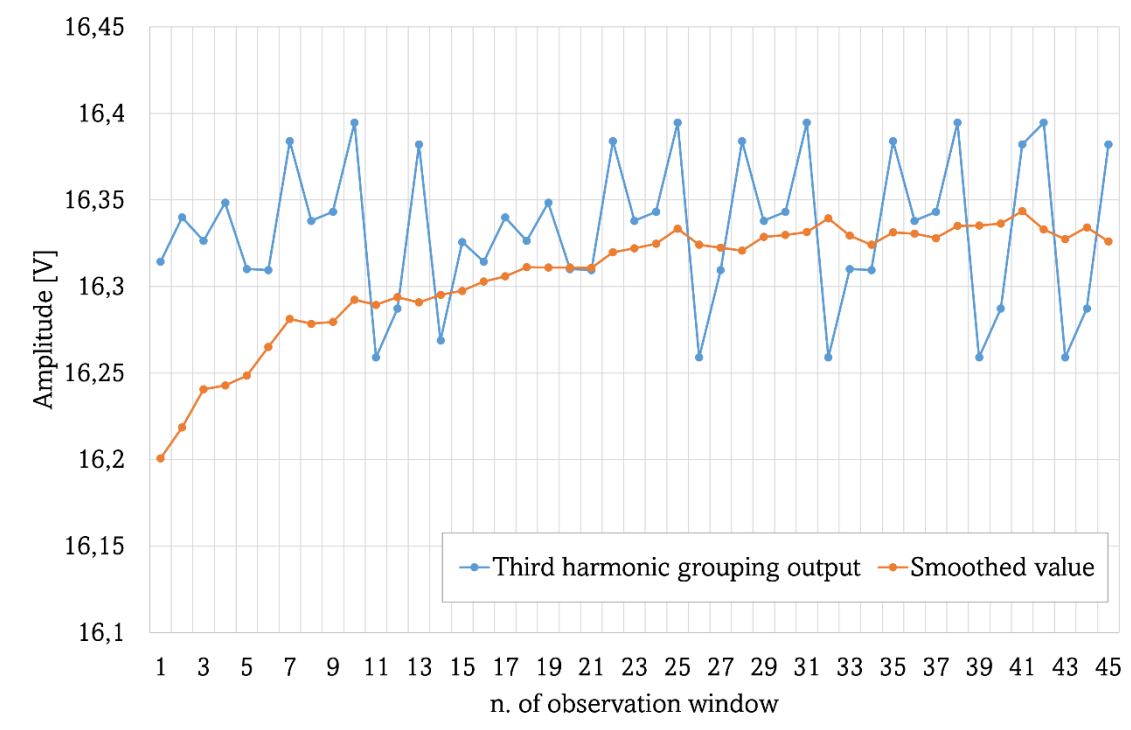

Fig. 3. 20 - Case 1 results (fs= 24 kSa/s and 2048 points after the interpolation; interpolation with first order Farrow algorithm); Grouping output and smoothing output for the third harmonic component. No stationary signal.

3.6 Results discussion

From the results obtained in simulation it is possible to extract some specifications that allow to outline some characteristics that a measuring instrument for harmonic analysis must have to be compliant with the requirements of A-class.

For what concerns the sampling frequency f_s, to maintain the synchronization error under the 0.03% limit, it must be higher than 10 kHz. This also allows, implicitly, to respect the Shannon theorem, since the device is required to sample signals up to 2500 Hz (50th harmonic of a signal at 50 Hz) and therefore a minimum f_s of 5 kHz is required.

The simulation tests also demonstrate that a first order interpolation function can only be used with a sampling frequency higher than 24 kHz. Because it is requested to investigate the possibility of performing a sampling with f_s in the range 16 - 32 kHz, also preventing a worsening of the results, in terms of accuracy, in the transition from simulation to implementation on a low-cost device, it is believed that for interpolation a third-order algorithm is required. Moreover, comparing the results obtained with the Lagrange algorithm and with the Farrow algorithm, since the errors made are perfectly comparable, it was decided to use as algorithm the Farrow interpolator seen as the latter has a lower computational cost. Tests will be conducted using both 2048 and 4096 post-interpolation points.

For the memory required, the major part is used for the sample's storage. Interpolating to 2048 points, the accuracy results, obtained in simulations, appears the same of the 4096 cases but the FFT request half of the memory. For a low memory request, a 16 or 32 bit coding is requested.

4. IMPLEMENTATION OF METRICS ON LOW-COST DEVICES

After the test carried in simulations, the algorithms and the specifications chosen have been tested using real devices. First, a test benchmark for characterization has been realized using a NI9239 board as reference for the sampling and a VI in LabVIEW for the elaboration. The algorithms to be tested have been implemented on a microcontroller board chosen as test product for its specifications.

The results of the simulations carried out in previous chapter showed that a minimum sampling frequency of 10 kHz is required and, using a 16 bit coding, a minimum of 29 kbytes memory is required to test all the cases simulated. For a 32 bit coding, 57 kbytes are required. The tests conducted in simulation were useful to define some minimum specifications but did not allow to evaluate all aspects. It was therefore necessary to implement the metrics on a microcontroller device and test it under real operating conditions. Since the goal of the project is to explore the feasibility of using a low-cost device as a PQ measurement instrument of A-Class, it was decided to start from evaluating several commercial products already available and verify that, on them, the proposed metrics were functional in accordance with the requirements of the standard.

The first considered board was the STCOMET, as it was previously used for the implementation of measurement metrics, albeit for several purposes. This board has a direct 230 V input voltage with a 24-bit $\Sigma\Delta$ converter. The main limitation of the board, however, is the fixed sampling frequency that is equal to 7812,5 Hz and does not allow to use it as a test device for an instrument that respects the A-Class.

The second device is the NUCLEO-64 STM32F404. This board has an 84 MHz M4 core and finely variable sampling rate, with 12-bit ADC. In addition, there will be a flash memory of 251 kbytes and 96 kbytes of SRAM.

Finally, the NUCLEO STM32F767ZI device was considered; it has a M7 core and a 12-bit ADC with 0-3.3 V input range, and a maximum CPU frequency of 216 MHz. The device incorporates high-speed embedded memories with a flash up to 2 Mbytes, 512 kbytes of SRAM.

Since these last two devices are equipped with the same AD converter, considering the low price difference between the two, it was decided to use the second. In fact, it has a greater memory, necessary (as explained below) to acquire a sufficient number of samples to implement different solutions, as well as a greater clock frequency that allows processing data in less time, making this solution suitable for gapless sampling.

4.1 Development and characterization of the measurement system

4.1.1 ADC characterization

First tests conducted on the microcontroller board were finalized to characterize the analog-to-digital converter (ADC) of the board.

The selected board for this study is the NUCLEO STM32F767ZI, described in previous paragraph. This device has been selected because it is very close to the concept of low-cost device to be develop, while having a fairly high memory buffer and providing the possibility to vary the sampling frequency and the internal structure of the code for memory allocation, thus allowing its use in different configurations, to carry out all the necessary tests.

To compare the results obtained with a more accurate instrument, the same signal is acquired and processed using a performant device, the NI 9239, with a 24-bit ADC, -10/+10 V input range and a sampling frequency scalable from a maximum value of 12.8 MHz. The samples are sent to a VI (Virtual Instrument) in LabVIEW to perform the interpolation and the FFT, providing the reference for the error on harmonic components measurement determination.

For the generation of the reference signals, two calibrators (a Fluke 5720A for tests with sinusoidal signal and a Fluke 6100A for the generation of distorted signals) have been used, coupled with a Precision Ratio Transformer TEGAM PRT73, used as voltage divider to adapt the voltage signal to the board. A Tektronix AFG31152 signal generator was used to generate a DC voltage, added to the reference signal to adapt it to the ADC's input range of 0-3.3 V. An op-amp circuit has been used for a decoupling between the signal generator and the calibrator, so to avoid over-currents circulation (above the allowable limits for power calibrator output currents). An RC low pass filter was also added at op-amp output, to reduce high frequency noise and prevent aliasing phenomenon. The scheme of the test bench is reported in Fig. 4. 1.

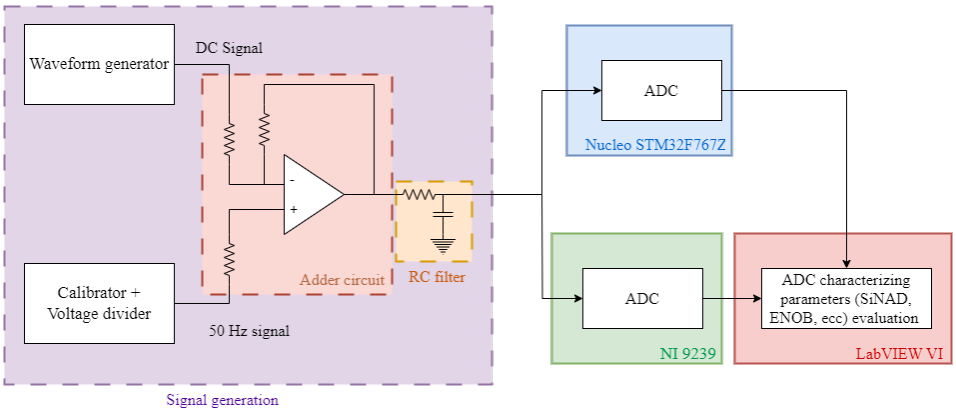

Fig. 4. 1 - Test bench system scheme for characterization of ADC

The initial test involves a basic configuration, consisting of three distinct sampling frequencies (16, 24, and 32 kHz). Because of the instability of the sampling frequency, even measuring exactly the frequency of the signal, it was not possible to determinate the exact number of points of an integer period to be sampled to have a synchronous sampling; for this reason, a Zero-Cross (ZC) function has been implemented.

This setup aims to analyse a 50 Hz sinusoidal signal within a 200 ms observation window and evaluate four parameters: ENOB, SiNAD, SFDR, and THD, other than amplitude.

In particular, the quantities evaluated are defined as:

- SiNAD (Signal to noise and distortion), expressed in dB, is the ratio of the rms signal amplitude to the mean value of the root-sums quare (rss) of all other spectral components, including harmonics:

$$SiNAD = 20\log\left(\frac{U_1}{\sqrt{U_2^2 + U_3^2 + \cdots U_n^2 + U_{noise}^2}}\right) \quad [4.\ 1]$$

- The effective number of bits (ENOB) is the equivalent number of bits of the ADC when both noise and distortion are considered. In fact, the resolution of a converter is specified by the number of bits used to represent the input analog value. However, real signals have noise, and real circuits are not perfect and can introduce additional noise and distortion to the signal. In fact, the ENOB is directly linked to the SiNAD value. Those imperfections reduce the number of bits of accuracy in the ADC. The mathematical expression of the ENOB is:

$$ENOB = \frac{SiNAD(dB) - 1.76}{6.02} \quad [4.\ 2]$$

- The Spurious Free Dynamic Range (SFDR) is defined as the ratio of the rms signal amplitude to the rms value of the highest spurious spectral content measured over the bandwidth of interest:

$$SFDR = 20\log\left(\frac{RMS_{signal}}{RMS_{higher\ amplitud\ harmonic}}\right) \quad [4.\ 3]$$

- Total harmonic distortion (THD) is the ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics (generally, only the first 5 are significant). THD of an ADC is generally specified with the input signal close to full-scale, although it can be specified at any level. THD expression is:

$$THD = 20\log\left(\frac{\sqrt{U_2^2 + U_3^2 + \cdots U_n^2 +}}{U_1}\right) \quad [4.\ 4]$$

To respect the dynamic range of the ADC, the signal is scaled to be adapted at the ADC input range (0-3.3 V).

The results are presented in the tables provided below. The results obtained in those tests show a severe loss of information of the signal, with a value of ENOB equal to quite 5 units under the real value of ADC number of bits.

Table 4. 1 - ADC characterization

fs [kHz]	N. of points	SINAD [dB]	ENOB [bit]	THD [dB]	SFDR [dB]	FFT amplitude [V]
16	2048	43,876	6,996	-63,290	55,694	1,6478
24		44,168	7,040	-65,046	62,209	1,6481
32		45,138	7,205	-63,909	64,785	1,6482
16	4096	45,015	7,180	-65,820	64,438	1,6469
24		45,070	7,188	-64,912	65,287	1,6430
32		44,880	7,162	-66,080	68,860	1,6485

For what concern the sampling frequency, consecutive acquisitions of a sinusoidal 50 Hz signal (generated with the calibrator) have been repeated to evaluate the variability of the imposed sampling frequency. In fact, using a ZC algorithm to be sure to acquire 10 integer period of the signal, the number of samples N only depend from the value of f_s. In Table 4. 2 the results for the case of f_s imposed equal to 24 kHz are reported.

The results confirm what described in previous chapter and reiterate the need of the interpolation algorithm to obtain a number of points equal to a power of 2 for the efficient implementation of the FFT, because of the impossibility to adapt the sampling frequency to the signal frequency.

Table 4. 2 - fs variability evaluation

Test	fs imposed [kHz]	n. of samples expected in 200 ms observation window	fs measured [kHz]	n. of samples acquired in 200 ms observation window
1	24	4800	24,113	4823
2	24	4800	24,005	4801
3	24	4800	24,082	4816
4	24	4800	24,032	4806
5	24	4800	23,952	4790
6	24	4800	24,008	4802
7	24	4800	24,012	4802
8	24	4800	23,996	4799
9	24	4800	24,067	4813
10	24	4800	24,07	4814

4.1.2 Algorithms characterization

Other than the variability introduced by transducers and conditioning accessories, the precision of measurement relies on both the hardware parts of the metering device and the software aspects (such as signal conditioning algorithms and harmonic analysis).

After ADC characterization, to seclude the contribute to the error of the interpolation algorithm in the harmonic detection, the Farrow algorithm has been implemented on the board and tested using as input an ideal signal generated in LabVIEW (230 V, 50 Hz sinusoidal signal + harmonics up to 50th; the amplitude of the harmonics is set as reported in Table 3. 1), excluding the ADC contribute. Then the FFT is processed, and the output results are compared to the LabVIEW original signal components. The same ideal signal is processed in LabVIEW with the interpolation (of the same order and to the same number of points used in Nucleo) and the spectral analysis.

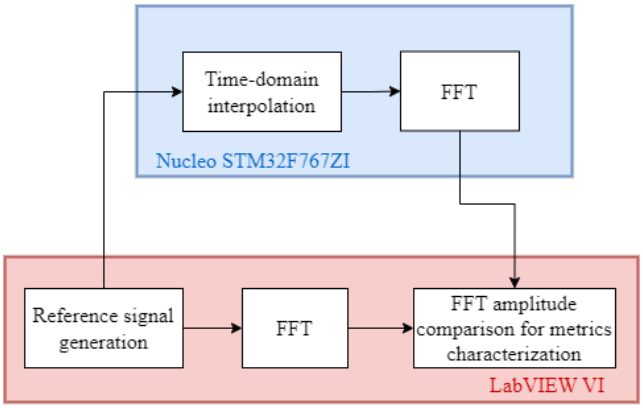

Fig. 4. 2 - Bench test system scheme for algorithms characterization

The errors are calculated as difference between the amplitude of the spectral analysis results and the set values. The graphic results for the cases of f_s = 16, 24 and 32 kHz with interpolation to 2048 points are reported. For the cases with 4096 points the errors are comparable. The FFT algorithm can be excluded too from this contribute, because of the use of an ARM function from CMSIS, that guarantees high precision. The results obtained are summarized in Table 4. 3.

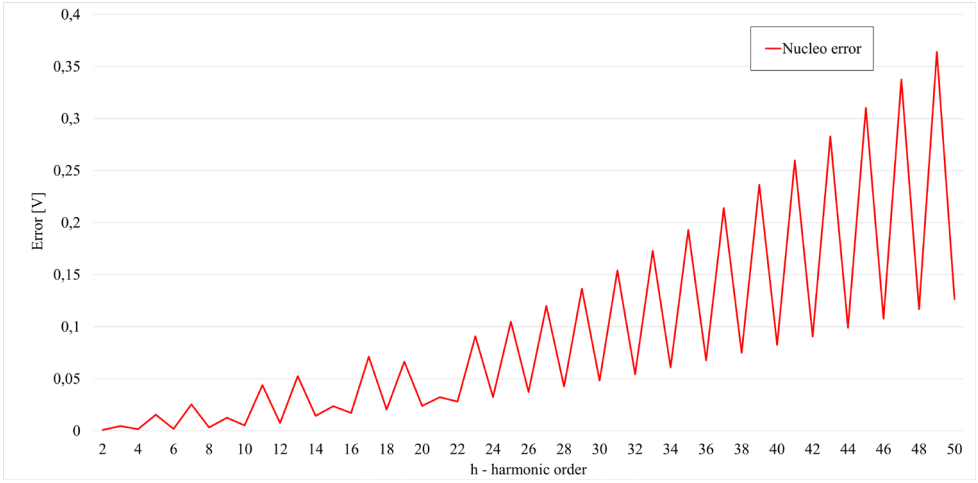

Fig. 4. 3 - Error committed in harmonics detection - fs=16 kHz, interpolation to 2048 points

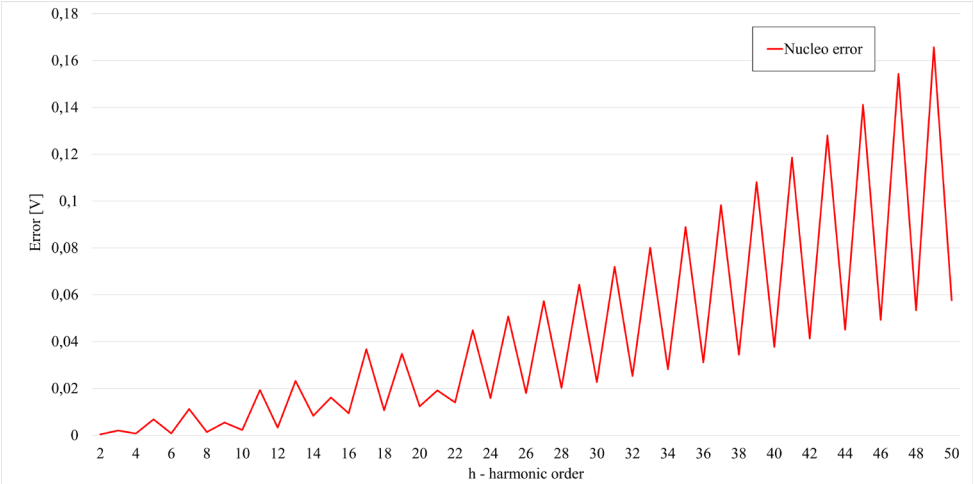

Fig. 4. 4 - Error committed in harmonics detection - fs=24 kHz, interpolation to 2048 points

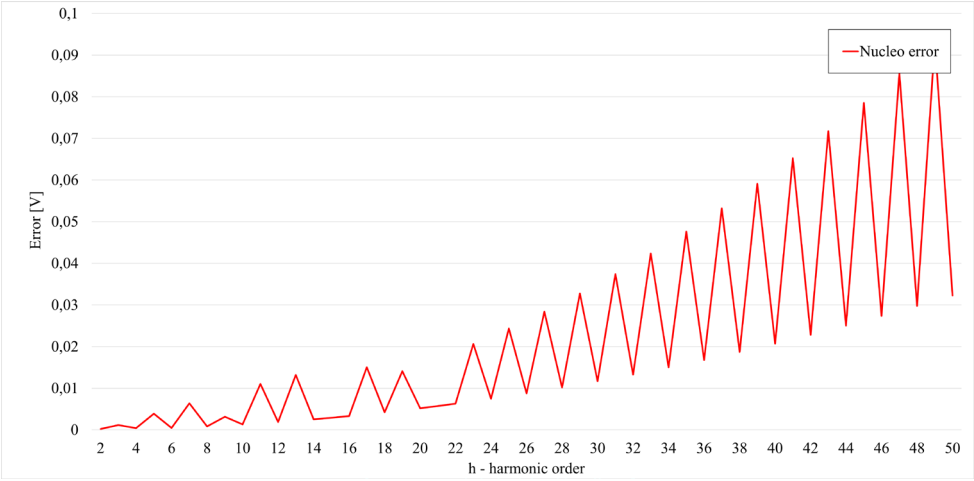

Fig. 4. 5 - Error committed in harmonics detection - fs=32 kHz, interpolation to 2048 points

Table 4. 3 - Error committed in harmonics detection

Harmonic order	Error [V]					
	fs = 16 kHz; 2048 points after interp.	fs = 24 kHz; 2048 points after interp.	fs = 32 kHz; 2048 points after interp.	fs = 16 kHz; 4096 points after interp.	fs = 24 kHz; 4096 points after interp.	fs = 32 kHz; 4096 points after interp.
2	0,0008	0,0004	0,0002	0,0008	0,0003	0,0002
3	0,0047	0,0020	0,0012	0,0046	0,0020	0,0011
4	0,0017	0,0007	0,0004	0,0016	0,0007	0,0004
5	0,0156	0,0068	0,0039	0,0153	0,0067	0,0038
6	0,0019	0,0008	0,0005	0,0018	0,0008	0,0005
7	0,0255	0,0112	0,0064	0,0250	0,0110	0,0062
8	0,0033	0,0014	0,0008	0,0033	0,0014	0,0008
9	0,0126	0,0054	0,0032	0,0124	0,0053	0,0031
10	0,0052	0,0022	0,0013	0,0051	0,0022	0,0013
11	0,0440	0,0193	0,0110	0,0431	0,0189	0,0108
12	0,0075	0,0032	0,0019	0,0073	0,0032	0,0018
13	0,0527	0,0232	0,0132	0,0516	0,0227	0,0129
14	0,0144	0,0083	0,0025	0,0141	0,0082	0,0025
15	0,0238	0,0161	0,0029	0,0233	0,0158	0,0029
16	0,0172	0,0094	0,0033	0,0168	0,0092	0,0033
17	0,0712	0,0368	0,0150	0,0698	0,0360	0,0147
18	0,0204	0,0107	0,0042	0,0200	0,0105	0,0041
19	0,0665	0,0348	0,0141	0,0652	0,0341	0,0138
20	0,0240	0,0124	0,0052	0,0236	0,0121	0,0051
21	0,0324	0,0191	0,0057	0,0318	0,0187	0,0056
22	0,0281	0,0140	0,0063	0,0275	0,0137	0,0062
23	0,0908	0,0448	0,0206	0,0890	0,0439	0,0202
24	0,0326	0,0159	0,0075	0,0319	0,0156	0,0073
25	0,1048	0,0508	0,0243	0,1028	0,0497	0,0239
26	0,0374	0,0180	0,0088	0,0367	0,0176	0,0086
27	0,1201	0,0572	0,0284	0,1177	0,0561	0,0278
28	0,0427	0,0202	0,0102	0,0419	0,0198	0,0100
29	0,1365	0,0643	0,0327	0,1338	0,0630	0,0321
30	0,0484	0,0227	0,0117	0,0474	0,0222	0,0114
31	0,1541	0,0719	0,0374	0,1510	0,0705	0,0367
32	0,0545	0,0253	0,0133	0,0534	0,0248	0,0130
33	0,1729	0,0801	0,0424	0,1695	0,0785	0,0415
34	0,0609	0,0281	0,0150	0,0597	0,0276	0,0147
35	0,1929	0,0889	0,0476	0,1891	0,0871	0,0467
36	0,0678	0,0312	0,0168	0,0664	0,0305	0,0165
37	0,2141	0,0982	0,0532	0,2098	0,0962	0,0521
38	0,0750	0,0344	0,0187	0,0735	0,0337	0,0183
39	0,2364	0,1081	0,0591	0,2317	0,1059	0,0579
40	0,0827	0,0378	0,0207	0,0810	0,0370	0,0203
41	0,2599	0,1186	0,0653	0,2547	0,1162	0,0640
42	0,0907	0,0413	0,0228	0,0889	0,0405	0,0224
43	0,2828	0,1280	0,0718	0,2771	0,1255	0,0703
44	0,0991	0,0451	0,0250	0,0971	0,0442	0,0245
45	0,3102	0,1411	0,0785	0,3040	0,1383	0,0770
46	0,1078	0,0492	0,0273	0,1057	0,0482	0,0268
47	0,3375	0,1543	0,0856	0,3308	0,1512	0,0839
48	0,1169	0,0533	0,0298	0,1146	0,0523	0,0292
49	0,3640	0,1656	0,0930	0,3567	0,1623	0,0911
50	0,1264	0,0577	0,0323	0,1239	0,0565	0,0316

4.1.3 Experimental setup validation

After ADC and metrics characterization, in order to develop and characterize the measurement system, with all the aspects it embraces, different evaluation tests have been conducted. To validate the results obtained in simulation, the interpolation algorithms and the FFT were implemented on a commercial low-cost microcontroller board, in order to process a complete harmonic analysis and evaluate the performance of the device. The setup is described in Fig. 4. 6 and a test bench photo is reported in Fig. 4. 8.

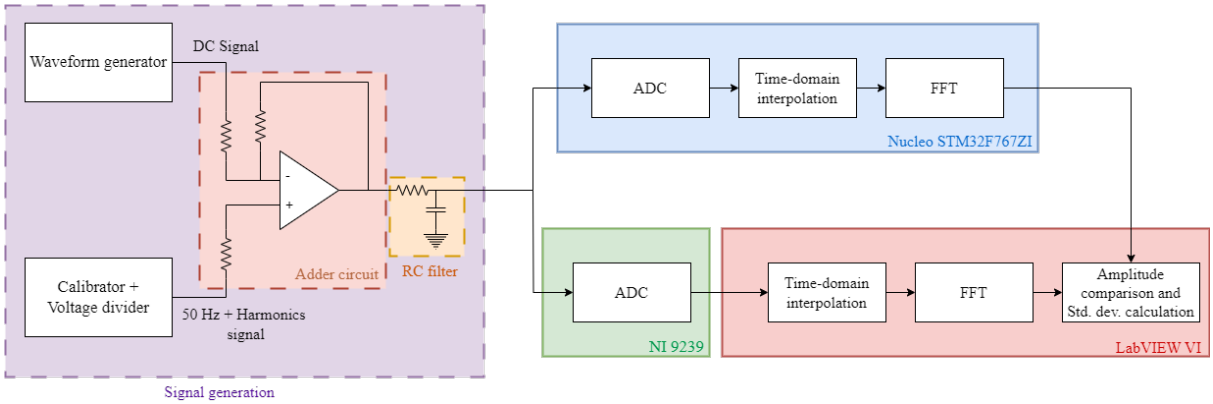

Fig. 4. 7 - Bench test system scheme

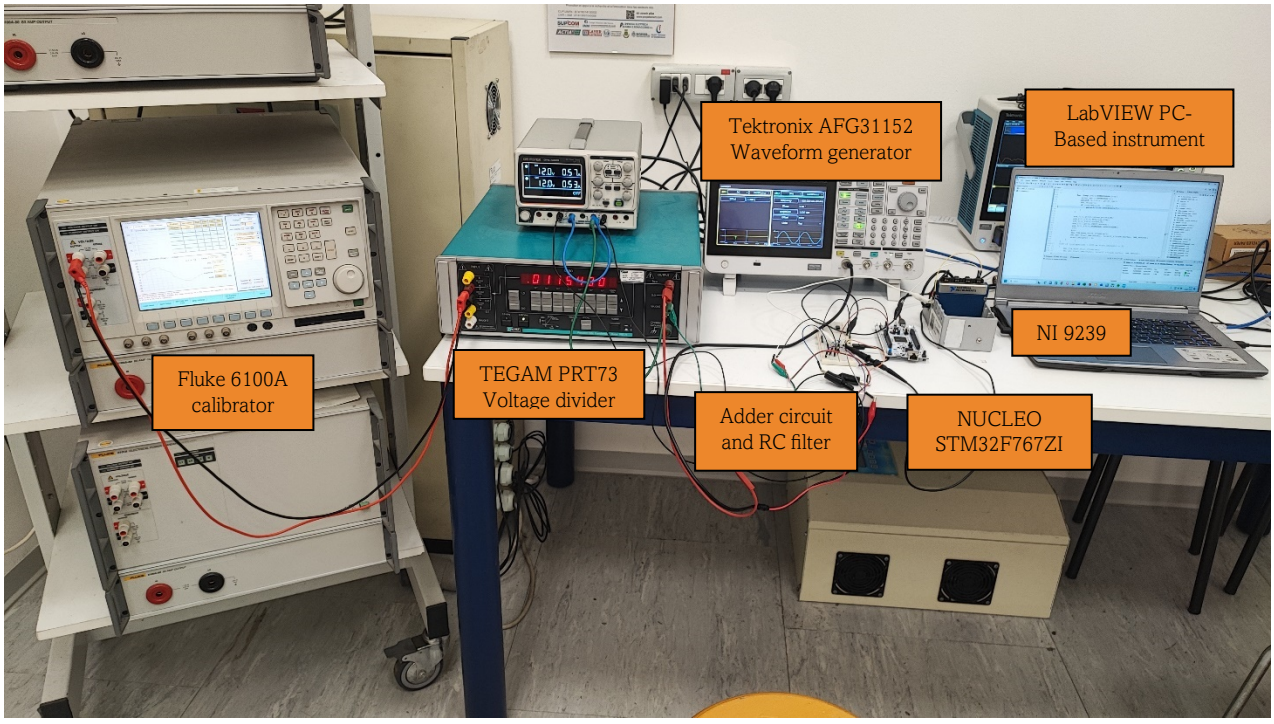

Fig. 4. 8 - Photo of the test bench

The voltage test signal, generated with calibrator, has the same features as the one presented in chapter 3, created starting from standard IEC 50160 and reported in Fig. 3. 2. The tests with the microcontroller board were carried out with three different values of f_s (16, 24, and 32 kHz) and a number of points after the interpolation equal to 2048 and 4096 points. The spectral analysis results were compared with those obtained with the PC-based instrument, using the NI board for sampling. For NI 9239 the values of sampling frequencies set for the Nucleo were not exactly allowed, since only values equal to $f_s = f_M/(256 \cdot n)$ can be set, where f_M is the DAQ time base (12.8 MHz) and n can

be an integer number, starting from 1. For this reason, sampling frequencies set in NI 9239 are equal to 16.67, 25 and 33,34 kHz. The signal was sampled for 200 ms (amplitude of observation window T_W equal to 10 time the fundamental period $T_1 = 10 \cdot 20\ ms$). For every harmonic component, the phase was equal to zero.

In those tests, mean value and standard deviation, for each harmonic, is calculated. The graphic results are reported in figures from Fig. 4. 9 to Fig. 4. 14. The tested cases are summarized in Table 4. 4.

Table 4. 4 - Tested cases

Case	fs [kHz]	Points after interpolation
1	16	2048
2	24	
3	32	
4	16	4096
5	24	
6	32	

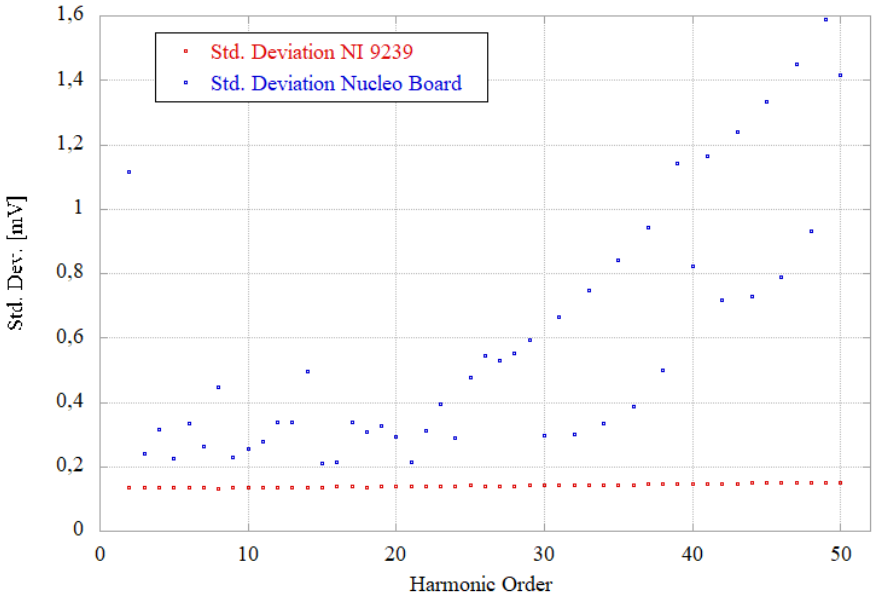

Fig. 4. 9 - Standard deviation comparison of Nucleo board and NI 9239 board - Case 1 - fs=16 kHz, interpolation to 2048 points

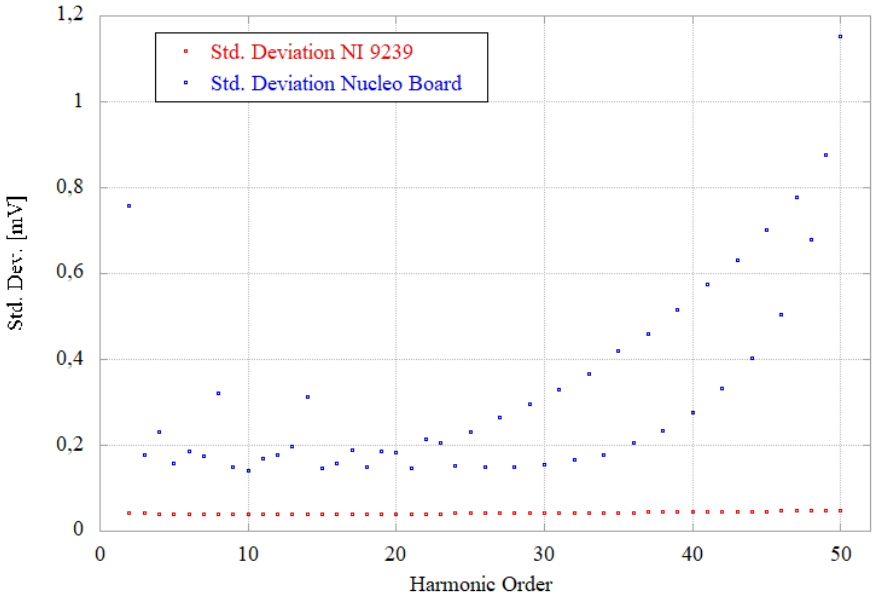

Fig. 4. 10 - Standard deviation comparison of Nucleo board and NI 9239 board - Case 2 - fs= 24 kHz, interpolation to 2048 points

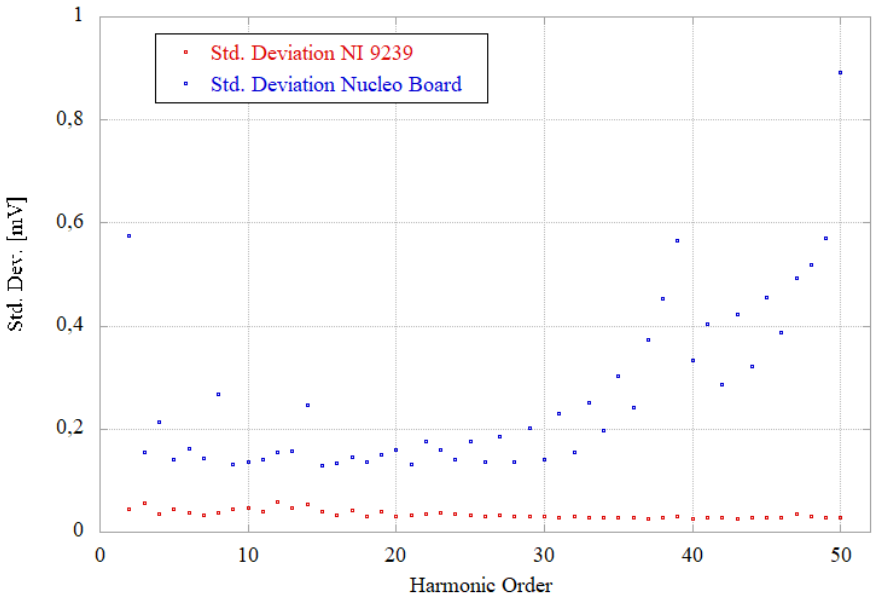

Fig. 4. 11 - Standard deviation comparison of Nucleo board and NI 9239 board - Case 3 - fs= 32 kHz, interpolation to 2048 points

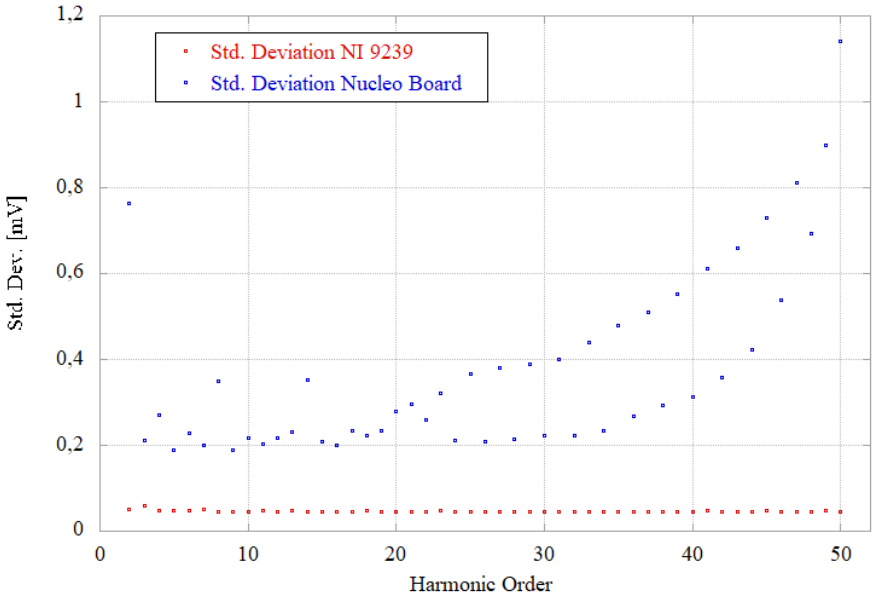

Fig. 4. 12 - Standard deviation comparison of Nucleo board and NI 9239 board - Case 4 - fs=16 kHz, interpolation to 4096 points

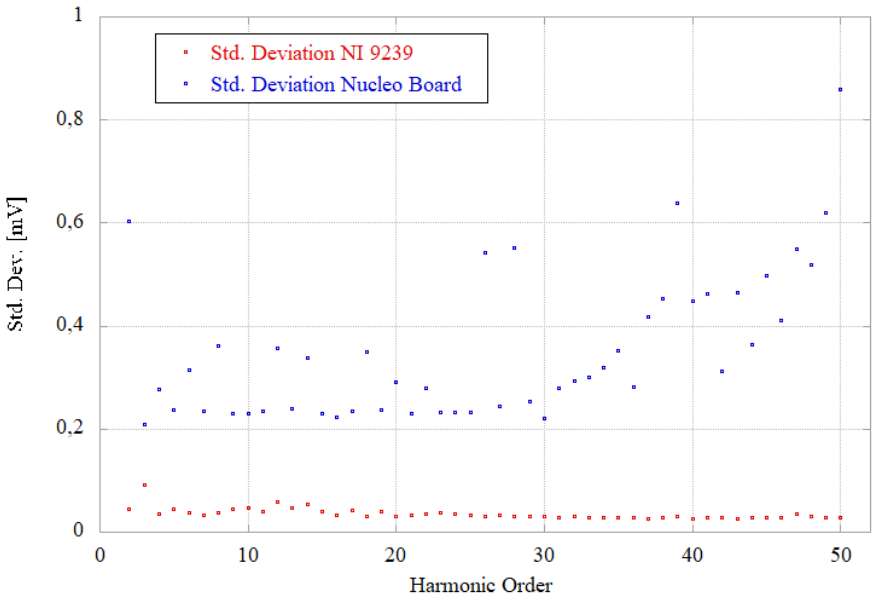

Fig. 4. 13 - Standard deviation comparison of Nucleo board and NI 9239 board - Case 5 - fs= 24 kHz, interpolation to 4096 points

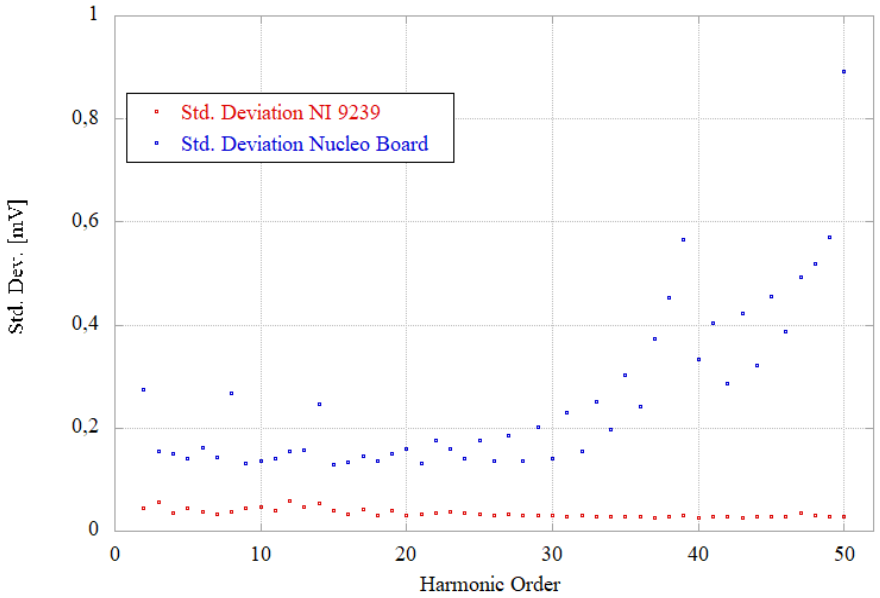

Fig. 4. 14 - Standard deviation comparison of Nucleo board and NI 9239 board - Case 6 - fs= 32 kHz, interpolation to 4096 points

Table 4. 5 - Amplitude comparison of cases 1-6 (Table 4. 4 - Tested cases)

Harmonic order h	FFT amplitude results [V]						
	NI 9239 Fs = 50 kHz	Nucleo board					
		Case 1 fs = 16 kHz; 2048 points	Case 2 fs = 24 kHz; 2048 points	Case 3 fs = 32 kHz; 2048 points	Case 4 fs = 16 kHz; 4096 points	Case 5 fs = 24 kHz; 4096 points	Case 6 fs = 32 kHz; 4096 points
2	0,0316	0,0316	0,0317	0,0315	0,0316	0,0316	0,0316
3	0,0789	0,0790	0,0795	0,0796	0,0789	0,0791	0,0795
4	0,0158	0,0158	0,0158	0,0157	0,0158	0,0158	0,0158
5	0,0946	0,0947	0,0949	0,0949	0,0947	0,0949	0,0949
6	0,0079	0,0080	0,0079	0,0079	0,0079	0,0079	0,0079
7	0,0788	0,0787	0,0789	0,0790	0,0786	0,0788	0,0791
8	0,0079	0,0080	0,0079	0,0079	0,0079	0,0080	0,0079
9	0,0237	0,0236	0,0237	0,0239	0,0235	0,0237	0,0238
10	0,0079	0,0080	0,0079	0,0079	0,0079	0,0080	0,0079
11	0,0552	0,0548	0,0551	0,0552	0,0547	0,0550	0,0552
12	0,0079	0,0079	0,0079	0,0078	0,0079	0,0079	0,0079
13	0,0473	0,0466	0,0472	0,0471	0,0466	0,0470	0,0473
14	0,0079	0,0079	0,0078	0,0078	0,0078	0,0079	0,0079
15	0,0079	0,0078	0,0078	0,0079	0,0077	0,0078	0,0080
16	0,0079	0,0078	0,0077	0,0078	0,0078	0,0079	0,0078
17	0,0315	0,0310	0,0313	0,0314	0,0309	0,0313	0,0315
18	0,0079	0,0078	0,0078	0,0078	0,0078	0,0079	0,0079
19	0,0236	0,0231	0,0235	0,0235	0,0230	0,0234	0,0237
20	0,0079	0,0078	0,0078	0,0078	0,0077	0,0078	0,0079
21	0,0079	0,0078	0,0078	0,0079	0,0077	0,0078	0,0079
22	0,0079	0,0077	0,0078	0,0078	0,0077	0,0078	0,0079
23	0,0236	0,0230	0,0234	0,0234	0,0229	0,0234	0,0236
24	0,0079	0,0077	0,0078	0,0078	0,0076	0,0078	0,0079
25	0,0236	0,0228	0,0234	0,0234	0,0227	0,0233	0,0235
26	0,0079	0,0076	0,0078	0,0078	0,0076	0,0078	0,0079
27	0,0236	0,0226	0,0234	0,0234	0,0225	0,0232	0,0235
28	0,0079	0,0075	0,0078	0,0078	0,0075	0,0077	0,0078
29	0,0236	0,0223	0,0234	0,0233	0,0223	0,0231	0,0235
30	0,0079	0,0074	0,0078	0,0078	0,0074	0,0077	0,0078
31	0,0236	0,0221	0,0234	0,0234	0,0221	0,0230	0,0235
32	0,0079	0,0074	0,0077	0,0078	0,0073	0,0076	0,0078
33	0,0236	0,0219	0,0233	0,0233	0,0218	0,0228	0,0235
34	0,0079	0,0073	0,0078	0,0078	0,0072	0,0076	0,0078
35	0,0236	0,0216	0,0233	0,0233	0,0215	0,0227	0,0235
36	0,0079	0,0072	0,0077	0,0077	0,0072	0,0076	0,0078
37	0,0236	0,0213	0,0233	0,0232	0,0212	0,0225	0,0234
38	0,0079	0,0071	0,0077	0,0077	0,0070	0,0075	0,0078
39	0,0236	0,0209	0,0232	0,0232	0,0209	0,0224	0,0234
40	0,0079	0,0069	0,0077	0,0077	0,0069	0,0074	0,0078
41	0,0236	0,0206	0,0232	0,0232	0,0206	0,0222	0,0234
42	0,0079	0,0068	0,0077	0,0077	0,0068	0,0074	0,0078
43	0,0236	0,0202	0,0232	0,0232	0,0202	0,0220	0,0234
44	0,0079	0,0067	0,0078	0,0077	0,0067	0,0073	0,0078
45	0,0236	0,0198	0,0231	0,0231	0,0198	0,0218	0,0233
46	0,0079	0,0065	0,0078	0,0077	0,0065	0,0072	0,0078
47	0,0236	0,0194	0,0230	0,0231	0,0193	0,0215	0,0233
48	0,0079	0,0064	0,0078	0,0077	0,0064	0,0071	0,0079
49	0,0236	0,0187	0,0230	0,0230	0,0187	0,0211	0,0233
50	0,0079	0,0062	0,0079	0,0077	0,0062	0,0070	0,0079

As known, in the case of a stationary signal, the stability of the measuring system can be assessed analysing the standard deviation. Since the previously characterized metrics gave solid results, in terms of accuracy and stability, these tests show that the ADC of the Nucleo board under consideration is actually not stable, introducing a not negligible variability in the final result. The comparison is made with the NI9239 board which, has a much more stable behaviour as predictable.

4.2 Experimental tests with low-cost device – harmonics measurement error

To evaluate the performance of the device chosen for the implementation of the chosen PQ metrics, a measurement chain was first implemented, including the acquisition of a 200 ms portion of signal and a complete harmonic analysis, according to the requirements of the standard IEC 61000-4-7. For all the test conducted, total processing time $(T_{process})$ has been measured, to discharge the solutions with a $T_{process}$ higher than 200 ms that cannot be used for a gapless sampling device, for the reasons described in previous chapters. According to the standard, for a S-Class instrument, "at least one 10/12-cycle value shall be sampled each 50/60 cycles ". For a 50 Hz system, after 10 periods acquisition, 40 periods without sampling are allowed i.e. a total time of 800 ms (40 · 20 ms) is available for samples processing. The solutions tested that have a processing time higher than 800 ms are not compliance with S-Class requirements.

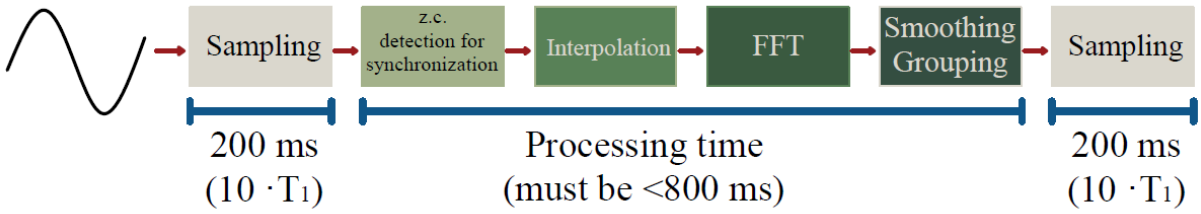

Fig. 4. 15 - Block scheme of measurement chain implemented on Nucleo board

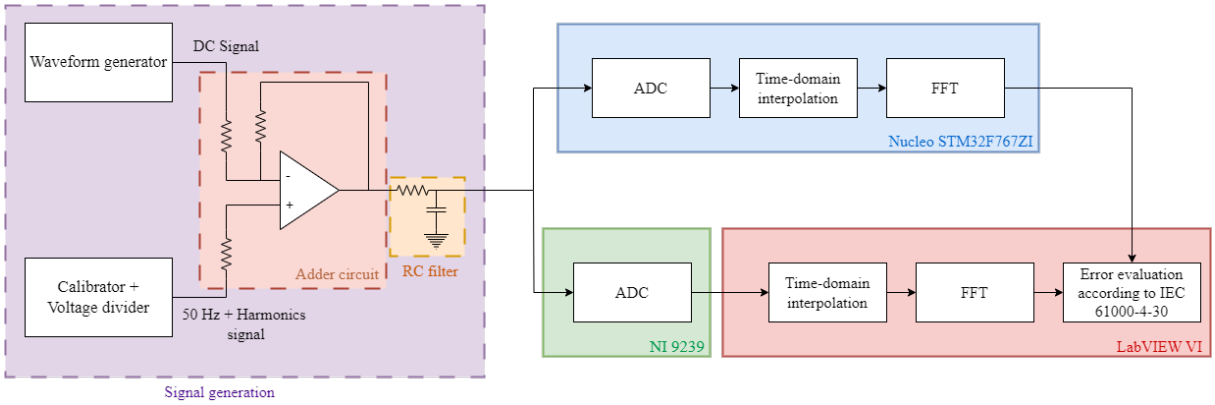

Fig. 4. 16 - Bench test system scheme for error evaluation

Testes for harmonic measurement accuracy estimation have been conducted with the setup described in paragraph 4.1.3 and reported in Fig. 4. 8 [67]. The tests are the same simulated with LabVIEW software in previous chapter and summarized in Table 4. 4. The error committed in the measurement of every harmonic component is compared with the limit imposed by the standard for the A – Class instruments. The measurements have been repeated 1000 times; for each case, mean value, maximum, minimum and standard deviation of the error for each harmonic component have been determined. In the figures from Fig. 4. 17 to Fig. 4. 22 the mean value of the error is reported, along with standard deviation and maximum error.

For the interpolation of the points a third order Farrow algorithm has been used. To obtain the most accurate reference, the signal with the NI 9239 has been acquired at the maximum values of sampling frequencies to be set equal to 50 kSa/s.

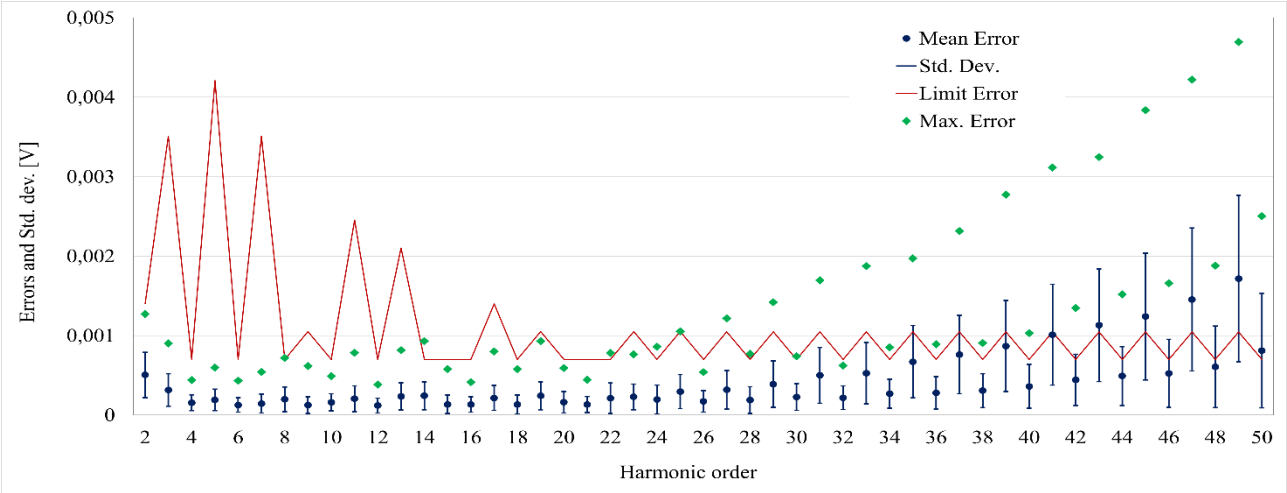

Fig. 4. 17- Error evaluation for Case 1 - fs= 16 kHz, interpolation to 2048 points

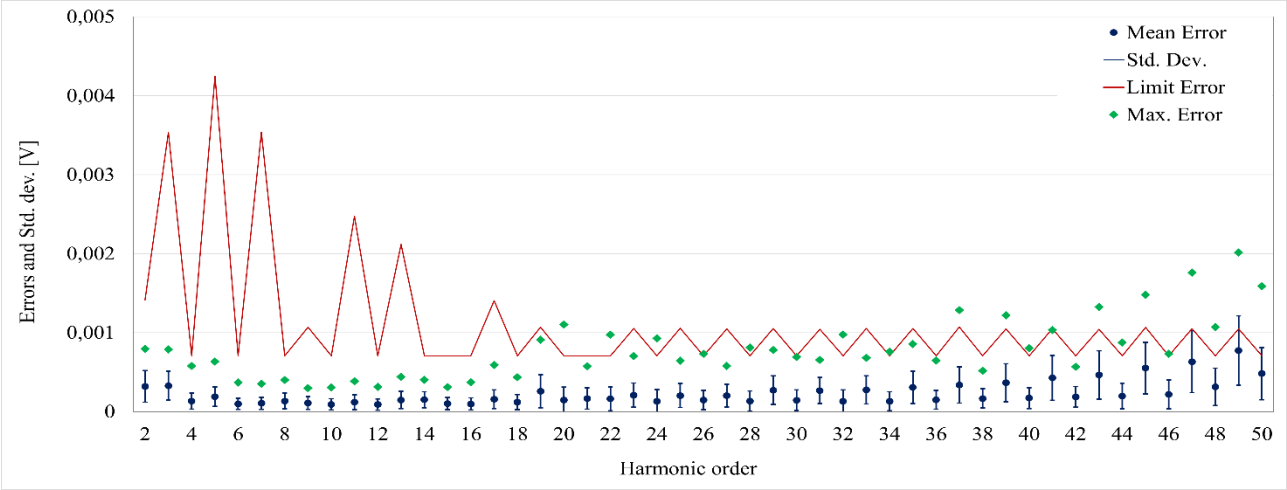

Fig. 4. 18 - Error evaluation for Case 2 - fs= 24 kHz, interpolation to 2048 points

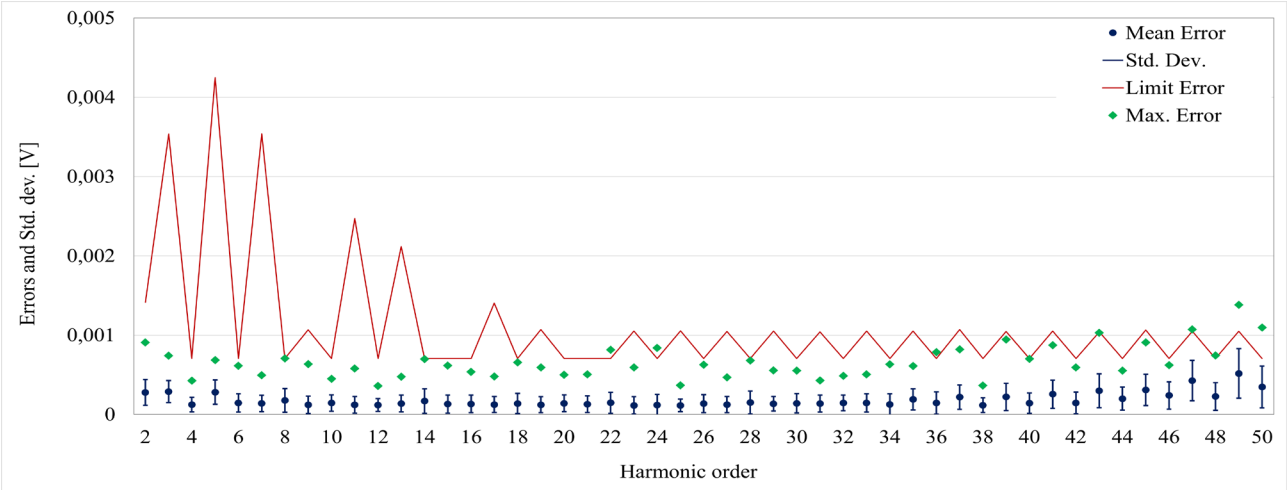

Fig. 4. 19 - Error evaluation for Case 3 - fs= 32 kHz, interpolation to 2048 points

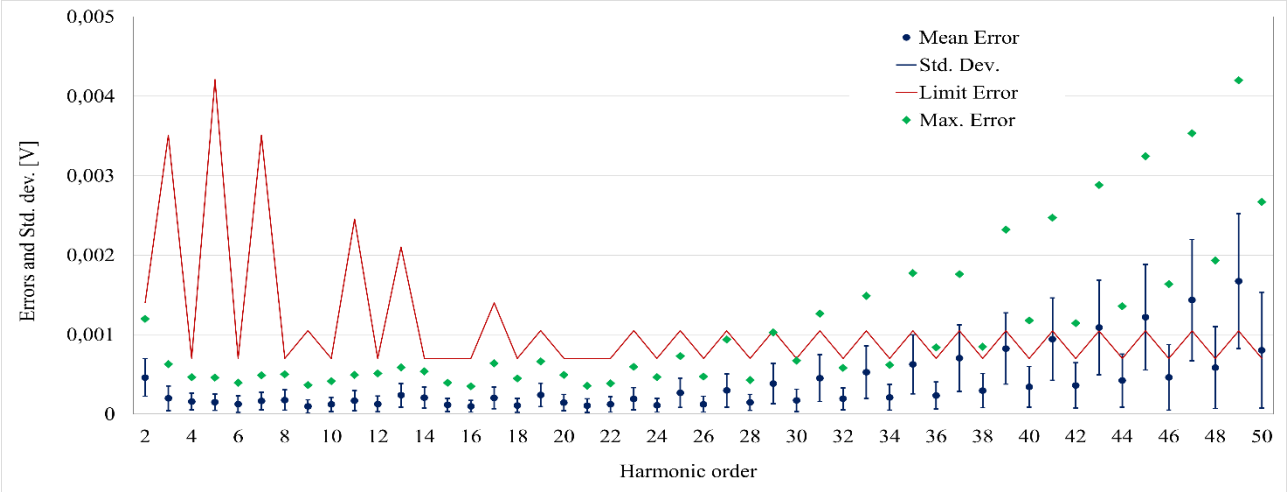

Fig. 4. 20 - Error evaluation for Case 4 - fs= 16 kHz, interpolation to 4096 points

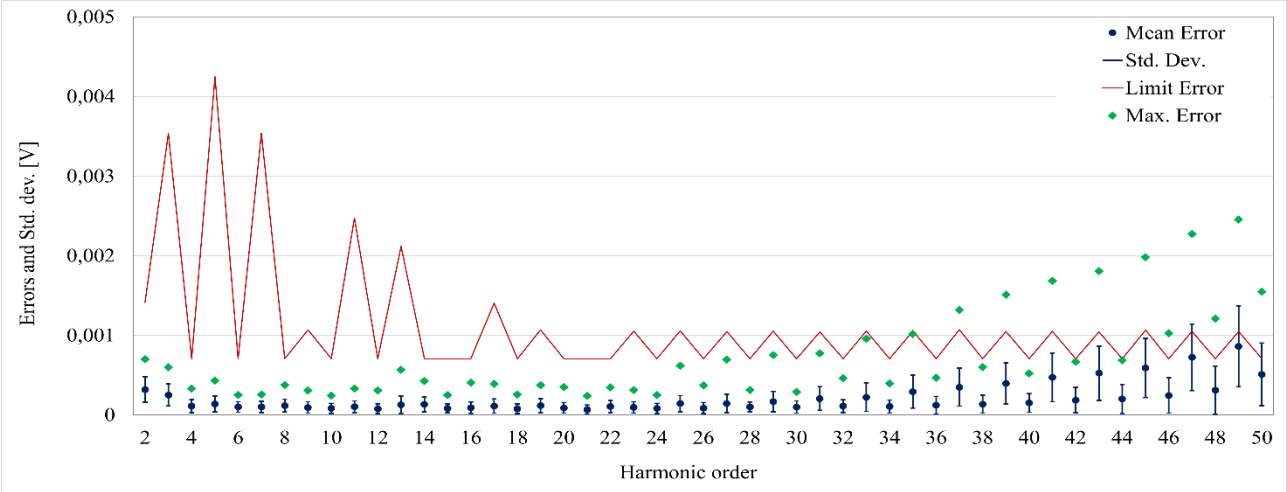

Fig. 4. 21 - Error evaluation for Case 5 - fs= 24 kHz, interpolation to 4096 points

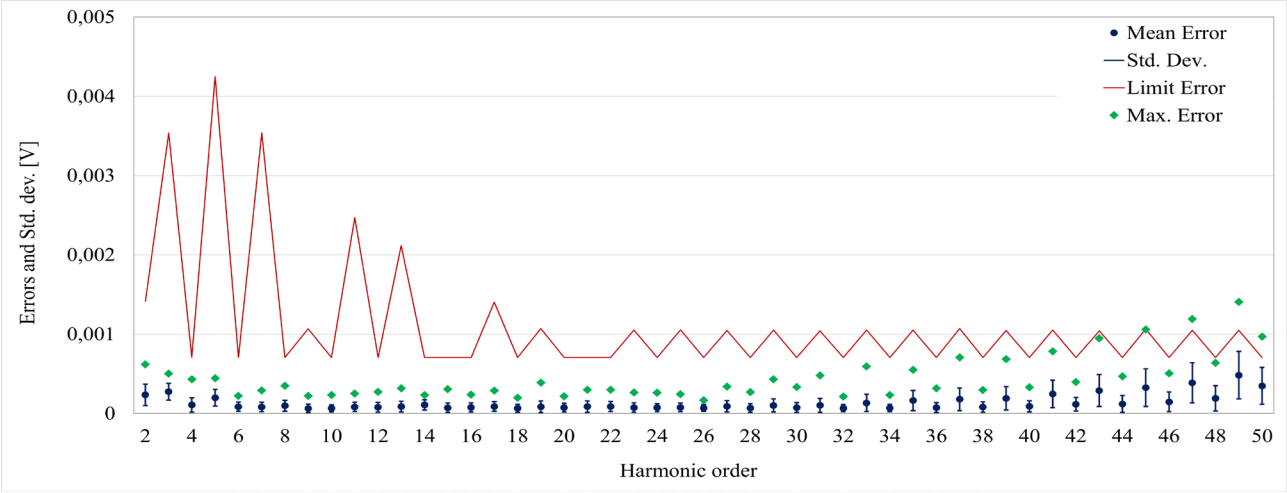

Fig. 4. 22 - Error evaluation for Case 6 - fs= 32 kHz, interpolation to 4096 points

Table 4. 6 - Standard accuracy limitation compliance for cases 1-6

Error limitation on harmonics measurement						
	Sampling frequencies and points after the interpolation					
	Case 1 fs = 16 kHz; 2048 points	Case 2 fs = 24 kHz; 2048 points	Case 3 fs = 32 kHz; 2048 points	Case 4 fs = 16 kHz; 4096 points	Case 5 fs = 24 kHz; 4096 points	Case 6 fs = 32 kHz; 4096 points
Farrow 3rd order interpolation	Not respected	Not respected	Not respected	Not respected	Not respected	Not respected

4.3 Test results discussion

As visible, the results obtained with the board, in terms of accuracy in the measurement of harmonics, differ from that obtained in simulation. In fact, although the algorithm used is a third order function, the standard is not respected for any of the frequencies tested (16, 24 and 32 kHz), neither with 2048 or with 4096 points after interpolation. A worsening of the error made on the measurement of harmonics of a major order was predictable, because of the results obtained in the ADC characterization tests, which showed very low characteristic parameter values. Nevertheless, the fact that even at the highest sampling frequencies the limits imposed for A-class of the standard are not met, involves the need to implement different techniques and try different solutions to improve the performance of the converter and reduce the errors made.

The total time required for the operations is largely lower than 200 ms for all the tested cases.

4.4 Solutions for improving device accuracy

Analysing the results obtained in the harmonic measurement and characterization tests of the device, it is plausible to attribute the non-compliance with the limits imposed by the standard to the behaviour of the A-D converter, more than the software part of the measurement chain. For this reason, different solutions have been tested with the same setup, comparing the results obtained in terms of measurement accuracy but also time required.

Analysing the behaviour of the ADC and the trend of the results, it possible to assume that an increase of the sampling frequency can reduce the error in harmonics detection.

However, the simple increment of f_s does not take into account either the instability of the sampler, which is affected by variations in the sampling frequency and therefore does not allow stable sampling, nor the problems that occur due to noise, even if reduced, especially for smaller harmonics. In fact, it is precisely on the higher order harmonics that the noise has a greater effect.

In order to solve these problems, it was decided to include, together with the increase of the sampling frequency, techniques to improve the sampling, starting from the operation of high-performance converters, such as sigma-delta converters [68–70].

4.4.1 Solution 1 – Oversampling, digital filtering and decimation

To improve the ADC performance a second series tests were carried out by implementing an oversampling technique for data acquisition [70, 71]. Sampling frequencies were set to integer multiple values of 16, 24 and 32 kHz; after the zero-crossing task, further pre-processing of sampled data with digital filter (first order) and decimation was implemented, in order to obtain equivalent sampling frequencies (and number of samples) equal to the values of the first series of tests, i.e. fs_eq = 16-24-32 kHz and, for a 50 Hz signal, N_eq = 3200-4800-6400 samples.

As known, this technique allows reducing the quantization noise in the frequency range of interest, to obtain an improvement of harmonic detection at high frequencies (Fig. 4. 23) [71–73]. In fact, the quantization noise amount depends on the acquisition system features and it is distributed all over the frequency range up to the Nyquist frequency; thus, the higher the sampling frequency is, the lower is the noise level; after filtering, a part of the noise is removed and with decimation the samples are reduced to obtain the desired equivalent sampling frequency and number of samples to be further processed.

From a theoretical viewpoint, with the respect to the sole ADC quantization error, to improve the resolution of n bits, an oversampling factor k equal to $2^{(n \cdot 2)}$ is needed [71]. For example, with an equivalent sampling frequency of 16 kHz, an improvement of 1, 2, or 3 bits of resolution require an oversampling factor of 4, 16, or 64 (i.e. sampling frequency of 64 kHz, 256 kHz or 1024 kHz), respectively.

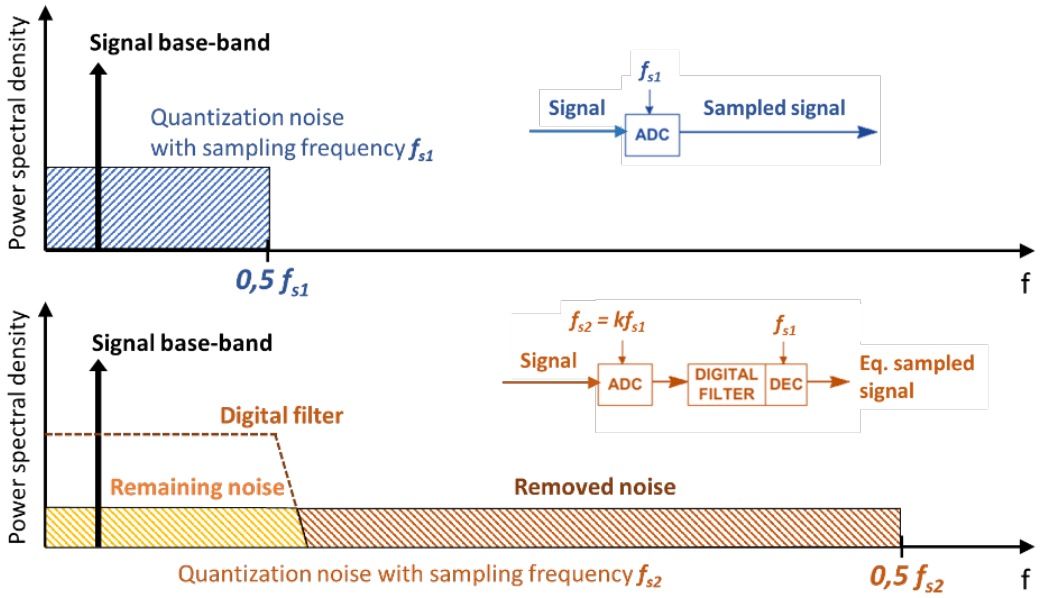

Fig. 4. 23 - Quantization noise reduction using oversampling and digital filtering

First implementation of the metrics has been adapted to the existing code, with gap sampling of 200 ms observation window. Algorithm implemented on the microcontroller board consist of a sampling task that collect a given number of samples, variable with the sampling frequency, then a zero cross function is implemented to take an integer number of periods. The digital first order filter is implemented and, after decimation of the samples, a number of samples of an equivalent sampling frequency is obtained. After that, interpolation and FFT task are processed as for the previous configuration. This implies a high number of operations to check the start and the end of the 10 periods of the signal, that require a huge amount of time.

The test conducted for the characterization of the device, described in chapter 4.1, have been repeated with the effective configuration for all the cases summarized in Table 4. 7. Apart from the rounding due to coding, the algorithms implemented on board cause almost negligible errors compared to those introduced by the ADC. The results of the characterization of the complete system are reported in Table 4. 8

Table 4. 7 - Tested cases 7 - 42

Case	Sampling frequency [kHz]	Equivalent sampling frequency [kHz]	Points after interpolation	Case	Sampling frequency [kHz]	Equivalent sampling frequency [kHz]	Points after interpolation
7	288	16	2048	25	672	16	2048
8		24		26		24	
9		32		27		32	
10		16	4096	28		16	4096
11		24		29		24	
12		32		30		32	
13	384	16	2048	31	768	16	2048
14		24		32		24	
15		32		33		32	
16		16	4096	34		16	4096
17		24		35		24	
18		32		36		32	
19	480	16	2048	37	960	16	2048
20		24		38		24	
21		32		39		32	
22		16	4096	40		16	4096
23		24		41		24	
24		32		42		32	

Table 4. 8 - ADC characterization for cases 7-42

fs [kHz]	fs_eq [kHz]	N. of points	SINAD [dB]	ENOB [bit]	THD [dB]	SFDR [dB]	FFT amplitude [V]
288	16	2048	49,32	7,9	-63,43	62,5	1,628
	24		49,47	7,9	-63,19	65,22	1,628
	32		53,12	8,0	-63,33	62,15	1,628
	16	4096	51,5	8,3	-64,57	77,52	1,628
	24		51,44	8,2	-64,55	68,46	1,628
	32		51,89	8,3	-64,35	73,55	1,628
384	16	2048	48,45	7,8	-63,4	55,97	1,627
	24		52,22	8,0	-62,76	59,48	1,627
	32		50,39	8,1	-63,06	61,69	1,627
	16	4096	53,93	8,7	-62,43	64,47	1,627
	24		55,15	8,9	-62,92	78,55	1,627
	32		55,63	8,9	-62,76	47,79	1,627
480	16	2048	49,19	7,9	-61,61	56,18	1,625
	24		50,76	8,1	-62,25	59,38	1,625
	32		51,32	8,1	-64,17	68,48	1,625
	16	4096	48,15	7,7	-61,71	76,44	1,628
	24		55,9	7.9	-62,19	68,65	1,625
	32		49,33	8.5	-63,37	72,49	1,625
672	16	2048	49,9	7,5	-59,92	55,92	1,623
	24		51,62	7.9	-59,72	65,59	1,623
	32		48,2	8,3	-60,25	71,38	1,623
	16	4096	54,68	8,2	-59,38	69,62	1,623
	24		51,43	8,8	-60,24	74,63	1,623
	32		54,89	8,8	-60,37	68,75	1,623
768	16	2048	48,86	7,8	-58,8	56,18	1,621
	24		47,52	7,6	-57,4	59,57	1,622
	32		51,57	8,3	-58,23	61,55	1,622
	16	4096	52,77	8,5	-57,71	70,2	1,622
	24		52,61	8,4	-57,75	78,4	1,622
	32		54,34	8,7	-58,27	66,21	1,622
960	16	2048	47,52	7,6	-53,82	72	1,62
	24		49,64	7,5	-53,83	74,94	1,62
	32		47,75	7,9	-54,48	71,3	1,62
	16	4096	51,57	8,3	-58,23	71,55	1,622
	24		52,61	8,2	-57,75	78,4	1,621
	32		51,43	8,2	-57,24	74,63	1,623

As for the previous configuration, a complete series of test of harmonic analysis have been conducted to evaluate the error committed in different cases, comparing the value obtained using the Nucleo board with the values measured with the reference system. Some graphic examples of medium error, standard deviation and maximum error evaluation are reported below.

The time to complete all the operations has been measured and compared with the 200 ms limitation for a gapless device. For the measurement, the internal timer of the Nucleo board and an external device (Tektronix oscilloscope MSO54) have been used, to have two different and comparable reference. For those configurations, the number of points to compare in the zero-crossing function is really higher than for the tests done before. In fact, with this configuration, the ZC is processed after the sampling and before the decimation, so the points to search for zero condition are increased by a factor k, equal to the oversampling factor. For this reason, the cases with the higher sampling frequency, even if permit to respect the limitation on accuracy, request more time than 200 ms. Some examples (taken from the oscilloscope) are reported in figures Fig. 4. 30 and Fig. 4. 31.

The results, regarding harmonics measurement error and time required, are summarized in Table 4. 9.

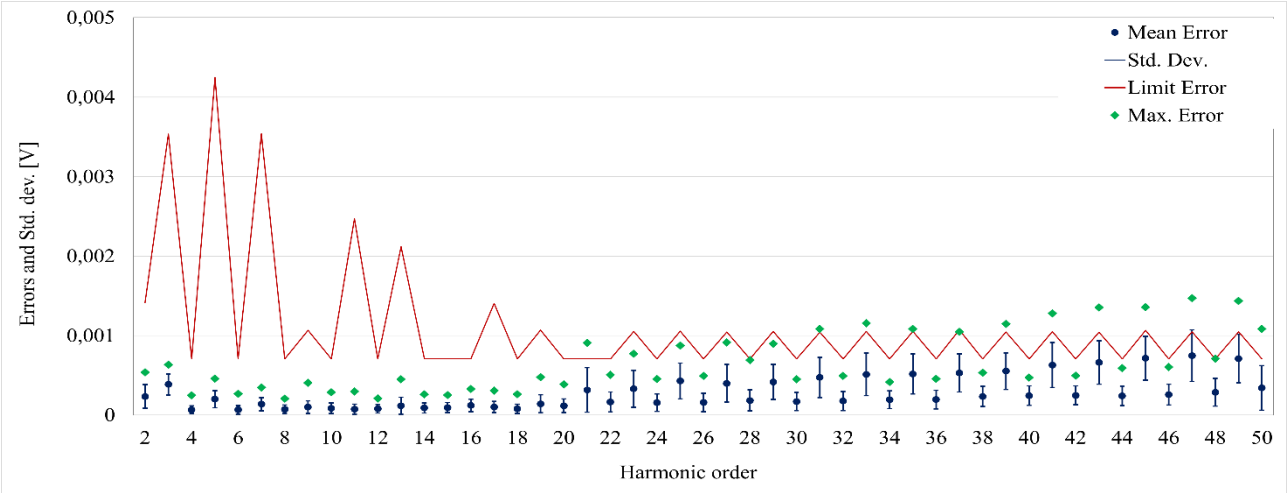

Fig. 4. 24 - Error evaluation for Case 7 - fs = 288 kHz, fs_eq = 16 kHz, interpolation to 2048 points

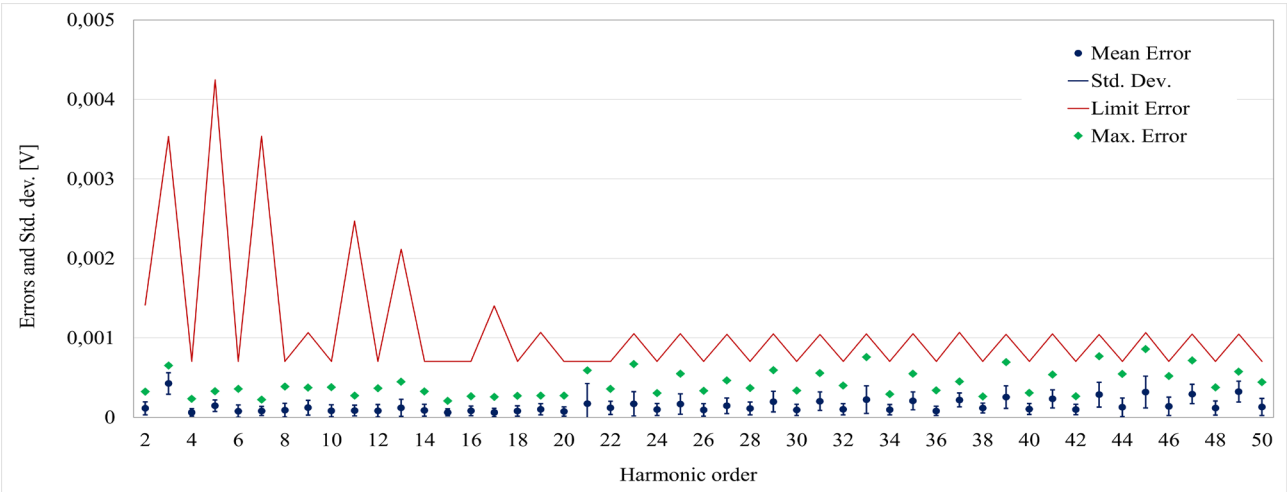

Fig. 4. 25 - Error evaluation for Case 9 - fs = 288 kHz, fs_eq = 32 kHz, interpolation to 2048 points

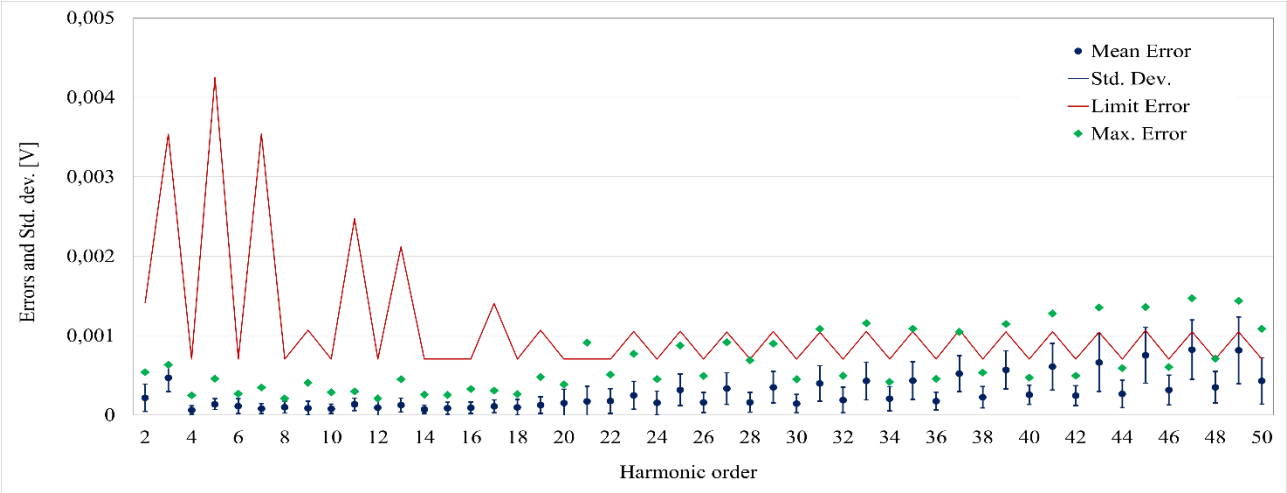

Fig. 4. 26 - Error evaluation for Case 13 - fs = 384 kHz, fs_eq = 16 kHz, interpolation to 2048 points

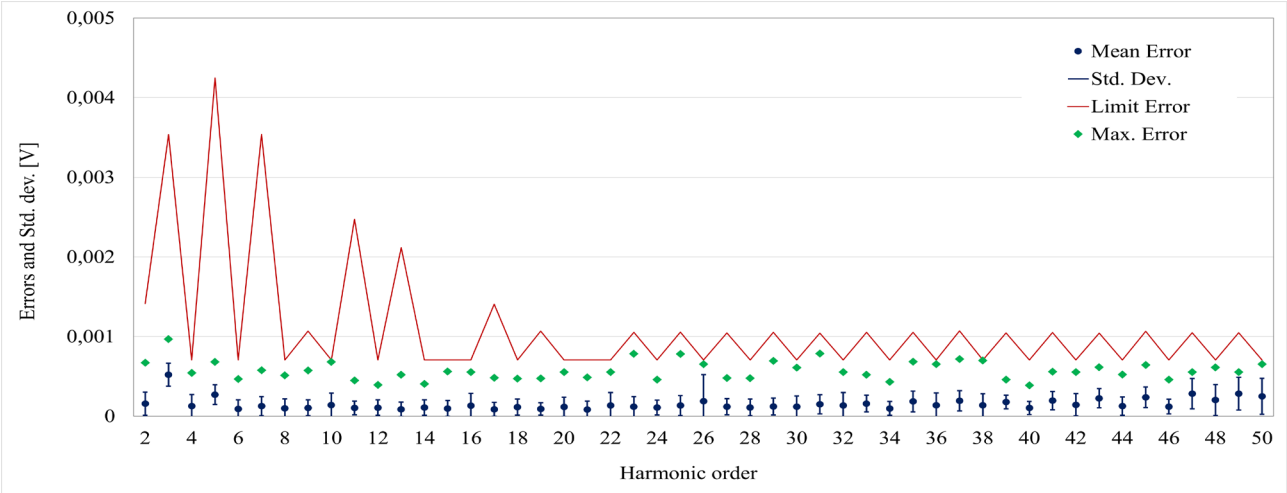

Fig. 4. 27 - Error evaluation for Case 15 - fs = 384 kHz, fs_eq = 32 kHz, interpolation to 2048 points

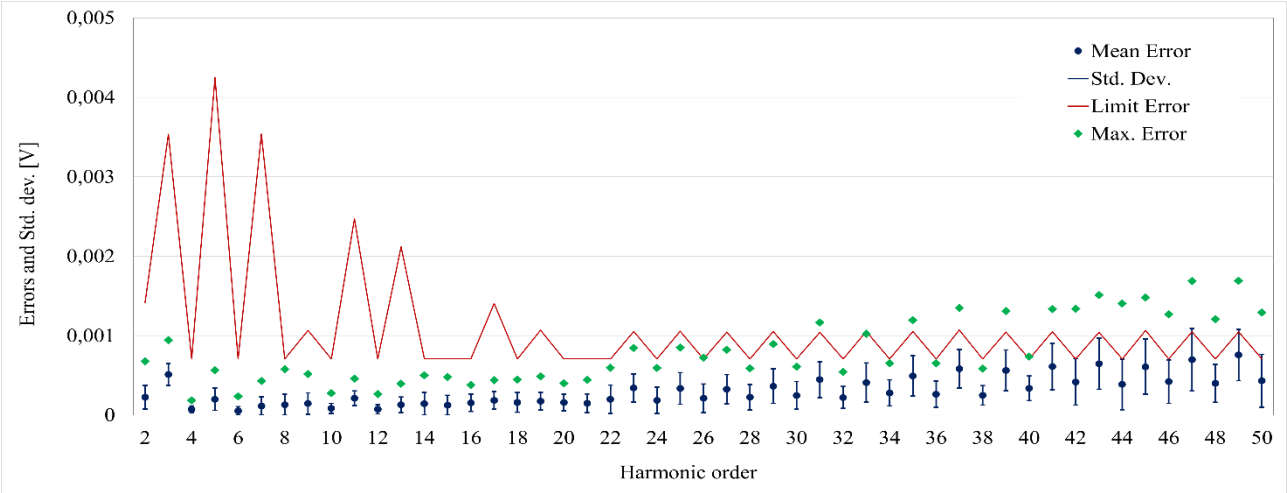

Fig. 4. 28 - Error evaluation for Case 31 - fs = 768 kHz, fs_eq = 16 kHz, interpolation to 2048 points

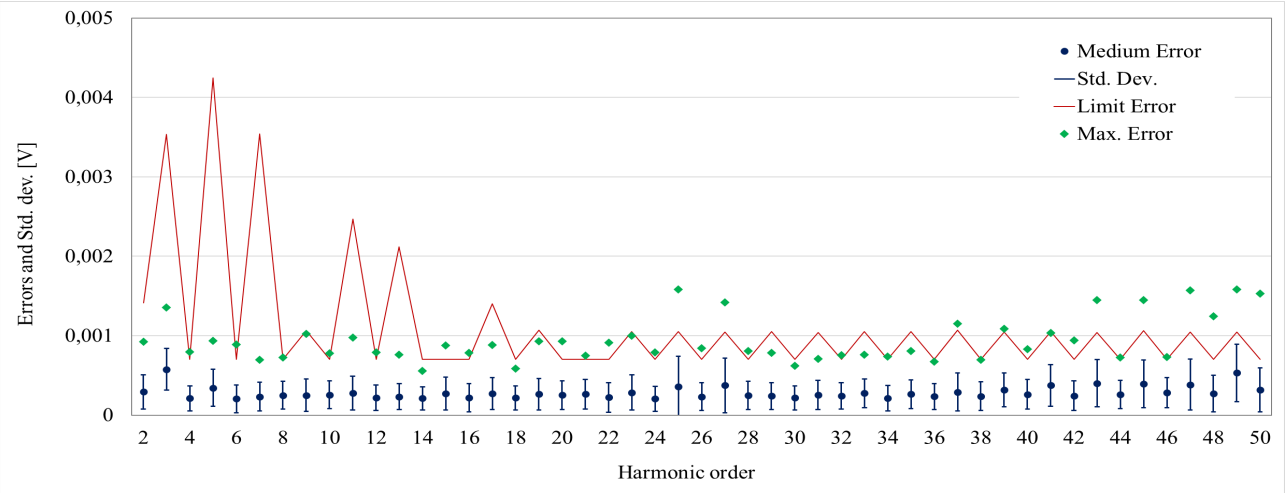

Fig. 4. 29 - Error evaluation for Case 32 - fs = 768 kHz, fs_eq = 24 kHz, interpolation to 2048 points

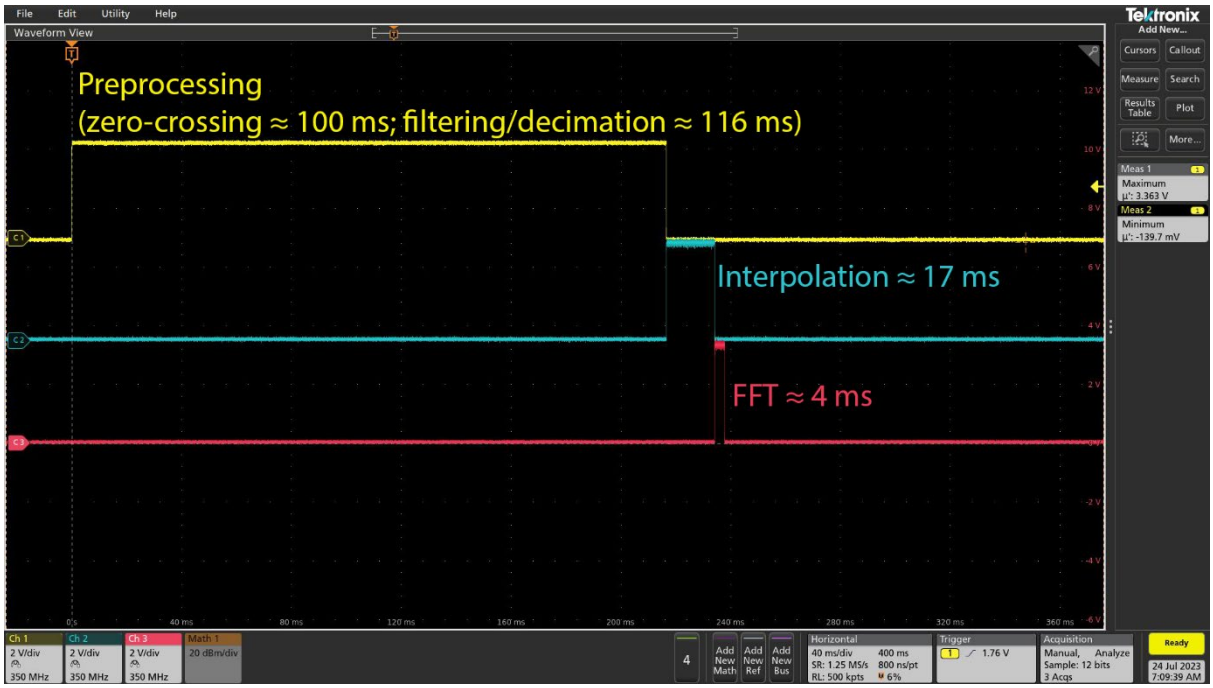

Fig. 4. 30 - Time estimation for Case 7 - fs = 288 kHz, fs_eq = 16 kHz, interpolation to 2048 points

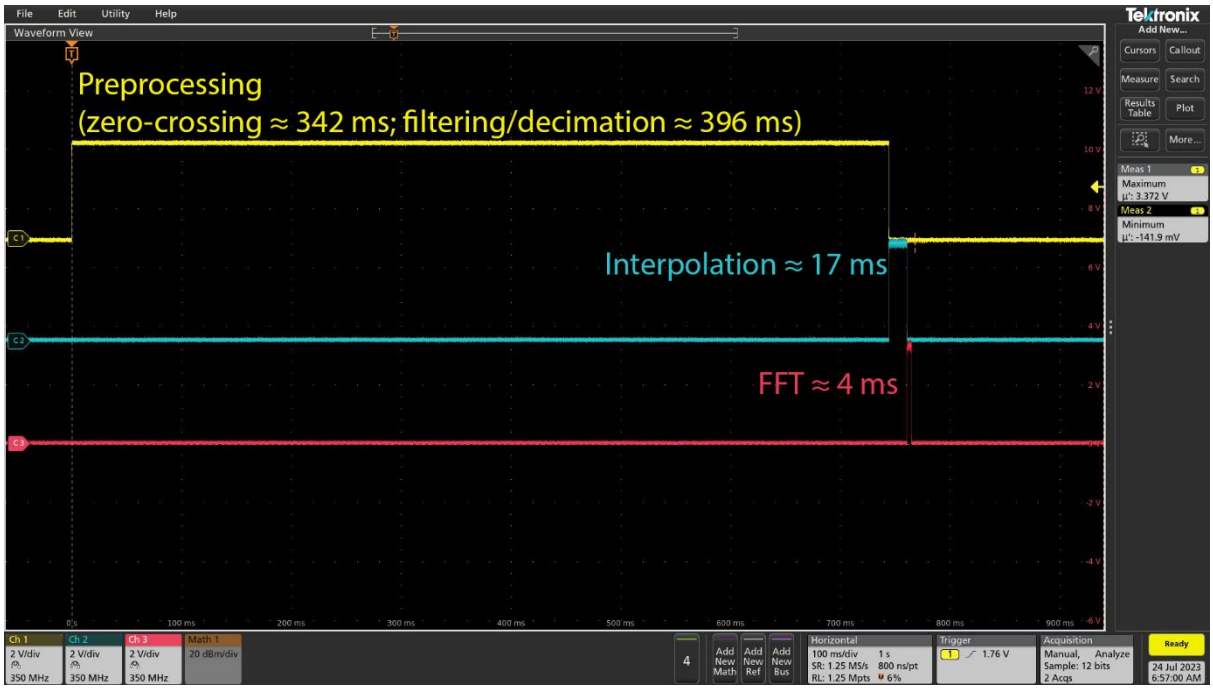

Fig. 4. 31 - Time estimation for Case 39 - fs = 960 kHz, fs_eq = 32 kHz, interpolation to 2048 points

Table 4. 9 - Standard accuracy and time limitation compliance for cases 7-42

Case			A-Class	
Sampling frequency	Equivalent sampling frewquency	Points after the interpolation	Error requirement	Time requirement
288	16	2048	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
	16	4096	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
384	16	2048	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
	16	4096	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
480	16	2048	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
	16	4096	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
672	16	2048	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
	16	4096	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
768	16	2048	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
	16	4096	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
960	16	2048	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected
	16	4096	Not respected	
	24		Respected	Not respected
	32		Respected	Not respected

4.4.2 Solution 2 – Moving average technique

For this solution, the tests was carried out by implementing a different oversampling technique. For each base sampling frequency value (fs_eq = 16, 24, 32 kHz), three effective sampling frequencies were used, equal to 10 times, 20 times and 30 times fs_eq; than the average value was calculated over 10, 20 or 30 acquired samples, respectively. A schematic example of the implemented moving average technique (average over 10 samples) is showed in Fig. 4. 32.

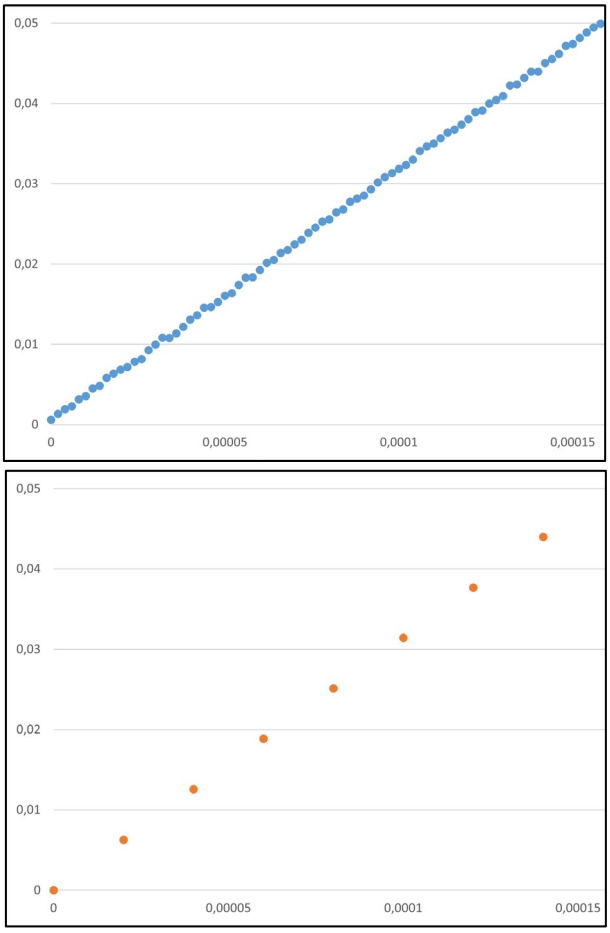

Fig. 4. 32 - Moving average value technique

For 10, 20 or 30 samples collected, a mean value of the amplitude is calculated to exclude the contribute of the low but significant variation of the value of the samples, that can alterate the results especially for the higher order harmonics. The ZC is implemented to synchronize 10 periods T_w.

This procedure allowed reducing the signal noise, with a lower computational cost, if compared with the previous case of filtering and decimation [71, 72]. As for the tests of previous section, after the moving average a new sequence of "average samples" was obtained, with equivalent sampling parameters equal to the values of the first series of tests, i.e. fs_eq = 16-24-32 kHz and N_eq = 3200-4800-6400 samples respectively, for a 200 ms T_w. Then Farrow interpolation (to 2048 or 4096 points) and FFT were carried out to obtain the harmonics measurements. The results of the test conducted for the characterization of the device with this technique are reported in Table 4. 11.

Table 4. 10 - Tested cases 49-66

Case	Sampling frequency [kHz]	Points for the mean value	Points after interpolation	Equivalent sampling frequency [kHz]
43	160	10	2048	16
44	320	20		
45	480	30		
46	160	10	4096	
47	320	20		
48	480	30		
49	240	10	2048	24
50	480	20		
51	720	30		
52	240	10	4096	
53	480	20		
54	720	30		
55	320	10	2048	32
56	640	20		
57	960	30		
58	320	10	4096	
59	640	20		
60	960	30		

Table 4. 11 - ADC characterization for cases 43 - 60

f_s [kHz]	Points for mean value	N. of points	f_{s_eq} [kHz]	SINAD [dB]	ENOB [bit]	THD [dB]	SFDR [dB]	FFT amplitude [V]
160	10	2048	16	46.11	7.5	-65.84	69.99	1,625
320	20			48.07	7.8	-64.64	63.21	1,625
480	30			47.31	7.6	-63.11	65.65	1,625
160	10	4096		53.42	8.3	-66.61	98.55	1,628
320	20			55.54	8.5	-63.81	66.50	1,625
480	30			50.45	8.6	-62.00	71.43	1,625
240	10	2048	24	49.88	7.5	-66.17	63.77	1,623
480	20			46.99	8.0	-62.23	64.99	1,623
720	30			51.17	8.2	-60.37	65.77	1,623
240	10	4096		53.73	8.6	-63.67	72.69	1,623
480	20			56.34	8.2	-62.13	70.75	1,623
720	30			51.24	9.1	-60.51	72.88	1,623
320	10	2048	32	50.64	7.9	-65.28	67.96	1,622
640	20			50.74	8.1	-59.48	67.03	1,622
960	30			49.42	8.1	-59.90	64.13	1,622
320	10	4096		56.92	8.5	-65.14	70.59	1,622
640	20			53.47	8.6	-61.94	69.90	1,622
960	30			54.67	9.2	-61.55	70.87	1,622

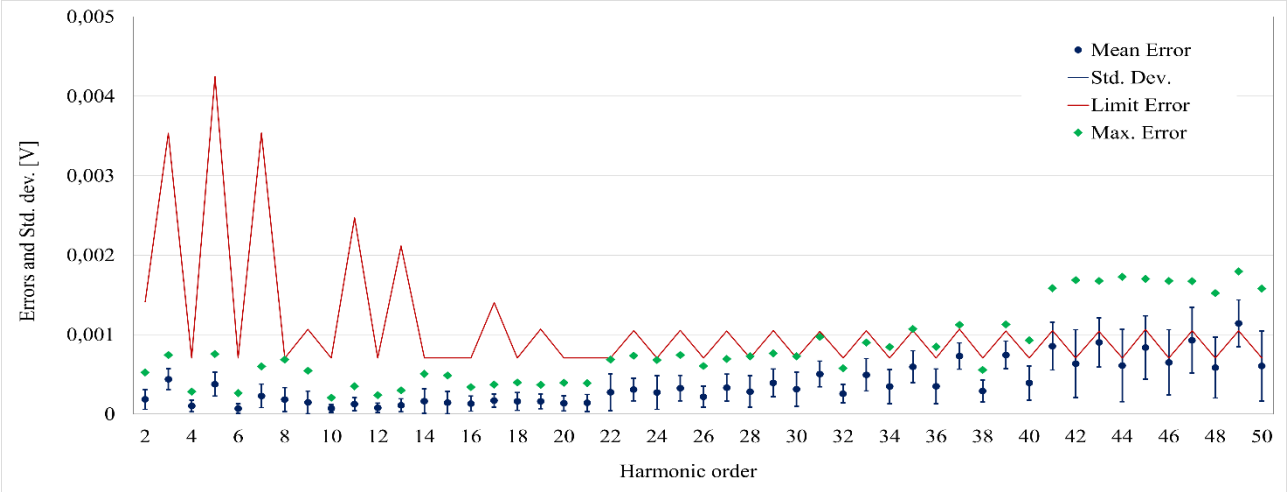

Fig. 4. 33 - Error evaluation for Case 43 - fs = 160 kHz, fs_eq = 16 kHz, interpolation to 2048 points

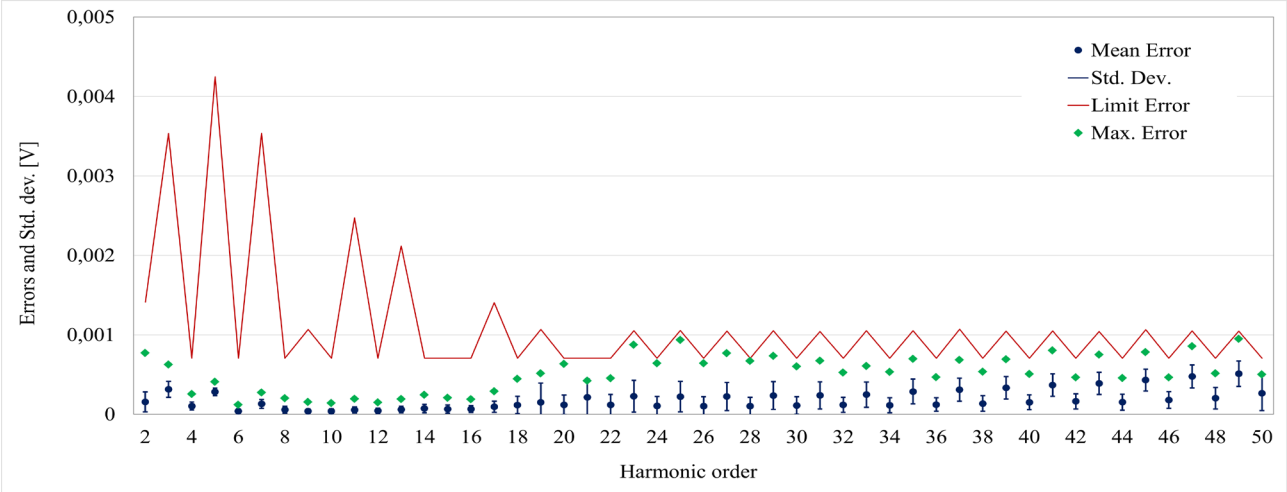

Fig. 4. 34 - Error evaluation for Case 49 - fs = 240 kHz, fs_eq = 24 kHz, interpolation to 2048 points

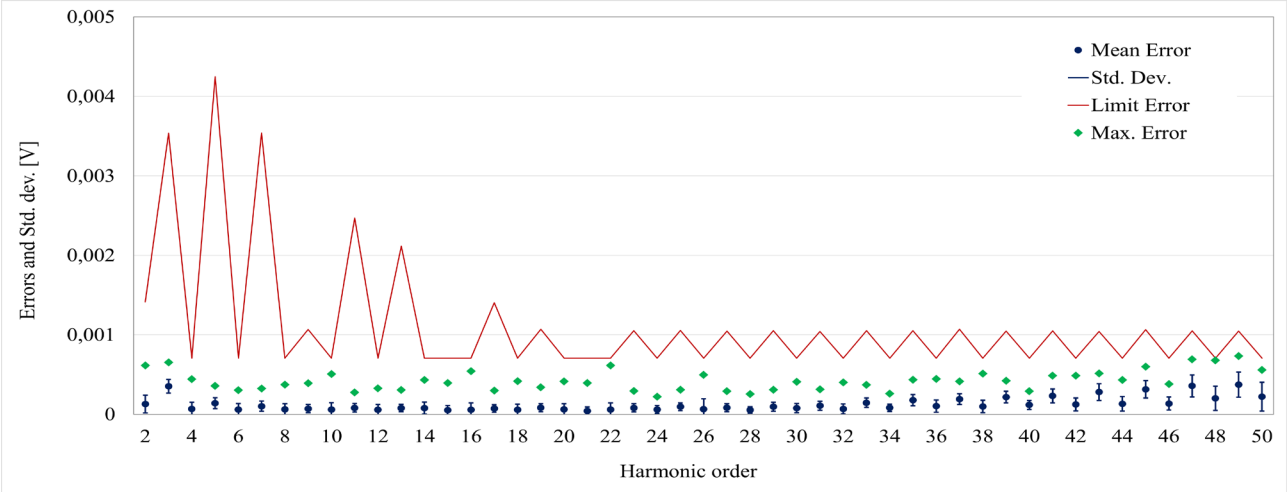

Fig. 4. 35 - Error evaluation for Case 55 - fs = 320 kHz, fs_eq = 32 kHz, interpolation to 2048 points

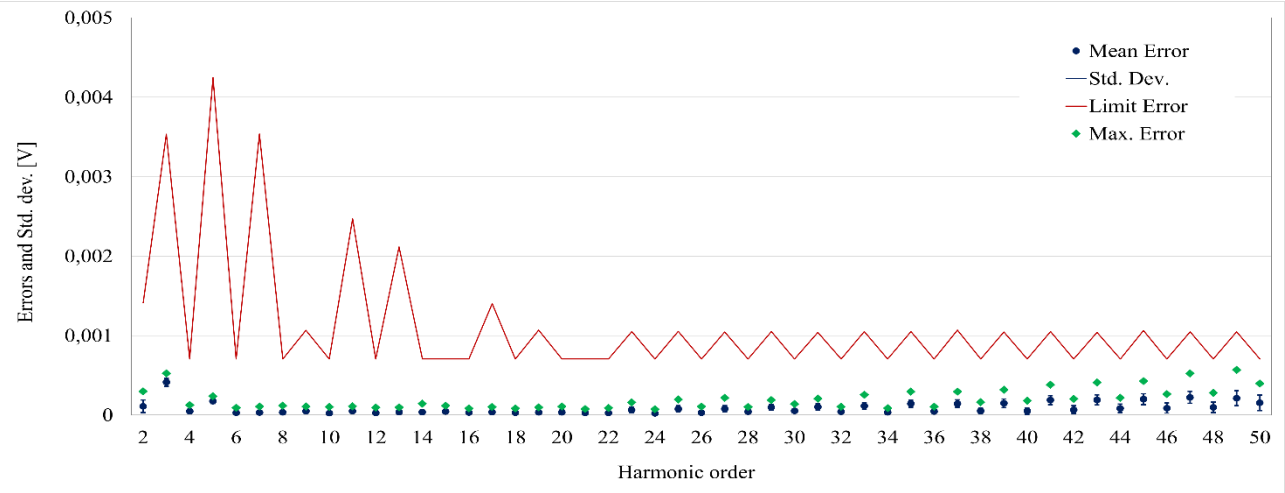

Fig. 4. 36 - Error evaluation for Case 58 - fs = 320 kHz, fs_eq = 32 kHz, interpolation to 4096 points

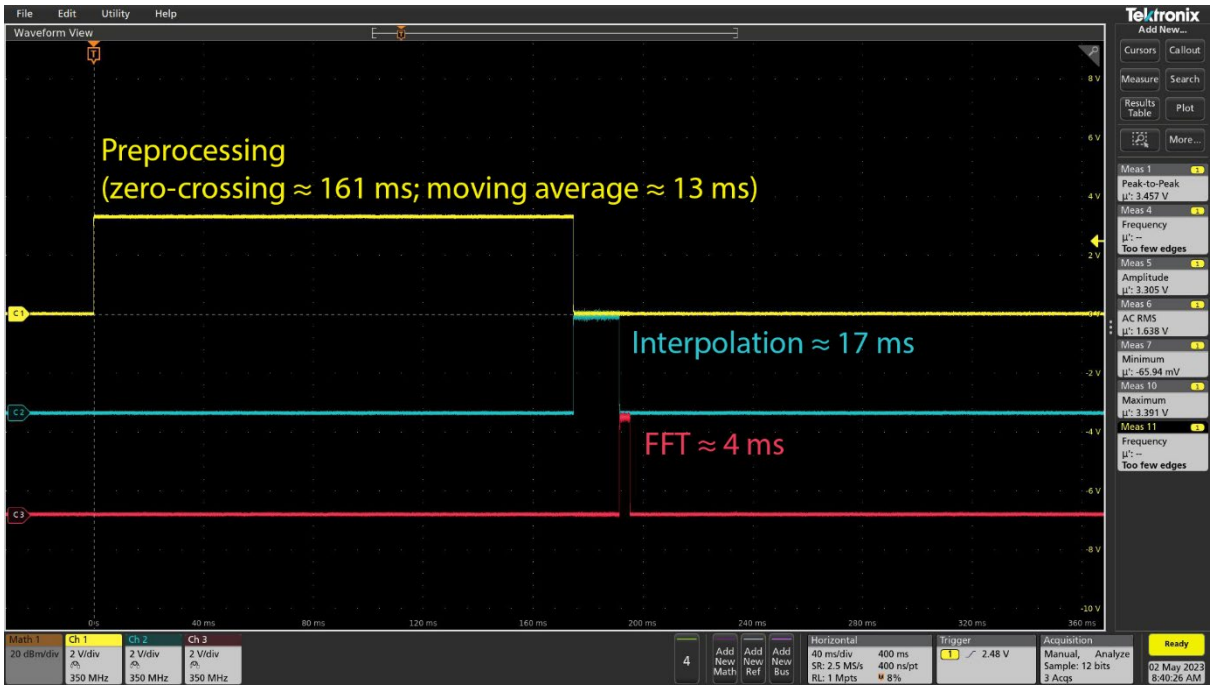

Fig. 4. 37 - Time estimation for Case 50 - fs = 480 kHz, fs_eq = 24 kHz, interpolation to 2048 points

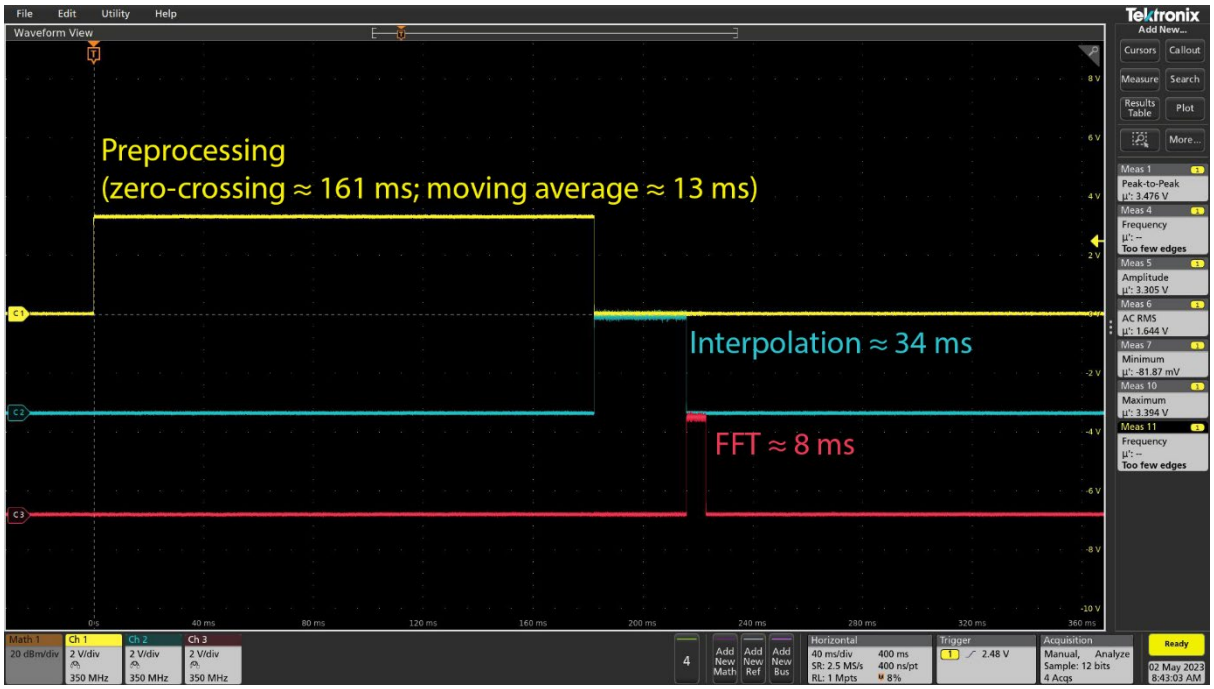

Fig. 4. 38 - Time estimation for Case 53 - fs = 480 kHz, fs_eq = 24 kHz, interpolation to 4096 points

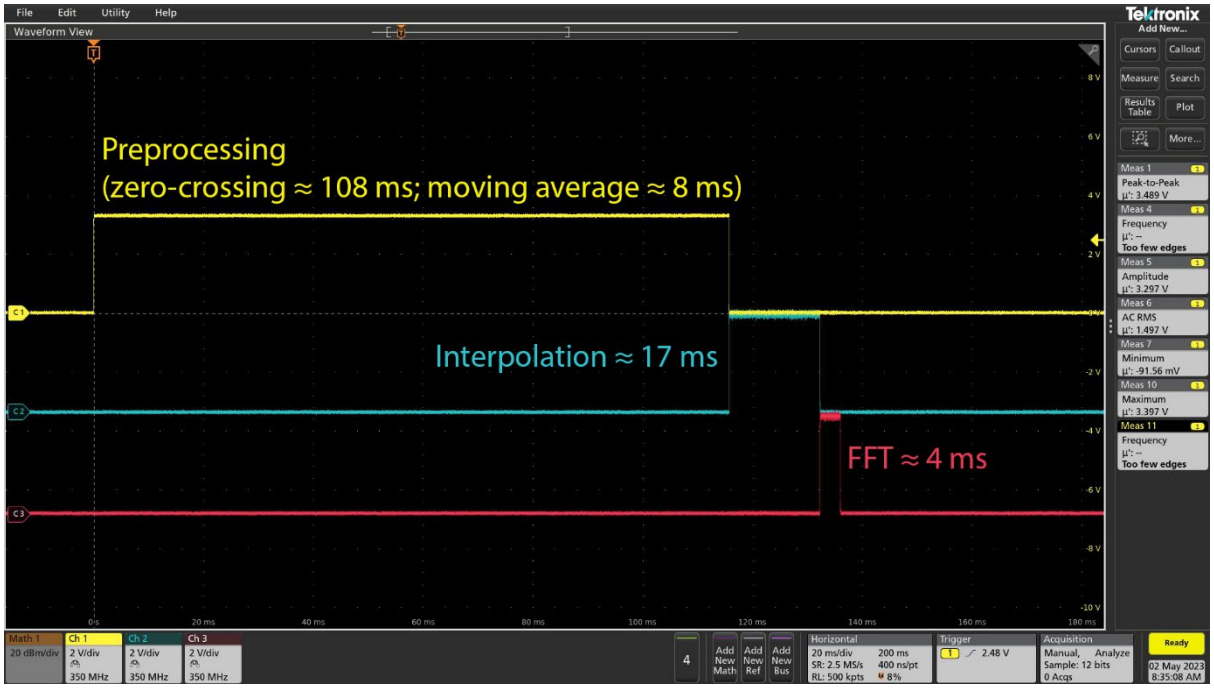

Fig. 4. 39 - Time estimation for Case 55 - fs = 320 kHz, fs_eq = 32 kHz, interpolation to 2048 points

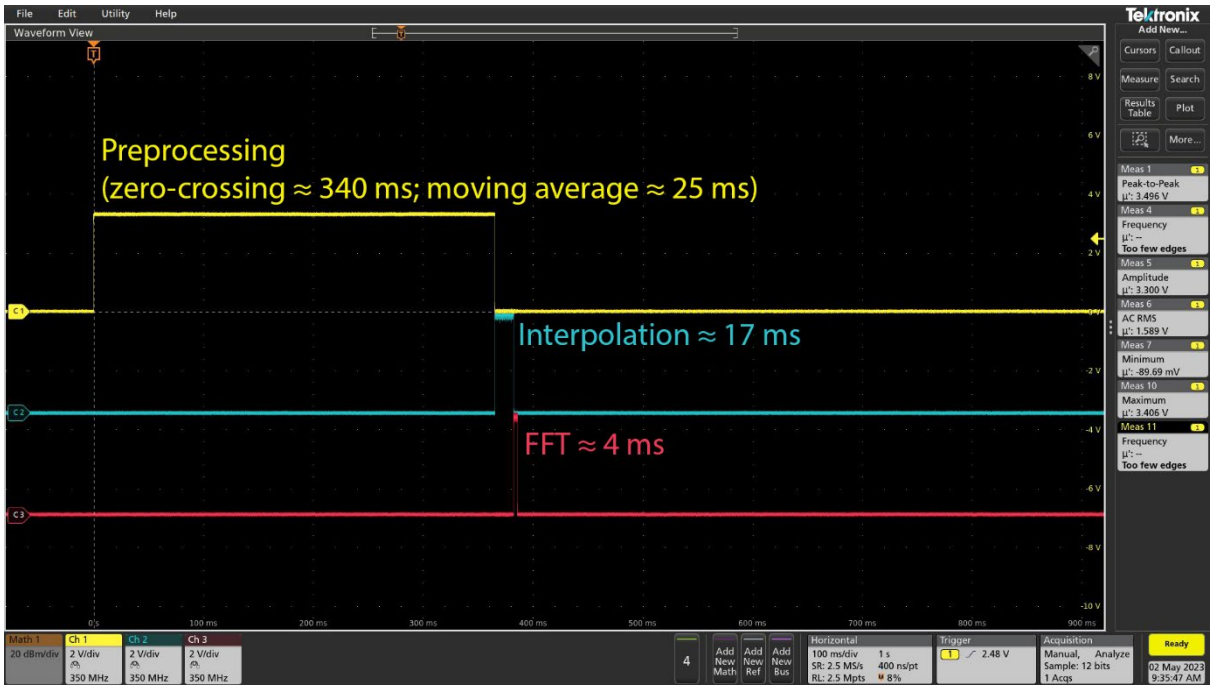

Fig. 4. 40 - Time estimation for Case 57 - fs = 960 kHz, fs_eq = 32 kHz, interpolation to 2048 points

Table 4. 12 - Standard accuracy and time limitation compliance for cases 49 – 66

Case				A-Class	
Sampling frequency	Points for mean value	Equivalent sampling frequency	Points after the interpolation	Error requirement	Time requirement
160	10	16	2048	Not respected	Respected
320	20			Not respected	Respected
480	30			Not respected	Respected
160	10		4096	Not respected	Respected
320	20			Not respected	Respected
480	30			Not respected	Respected
240	10	24	2048	Respected	
480	20			Respected	
720	30			Respected	Not respected
240	10		4096	Respected	
480	20			Respected	Not respected
720	30			Respected	Not respected
320	10	32	2048	Respected	
640	20			Respected	Not respected
960	30			Respected	Not respected
320	10		4096	Respected	
640	20			Respected	Not respected
960	30			Respected	Not respected

4.5 Analysis of results

The techniques tested for the ADC improvement demonstrated an effective behaviour, making possible the reduction of the error in harmonics measurement even using the 12-bit ADC of the Nucleo board. For the first solution, despite increasing in sampling frequency with subsequent filtering, it is possible, in some cases, to respect the accuracy limits imposed by the standard, the time needed to complete the operations with this configuration does not allow to respect the imposed limit of 200 ms. However, analysing the different operations individually, it is visible that the zc operation for the synchronization of the post-sampling signal requires a very high amount of time. Synchronizing the signal with a different process, such as a real time zero crossing, it would be possible to reduce the overall time and some of the rejected solutions would be usable. This would require naturally a more powerful CPU or a different approach. These tests will be the subject of future evaluations, for optimization of the codes for the realization of the device.

Another problem with this technique is that there is an enormous memory required for high-frequency sample storage. As already reported above, in fact, the code is implemented in order to carry out the filtering and the decimation only after completing the sampling, therefore requiring to write in memory all the samples. The amount of memory required is therefore considerably greater than the one required for a code with base f_s. In Table 4. 13, the required memory values are shown as the number of samples entering varies.

Table 4. 13 - Memory requirement for sampling only - oversampling technique

Memory required [kbyte] per 200 ms acquisition (10 periods)			
		Samples	Sampled acquired [kbyte]
N. bit = 16	fs = 288 kHz	57600	112,5
	fs = 384 kHz	76800	150,0
	fs = 480 kHz	96000	187,5
	fs = 672 kHz	134400	262,5
	fs = 768 kHz	153600	300,0
	fs = 960 kHz	192000	375,0

As for the first solution, with the moving average technique it was found that the increase of the sampling frequency allowed to respect the accuracy limits imposed by the standard. However, with the different processing technique of the samples, the best accuracy is not obtained so much at the higher frequencies, as with the increase of the number of equivalent points on which the average is calculated. This allows for example to already comply with the standard limits at the frequency of 240 kHz, averaging 10 points and obtaining an fs_eq of 24 kHz.

This technique also requires a much lower computational cost compared to post-oversampling digital filtering, as can be seen from the time measurements that are significantly lower.

Also, in terms of memory, it is not necessary to save a large number of samples for this solution, because is possible to limit the sampling frequency. This implies that a smaller memory buffer is required. After that, there is the possibility of optimizing the code implementing the moving average in real time, while the samples are acquired, to have an even smaller buffer for the sole allocation of samples related to the equivalent sampling frequency. As for the solution 1, the optimization of the synchronisation technique would save a great deal of time and therefore allow the use of solutions with higher f_s, if required.

5. CONCLUSION

The work has presented an experimental study on the feasibility of harmonic analysis implementation on commercial microcontroller devices, according to IEC 61000-4-30 Class A and IEC 61000-4-7 Class I requirements. An extended experimental characterization has been carried out on a case study device, aimed at analysing its performances in terms of both measurement accuracy and computational cost. Different solutions have been tested, concerning signal processing algorithms and data acquisition.

As regards the spectral analysis, a focus has been made on time-domain interpolation algorithms for FFT efficient calculation. In detail, Farrow interpolation algorithm is proposed as valid alternative to Lagrange polynomial interpolation, thanks to its lower computational cost. The obtained results show the feasibility of the proposed algorithm. Moreover, the adoption of a time-domain interpolation technique allows gaining more flexibility in terms of sampling frequency and number of acquired samples and reaching a suitable tradeoff between accuracy requirements for spectral analysis, device memory and processing capabilities, and computational burden.

The proposed algorithm has been implemented on the case study microcontroller board and several experimental tests have been carried out by using the on-board ADC for signal acquisition. Different sampling strategies have been tested, to identify a suitable solution for both data acquisition and processing, capable to comply with Standards requirements. The results of the experimental tests have shown that the metrological performances of the low-cost solution can be improved by implementing efficient sampling and processing strategies; in detail, the best results, in terms of both measurement accuracy and processing time, have been obtained by implementing an oversampling technique with a moving average for noise reduction. The obtained results demonstrate the feasibility of the spectral analysis implementation, with respect to IEC 61000-4-7 accuracy requirements.

As regards memory and computational cost, the limited metrological performances of the on-board ADC required the adoption of ad-hoc solutions for signal preprocessing. Even if in some cases the results were compatible with a possible gapless implementation, the signal acquisition and preprocessing tasks increased the overall computational cost and memory allocation. This may pose limitations on the possibility of implementing not only harmonic analysis but also other PQ metrics on the same device.

In this viewpoint, further work would be to investigate the possibility to use an external ADC for the board, in particular low cost with high accuracy devices, based on sigma-delta technology, are suitable to be combined with a general-purpose microcontroller to collect the samples and then processed them using the low-cost hardware. In this way, no high frequency values or particular solution are required, since signals over-sampling is resolved by the external sigma-delta ADC.

Another possibility that will be investigated consist of pre-processing techniques optimization, to reduce the computational cost of the heaviest algorithms, starting from the zero cross function real-time implementation. The consecutive step could be the gapless sampling implementation on the studied device, to validate the possibility of a A-Class power quality meter starting from a low-cost board.

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