Control Engineering Practice 169 (2026) 106746

Contents lists available at ScienceDirect

Control Engineering Practice

journal homepage: www.elsevier.com/locate/conengprac

Robust control of interleaved boost converter with active disturbance compensation

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ARTICLE INFO

Keywords:
Active disturbance rejection control
DC-DC Power converters
Interleaved converter
Sliding mode robust control

ABSTRACT

Nowadays, extensive research is conducted on interleaved DC-DC boost converters due to their ability to minimize current ripple and enhance fault tolerance. In this article, we present a control methodology that achieves effective output voltage regulation while demonstrating robustness against uncertainties in parameters, variations in the source supply voltage, and deviations in load. These objectives are achieved by developing an equivalent circuit model for the interleaved boost converter and formulating a linear representation using the exact linearization technique. Subsequently, trajectory tracking control strategies are employed, incorporating a sliding mode element to manage parameter uncertainties and compensate for disturbance errors. The controller, applied to the equivalent boost converter model, adjusts the duty cycle of each individual MOSFET command signal. This control mechanism utilizes the output voltage and the sum of the currents within the converter's branches as feedback variables. Experimental results illustrate the effectiveness and feasibility of the presented methodology.

1. Introduction

Recently, there has been widespread research interest in interleaved DC-DC boost converters; it is mainly due to their performance in ripple minimization and high efficiency, together with fault tolerance. For these reasons, they are prominently featured in specialized literature. It is common knowledge that interleaved conversion involves parallel connections that operate at the same switching frequency. Besides, the consecutive switching instants are deliberately delayed by the switching period divided by the number of branches. In this configuration, each branch is connected to the same source, output capacitor, and load (Miwa et al., 1992). In contrast to interleaved configuration, to reduce current ripples and to increase efficiency of the system, alternative solutions are found in boost converters controlled through suitable techniques where both voltages and currents are contemporaneously regulated to prevent overshoots or excessively high ripples (Alonge et al., 2023; Sferlazza et al., 2020), or in configurations that use inductors in the quasi-saturation region achieving a better power density with reduced size inductors (Pilato et al., 2024; Scirè et al., 2025; Sciré & Montana, 2025). In (Kolar et al., 2012), furthermore, the advantages of the interleaved configuration are assessed in terms of efficiency, harmonic management, and loss reduction. As such, (Giral et al., 1999), N identical boost converters are interconnected in parallel to enforce the output voltage reaching the desired value, thereby reducing ripple in both the input current and output voltage. In the context of plug-in hybrid electric vehicle applications, (Hegazy et al., 2011) investigates an interleaved two-phase DC-DC boost converter, employing a frequency domain control, it adopts a simplified transfer function from duty-cycle to voltage and duty-cycle to current. The interleaving topology for power converters is well established in the literature, with numerous studies addressing its control methodologies. Traditional approaches often rely on PI-based control, as seen in (Miwa et al., 1992), where a two-phase interleaved boost converter in discontinuous conduction mode (DCM) achieves high efficiency and low diode losses through a combination of PI control for voltage regulation and bang-bang control for current management. More advanced control

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https://doi.org/10.1016/j.conengprac.2025.106746
Received 4 June 2025; Received in revised form 27 December 2025; Accepted 27 December 2025
Available online 6 January 2026

techniques based on state-space modeling have also been explored. For instance, (Veerachary et al., 2001) presents a state-space model of an interleaved boost converter, although it is primarily utilized for steady-state analysis rather than dynamic control design. Similarly, (Lai et al., 2012) employs a frequency-domain approach to regulate phase currents through static control, which does not account for system dynamics. Recent advances have introduced intelligent control techniques such as machine learning-based controllers (Qie et al., 2022; Reddy & Sudhakar, 2018) and optimization-based strategies like model predictive control (MPC) (Denaro et al., 2023; Sartipizadeh et al., 2021; Zhao et al., 2020). While these methods improve performance and robustness, they often require complex computational resources or rely on approximate models. Alternative nonlinear model-based control techniques such as backstepping (Hao et al., 2022; Xu et al., 2020), sliding mode control (SMC) (Jiang et al., 2019), $\mathcal{H}_\infty$ control (Keskin et al., 2021), passivity-based control (Liu et al., 2021), and feedback linearization (FL) (Gkizas et al., 2018; Koundi et al., 2022) have also been proposed. Additionally, active disturbance rejection control (ADRC) (Smadi et al., 2023; Zhuo et al., 2019, 2021) has been utilized to compensate for disturbances and parameter uncertainties. However, these techniques face challenges in robustness and disturbance estimation accuracy. In response to these limitations, this paper introduces an innovative control strategy for interleaved boost converters based on an extended third-order model derived from the conventional second-order averaged model. By incorporating the duty cycle as an additional state variable, this dynamic input model allows discontinuities in the auxiliary input to translate into smooth variations in the duty cycle. The proposed approach enhances control flexibility and ensures smoother transitions, particularly advantageous in high-performance power electronics applications. Using a nonlinear transformation, this model is converted into the Brunovsky canonical form (Gehan et al., 2017), enabling the design of a trajectory-tracking control law that ensures convergence to zero of the tracking error. The proposed control approach integrates Active Disturbance Rejection Control to estimate and compensate for endogenous disturbances through an Extended State Observer (ESO). Unlike traditional ADRC approaches, which assume a known system structure and rely on predefined disturbance rejection mechanisms, our method explicitly considers parametric uncertainties and estimation errors, and a Sliding Mode (SM) component is incorporated into the control law to improve robustness.

Combining ADRC with a sliding mode correction mechanism ensures robustness against modeling inaccuracies, external disturbances, and parameter variations. This hybrid control structure effectively mitigates common limitations found in conventional control approaches, such as sensitivity to noise in SMC and estimation errors in ADRC. Unlike MPC-based approaches, which require an approximate model for trajectory evaluation, or backstepping and traditional ADRC methods, which lack robustness against parametric uncertainties, our method provides an alternative framework leveraging exact linearization. This methodology enables a more precise control action without relying on predictive models or iterative optimization routines, making it computationally efficient and better suited for real-time applications. Additionally, this work builds upon our previous study (Sferlazza et al., 2023) by extending the theoretical foundation and providing a comprehensive experimental validation on a silicon carbide-based interleaved boost converter prototype. The proposed control design has been rigorously tested under various operating conditions, demonstrating its robustness and reliability. Extensive experimental verification, including transient response analysis, disturbance rejection capability, and steady-state performance evaluation, further validates the superiority of the proposed approach over existing techniques.

2. Dynamic model of the N-phases interleaved boost converter

The N-phases interleaved boost converter electrical circuit is depicted in Fig. 1.

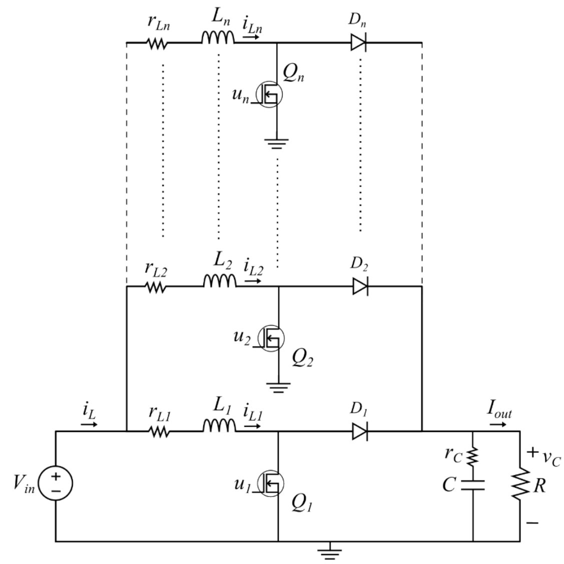

Fig. 1. Electrical circuit of the N-Phases interleaved boost converter.

Under the assumption of a boost converter designed for continuous conduction mode and neglecting the parasitic resistance of the capacitor, its analytical model description can be written as follows:

$$\dot{i}_{L_i} = \frac{1}{L_i}\left(-r_{L_i} i_{L_i} - (1-u_i)v_C + V_{in}\right), \quad i=1,\cdots,N \tag{1}$$

$$\dot{v}_C = \frac{1}{C}\sum_{i=1}^{N}(1-u_i)i_{L_i} - \frac{1}{RC}v_C, \tag{2}$$

where $u_i \in \{0,1\}$ ($u_i = 0$ if the switch is in the OFF state and $u_i = 1$ if the switch is in the ON state). This model encompasses all operational conditions. Besides, when designing a controller, a further advantage is achieved by associating an averaged model with this one, obtained by replacing the discontinuous inputs u_i with continuous inputs $\lambda_i \in [0,1]$. This averaged model is given by:

$$\dot{i}_{L_i} = \frac{1}{L_i}(-r_{L_i} i_{L_i} - (1-\lambda_i)v_C + V_{in}), i=1,\cdots,N \tag{3}$$

$$\dot{v}_C = \frac{1}{C}\left(\sum_{i=1}^{N}(1-\lambda_i)i_{L_i} - \frac{1}{R}v_C\right), \tag{4}$$

It is essential to highlight that specific symmetry conditions are incorporated into this model. In particular, all phases use identical inductors, resulting in uniform values for inductance and parasitic resistance, denoted by L and r_L, respectively. Furthermore, within each switching period T_s, the same value of $\lambda_i = \lambda$ is applied across all N-phases and the command signals to the MOSFET gates are shifted by T_s/N each other. This setup ensures that the average phase currents are equal, leading, from (3) and (4), to the following averaged dynamic model:

$$\dot{i}_L = \frac{1}{L_{eq}}(-r_{L_{eq}} i_L - (1-\lambda)v_C + V_{in}), \tag{5}$$

$$\dot{v}_C = \frac{1}{C}\left((1-\lambda)i_L - \frac{1}{R}v_C\right), \tag{6}$$

where the input current i_L is given by $i_L = \sum_{i=1}^{N} i_{L_i}$, $L_{eq} = L/N$, and $r_{L_{eq}} = r_L/N$. The model (5) and (6) shows that, in the above-illustrated hypotheses, the N-phases interleaved converter is equivalent to a single-phase conventional boost converter with parameters L_{eq} and $r_{L_{eq}}$. Moreover, since this model has single control variable (i.e., λ), the control of the boost interleaving can be carried out by controlling the equivalent conventional single-phase boost described by (5) and (6).

The set of equilibrium states, corresponding to a generic value of the output V_C^* is given by:

$$I_L^* = \frac{NV_{in}}{r_L + NR(1-\lambda_e)^2}, \tag{7}$$

where:

$$\lambda_e = 1 - \frac{RV_{in} + \sqrt{(R(RV_{in}^2 - 4r_{L_{eq}}V_C^{*2}))}}{2RV_C^*} \tag{8}$$

is the obtained from the solution of the following second-order equation with $\xi = 1 - \lambda_e$:

$$RV_C^*\xi^2 - RV_{in}\xi + r_{L_{eq}}V_C^* = 0. \tag{9}$$

3. Motivation and control methodology

Among model-based control strategies for nonlinear systems, Feedback Linearization (FL) offers a way to transform the nonlinear dynamics into an equivalent linear system through a suitable nonlinear state feedback. This transformation typically yields a chain of integrators driven by an auxiliary control input and a total disturbance term, which combines linear and nonlinear couplings linked to system dynamics and parameters. In ideal conditions, this disturbance can be exactly compensated, enabling the desired closed-loop behavior. However, FL is highly sensitive to modeling errors and parameter uncertainties, since the required nonlinear compensation relies on precise knowledge of the system. Active Disturbance Rejection Control (ADRC) addresses this limitation by estimating the total disturbance through an Extended State Observer (ESO) and compensating it online. For this reason, ADRC can be viewed as a robust counterpart of FL, capable of handling parameter variations, unmodeled dynamics, and exogenous disturbances. Despite this advantage, ADRC performance may degrade when the disturbance estimation is inaccurate or when uncertainties affect the control channel itself, such as errors in the forcing coefficient, which the ESO cannot observe. To enhance robustness in these critical situations, this paper introduces an advanced ADRC scheme that augments the nominal control law with a Sliding Mode (SM) term. The SM gain is computed by enforcing the sliding condition on a surface defined as a linear combination of the tracking error and its derivative. Therefore, the main objective of this work is to achieve a higher level of robustness compared with existing nonlinear control strategies reported in the literature. The main steps of the proposed methodology can be summarized as follows:

A. The first step involves extending the plant state equations (5) and (6) to include the duty cycle among the state variables, by defining an auxiliary plant input. This formulation yields a third-order model and ensures a smooth control variable, as discussed in the introduction.

B. Since ADRC relies on a model expressed in the Brunovsky canonical form, the second step consists of performing an exact feedback linearization of the extended third-order model. This transformation results in a linear, time-invariant model in Brunovsky form, where the new state variables are nonlinear functions of the original states, and the control input depends on both the auxiliary input and an equivalent endogenous disturbance.

C. The third step involves applying state-feedback control to the linearized Brunovsky model, which is fully controllable. Implementation of this controller requires knowledge of the state variables and their derivatives. These quantities, together with the equivalent disturbance introduced in Step B, are estimated using a Linear Extended State Observer (LESO).

D. Finally, to enhance robustness against parametric and modeling uncertainties, LESO estimation errors, measurement noise, and supply voltage variations, a sliding-mode control component is incorporated into the overall controller design to obtain the full robustness against parameter variations, unmodeled dynamics, and exogenous disturbances.

These steps are declined in the following subsections.

3.1. Exact linearization of the single-phase equivalent boost model

In this paper, linearization is applied to the dynamic model of the converter with an integral-type dynamic input, assuming $r_L = 0$. This model presents advantages due to the influence of the integrator (see (Fossen & Strand, 1999)). The extended state-space model for the single-phase equivalent boost converter with a dynamic integral input is derived by expanding the state of model (5) and (6) with the addition of the following equation:

$$\dot{\lambda} = \delta, \tag{10}$$

Here, δ serves as the auxiliary input. This approach treats the converter control variable λ as a third state variable. The control variable λ is subsequently obtained by integrating the auxiliary control input δ, allowing for effective filtering of its high-frequency components. The extended state-space model consists of (5), (6) and (10), where the state variables of the extended model are i_L, v_C and λ, while δ is the auxiliary control input. The output variable is v_C. In this way, a smooth duty-cycle is obtained as the integral of the auxiliary input δ, with the aim of attenuating possible discontinuities present in δ.
Defining:

$$z_1 = Cv_C^2 + Li_L^2, \tag{11}$$

as the output of the linearized model, the Brunovsky canonical form can be written as follows:

$$\dot{\boldsymbol{z}} = \boldsymbol{A}_z\boldsymbol{z} + \boldsymbol{b}_z\mu \tag{12}$$

$$y_z = z_1 \tag{13}$$

where:

$$\boldsymbol{A}_z = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix}, \boldsymbol{b}_z = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix},$$

$$\mu = \alpha\delta + \eta, \tag{14}$$

$$\alpha = 2\left(\frac{V_{in}}{L} + \frac{2}{RC}i_L\right)v_c, \tag{15}$$

$$\eta = \frac{8}{R^2C}v_C\dot{v}_C - 2(1-\lambda)\left(\frac{V_{in}}{L}\dot{v}_C + \frac{2}{RC}(\dot{v}_C i_L + v_C\dot{i}_L)\right). \tag{16}$$

where η is considered as an endogenous disturbance.

3.2. Control strategy for the linearized model

The previously introduced Brunovsky canonical form is controllable and results in the following input-output model:

$$\dddot{y}_z = \mu. \tag{17}$$

The control law for the model in (17) is derived from the following result.

Theorem 1. *The control law given by:*

$$\mu = \dddot{z}_{1,ref} - \gamma_{z2}(\ddot{z}_1 - \ddot{z}_{1ref}) - \gamma_{z1}(\dot{z}_1 - \dot{z}_{1ref}) - \gamma_{z0}(z_1 - z_{1ref}). \tag{18}$$

where $z_{1ref} = Cv_{C,REF}^2 + LI_L^{*2}$, and I_L^{*2} are obtained by means of (7) and (9) putting $V_C^* = v_{C,REF}$. Eq. (18) induces asymptotic stability to dynamics (17) if the polynomial $(s-\omega_c)^3 = s^3 + \gamma_{z2}s^2 + \gamma_{z1}s + \gamma_{z0} = 0$ is Hurwitz; ω_c is a free-parameter to be chosen.

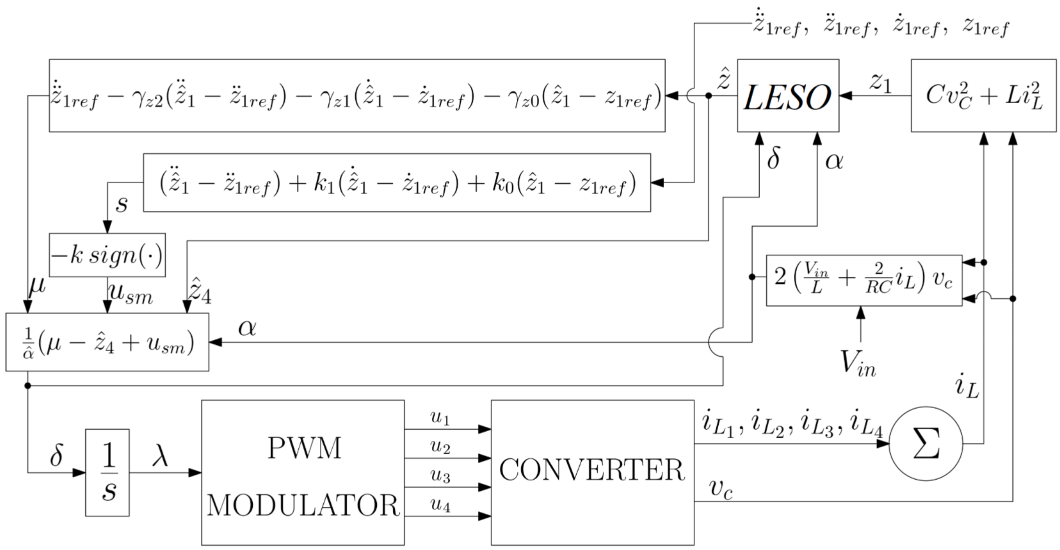

Fig. 2. Block diagram of the proposed control algorithm.

Proof. Putting $e_{yz} = y_z - y_{z,ref}$, substituting (18) into (17), the following equation is obtained:

$$\dddot{e}_{yz} + \gamma_{z2}\ddot{e}_{yz} + \gamma_{z1}\dot{e}_{yz} + \gamma_{z0}e_{yz} = 0, \tag{19}$$

which implies that $\lim_{t\to\infty} e_{yz} = 0$ if the hypothesis is met. □

Since the aim is to determine the plant input δ by inverting (14):

$$\delta = \alpha^{-1}(\mu - \eta), \tag{20}$$

it is also necessary to estimate the disturbance η. These objectives can be achieved using a Linear Extended State Observer. The LESO for (12), with extended state assuming $z_4 = \eta$, is given by:

$$\dot{\hat{z}}_1 = \hat{z}_2 + \epsilon^{-1}\beta_1 e_z, \tag{21}$$

$$\dot{\hat{z}}_2 = \hat{z}_3 + \epsilon^{-2}\beta_2 e_z, \tag{22}$$

$$\dot{\hat{z}}_3 = \hat{z}_4 + \epsilon^{-3}\beta_3 e_z + \alpha\delta, \tag{23}$$

$$\dot{\hat{z}}_4 = \epsilon^{-4}\beta_4 e_z. \tag{24}$$

Here, $e_z = z_1 - \hat{z}_1$, and the parameters β_i, $i = 1,\dots,4$, are typically chosen as the coefficients (in descending order) of the polynomial $(s - \omega_0)^4$, where ω_0 is an appropriately selected parameter (see (S. S.-T. Yau & Gao, 2007)). Furthermore, in (Guo & Zhao, 2011), it is shown that if $|\eta|$ and $|\dot{\eta}|$ are bounded, the estimation error of the LESO converges asymptotically uniformly to zero. Note that $\hat{z}_4$ represents the estimated value of η.

3.3. Sliding mode component design

The ADRC control law is a powerful tool for controlling both linear and nonlinear uncertain systems, but it has two inherent limitations: (1) performance degradation due to errors in estimating the total disturbance η, and (2) uncertainty in the control gain α. These issues have not been explicitly addressed in existing literature for power converters control, and as already said, are the robustness requirements presented in this paper.

Estimation errors in η can arise because the control input δ is applied through the uncertain gain α, and because the disturbance estimation relies on signals like v_c and i_L, which are affected by noise and biases. While the LESO shows robustness in estimating z_1, errors in the measured signals propagate to all estimated states, including the disturbance. The second issue is more critical: since the control input is scaled by α, variations in this parameter cannot be compensated by the LESO and thus affect control performance. Prior work (e.g., (Han, 2009)) considers limited variations of α ($\pm 50\%$), but in practical scenarios, such as control with variable input voltage, α may vary by a factor of 2–3 or more, since it depends on the circuit parameters, including the supply voltage V_{in} and the state variables v_C and i_L. This necessitates a specific strategy to ensure robustness.

In the following, we propose a solution that explicitly addresses both sources of uncertainty and provides a theoretical justification for its effectiveness. Based on the above considerations, the basic ADRC has been enhanced by incorporating a sliding mode control component into the existing control law (20), to address the two previously mentioned limitations.

Assumption 1. It is assumed that the maximum error in the η is bounded, therefore:

$$\left|\tilde{\eta}\right| = \left|\eta - \hat{\eta}\right| \le \epsilon_\eta \left|\hat{\eta}\right|. \tag{25}$$

where $\hat{\eta}$ is the estimate of η.

Moreover, denoting α_m and α_M the minimum and the maximum values of α, $\alpha \in [\alpha_m, \alpha_M]$, assuming $\hat{\alpha} = \sqrt{\alpha_m \alpha_M}$ and $\beta = \sqrt{\alpha_M/\alpha_m}$, it follows that:

$$\frac{\alpha}{\hat{\alpha}} \in [\beta^{-1}, \beta]. \tag{26}$$

See (Slotine & Li, 1991) for further details. ⌟

Theorem 2. *Assume that the control input δ in (20) is replaced with the following:*

$$\delta = \frac{1}{\hat{\alpha}}(\mu - \hat{z}_4 + u_{sm}), \tag{27}$$

where μ is the control input (18) designed for the case of nominal η and α values and u_{sm} is:

$$u_{sm} = -\mathcal{K}\, sign(s), \tag{28}$$

$$s = \ddot{e}_{yz} + k_1\dot{e}_{yz} + k_0 e_{yz}, \tag{29}$$

where $e_{yz} = y_z - y_{z,ref}$, and k_0 and k_1 are such that the polynomial $s^2 + k_1 s + k_0 = 0$ is Hurwitz. If the gain $\mathcal{K}$ is designed as follows:

$$\mathcal{K} \ge |\mu - \hat{z}_4| + \epsilon_\eta \beta |\hat{z}_4| + \beta|\hat{z}_4 + k_1\ddot{z}_1 + k_0\dot{z}_1 + \rho|, \tag{30}$$

with ϵ_η satisfying (25) and ρ is a positive constant, then the system (12) and (13) slides on the surface $s = 0$, for each value of the uncertainties satisfying Assumption 1. ⌟

Proof. By selecting as Lyapunov function $V(s) = \frac{1}{2}s^2$, its derivative is $\dot{V}(s) = s\dot{s}$ and it is negative definite if the following inequality holds:

$$\dot{s}\mathrm{sign}(s) \le -\rho. \tag{31}$$

for any positive constant ρ,

Inequality (31) is satisfied if $\mathcal{K}$ is chosen such that

$$\mathcal{K} \geq |\mu - \hat{z}_4| + \epsilon_\eta \beta |\hat{z}_4| + \beta |\hat{z}_4 + k_1 \ddot{z}_1 + k_0 \dot{z}_1 + \rho|, \tag{32}$$

where parameter ϵ_η is determined by assuming that $\frac{|\eta - \hat{\eta}|}{|\hat{\eta}|} \leq \epsilon_\eta$, and if the derivatives of $y_{z,ref}$ are assumed zero. □

Theorem 2 is crucial as it provides a rigorous method to design a robust control input that addresses the issues discussed earlier, particularly when $\frac{\alpha}{\hat{\alpha}}$ varies within the range (26) and the disturbance estimation error $|\tilde{\eta}|$ satisfies (25). The proposed conditions are specifically developed for the target application.

Remark 1. As mentioned above, the duty cycle λ is obtained by integrating δ. This implies that the duty cycle does not contain discontinuous terms like in the classical sliding mode controllers, because the term u_{sm} will be integrated over time to generate λ. For this reason, the proposed technique does not suffer from the most common problems related to the sliding mode control, like chattering and excessive stress on the system due to a highly discontinuous input. ⌟

Remark 2. There two ways to satisfy condition (32): using a conservative upper bound for $\mathcal{K}$, ensuring robustness under all conditions but increasing chattering; or adopting a time-varying $\mathcal{K}$ based on parameter variations and estimated/measured state values. This work adopts the second approach. Notably, $\mathcal{K}$ depends only on known quantities like nominal values of α or η and known bounds given in Assumption 1. ⌟

The block diagram of the proposed control algorithm is illustrated in Fig. 2. Note that once λ is determined, it is applied uniformly across all N-phases of the interleaved boost converter. Each phase's period is appropriately delayed by T_s/N seconds, where T_s is the modulation period and N represents the number of phases.

3.4. Comparison with other approaches

The approach illustrated so far, directly gives the duty-cycle as the control variable; this allows the implementation of the control of the interleaving boost converter at constant switching frequency. Other papers use sliding mode techniques for designing a control law and carry out the implementation of the control at a fixed switching frequency. In this way, the duty-cycle is determined by applying the equivalent control method. However, the dynamic behavior degrades with respect to that obtained under sliding mode control (see (Tan et al., 2005).

Model predictive control is based on the knowledge of a model of the plant under study. Consequently, if the parameters are not perfectly known, there exist unmodeled dynamics, and the input voltage varies during operations, the performance degrades and the robustness is not guaranteed.

The control techniques based on feedback exact linearization are very sensitive to the parametric uncertainties that cannot be compensated. This occurs in both the coordinate transformation that brings to the linearized model, and the online disturbance computation based on the model. As for the MPC technique, the robustness property cannot be guaranteed (see (Yu et al., 2021; Zhao et al., 2020)).

ADRC control technique could be robust against the parametric uncertainties if the model of the plant is directly in the Brunovsky canonical form, either without disturbance or a disturbance exogenous, i.e. independent of the parameters of the plant, including the input supply voltage. Unfortunately, the plants of the real world are described by models having more general forms. In these cases, it is necessary to manipulate the model in order to obtain the Brunovsky canonical form. Based on the above considerations, this prevents the robustness property to be reached. The control method described in this paper allows to overcome the problem in question including the additional sliding mode control component.

Finally, the PID-type controller was one of the first controller proposed in the literature. This controller can be designed using a linearized model of the boost obtained using the low signal approach. In the present paper, with the aim of compare the controller designed as shown in the previous Sections with a standard controller used in industrial environment, it is designed a PI controller. The parameters of this controller are chosen using the classical frequency domain approach. However, the implementation of the family of PID-type controller leads to a poor dynamics of the closed loop control system, with either an under-damped oscillating response with overshoot, or over-damped slow step response (see (Saadi et al., 2023; Saurav & Ghosh, 2022; Scirè et al., 2020)).

4. Experimental set-up

This Section presents the experimental setup built to validate the proposed controller. In Fig. 1, the converter under test is shown, while Fig. 2 illustrates the block diagram of the implemented control algorithm. A view of the overall test bench is provided in Fig. 3. Furthermore, Table 2 shows the components used in the experiments, along with their corresponding values. The same Table shows the experimental values for the input voltage V_{in} and the target value for the output voltage $v_{C,}$.

The proposed controller includes several free parameters, ω_c, ω_o, ϵ, ϵ_η, and ρ, whose selection criteria are summarized below and in Table 1: Starting with ρ, as discussed in (Slotine & Li, 1991), this parameter determines the time required for the system trajectories to reach the sliding surface $s = 0$. The reaching time is inversely proportional to ρ. Since ρ directly influences the gain $\mathcal{K}$, it must be tuned carefully to avoid introducing excessive ripple into the output voltage dynamics. The LESO parameters ω_o and ϵ shape the observer dynamics, estimation accuracy, and the amplitude of high-frequency components affecting the estimated signals. Increasing ω_o improves the transient response but also amplifies high-frequency noise. Conversely, reducing ϵ enhances the estimation accuracy of both the derivative of z_1 and the endogenous disturbance. However, ϵ cannot be chosen too small, as this would trigger the peaking phenomenon; indeed, peaking becomes significant when ϵ is sufficiently small. The final values of these parameters were determined using the equivalent conventional-boost model, by applying a step variation of λ corresponding to the desired output voltage and evaluating the estimation error, defined as the difference between the measured and estimated values of z_1 during the transient. The parameter ϵ_η was selected such that the absolute difference between the disturbance and its estimate is roughly 40% of the estimated value. Under nominal operating conditions, this assumption was validated: simulation results showed that ϵ_η, computed according to (25), converges to values well below 0.4 within a few milliseconds. Finally, the bandwidth of the state-feedback controller, ω_c, dictates the dynamic performance of the overall control system. As with ω_o, increasing ω_c improves the dynamic response but also introduces additional high-frequency content into the output voltage. The chosen value therefore reflects a balance between dynamic performance and sensitivity to noise.

The controller's implementation took place on the F28379D LaunchPad development kit, tailored for the C2000 Delfino MCU by Texas Instruments. This kit serves as an evaluation and development platform for the TMS320F28379D microcontroller, chosen for its 32-bit architecture and the presence of a dedicated co-processor, known as the Control Law Accelerator (CLA), capable of fast floating-point computations. The control algorithm is executed at a switch frequency of 100 kHz by the CLA. In contrast, tasks without stringent timing requirements are delegated to the main CPU. The algorithm's source files were generated using Matlab-Simulink software. MOSFET gates are controlled, through a driver, by the processor's PWM generator modules. The output voltage (v_C) and the input current (i_L) are sampled through LEM Hall-effect sensors installed in an appropriately designed signal conditioning board.

Five tests were conducted to validate the proposed control strategy, named $Test_{1,2,3,4,5}$. Each of the five tests evaluated performance under

Table 1
Qualitative effect of controller parameter variations on the converter behavior.

Parameter	Role	Increase	Decrease
ρ	Boundary condition in (31)	Faster convergence of s to zero; faster output voltage dynamics	Slower convergence of s to zero; slower output voltage dynamics
ω_o	LESO bandwidth	Faster estimation dynamics; increased noise	Slower estimation dynamics; decreased noise
ϵ	LESO tuning parameter	Lower estimation accuracy; reduced peaking	Higher estimation accuracy; risk of peaking
ϵ_η	Upper bound of relative disturbance estimation error	More conservative disturbance error compensation	Less conservative disturbance error compensation
ω_c	Controller bandwidth	Faster controller dynamics; faster output voltage dynamics	Slower controller dynamics; slower output voltage dynamics

Table 2
Electrical component values.

Name	Value	Model	Description
$L_{1,2,\ldots,N}$	47 μH	Wurth E. 7443763540470	Inductors
L_{Test_5}	10 μH	Coilcraft MSS1278-103	Auxiliary inductor for $Test_5$
$D_{1,2,\ldots,N}$		Bourns BSDW20S65C6	SiC Diodes
$Q_{1,2,\ldots,N}$		Cree C3M0065090	SiC Mosfet
R	20 Ω		Load Resistor
C	42 μF		Capacitor bank
V_{in}	60 V		Input Voltage
$v_{C,REF}$	120 V		Reference Output Voltage

Table 3
IAE and ISE indexes in $Test_{1,3,4,5}$.

TEST		v_C		i_L	
		IAE	ISE	IAE	ISE
1- Startup	ADRC	0.419	16.17	8.22	741.4
	ADRC-SM	0.329	11.53	8.20	738.1
	PI	0.661	21.20	8.26	751.02
3- R down	ADRC	0.0173	4.8	10.55	1115
	ADRC-SM	0.0162	4.4	10.52	1113
	PI	0.0180	5.1	10.59	1116
4- v_C down	ADRC	0.0218	9.01	10.583	1120
	ADRC-SM	0.0215	8.88	10.576	1118
	PI	0.0219	9.02	10.627	1129
5- L up	ADRC	0.4976	18.54	8.97	823.73
	ADRC-SM	0.3951	13.23	8.95	819.89
	PI	0.7614	24.29	9.02	834.67

a specific operating condition. In more detail, $Test_1$ was conducted to assess the response to applying a step reference; $Test_2$ was aimed at evaluating steady-state behavior. $Test_{3,4,5}$ are robustness tests to parametric variations, specifically conducted to evaluate the performance of the converter when a variation in the input voltage V_{in} (from 60 V to 50 V) occurs, when a change in the load resistance R (from 20 Ω to 15 Ω) occurs and when a change in the inductance value (from 47 μH to 57 μH) occurs in one of the four converter inductors. During $Test_{1,3,4,5}$, three different experiments were carried out to demonstrate the behavior of the converter under the assumption that the sliding mode component of the control law is either present or disabled. Additionally, another test was conducted using a classical PI controller to compare its performance with our proposed approach. For these tests, the waveforms corresponding to the controller without the sliding mode component, named ADRC, are shown in blue, while those obtained by adding the sliding mode component, named ADRC-SM, are depicted in orange. Additionally, the waveforms related to the PI controller, named PI, are represented in yellow. The dashed lines indicate the desired behavior. The graphs of the acquired waveforms and the related comments are provided in the following section.

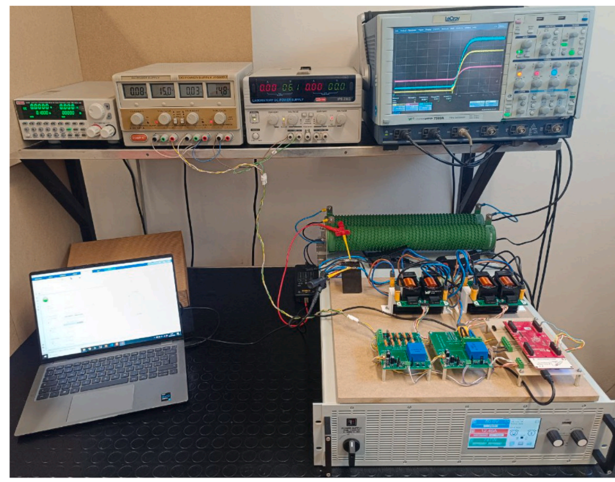

Fig. 3. Equipment and setup used for the testing.

5. Experimental results

This Section gives experimental results for $Test_{1,2,3,4,5}$. To quantitatively assess the control performance for $Test_{1,3,4,5}$, two standard performance indices are considered: the Integral of Absolute Error (IAE) and the Integral of Squared Error (ISE), defined respectively as

$$\text{IAE} = \int_0^{t_f} |e(\tau)| d\tau, \tag{33}$$

$$\text{ISE} = \int_0^{t_f} e^2(\tau) d\tau, \tag{34}$$

where $e(\tau)$ denotes the error between the reference signal and the actual output, and t_f is the duration of the observation. The IAE provides a measure of the overall tracking accuracy, weighting all deviations equally, while the ISE emphasizes larger errors due to the squared term, making it more sensitive to transient deviations.

The results obtained are shown in Tables 3, and 4 and discussed throughout this section.

The results of $Test_1$ are reported in Fig. 4 with a focus on the converter's power-on operation. The startup sequence was triggered to turn on at $t = 1$ s. The graph includes two subplots: the upper one shows the dc-bus voltage v_C while the lower one shows the input current i_L for the three control approaches ADRC, ADRC-SM, PI. The color convention (blue for ADRC, orange for ADRC-SM, and yellow for the PI) is maintained throughout the subsequent figures. From the analysis of Fig. 4, it is evident that the introduction of the sliding mode action significantly improves the system's dynamic response. Specifically, using a classical PI controller results in a settling time of approximately 35 ms, but with a noticeable and pronounced initial overshoot in both voltage and current. With the proposed control approach, but without the sliding mode component, the settling time is reduced to about 20 ms. Further improvement is achieved by adding the sliding mode component, which decreases the settling time to approximately

Table 4
Settling time, startup overshoot and startup undershoot in $Test_{1,3,4,5}$.

TEST		v_C			i_L		
		Settling time (ms)	Startup overshoot (%)[a]	Startup undershoot (%)[a]	Settling time (ms)	Startup overshoot (%)[b]	Startup undershoot (%)[b]
1- Startup	ADRC	15	-	-	15	-	-
	ADRC-SM	20	-	-	20	-	-
	PI	35	4.2	-58	35	7.1	-80
3- R down	ADRC	15	-	-	15	-	-
	ADRC-SM	15	-	-	15	-	-
	PI	15	-	-	15	-	-
4- v_C down	ADRC	20	-	-	20	-	-
	ADRC-SM	25	-	-	25	-	-
	PI	40	-	-	40	-	-
5- L up	ADRC	17	-	-	17	-	-
	ADRC-SM	22	-	-	22	-	-
	PI	37	-	-	37	-	-

[a] Percentage referred to $v_{C,REF}$.
[b] Percentage referred to I_L^*.

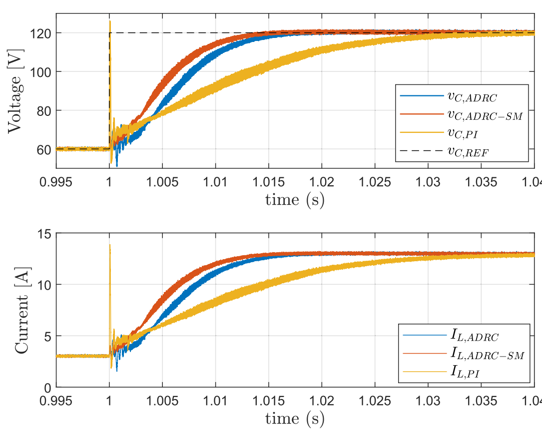

Fig. 4. Output voltage v_C and input current i_L, with and without sliding mode and with PI during a startup sequence in $Test_1$.

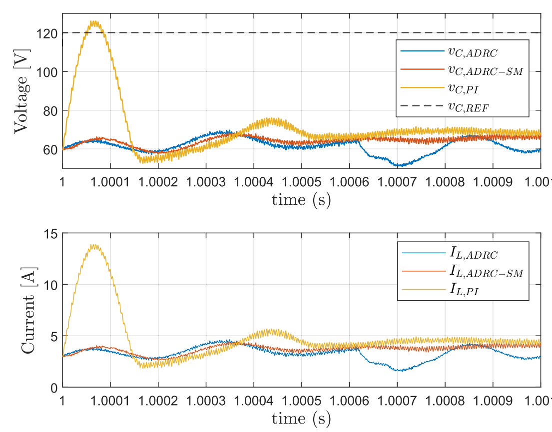

Fig. 5. Zoomed depiction of output voltage v_C and input current i_L, with and without sliding mode and with PI during a startup sequence in $Test_1$.

15 ms. Regarding the input current i_L, improved performance is observed in the test with the sliding component added, as there is no overshoot in this case. This behavior also reduces ohmic losses in the inductors. Similarly, the reduced overshoot in the output voltage limits the stress on the output capacitor, enhancing the overall reliability of the converter. $Test_1$ further demonstrates that, once the transient is over, the output voltage v_C stabilizes at the desired value of 120 V, while the input current i_L settles around 13 A.

A detailed analysis of the first millisecond is reported in the zoomed transient in Fig. 5 reveals that the voltage and current overshoots observed in the case of the PI controller are primarily due to the inherent response of the regulated system during the initial transient. These overshoots arise from the combined effect of the proportional action and the duty-cycle saturation within the interval [0.01, 0.8], which temporarily drives the output voltage above its reference before the integral action compensates for the excess. Differently, the responses obtained with the ADRC and ADRC-SM controllers do not exhibit such overvoltage or overcurrent behavior. This confirms the capability of the proposed control schemes to ensure smooth and well-damped transients, representing a significant performance advantage over conventional PI control.

The analysis of the IAE and ISE indices in Table 3 confirms that the proposed ADRC-SM solution, achieves the best values for both indices, followed by the ADRC one and the PI.

Fig. 6 shows the data collected from $Test_2$, in which we examine the converter's performance in a steady state. This figure presents the waveforms for the output voltage v_C, the input current i_L, and a detailed view of the four input currents $i_{L1,2,3,4}$. In the first subplot, focusing on the output voltage, it is noted that the target value is maintained with a ripple of less than 1 V. The output current i_L stabilizes and remains constant at about 13 A, corresponding to the equilibrium value I_L^* as calculated from (7) and (8) setting $V_C^* = v_{C,REF}$. The third subplot illustrates the behavior of the input currents; in this chart, it is observable that these triangular currents fluctuate slightly over a range from just above 0 to 6 A and have a period of 10 μs, which aligns with the 100 kHz frequency of the PWM modulator. It is important to note that, in this figure, the time scale is more condensed specifically to highlight the waveform shapes of the currents $i_{L1,2,3,4}$, which would not be visible on a larger scale.

Fig. 7 shows the waveforms captured in $Test_3$ for all three scenarios: ADRC, ADRC-SM, PI. In this Test, at $t = 1$ s, the load resistance is reduced from the initial value of 20 Ω to 15 Ω. The upper subplot shows the output voltage v_C. Regarding the upper plot, which shows the voltage v_C, the behavior is similar in all three cases, with an undershoot of about half a volt. Looking at the lower subplot, which is related to the input current i_L, it is noted that this current reaches the new steady-state value (around 16.5 A) in approximately 15 ms for all three solutions: ADRC, ADRC-SM, and PI. However, ADRC-SM exhibits the lowest values for the IAE and ISE indices for i_L and v_C.

An overshoot of about 1.5 A is detected in the Test with the PI controller. The overall analysis of this figure, in addition to confirming the

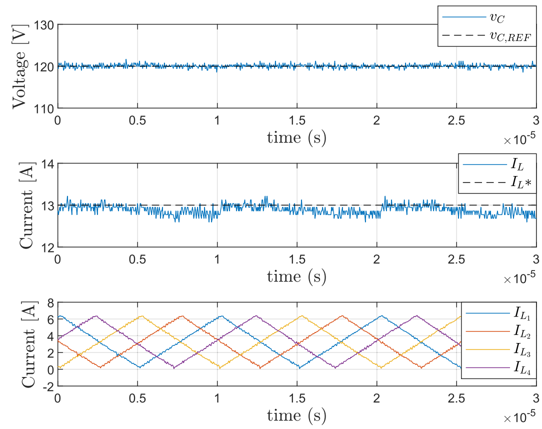

Fig. 6. Output voltage v_C, input current i_L, and input current for each of the 4 stages $i_{L1,2,3,4}$ at steady state in $Test_2$.

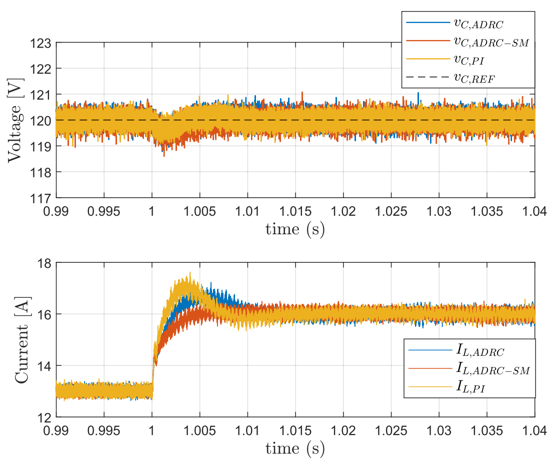

Fig. 7. Output voltage v_C and input current i_L, with and without sliding mode and with PI during a load variation in $Test_3$.

control scheme's robustness against parametric variations, demonstrates the clear performance improvement achieved with the introduction of the sliding mode component.

Fig. 8 shows the behavior of the converter for all three scenarios: ADRC, ADRC-SM, PI, when the input voltage V_{in} experiences an undesirable decrease of 10 V from the nominal value of 60 V. The upper plot shows the trend of the output voltage v_C, where no significant differences can be observed in either the undershoot (approximately 1 V) or the recovery time to the reference value (around 15 ms) for all three scenarios. This behavior is also evident from the analysis of the performance indices in Table 3, which highlights similar results. On the other hand, the lower subplot reveals that the current trend differs among the three implemented strategies. Specifically, the PI solution exhibits no overshoot but recovers the new equilibrium state in approximately 40 ms, while the ADRC and ADRC-SM solutions do so in about 25 ms and 20 ms, respectively. The trends related to our proposed controller show limited overshoot. However, the analysis of the performance indices suggests that the ADRC-SM solution achieves the best overall results.

Finally, Fig. 9 shows the trends in the three scenarios when one of the inductors in the four-stage interleaving converter undergoes a variation. Specifically, by observing the trends, they appear similar to those observed in the startup test. However, since the converter operates in an unbalanced condition, a general performance degradation is expected, which manifests as an increase in ripple (both in the voltage v_C and the current i_L) and an increase in the step response time. This performance

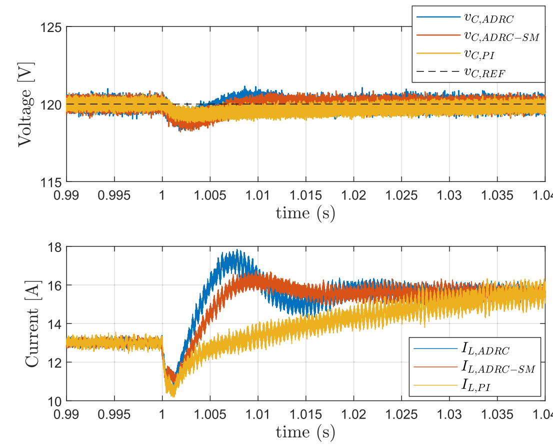

Fig. 8. Output voltage v_C, input voltage V_{in} and input current i_L, with and without sliding mode and with PI during input voltage variation in $Test_4$.

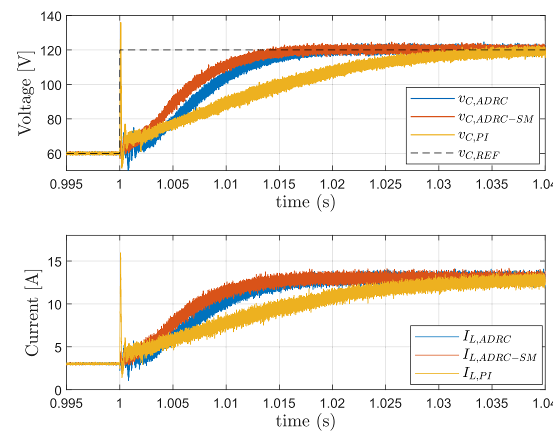

Fig. 9. Output voltage v_C, input voltage V_{in} and input current i_L, with and without sliding mode and with PI during Inductor variation in $Test_5$.

degradation is also evident when analyzing the indices in the table between $Test_5$ and $Test_1$. Nevertheless, the proposed ADRC-SM control strategy consistently achieves better results, once again confirming the robustness of the proposed control strategy.

As confirmed by the experimental waveforms here reported, the smoothness of the control variable λ is effectively achieved by the proposed ADRC-SM approach. Although the auxiliary control input δ includes high-frequency components due to the structure of the controller and the sliding-mode term, their effect on λ is attenuated by the integration process. Conversely, in the PI controller, the proportional term directly transfers high-frequency components from the voltage-error signal to λ, resulting in higher ripple in the control and output voltage. This explains the reduced ripple observed in the ADRC-SM case and supports the considerations outlined in Remark 1.

6. Conclusion

A robust nonlinear control strategy has been designed for an interleaved boost converter, utilizing extended linearization, active disturbance compensation, and a sliding mode element to improve the closed-loop system's robustness. An experimental setup consisting of a four-phase interleaving converter was developed to validate the proposed controller. Five different types of tests were conducted to evaluate the performances under a specific operating condition: (i) step reference, (ii) steady-state behavior, (iii) input voltage variations, (iv) parametric variation of the load resistance, and (v) parametric variation of the inductance. The converter behavior was analyzed considering that the sliding mode component of the control law is either present or disabled. Through these tests and comparisons, the effectiveness of the proposed control solution was highlighted; furthermore, the addition of the sliding mode component improved the system's behavior in terms of dynamic precision, even in the presence of disturbances.

The experimental campaign was deliberately structured to investigate the most critical operating conditions expected in practical applications, focusing on wide variations of system parameters and operating points. Changes in the input voltage, load resistance, and inductance values were selected to assess the controller robustness against parametric uncertainties and plant variations that commonly arise in real converters. These tests provide a representative and meaningful validation of the proposed control strategy, demonstrating its ability to maintain stable operation and satisfactory dynamic performance over a broad operating range.

Furthermore, the proposed technique does not suffer from the most common problems related to the sliding mode control, like chattering and excessive stress on the system due to a highly discontinuous input. Hence, the outcomes demonstrate the suggested method's efficacy and robustness in parameter variations, encompassing tolerances in inductors and capacitors. Additionally, it preserves the benefits associated with the interleaved topology.

CRediT authorship contribution statement

Giovanni Garraffa: Writing – review & editing, Writing – original draft, Software, Investigation, Conceptualization; **Daniele Scirè:** Writing – review & editing, Writing – original draft, Methodology, Investigation, Conceptualization; **Francesco Alonge:** Writing – original draft, Formal analysis, Conceptualization; **Filippo D'Ippolito:** Writing – review & editing, Supervision, Resources; **Giuseppe Lullo:** Writing – review & editing, Validation; **Giuseppe Costantino Giaconia:** Writing – review & editing, Project administration, Funding acquisition; **Alessandro Busacca:** Writing – review & editing, Project administration, Funding acquisition; **Gianpaolo Vitale:** Writing – review & editing, Methodology, Conceptualization; **Antonino Sferlazza:** Writing – review & editing, Writing – original draft, Supervision, Investigation, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Funding

This research was funded by : - The SiciliAn MicronanOTecH Research and Innovation CEnter "SAMOTHRACE" (MUR, PNRR-M4C2, ECS_00000022), spoke 3-Università degli Studi di Palermo "S2-COMMs-Micro and Nanotechnologies for Smart & Sustainable Communities, - The European Project GaN4AP (Gallium Nitride for Advanced Power Applications). The project has received funding from the Electronic Component Systems for European Leadership Joint Undertaking (ECSEL JU), under grant agreement No.101007310. The work of Daniele Scirè and Antonino Sferlazza has been partially supported by the funding D26_PREMIO_GRUPPI_RIC_2022 from the Department of Engineering of the University of Palermo.

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