A simple DC-Link Voltage Balancing Strategy for NPC Three-level Inverters

Preferred Topic 1: Measurement, Supervision and Control for Power Converters
Preferred Subtopic 1: *Standard and Advanced Current / Voltage / Synchronization Control Techniques*

Origin: University of Messina

Preference*:* Poster Session

Keywords — «3-Level NPC», «Two-level inverters (TLIs)», «Capacitor voltage balancing», «Total Harmonic Distortion», «Pulse Width Modulation (PWM)».

Abstract — Three-level neutral point clamped PWM inverters overcome some limitations of two-level inverters in medium voltage applications, leading to lower device ratings and greater efficiency. However, they are burdened by an intrinsic drawback of the neutral point clamped structure, which causes, under some operating conditions, a voltage imbalance of the DC link capacitors. In this paper, such an issue is faced on a system driven by a dual-carrier PWM strategy through a simple hysteretic control. The proposed technique features a very low computational burden and does not need additional power circuits or sensors. It is first presented theoretically, then its performance is evaluated through simulations.

1. Introduction

Conventional two-level inverters largely dominate the field of low-voltage electric motor drives, however, three-level inverters are often preferred for equipping high-power, medium-voltage drives [1], HVDC transmission systems [2], STATCOM [3], active power filters [4], as well as wind and solar generation plants connected to medium voltage grids [5]. In fact, three-level inverters overcome some structural issues of two-level inverters when used in medium voltage applications, such as reduced efficiency and impractical voltage ratings of power devices. By partitioning the DC input voltage by two series connected dc-bus capacitors, the power devices equipping 3-Level NPC inverters must withstand only half of the total DC input voltage, resulting in lower voltage and thermal stress. Hence, the DC-link voltage can be made higher, thus reducing the DC-link current, phase conductor size and the associated losses. Compared with two-level PWM, three-level PWM operation achieves lower switching power losses, a lower output voltage THD and lower electromagnetic emissions. As a result, three-level inverters can operate not only at higher DC input voltages, but also at higher switching frequencies, than two-level inverters equipped with power devices of the same technology and with the same current rating. This is an essential advantage, because it not only allows to reduce the size and cost of the magnetic components and the cooling system, but also to achieve greater efficiency. Among the three-level inverter topologies developed over the last decades, the 3-Level NPC is one of the most popular, being the simplest and cheapest [6], [7]. Thanks to these advantageous features, three-level NPC inverters have been recently used even on low voltage drive applications, successfully competing with two-level inverters [8]. However, an intrinsic issue of the 3-Level NPC inverter structure hindering a wider usage, is the occurrence of a fluctuation of the voltage of the Neutral Point (NP), which is the point of connection of the two dc link capacitors [8]. -A neutral point voltage oscillation at three times the frequency of the output voltage is structural on 3-Level NPC inverters, being correlated to voltage clamping and three level operation. ―This oscillation leads to unsatisfactory operation, because deteriorating the output ac voltage waveform, which exhibits low-order even harmonics, moreover, it causes unbalanced voltage stress on the power devices and increased output current ripple, which may lead to unexpected inverter failures [9]. Neutral point voltage drifts may also occur, caused by difference on parameters of dc link capacitors and power switches as well as by unbalanced load operation. -A reasonably equal voltage sharing between the two dc link capacitors must be guaranteed to obtain on 3-Level NPC inverters the best possible performance. The simplest way to achieve it being the use of large dc link capacitors [8]. However, this easily leads to unacceptably bulky and expensive capacitors, powering the development of active neutral point voltage control approaches. These can be grouped into two categories: techniques based on additional power circuits and techniques exploiting purposely modified PWM strategies. The neutral-point voltage can be controlled through two additional power converters managing the voltage of the dc link capacitors; however, this requires the introduction of extra power devices, transformers and control systems, which increase the cost and complexity of the inverter [10]. –Hence the control of the neutral point voltage through purposely developed PWM strategies has gained great interest, being cheaper and more efficient [11]. The basic principle of these techniques is to measure the actual capacitor voltages and then select a proper switching path to correct the voltage imbalance. They can be divided into two groups, being derivative

of basic space-vector (SV) and carrier-based (CB) techniques. In SV based techniques, which are widely used in machine drive applications [12]-[14], dc link voltage balancing is achieved by properly selecting redundant voltage vectors on the basis of the amplitude of the voltage imbalance and the direction of the current circulating through the neutral point. Even effective, these techniques are however characterized by a high computational burden. CB techniques generally feature a lower computational burden [15]-[19]. They rely on addition of zero-sequence components to the output AC voltage reference to regulate the charging and discharging of the dc-bus capacitors. This is achieved by acting on the voltage reference or on carrier signals. Both SV and CB based techniques require information on dc link capacitors voltage and phase current, leading to the introduction of voltage and current transducers, that would not otherwise be required in several applications, such as motor drives using scalar volt/hertz control. In this paper, a simple neutral point voltage control strategy for 3-Level NPC inverters is described requiring no voltage or current transducers, moreover, being mainly based on analog electronic circuits, the additional computation burden is negligible, so it can be implemented even on systems equipped with cheap microprocessors. The proposed technique is based on preventing the occurrence of null voltage switching combinations, which are responsible for the variation of the neutral point voltage, every time that this exceeds some predefined thresholds. The proposed technique negligibly impacts on output voltage THD and is able to limit the magnitude of the oscillation of the neutral point voltage, as well as to compensate for any drift of its mean value. The effectiveness of the proposed technique in controlling the neutral point voltage on a system driven by a dual carrier CB PWM strategy is demonstrated through simulations.

2. 3-Level NPC inverter operation

A 3-Level NPC inverter is depicted in Fig. 1, the DC-link is splitted into two buses by means of a voltage divider composed of two series-connected capacitors C_H and C_L. Each leg features four switches and two diodes whose common point is connected to the common point of the two DC-link capacitors. As shown in Table 1, three switching combinations are possible for a generic *j-phase* leg, namely P, N and O, respectively giving a leg output voltage equal to $V_{DC}/2$, $-V_{DC}/2$ and *0*. In the P combination, S_{j1} and S_{j2} are turned on, in the N combination S_{a3} and S_{j4} are turned on while the O combination is obtained by turning on the switches S_{j2} and S_{j3}.

As shown in the vector diagram of Fig. 2 a total of *27* (3^3) switching combinations are possible on a three-phase 3-Level NPC inverter, out of which three are null or zero vectors and 24 are active vectors. The *24* active voltage vectors can be in turn grouped into *12* small vectors, *6* medium vectors and *6* large vectors, respectively featuring a voltage vector of magnitude $V_{dc}/3$, $\sqrt{3}V_{dc}/3$ and $2V_{dc}/3$.

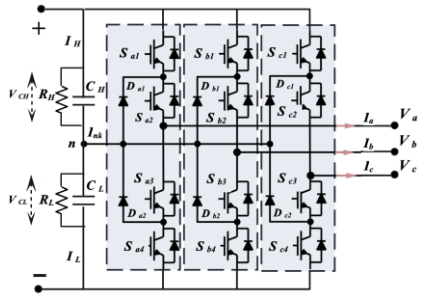

Fig. 1: Schematic of a three-phase 3-Level NPC inverter

TABLE 1: 3L NPC inverter leg

Switching combination					Pole Voltage	On-state devices	i_{nj}
	S_{j1}	S_{j2}	S_{j3}	S_{j4}			
P	*ON*	*ON*	*OFF*	*OFF*	$+V_{DC}/2$	$i_j>0$ S_{j1}, S_{j2} $i_j<0$ D_{j1}, D_{j2}	*0*
O	*OFF*	*ON*	*ON*	*OFF*	*0*	$i_j>0$ D_{j1}, S_{j2} $i_j<0$ D_{j2}, S_{j3}	i_j
N	*OFF*	*OFF*	*ON*	*ON*	*-Vdc/2*	$i_j>0$ D_{j4}, D_{j3} $i_j<0$ S_{j3}, S_{j4}	*0*

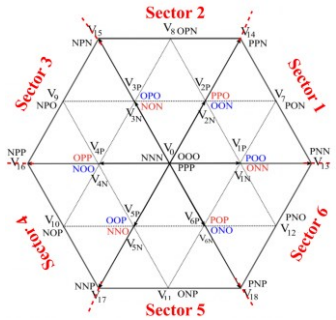

Fig. 2: Voltage vector diagram for a 3-Level NPC converter

The clamping diodes D_{j1} and D_{j2}, are connected to the DC link neutral point *n*, to limit the maximum voltage sustained by power switches to half of the DC-link voltage V_{DC}. However, in practice, the potential of the neutral point *n* is not stable, because the voltages of the two dc link capacitors V_{CH} and V_{CL} continuously oscillate around $V_{DC}/2$. In fact, if a positive current i_n circulates through the connection between the common point of the clamping diodes and the neutral point *n*, C_L is charged and C_H is discharged, while a negative i_n leads to charging C_H and discharging C_L. In each sector of the 3-Level NPC inverter voltage vector five types of vector combinations exist, which

have different effects on the gradient of the neutral point voltage V_n, as shown in Table 2 dealing with the vectors of the sector 1.

TABLE 2: Sector 1-Effects of voltage vectors on V_n

Voltage vector type	Switching combination	$d(V_n)/dt$
Null	PPP OOO NNN	*0*
Medium	PON	*≠0*
P-small	POO PPO	*≠0*
N-small	ONN OON	*≠0*
Large	PNN PPN	*0*

Neutral point voltage drift is caused by small and medium voltage vectors which include some O switching combinations, causing the circulation of the current i_n. Under the hypothesis that C_H=C_L=C it can be found that:

$$\frac{dV_n}{dt} = \frac{d(V_{CL} - V_{CH})}{dt} = \frac{1}{C} i_n = \frac{1}{C} \sum_{j=a,b,c} i_{nj} \qquad (1)$$

being i_{nj} the contribution of the j leg (j=a,b,c) to the current i_n, which is given by:

$$i_{nj} = i_j s_j \qquad (2)$$

where i_j=$I\sin(\omega t+\varphi)$ is the phase current and the duty cycle s_j (0<s_j<1) is defined as:

$$s_j = \frac{T_{Oj}}{T_s} \qquad (3)$$

where T_s is the inverse of the switching frequency and T_{Oj} the amount of time within T_s for which the j leg takes the switching combination O. The duty cycle s_j is given by:

$$s_j = 1 - m\,|sin(\omega t)| \qquad (4)$$

where: m=$2V_{ref}/V_{DC}$ (0<m<1) is the voltage modulation index.
Hence:

$$i_{nj} = I\sin(\omega t + \varphi)\left|1 - m\,|sin(\omega t)|\right| \qquad (5)$$

As shown in Fig. 3, under steady-state conditions the current i_{nj} exhibits an oscillation at the frequency of the reference voltage signal, or fundamental frequency, whose amplitude is a function of the amplitude of the phase current, the angular displacement φ between voltage and current -and of the modulation index [19]. This impresses an oscillation at three times the fundamental frequency to the current i_n. According to (1) the oscillation of i_n generates in turn a ripple on the neutral point voltage at three times the fundamental frequency, which is proportional to the magnitude of i_n and inversely proportional to the fundamental frequency and to the capacitance C of the dc link capacitors. Such an oscillation leads to additional voltage stress on the power switches and the rise of unwanted low-order even harmonics on the output voltage.

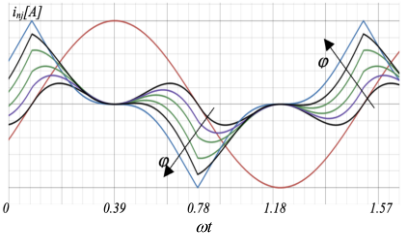

Fig. 3: Current i_{nj} (I= 50A, j=0÷1.57rad, m=0.8)

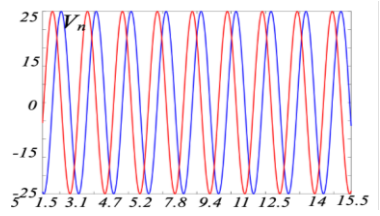

Fig. 4: (red) Current i_n, (blue) V_n (C=10 mF, I= 50A, φ=.7rad, m=0.8)

Moreover, a drift of the neutral point voltage can be generated by parametric differences between the dc link capacitors, causing different gradients of the voltages V_{CH} and V_{CL}, as well as, by the parametric spread of power switches, or by unbalanced load operation, which may lead to uneven i_{nj} current components.

3. Neutral Point Voltage Control

According to a dual carrier PWM approach, on a generic j leg during the positive fundamental half-period, the switch S_{j2} is kept on, while the output voltage is regulated by acting on S_{j1} and S_{j3}, thus generating a sequence of P and O switching combinations, as shown in Fig. 5. During the negative fundamental half-period instead the switch S_{j3} is kept on, while the output voltage is regulated by acting on S_{j2} and S_{j4}, leading to a sequence of N and O switching combinations. The occurrence of O switching combinations is the cause of the circulation of the current i_{nj} and, according to (1), of fluctuation of the neutral point voltage. Hence, the variation of the neutral point voltage can be avoided by preventing the occurrence of O switching combinations. This can be easily achieved by switching from three level PWM operation to a two-level switching strategy, as that of

Fig. 6, leading to a sequence of only P and N switching combinations.

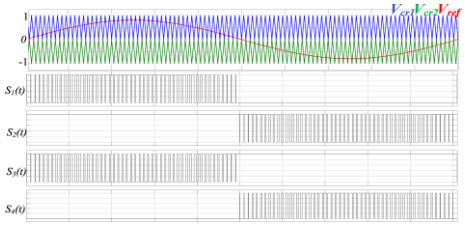

Fig. 5: Dual carrier, ~~three~~ three-level PWM.

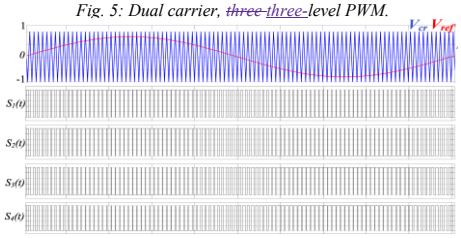

Fig. 6: Single carrier, ~~two~~ two-level PWM.

3.1 Attenuation of neutral point voltage oscillation

The magnitude of the fluctuation of the neutral point voltage at three times the fundamental frequency can be clamped to a given value by means of the hysteresis controller shown in Fig. 7.

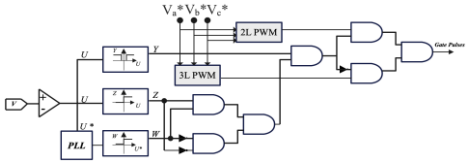

Fig. 7: Neutral point voltage hysteresis control.

When the neutral point voltage reaches the borders of the hysteresis band, the PWM is switched from three to two levels, leading to a null current i_n and so locking the neutral point voltage at half the width of the hysteresis band. When the first fourth of the period is reached over the positive half period, or the third one is reached on the negative half period, the hysteresis regulator is disengaged, and the inverter turns back to three-level operations. Periodical disengagement of the hysteresis regulator is obtained by exploitation of a signal V_{n90} in quadrature with the neutral point voltage ripple, obtained through a PLL system. The sign of V_n and V_{n90} signals are processed to detect the end of the first and third quarter of the period of the neutral point voltage ripple providing a synchronization, which while not required for ripple limiting, is essential to compensate for neutral point voltage drifts. In fact, it allows to differently act on positive and negative half-periods of the i_n waveform.

A schematic of the basic PLL system generating the quadrature signal V_{n90} is shown in Fig. 8.

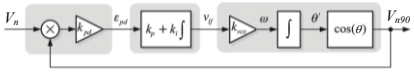

Fig. 8: PLL quadrature signal generator.

A peak limitation of the neutral point voltage waveform is then obtained, fully independent from operating conditions, and not affecting the phase current waveform, as it is shown in Fig. 9.

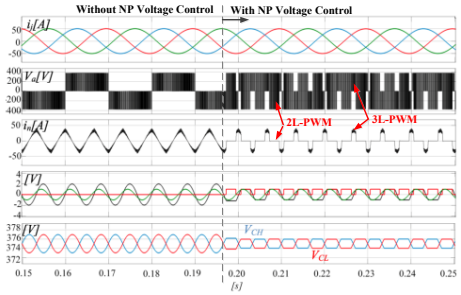

Fig. 9: Neutral point voltage oscillation peak control.

3.2 Compensation of neutral point voltage drift

Any drift of the neutral point voltage v_n is caused by a variation of the average value of the current i_n, which under ideal conditions is null. The proposed hysteretic regulator is able to compensate for any drift of the neutral point voltage by acting on the average current circulating through the neutral point. In fact, in case of a positive drift, the neutral point voltage waveform shifts upwards within the hysteresis band, causing an asymmetrical v_n peak limitation, the positive half-periods being cut down more than the negative ones. This results in an asymmetrical i_n waveform, featuring a negative mean value, which leads to a reduction of the average value of i_n. This in turn lowers the mean value of v_n, thereby compensating for the positive drift, as shown in Fig. 10. A similar automatic compensation takes place also in case of a negative drift of the neutral point voltage.

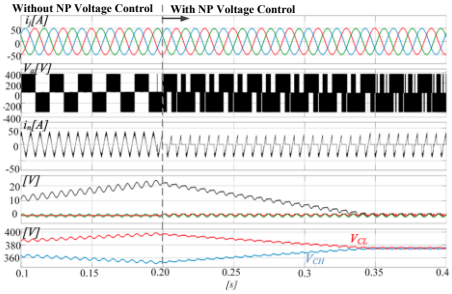

Fig. 10: Neutral point voltage drift compensation

4. Performance assessment

Simulations have been carried out using MATLAB-Simulink to assess the ~~consistence~~ consistency of the proposed approach in limiting the oscillation of the neutral point voltage and in compensating any drift. A 3-Level NPC converter is considered connected to a three-phase RL ~~wye~~ wye-connected load ($R=1\Omega$ and $L=10\text{-}20mH$). Inverter parameters are listed in Table 3.

Table 3: 3L NPC inverter parameters

Parameter	Value
V_{AC} (peak)	*325 V*
V_{DC}	*800 V*
C_H, C_L	*0.75 mF*
C_D	*10mF*
R_H, R_L	*200 Ω*

The proposed control technique can be implemented according to a mixed analog/digital approach, requiring no voltage, no~~r~~ current transducers. The neutral point voltage is simply achieved as the difference between the real neutral point n and a virtual one n' obtained through a capacitive voltage divider C_D, as shown in Fig. 11.

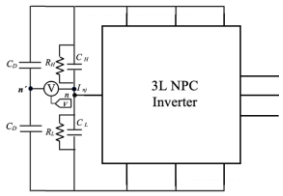

Fig. 11: Detection of the neutral point voltage.

In Figs. 12-14 simulations are shown dealing with the effect of the neutral point voltage ripple control when progressively increasing the load current from *10A* to *100A*. The higher the magnitude of the load current the more evident is the operation~~intervention~~ of the hysteretic control to keep within $\pm 15V$ the neutral point voltage ripple.

The inverter operating at *100A* without neutral point voltage control is shown in Fig. 15, a $\pm 50V$ ripple is generated. Phase voltage harmonic spectra are shown in Fig. 16 to compare the performance of the inverter with and without neutral point voltage control. In the ~~low~~ low-frequency range, the proposed technique performs better eliminating some harmful harmonics, as a result, the THD computed up to the 37th harmonic is 5.3% with voltage limitation and 7.9% without voltage limitation. Hence a ~~–~~2.6% reduction of the THD is achieved, however, at high frequency the harmonics generated by two-level modulation are higher than those achieved with the ~~three~~ three-level PWM. As shown in Fig. 17, two *2 mF* dc link capacitors are ~~–~~required to obtain without control a $\pm 15V$ ripple. Hence, thanks to the proposed control approach the dc link capacitors can be reduced up to *63%*. ~~–~~An optimal width of the hysteresis band than should be identified leading to an optimal trade-off between dc-link capacitance reduction and ~~high~~ high-frequency harmonics impact.

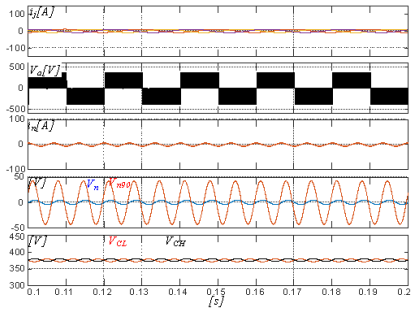

Fig. 12: V_n ripple control: 50Hz, 10A, ±15V hysteresis band.

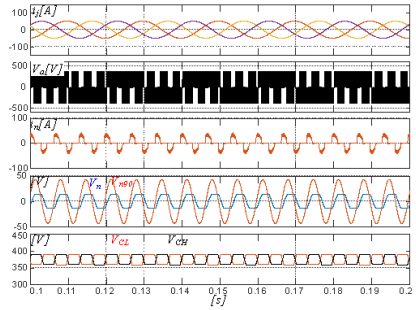

Fig. 13: V_n ripple control: 50Hz, 50A, ±15V hysteresis band.

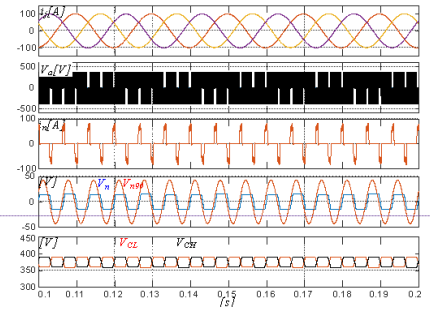

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Fig. 14: V_n ripple control: 50Hz, 100A, ±15V hysteresis band.

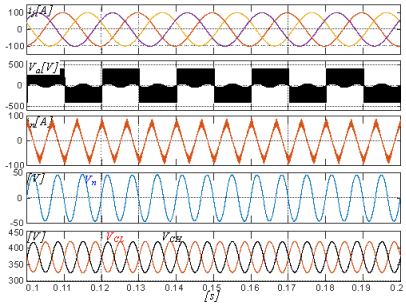

Fig. 15: No V_n control: 50Hz, 100A.

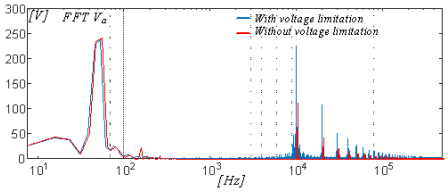

Fig. 16: Voltage FFT and THD with and without V_n control.

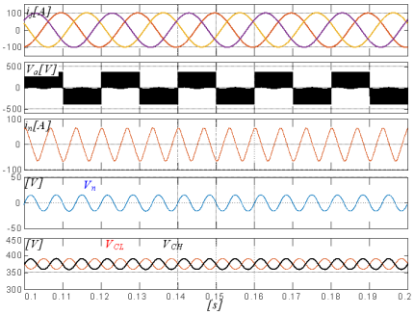

Fig. 17: No V_n control: 50Hz, 100A and C=2mF.

The proposed approach is effective not only at steady state, but also in case of speed and load variations, as shown in Figs. 18 and 19.

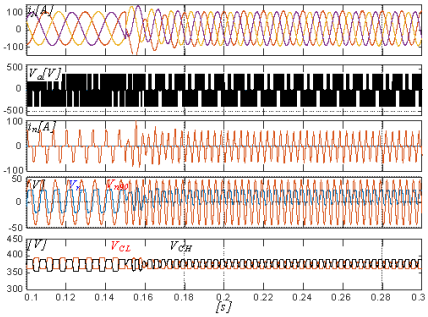

Fig. 18: V_n ripple control: 50 to 100 Hz, 100A, ±15V hysteresis band.

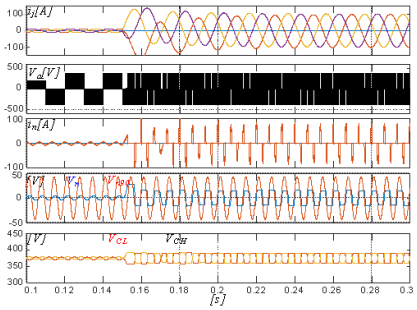

Fig. 19: V_n ripple control: 50Hz, 10 to 100A, ±15V hysteresis band.

Compensation of a neutral point voltage drift is addressed in Fig. 20. A *200 Ω* resistance is parallel connected to the upper dc link capacitor C_H to generate a permanent current unbalance, which would lead to a progressive drift of the neutral point voltage without the hysteretic control, leading the capacitor C_H to be completely discharged and the voltage on C_L reaching the DC Bus voltage. The compensation of neutral point drifts is fully achieved also in the case of speed and load variations, as shown in Figs. 21 and 22.

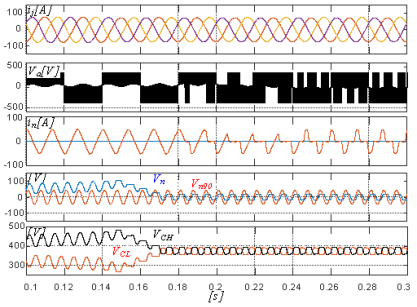

Fig. 20: V_n drift control: 50Hz, 75A, ±15V hysteresis band.

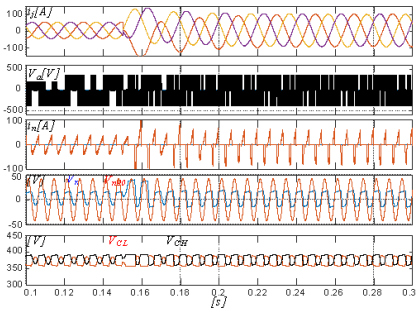

Fig. 21: V_n drift control: 50Hz, 50 to 100A, ±15V hysteresis band.

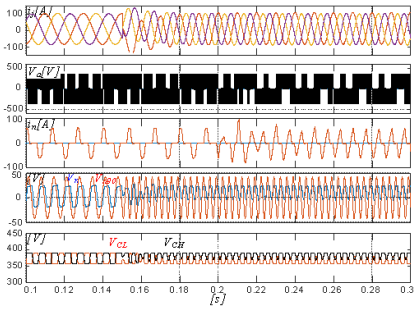

Fig. 22: V_n drift control: 100A, 50 to 100Hz, ±15V hysteresis band.

5. Conclusion

To overcome the dc-link capacitors voltage imbalance in neutral point clamped three-level inverters, a simple control technique has been proposed in this paper for ~~inverter~~inverters driven by a dual carrier PWM. The proposed technique prevents the occurrence of null voltage switching combinations, which are responsible for dc-link capacitors voltage imbalance, every time that the variation of the neutral point voltage exceeds some predefined thresholds. The proposed technique does not require voltage or current transducers, neither additional power circuits while, as it has been demonstrated by simulations, it is able to effectively limit the magnitude of the ripple of the neutral point voltage, as well as to compensate for any drift of the mean value. Future works will address the development of suitable criteria to optimally selecting the width of the hysteresis band, in such a way to achieve an optimal trade-off between size of the dc-link capacitors and the impact of ~~high~~ high-frequency switching harmonics.

Acknowledgment

This work has been partially supported by the Italian inter-university PhD program in "Sustainable development and climate change" managed by IUSS Pavia and University of Messina Italy.

References

[1] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications" IEEE Trans. Ind. Appl., vol. 41, no. 3, pp. 855–865, May/Jun. 2005.

[2] G. Lipphardt, "Using a three-level GTO voltage source inverter in a HVDC transmission system," in Fifth European Conf. on Power Electronics and Applications, pp. 151-155, September 1993.

[3] M. Saeedifard, H. Nikkhajoei, R. Iravani, "A Space Vector Modulated STATCOM Based on a Three-Level Neutral Point Clamped Converter," IEEE Trans. Power Delivery, vol. 22, no. 2, pp. 1029-1039, April 2007.

[4] O. Vodyakho, C. C. Mi, "Three-Level Inverter-Based Shunt Active Power Filter in Three- Phase Three-Wire and Four-Wire Systems," IEEE Trans. Power Electronics, vol.24 , no. 5, pp. 1350-1363, May 2009.

[5] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez, J. Balcells, "Interfacing Renewable Energy Sources to the Utility Grid Using a Three-Level Inverter," IEEE Trans. Industrial Electronics, Vol. 53, no. 5, pp. 1504-1511, October 2006.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point Clamped PWM Inverter," Proceedings of the Industry Applications Society Conference, pages 761-766, September/October 1980.

[7] J. Rodriguez, S. Bernet, P. K. Steimer and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," in IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2219-2230, July 2010.

[8] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in Conf. Rec. IEEE IAS Annu. Meeting, Toronto, ON, Canada, Oct. 1993, pp. 965–970.

[9] S. K. Giri, S. Chakrabarti, S. Banerjee, and C. Chakraborty, "A carrier based PWM scheme for neutral point voltage balancing in three level inverter extending to full power factor range," IEEE Trans. Ind. Electron., vol. 64, no. 3, pp. 1873–1883, Mar. 2017.

[10] C. Nikola, B. Dushan, "A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped Voltage Source PWM Inverters," IEEE Trans. Power Electronics, vol. 15 , no. 2, pp. 242–249, March 2000.

[11] B. P. Schmitt and R. Sommer, "Retrofit of fixed induction motors with medium voltage drive converters using NPC three-level inverter high voltage IGBT based topology," in Proc. IEEE ISIE, Pusan, Korea, Jun. 2001, vol. 2, pp. 746–751.

[12] Y. Jiao, F. C. Lee and S. Lu, "Space vector modulation for 3-level NPC converter with neutral voltage balancing and switching loss/noise reduction," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, 2014, pp. 1780-1787.

[13] D. Woldegiorgis, E. Soria, Y. Wei, H. Mhiesan and A. Mantooth, "Simplified Space Vector Modulation Strategy for Three-level Inverters," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 2020, pp. 2963-2967.

[14] S. Busquets-Monge, J. Bordonau, D. Boroyevich and S. Somavilla, "The nearest three virtual space vector PWM - a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter," in IEEE Power Electronics Letters, vol. 2, no. 1, pp. 11-15, March 2004.

[15] D. Woldegiorgis, Y. Wei, H. Mhiesan and A. Mantooth, "A New Dclink Capacitor Voltage Balancing Method for Three-level SVM Strategies Based on Two-level Space Vector Diagram," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), Nanjing, China, 2020, pp. 1746-1751.

[16] D. Woldegiorgis, Y. Wei and A. Mantooth, "Simple

Carrier Based Capacitor Voltage Balancing Technique for Three-Level Voltage Source Inverters," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 2021, pp. 528-533.
[17] R. Rojas, T. Ohnishi, and T. Suzuki, “An improved voltage vector control method for neutral-point-clamped inverters,” IEEE Trans. Power Electron., vol. 10, no. 6, pp. 666–672, Nov. 1995.
[18] C. Newton and M. Sumner, “Neutral point control for multi-level inverters: Theory, design and operational limitations,” in Conf. Rec. IEEE IAS Annu. Meeting, New Orleans, LA, USA, Oct. 1997, pp. 1336–1343.
[19] I. López *et al.*, ‘Generalized PWM-Based Method for Multiphase Neutral-Point-Clamped Converters With Capacitor Voltage Balance Capability’, *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4878–4890, 2017.