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Assessment of a Hybrid Modulation Strategy for Asymmetrical Cascaded Multilevel Inverters Under Comparative Analysis

Gerlando Frequente *, Massimo Caruso, Giuseppe Schettino and Rosario Miceli

Department of Engineering, University of Palermo, Viale delle Scienze, Building No. 9, 90128 Palermo, Italy; massimo.caruso16@unipa.it (M.C.); giuseppe.schettino@unipa.it (G.S.); rosario.miceli@unipa.it (R.M.)
* Correspondence: gerlando.frequente@community.unipa.it; Tel.: +39-335-658-7131

Abstract

This paper presents a novel hybrid modulation technique for Asymmetrical Cascaded H-Bridge Multilevel Inverters (ACHBMLIs), specifically designed to enhance both efficiency and harmonic performance. Unlike conventional strategies, the proposed method optimizes the switching scheme by operating the high-voltage H-Bridge at the fundamental frequency, thereby significantly reducing switching losses while maintaining low harmonic distortion levels comparable to traditional Pulse Width Modulation (PWM). To assess the effectiveness of the approach, a comprehensive comparison was conducted against two widely adopted modulation techniques for ACHBMLIs: Multicarrier Pulse Width Modulation (MPWM) and the Staircase Modulation Strategy (SMS). The evaluation involved both simulation and real-time Hardware-in-the-Loop (HIL) testing of a 7-level three-phase ACHBMLI, with a focus on key performance indicators such as voltage and current harmonic distortion, as well as converter efficiency. The results demonstrate that the proposed hybrid modulation achieves higher efficiency than PWM and lower current Total Harmonic Distortion (THD) than SMS. These findings highlight the potential of the hybrid strategy as a compelling solution for applications that demand an optimal balance between energy efficiency and waveform quality.

Keywords: power electronics; asymmetrical cascaded H-bridge multilevel inverter; modulation technique; real-time validations

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1. Introduction

Multilevel Inverters (MLIs) are increasingly favored by researchers in both industry and academia for high-power electronics applications. Their growing popularity is attributed to several key advantages, including modularity, low switching frequency, reduced output filter volume, and minimal Electromagnetic Interference (EMI) radiation. These features make multilevel inverters efficient and reliable for handling high power levels.

In addition to these advantages, MLIs are crucial in advancing transportation electrification and integrating renewable energy into the electrical grid [1,2]. Among the various MLI topologies discussed in the literature [3], the Cascaded H-bridge Multilevel Inverter (CHBMLI) is widely adopted due to its modular design and fault-tolerant capability. This topology allows for increased voltage levels by adding additional H-bridge modules [4], making it a flexible solution for various applications. However, CHBMLIs require separate DC sources, which limits their applicability to systems where such sources are readily available, including photovoltaic systems [5–7] hybrid energy storage systems [8,9], electric drives [10] and automotive applications [11]. Furthermore, CHBMLIs are particularly well-suited for grid-connected applications, where they can be utilized as a Static Synchronous Compensator (STATCOM) to regulate voltage [11,12].

However, to increase the number of generated levels, it is necessary to add more cascaded H-bridges, making the system more complex. Therefore, an alternative approach is the use of Asymmetric Multilevel Inverters (AMLIs), which help reduce the number of required power components. AMLI architectures are designed by applying different voltage amplitudes across the DC-link capacitors. This method allows for an increase in voltage levels while preserving the same hardware setup compared to symmetric configurations, leading to reduced overall costs. Numerous researchers have introduced innovative asymmetric topologies. For instance, in Ref. [13], the authors analyzed the performance of a novel MLI structure capable of generating an output voltage with 13 levels in a symmetric configuration, while in an asymmetric configuration, it can produce a 17-level output waveform, achieving a THD of 3% and an efficiency of 97%. The advanced K-type AMLI proposed in Ref. [14] demonstrated the highest experimental efficiency of 96.74%, with an output voltage THD of 5.3% without filters. Among the recently proposed AMLIs, a notable and efficient solution is the ACHBMLI [15], which retains all the benefits of the CHBMLI structure while enabling higher voltage levels through the appropriate selection of DC voltage amplitudes without requiring additional H-bridge modules and maintaining low hardware complexity. The literature identifies two approaches for selecting DC voltage amplitudes: the binary method, where the voltage ratio among DC sources follows a 1:2:4. . . progression, and the tertiary method, characterized by a 1:3:9. . . ratio [16]. A notable improvement is discussed in Ref. [17], where the ratio among the three sources of ACHBMLI is set to 1:2:6.

A widely discussed topic in the literature is the modulation techniques used to generate signals for driving the switches of converters. This subject is particularly important because these techniques significantly affect the performance of converters in terms of power dissipation and the harmonic content of the generated voltages. Based on the operating switching frequency, these techniques can be classified as follows, based on the frequency modulations:

- Low-frequency modulation techniques, such as Refs. [18–20]. According to Refs. [17,21] staircase modulation is the most suitable method for controlling an ACHBMLI converter. This strategy enables the generation of a staircase voltage waveform through a simple real-time algorithm that can be implemented on standard electronic devices. However, its main drawback is the presence of low-order voltage harmonics.
- High-frequency modulation techniques, such as MPWM [22–24], enabling the generation of current with low THD. However, the large number of switching events substantially increases switching losses.

Recently, researchers have explored hybridizing existing PWM strategies to leverage their advantages. For instance, a hybrid multicarrier PWM method for CHBMLIs is presented in Ref. [25], where two legs of each H-bridge cell operate at different switching frequencies to reduce switching events. However, this approach produces an unbalanced switching loss distribution, leading to varying device lifetimes among H-bridge cells. Another hybrid PWM technique, proposed in Ref. [26], aims to improve lower-order harmonics and minimize output voltage errors. However, it suffers from increased harmonic content when the carrier frequency is low. Additionally, a PWM method combining steady-state Nearest Level (NL) PWM and transient Carrier-Based (CB) PWM is introduced in Ref. [27] for motor drive applications. While effective in such contexts, its output current harmonic performance degrades when applied in grid-connected systems.

In Ref. [28], a hybrid PWM technique that integrates Nearest Level (NL) PWM and Carrier-Based (CB) PWM to optimize switching loss and harmonic distortion. Particle Swarm Optimization (PSO) is employed to determine the optimal hybridization level, minimizing power loss while ensuring compliance with grid code standards. The approach is experimentally validated on an MLI across various modulation indices. In Ref. [29], a hybrid modulation scheme is implemented for an ACHBMLI-STATCOM with a 1:2:6 DC voltage ratio, maximizing output voltage levels. Different H-bridges operate at varying switching frequencies to reduce losses and improve efficiency. Experimental results confirm effective reactive power.

In general, hybrid or modified modulation techniques are often employed to overcome the limitations of conventional approaches. For instance, in Ref. [30], a modified variable carrier-based discontinuous PWM strategy was proposed and implemented on a three-level inverter. The method achieves harmonic performance comparable to Selected Harmonic Elimination Pulse Width Modulation (SHEPWM) at low carrier ratios while overcoming the drawback of slow dynamic response.

However, hybrid modulation techniques can also be applied to DC-link capacitor voltage balancing, as demonstrated in Ref. [31] for a four-level Neutral-Point Clamped (NPC) inverter. The proposed method combines a three-level Space Vector Pulse Width Modulation (SVPWM) and a two-level PWM technique. A major strength of this approach lies in its ease of implementation on digital hardware, since the modulation process is almost identical to that of conventional SVPWM.

In Refs. [32,33], a hybrid technique combining two carrier signals with different frequencies was proposed to reduce switching losses in VSI inverters. A comprehensive analysis, including comparative evaluations with conventional and ripple-elimination methods, demonstrates the superiority of the proposed approach. The results show a significant reduction in current ripples while maintaining the full five-level output voltage, thus enhancing both reliability and efficiency in V2G systems. Specifically, the proposed method eliminates current ripples at their peak regions by synchronizing the switching signals of the power devices.

In Ref. [34], a modified carrier-based pulse-width modulation algorithm, termed per-phase discontinuous PWM, was introduced to generate different non-switching intervals for the phase leg most affected by aging, by injecting an appropriate zero-sequence voltage into the reference signals. These non-switching intervals prevent certain phase legs from commutating, thereby reducing switching frequency and corresponding losses. The careful design of variable clamping intervals enables a desirable decrease in per-phase switching frequency for two-level, three-phase voltage source inverters, while ensuring that the output performance remains largely unaffected.

As described in the literature, hybrid or modified modulation techniques are often employed to balance DC-link voltages in NPC inverters or to reduce current ripple. In this work, however, we propose a hybrid modulation technique aimed at improving efficiency while preserving excellent harmonic performance in both load voltage and current. Unlike the approaches commonly found in the literature, the proposed technique is specifically designed to be suitable for ACHBMLI configurations.

To validate the proposed method, a comprehensive comparative analysis is conducted against the two most widely adopted ACHBMLI modulation strategies reported in the literature, PWM, known for its high-quality voltage output, and SMS, recognized for its high efficiency and reduced switching losses. The proposed modulation is further distinguished by the inclusion of a thermal stress assessment, an aspect often overlooked in previous work, thus providing deeper insight into the reliability of the power devices.

Finally, this study demonstrates that a fundamental-frequency switching scheme can be effectively integrated with high-frequency modulation without compromising grid compliance or drive performance. The presented results—covering voltage and current quality, converter losses, efficiency, and thermal behavior—offer a comprehensive evaluation framework and extend the current understanding of asymmetric multilevel inverter performance

2. Mathematical Model of the ACHBMLI

The system analyzed in this article is shown in Figure 1. It consists of a three-phase seven-level (3-P 7-L) ACHBMLI, which is composed of six H-bridges. Each inverter leg consists of two cascaded H-bridges configured asymmetrically, meaning that the two bridges operate at different DC voltage levels. Specifically, HBb is the H-bridge with twice the DC voltage of the other bridge, referred to as HBa.

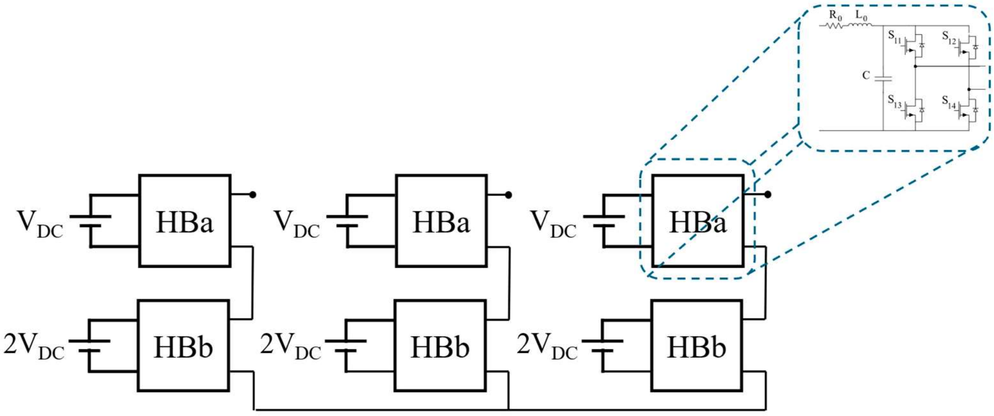

Figure 1. Three-phase 7-level ACHBMLI.

As previously mentioned, AMLIs allow for a higher number of voltage levels while maintaining the same hardware configuration as an MLI. For an ACHBMLI in a binary configuration, the number of voltage levels N_a, as reported in Ref. [35], is given by:

$$N_a = 2^{n+1} - 1. \tag{1}$$

The mathematical model of a generic phase ACHBMLI is described as follows:

$$\begin{cases} v_{HBa}(t) = v_{Ca}(t)(G_{a1} - G_{a2}) \\ \frac{di_{0a}(t)}{dt} = -\frac{r_0}{L_0} i_{0a}(t) - \frac{v_{Ca}(t)}{L_0} + \frac{V_{DC}}{L_0} \\ \frac{dv_{Ca}(t)}{dt} = -\frac{1}{C} i_{load}(t)(G_{a1} - G_{a2}) + \frac{1}{C} i_{0a}(t) \end{cases} \tag{2}$$

$$\begin{cases} v_{HBb}(t) = v_{Cb}(t)(G_{b1} - G_{b2}) \\ \frac{di_{0b}(t)}{dt} = -\frac{r_0}{L_0} i_{0b}(t) - \frac{v_{Cb}(t)}{L_0} + \frac{2V_{DC}}{L_0} \\ \frac{dv_{Cb}(t)}{dt} = -\frac{1}{C} i_{load}(t)(G_{b1} - G_{b2}) + \frac{1}{C} i_{0b}(t) \end{cases}, \tag{3}$$

$$v_x(t) = v_{HBa}(t) + v_{HBb}(t), \tag{4}$$

here, HBb represents the H-bridge with a DC-link voltage that is twice that of HBa. The output voltages of HBa and HBb are denoted as v_{HBa} and v_{HBb}, respectively. The gate signals of the asymmetric inverter are G_{a1}, G_{a2}, G_{b2} and G_{b2}, while i_{0a} and i_{0b} represent the input currents of the H-bridges. The voltages across the respective DC-link capacitors are v_{Ca} and v_{Cb}. The circuit parameters are: C DC-link capacitance, r_0 and L_0 are, respectively, the resistance and inductance of the power supply circuit.

To develop a model that accounts for diode current conduction, the Generalized Switching Functions (GSF) [36] must be implemented, as shown in Equation (5)

$$\begin{cases} G_{i1} = [(i_{load}(t) \geq 0)\ S_{i1}] + [(i_{load}(t) < 0)\ \overline{S_{i3}}] \\ G_{i3} = [(i_{load}(t) \leq 0)\ S_{i3}] + [(i_{load}(t) > 0)\ \overline{S_{i1}}] \\ G_{i2} = [(i_{load}(t) \leq 0)\ S_{i2}] + [(i_{load}(t) > 0)\ \overline{S_{i4}}] \\ G_{i4} = [(i_{load}(t) \geq 0)\ S_{i4}] + [(i_{load}(t) < 0)\ \overline{S_{i2}}] \end{cases} \quad (5)$$

The efficiency η of an ACHBMLI is influenced by several factors, primarily related to power losses occurring during operation. These losses can be categorized into switching losses P_{sw} and conduction losses P_{cond}. Switching losses arise during the turn-on and turn-off transitions of the power semiconductors and are affected by switching frequency, semiconductor characteristics, and modulation techniques. While higher switching frequencies enhance output voltage quality, they also lead to increased losses. Conduction losses, on the other hand, occur when power devices are in the ON state and depend on their internal resistance and current flow. Thus, the efficiency of an inverter is determined using the following formula:

$$\eta = \frac{P_{in}}{P_{in} + P_{sw} + P_{cond}} 100 \quad (6)$$

where η represents the efficiency of the ACHBMLI, P_{in} is the input power.

Several factors impact the overall efficiency of the converter. The modulation strategy plays a crucial role, as different techniques, such as SMS or PWM, influence how losses are distributed and how efficiently the converter operates. The selection of semiconductor components, such as IGBTs or SiC MOSFETs, also affects switching and conduction losses. Thermal management is another critical factor, as higher temperatures increase resistance and switching times, ultimately reducing efficiency. Additionally, load conditions significantly impact performance, as efficiency varies with the modulation index and load demand. At lower modulation indices, harmonic distortion tends to increase, which can degrade the overall efficiency.

By optimizing switching strategies, ACHBMLIs can achieve higher efficiency, which is particularly important in automotive applications, where reducing losses directly contributes to extended vehicle range and improved energy utilization.

The other important parameter analyzed is the THD, which is crucial for evaluating the quality of the output voltage and current in an ACHBMLI. It quantifies the distortion introduced by the presence of harmonic components in the waveform, which can negatively impact the performance of electrical drives and grid-connected systems. A lower THD ensures better power quality, reducing additional losses in the motor and minimizing electromagnetic interference. THD is calculated using the following formula:

$$THD = \sqrt{\frac{\sum_{n=1}^{\infty} V_n^2 - V_1^2}{V_1^2}} \cdot 100, \quad (7)$$

where V_n represents the rms voltage of the *n-th* harmonic component, and V_1 is the rms voltage of the fundamental frequency. Several factors affect THD levels in an ACHBMLI. The modulation strategy plays a key role, as different frequency modulation techniques present trade-offs between harmonic content and efficiency. The switching frequency also significantly impacts higher frequencies shift harmonic components to higher orders, making them easier to filter. However, this comes at the cost of increased power losses. The modulation index further influences THD, as lower modulation indices typically lead to a rise in low-order harmonics, degrading waveform quality. Finally, load conditions contribute to THD variations, as changes in speed and torque in electrical drive applications can cause variations in harmonic content.

3. Proposed Modulation Technique

This section provides a detailed description of the modulation techniques proposed. The two most widely used modulation techniques for ACHBMLIs are Multicarrier (MC)-PWM and SMS, each offering distinct advantages and drawbacks.

MC-PWM is highly effective in reducing harmonic content as its high-frequency harmonics are concentrated at multiples of the carrier frequency, making them easier to filter. As a result, in electrical drive applications, the stator currents exhibit very low THD, thereby enhancing overall system performance [37]. However, its main drawback is the high switching frequency, which leads to greater power dissipation in the inverter. This limits its applicability in medium-voltage, low-power systems, where minimizing power losses is critical.

SMS offers a key advantage in its low switching frequency. The main H-Bridge switches operate at a frequency equal to the modulation signal, significantly reducing switching losses and improving efficiency. By concentrating on switching events on the lower voltage modules, SMS enhances the power conversion efficiency of ACHBMLIs, making it a practical choice for various applications. However, its major limitation lies in the presence of low-order harmonics. While the overall THD remains relatively low, certain modulation indices can introduce problematic harmonics into the system. These harmonics may lead to increased torque ripple and degradation of the current waveform quality, potentially impacting the overall performance and efficiency of the drive [38].

A hybrid approach was developed to overcome those trade-offs. It integrates SMS and PD-PWM to achieve balanced power loss distribution and improved harmonic performance. This hybridization ensures low THD while maintaining switching losses and enhancing the efficiency of ACHBMLIs.

The PD-PWM technique, due to its high switching frequency, leads to increased switching losses, whereas the SMS, operating at a frequency comparable to the fundamental one, results in significantly lower switching losses. To address this trade-off, the proposed hybrid modulation technique was designed to combine the strengths of both strategies while mitigating their respective drawbacks. Figure 2 illustrates the operating principle of the proposed modulation scheme. The process of generating the HBb control signals remains the same as in SMS; however, the main distinction lies in the adoption of a high-frequency carrier signal to generate the control signals for HBa, which directly influences the system's switching characteristics and harmonic performance.

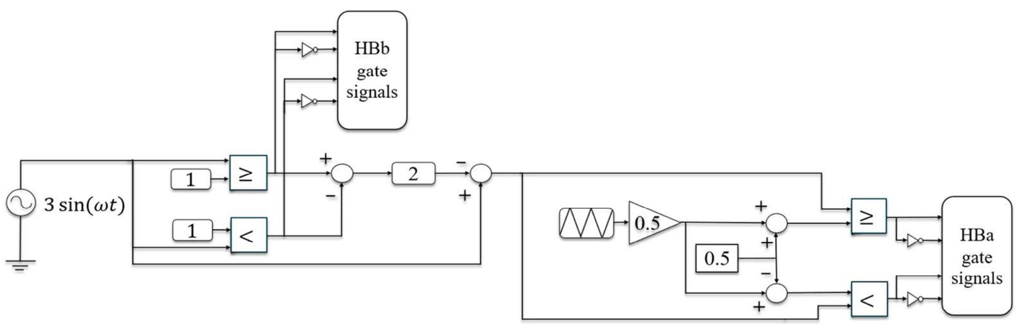

Figure 2. Principle of the proposed hybrid modulation technique operation for a 7-L ACHBMLI.

In this approach, the two H-bridges operate at different switching frequencies, allowing for an optimized balance between efficiency and harmonic performance. The HBb bridge switches at a frequency equal to the fundamental frequency, significantly reducing