Optimized Finite Control Set Model Predictive Control for a Three-Phase Five-Level Cascaded H-Bridge Multilevel Inverter fed Interior Permanent Magnet Synchronous Machine With On-Line Candidate Switching State Selection

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***Abstract*— Model predictive control is a novel control strategy that is attracting the scientific community due to the several advantages it offers, such as the ability to consider system nonlinearities, the possibility to synthesize a control for a MIMO system instead of multiple SISO, and so on. Control feasibility, due to the very high computational cost required to solve the optimal control problem, is a challenge. By considering electric drives fed by multilevel inverters, the control design is more challenging due to the increased number of available output voltage vectors. In this work, a simple algorithm for the voltage candidate reduction is presented: it allows for reducing the control computational cost, minimizing the switching losses, and minimizing *dv/dt* on phase voltage waveforms.**

Keywords—component, formatting, style, styling, insert

I. INTRODUCTION

Cascaded H-Bridge Multilevel Inverter (CHBMI) represents one of the most promising inverter topologies for medium voltage drives and transportation applications due to its modularity, lower number of required switching devices with respect to other Multilevel Inverter (MI) topologies, and fault-tolerant capability [1]-[5]. Recently, CHBMI is being adopted in medium-voltage high-power industrial electric drives [4]-[5]. In detail, in the range of 4.16-13.8 kV, CHBMI-based electric drives result to be the most efficient, if compared with other MI topologies, regardless of the semiconductor technology[6].

CHBMI is being employed also in the e-mobility sector [7], since it allows easy integration with the battery pack and an increment of the total DC link voltage, in accordance with the industry trend [8]-[9], without increasing the switching device voltage stress. Moreover, it allows for maximizing the vehicle performance and efficiency: the higher number of output voltage levels guarantees a lower voltage and current Total Harmonic Distortion (THD), with respect to traditional Three Phase Two-Level Voltage Source Inverters (3P-2L-VSIs). As a consequence, the adoption of the CHBMI leads to a torque ripple and iron loss reduction, especially when the switching frequency is reduced.

Model Predictive Control (MPC) is a novel control strategy that allows obtaining the control variables (i.e., the converter gate control signals) by solving a constrained optimal control problem, based on the system internal dynamic model and a cost function, over a finite prediction horizon[10]. Among the various proposed MPC algorithms discussed in the scientific literature, the Finite Control Set (FCS) MPC is gaining attention due to its numerous advantages, such as fast dynamic response, easy inclusion of nonlinearities, and ability to fulfil several conflicting control goals [11]-[13]. Although the computation capability of controllers is drastically increased over the years, one of the most challenging aspects deals with the computational burden, which increases exponentially with the number of the converter output voltage levels or with the prediction horizon[14]. In detail, with respect to a multilevel inverter topology, in order to solve the optimal control problem, the future state must be predicted for every possible set of controlled variables. As a consequence, even by adopting the shortest prediction horizon, the future state of the controlled system must be predicted a number of times which depends on the output voltage levels. By considering a Three Phase Five Level (3P-5L) CHBMI, the adopted MI topology in this work, the set of input variables is composed of 125 voltage vectors. Moreover, looking at the set of gate control signals, it is equal to 4096 combinations, due to the high number of redundant states. These features make the implementation of an FCS-MPC with an exhaustive search approach quite unfeasible. This challenge has been faced in the literature. By way of example, a modified MPC, based on space vector theory, with reduced available voltage vectors is proposed in [15]. In [16], the authors propose a model predictive control strategy for a cascaded H-bridge multilevel rectifier and the available voltage vector set is varied on-line depending on the system working conditions. In [17] and [18], authors propose

strategies in order to reduce the MPC computational growth with the prediction horizon from exponential to polynomial order, such as the Branch and Bound (B&B) approach. It is necessary to remark that the majority of the works in the literature deal with the CHBMI employed for a STATCOM application, but only a few papers address this challenge for CHBMI-based AC drives. Moreover, the practical implementation of most of the proposed solutions results to be quite challenging, and, if the B&B approach is adopted, the relative control computational time is variable and it makes complex the computational delay compensation. In this work, the implementation of a simple FCS-MPC for a three-phase five-level (3P-5L) CHBMI-fed IPMSM electric drive with online candidate states selection is presented. In detail, the proposed algorithm aims to reduce the MPC computational complexity and at the same time to reduce the switching losses, by the minimization of the H-Bridge (H-B) modules state transitions, and the output voltage *dv/dt*.

II. FCS-MPC FORMULATION

In this section, the optimal control problem is formulated. In detail, the adopted electric drive mathematical model is introduced, both on the IPMSM and on the CHBMI sides. The electric drive control scheme is reported in Fig.1. In detail, motor speed and currents are chosen as controlled variables. The outer control loop allows generating the current references in the *d-q* reference frame, for this purpose traditional PI controller is adopted. The inner control loop is synthesized as an FCS-MPC.

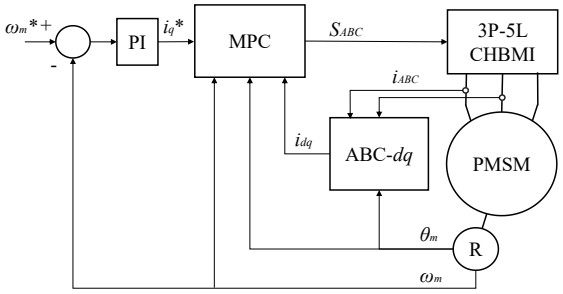

Fig. 1. Electric drive with FCS-MPC control block scheme.

A. IPMSM control model

For control formulation purposes, the IPMSM continuous-time state-space model in *d-q* reference frame is considered:

$$\boldsymbol{i}_{dq}(t) = \boldsymbol{F}\boldsymbol{i}_{dq}(t) + \boldsymbol{G}\boldsymbol{v}_{dq}(t) + \boldsymbol{H} \tag{1}$$

with

$$\boldsymbol{F} = \begin{bmatrix} -\frac{R}{L_d} & \frac{p\omega_m L_q}{L_d} \\ -\frac{p\omega_m L_d}{L_q} & -\frac{R}{L_q} \end{bmatrix}, \boldsymbol{G} = \begin{bmatrix} \frac{1}{L_d} & 0 \\ 0 & \frac{1}{L_q} \end{bmatrix}, \boldsymbol{H} = \begin{bmatrix} 0 \\ -\frac{p\omega_m \lambda_{PM}}{L_q} \end{bmatrix}, \tag{2}$$

where $\boldsymbol{v}_{dq}$ is the stator voltage vector, $\boldsymbol{i}_{dq}$ is the stator current vector, L_d and L_q are direct and quadrature inductances, R is the stator winding resistance, ω_m is the mechanical rotor speed, λ_{PM} is the permanent magnet flux and p is the pole pairs of the machine. By integrating equations (1) from $t=kT_s$ to $t=(k+1)T_s$, the discrete-time state-space model is obtained:

$$\boldsymbol{i}_{dq}(k+1) = \boldsymbol{A}\boldsymbol{i}_{dq}(k) + \boldsymbol{B}\boldsymbol{v}_{dq}(k) + \boldsymbol{K} \tag{3}$$

with

$$\boldsymbol{A} = \begin{bmatrix} 1-\frac{T_s R}{L_d} & \frac{p\omega_m T_s L_q}{L_d} \\ -\frac{p\omega_m T_s L_d}{L_q} & 1-\frac{T_s R}{L_q} \end{bmatrix} \boldsymbol{B} = \begin{bmatrix} \frac{T_s}{L_d} & 0 \\ 0 & \frac{T_s}{L_q} \end{bmatrix}, \boldsymbol{K} = \begin{bmatrix} 0 \\ -\frac{p\omega_m T_s \lambda_{PM}}{L_q} \end{bmatrix}, \tag{4}$$

where T_s is the sampling interval.

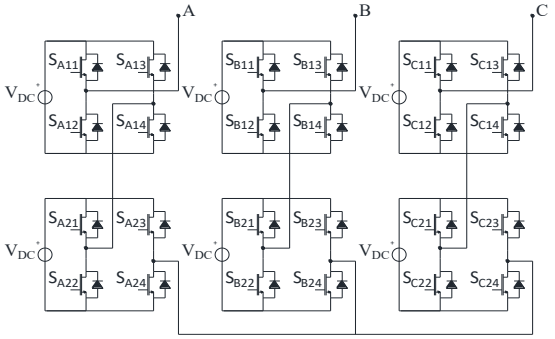

Fig. 2. Three-phase five-level CHBMI circuit diagram.

B. 3P-5L CHBMI control model

The inverter model must be defined and integrated with the motor model. With this aim, the input voltage vector v_{dq} must be expressed in terms of the converter switching states. In detail, with respect to the 3P-5L CHBMI scheme reported in Fig. 2, the phase voltage v_{jN} can be expressed as:

$$v_{jN} = \frac{v_{DC}}{2}\sum_{x=1}^{2}(S_{j,x1} - S_{j,x2} - S_{j,x3} + S_{j,x4}) \tag{5}$$

where v_{DC} is the H-B DC-link voltage and $S_{j,xy}$ is the H-B leg state variable, $j \in \{A, B, C\}$ identifies the converter phase, $x \in \{1, 2\}$ identifies the H-B phase module, and $y \in \{1, 4\}$ identifies the H-B leg. Since the switches on the same H-B leg must operate dually and in pairs in order to avoid the DC link short circuit, the following relations are introduced:

$$S_{j,x3} = 1 - S_{j,x1},\ S_{j,x4} = 1 - S_{j,x2}. \tag{6}$$

Replacing relations (6) in (5), the following relation is obtained:

$$v_{jN} = v_{DC}(S_{j,11} - S_{j,13} + S_{j,21} - S_{j,23}), \tag{7}$$

With respect to the schematic in Fig.3, it is possible to link the output-phase voltage vector, $\boldsymbol{v}_N(t)$ with the load-phase voltage vector $\boldsymbol{v}_n(t)$ as follows:

$$\boldsymbol{v}_n(t) = \boldsymbol{M}\boldsymbol{v}_N(t) \tag{8}$$

with

$$\boldsymbol{M} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{9}$$

Phase voltage vectors in *d-q* reference frame and *ABC* reference frame are linked by the relation:

$$\boldsymbol{v}_{dq}(t) = \boldsymbol{T}\boldsymbol{v}_n(t) \tag{10}$$

with

$$\boldsymbol{T} = \frac{2}{3}\begin{bmatrix} \cos(p\theta) & \cos\left(p\theta - \frac{2\pi}{3}\right) & \cos\left(p\theta + \frac{2\pi}{3}\right) \\ -\sin(p\theta) & -\sin\left(p\theta - \frac{2\pi}{3}\right) & -\sin\left(p\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{12}$$

where θ is the rotor angular position.

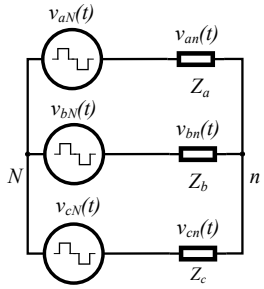

Fig. 3. Three-phase five-level CHBMI circuit diagram.

Replacing (8) in (10):

$$\boldsymbol{v}_{dq}(t) = \boldsymbol{TMv}_{N}(t) \tag{14}$$

By performing the product between the matrices $\boldsymbol{T}$ and $\boldsymbol{M}$ it is not difficult to prove that the matrix $\boldsymbol{T}$ is obtained again. Therefore, the relationship (12) can be simplified as:

$$\boldsymbol{v}_{dq}(t) = \boldsymbol{Tv}_{N}(t) \tag{13}$$

This result allows for avoiding the implementation of the $\boldsymbol{M}$ matrix in the MPC algorithm, reducing the control computational cost.

C. Prediction Horyzon and Cost Function

A prediction horizon N_p=1 is chosen and the cost function J is formulated as:

$$J = \left\| \boldsymbol{i}_{dq}^{*}(k+1) - \boldsymbol{i}_{dq}(k+1) \right\|_2^2 \tag{14}$$

where $\boldsymbol{i}_{dq}^{*}$ is the reference currents vector, $\boldsymbol{i}_{dq}$ is the future state current vector. The cost function penalizes the input current error only.

III. Proposed Algorithm

According to (7) and (12), phase voltages can assume values $v_{jN} \in \{-2V_{DC}, -V_{DC}, 0, V_{DC}, 2V_{DC},\}$ and input variables v_d and v_q values depend on the three phases voltage values combinations, for a total of 125 combinations. Moreover, taking into account the H-Bs state variables, the phase voltages v_{jN} depends on 16 states combinations, v_d and v_q depend on 4096 combinations. As a result, in order to minimize the cost function J, the future state current vector $\boldsymbol{i}_{dq}$ must be computed 4096 times, which is quite unfeasible on common controllers. In order to reduce the available future states, the switching devices state transitions, and minimize the phase voltage dv/dt, the following switching rules are introduced:

1. Only one H-B module per phase must be allowed to change its state;
2. Only one H-B leg per module must be allowed to change its state.

With respect to one phase, in order to comply with rule 1, the binary *enabling* variable M is introduced: when $M=1$ the upper H-B module is allowed to change state and the lower H-B module state is locked; when $M=0$ the upper H-B module state is locked and the lower H-B module is allowed to change state, as summarized in Fig. 4.

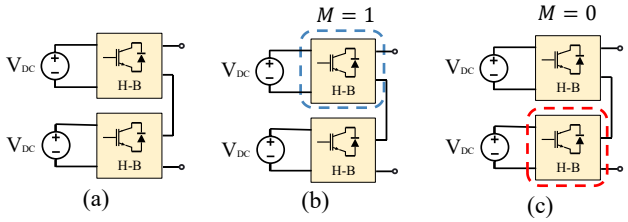

Fig. 5. (a) one phase of the 3P-5L-CHBMI; (b) $M=1$, the upper H-B is allowed to change state, the lower H-B state is locked; (c) $M=0$, the lower H-B is allowed to change state and the upper H-B state

The same criterion must be applied to other phases. To comply with rule 2, with respect to the state-unlocked H-B module per each phase, the future available states depend on the current state, according to Fig. 5. In detail, in Fig. 5(a), all the available state transitions for the state-unlocked H-B module are summarized. Available transitions depending on the current H-B module state (identified by the red circle) are summarized in Fig. 5(b), 5(c), 5(d) and 5(e). It can be noted that, complying with rules 1 and 2, the phase voltage variation $|\Delta v_{jN}|$ is minimized, and relation (14) is always satisfied:

$$\left|\Delta v_{jN}\right| = \left|v_{jN}(k) - v_{jN}(k-1)\right| \le V_{DC} \tag{14}$$

Moreover, the number of switching state candidates per iteration is reduced from 4096 to 27 and, at least, the number of commutations per each sampling period is minimized. The FCS-MPC can be formulated as follow:

$$\boldsymbol{v}_{dq,opt} = \arg\min J\left(\boldsymbol{i}_{dq}(k+1), \boldsymbol{v}_{dq}(k)\right)$$
$$subject\ to \begin{cases} \boldsymbol{i}_{dq}(k+1) = \boldsymbol{A}\boldsymbol{i}_{dq}(k) + \boldsymbol{B}\boldsymbol{v}_{dq}(k) + \boldsymbol{K} \\ \left|\Delta v_{jN}(k)\right| \le v_{DC} \\ \boldsymbol{v}_{dq}(k) \in \boldsymbol{\mathcal{U}}(k) \end{cases} \tag{15}$$

where $\boldsymbol{\mathcal{U}}(k)$ is the candidate input variables vector, which depends on the previous state of the converter, according to rules 1 and 2.

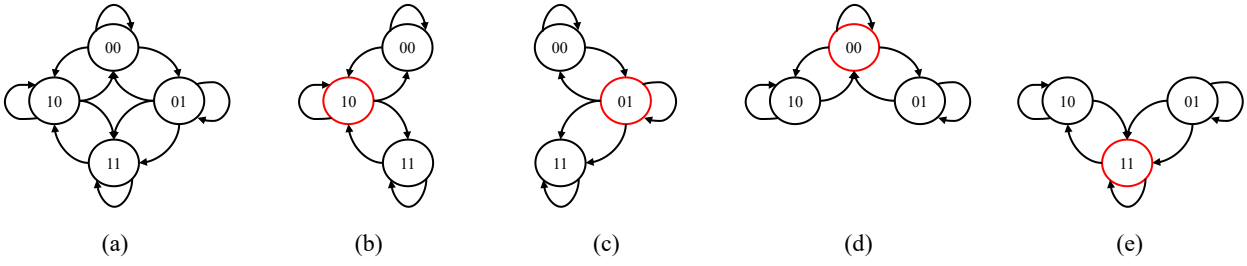

Fig. 4. (a) available H-B future states when rules 1 and 2 are complied, (b-e), available H-B future states when rules 1 and 2 are complied, taking into account the H-B current state (identified by the red circle).

IV. Algorithm Implementation

In this section, the algorithm implementation is discussed: in detail, the delay compensation strategy is presented and the algorithm structure is analyzed. The adopted controller is the System on Module (SoM) sbRIO 9651, whose technical data are reported in Table I. In detail, this controller consists of an FPGA and a DSP module, which can be programmed independently in the LabVIEW environment by selecting the FPGA or the Real Time target, respectively. The controller is fully integrated into a Power Electronics and Drives board (PED Board), whose technical data are reported in Table II. This system makes the implementation of power electronics and electric drive systems control extremely easy and user-friendly. The adopted sampling frequency f_s is equal to 10 kHz, which corresponds to a sampling interval of 100 µs.

TABLE I. SoM sbRIO 9651 technical data.

Quantity	Value
Type	Xilinx Zynq-7000 SoC
Architecture	ARM Cortex A-9
Speed	667 MHz
Cores	2
Logic Cells	85000
Flip-flops	106400
LUTs	53200
DSP slices	220

TABLE II. PED Board technical data.

Hardware	Features
PWM Channels	30x, 0-5V or 0-15 V selectable voltage
14 bit-ADC,	2x8 Channels, Simultaneous Sampling up to 600 kS/s, -5 - +5V or 0-10V
10 bit- ADC,	1x8 Channels, Up to 200 kS/s, 0-5 V inputs
12 bit-DAC,	1x4 Channels, 10 µs settling time
Digital I/O	46x3.3V standard
Ethernet	1x RS485

A. Delay Compensation

In order to maximize the state prediction accuracy, the delay compensation assumes a vital role. In detail, with respect to the ideal case depicted in Fig. 6 (a), the sampling and application instants coincide, which means that the delay time T_d due to the control action processing is zero.

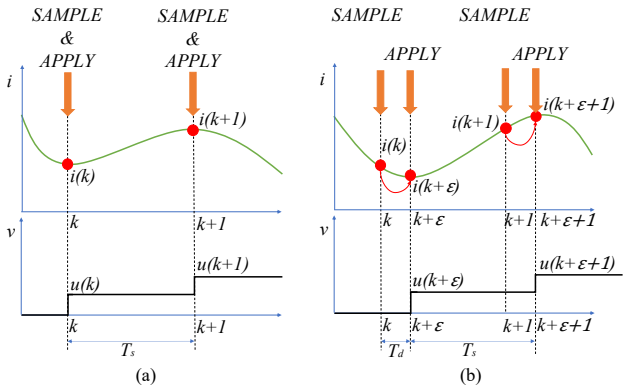

Fig. 6. (a) ideal case, $T_d = 0$, sample and apply instants coincide; (b) ideal case, $T_d \neq 0$, sample and apply instants don't coincide.

This condition is never reached since the processing time is always higher than zero, regardless of the controller technology and computational power. When $T_d \neq 0$, the sampled signals at the instant k do not represent the system state when the control action is applied at the instant $k+\varepsilon$, since during the delay time T_d the system keeps evolving. This phenomenon causes a ripple on the controlled quantities, whose amplitude depends both on the sampling interval T_s. In order to overcome this problem, a delay compensation strategy is adopted. In detail, assuming the delay time T_d is known and constant for each sampling period, and assuming the speed ω_m and the angular position θ constant over the sampling period, an initial prediction is performed to predict the system state at the instant $k+\varepsilon$. The state at the instant $k+\varepsilon$ represents the current state for the MPC algorithm. The initial prediction is performed according to (16):

$$\boldsymbol{i}_{dq}(k+\varepsilon) = \boldsymbol{A}_d \boldsymbol{i}_{dq}(k) + \boldsymbol{B}_d \boldsymbol{v}_{dq,opt}(k+\varepsilon-1) + \boldsymbol{K}_d \tag{16}$$

with

$$\boldsymbol{A}_d = \begin{bmatrix} 1-\frac{T_d R}{L_d} & \frac{p\omega_m T_d L_q}{L_d} \\ -\frac{p\omega_m T_d L_d}{L_q} & 1-\frac{T_d R}{L_q} \end{bmatrix} \quad \boldsymbol{B}_d = \begin{bmatrix} \frac{T_d}{L_d} & 0 \\ 0 & \frac{T_d}{L_q} \end{bmatrix} \quad \boldsymbol{K}_d = \begin{bmatrix} 0 \\ -\frac{p\omega_m T_d \lambda_{PM}}{L_q} \end{bmatrix} \tag{17}$$

and $\boldsymbol{v}_{dq,\,opt}$ is the optimal input vector applied to the system at the instant $k+\varepsilon-1$, which is also applied at the sampling instant k and whose value is known. Once the system state at the instant $k+\varepsilon$ is estimated, it is possible to predict the state at the instant $k+\varepsilon+1$ as follow:

$$\boldsymbol{i}_{dq}(k+\varepsilon+1) = \boldsymbol{A}\boldsymbol{i}_{dq}(k+\varepsilon) + \boldsymbol{B}\boldsymbol{v}_{dq}(k+\varepsilon) + \boldsymbol{K} \tag{18}$$

with matrices $\boldsymbol{A}$, $\boldsymbol{B}$ and $\boldsymbol{K}$ defined as in (4). Replacing (16) in (18) and rearranging, the following relation is obtained:

$$\begin{aligned} \boldsymbol{i}_{dq}(k+\varepsilon+1) = {} & \boldsymbol{A}\boldsymbol{A}_d \boldsymbol{i}_{dq}(k) + \boldsymbol{A}\boldsymbol{B}_d \boldsymbol{v}_{dq,opt}(k+\varepsilon-1) + \\ & \boldsymbol{A}\boldsymbol{K}_d + \boldsymbol{B}\boldsymbol{v}_{dq}(k+\varepsilon) + \boldsymbol{K} \end{aligned} \tag{19}$$

Looking at the matrices $\boldsymbol{B}_d$ and $\boldsymbol{K}_d$, it is possible to note that T_d is a common factor and can be put in evidence. By defining the term:

$$\boldsymbol{A}' = \boldsymbol{A}\frac{T_d}{T_s} \tag{20}$$

the relation (18) can be rearranged as:

$$\begin{aligned} \boldsymbol{i}_{dq}(k+\varepsilon+1) = {} & \boldsymbol{A}\boldsymbol{A}_d \boldsymbol{i}_{dq}(k) + \boldsymbol{A}'\boldsymbol{B}\boldsymbol{v}_{dq,opt}(k+\varepsilon-1) + \\ & (\boldsymbol{A}+\boldsymbol{I})\boldsymbol{K} + \boldsymbol{B}\boldsymbol{v}_{dq}(k+\varepsilon) \end{aligned} \tag{21}$$

B. Optimization

Looking at equation (21), it can be noted that only the term $\boldsymbol{B}\boldsymbol{v}_{dq}$ depends on the phase voltages v_A, v_B, v_C, and, as a consequence, on the set of gate signals to be tested to find the solution to the optimal control problem. For this reason, the term $\boldsymbol{i}_{dq,p1}(k+\varepsilon+1)$ can be defined:

$$\begin{aligned} \boldsymbol{i}_{dq,p1}(k+\varepsilon+1) = {} & \boldsymbol{A}\boldsymbol{A}_d \boldsymbol{i}_{dq}(k) + \boldsymbol{A}'\boldsymbol{B}\boldsymbol{v}_{dq,opt}(k+\varepsilon-1) + \\ & (\boldsymbol{A}+\boldsymbol{I})\boldsymbol{K} \end{aligned} \tag{22}$$

And the (21) can be rewritten as:

$$\boldsymbol{i}_{dq}(k+\varepsilon+1) = \boldsymbol{i}_{dq,p1}(k+\varepsilon+1) + \boldsymbol{B}\boldsymbol{v}_{dq}(k+\varepsilon) \tag{23}$$

The term $\boldsymbol{i}_{dq,p1}(k+\varepsilon+1)$ can be computed only once per sampling period. Replacing (13) in (23), the following relation is obtained:

$$\boldsymbol{i}_{dq}(k+\varepsilon+1) = \boldsymbol{i}_{dq,p1}(k+\varepsilon+1) + \boldsymbol{B}\boldsymbol{T}(k)\boldsymbol{v}_N(k+\varepsilon) \tag{24}$$

Expressing the phase voltages in p.u., (24) can be expressed as:

$$\boldsymbol{i}_{dq}(k+\varepsilon+1) = \boldsymbol{i}_{dq,p1}(k+\varepsilon+1) + v_{DC}\boldsymbol{B}\boldsymbol{T}(k)\dot{\boldsymbol{v}}_N(k+\varepsilon) \tag{25}$$

Also, the term $v_{DC}\boldsymbol{BT}$ can be computed only once per sampling period. Rearranging (25) for the last time:

$$\boldsymbol{i}_{dq}(k+\varepsilon+1)=\boldsymbol{i}_{dq,p1}(k+\varepsilon+1)+\boldsymbol{B}'(k+\varepsilon)\dot{\boldsymbol{v}}_N(k+\varepsilon) \quad (26)$$

with

$$\boldsymbol{B}'(k)=v_{DC}\boldsymbol{BT} \quad (27)$$

The proposed control is summarized in Algorithm I.

Algorithm 1 Model Predictive Control

function MPC ($\boldsymbol{i}_{dq}(k)$, $\boldsymbol{i}^*_{dq}(k)$, $\boldsymbol{S}_{opt}(k+\varepsilon-1)$, $\omega_m(k)$, $\theta_m(k)$, $M(k-1)$)
Compute $\boldsymbol{i}_{dq,p1}(k+\varepsilon+1)$, according to (22)
Compute $B'_{11}(k)$, $B'_{12}(k)$, $B'_{13}(k)$, $B'_{21}(k)$, $B'_{22}(k)$, $B'_{23}(k)$, according to (26)
if $M(k-1)=0$
  $M(k)\leftarrow 1$
  Define the set of available $S_{j,1y}(k+\varepsilon)$, according to Fig. 5
  $S_{j,2y}(k)\leftarrow S_{j,2y}(k-1)$
else if $M(k-1)=1$
  $M(k)\leftarrow 0$
  $S_{j,1y}(k)\leftarrow S_{j,1y}(k-1)$
  Define the set of available $S_{j,2y}(k+\varepsilon)$, according to Fig. 5
end if
Initialize cost function J_0
for l=1: 3
  Compute $\dot{v}_{AN}(l)$, according to (7)
  $\boldsymbol{i}_{dq,p2}(k+\varepsilon+1)\leftarrow \boldsymbol{i}_{dq,p1}(k+\varepsilon+1)+[B'_{11}\dot{v}_A(l)\ B'_{21}\dot{v}_A(l)]^T$
  for m =1: 3
    Compute $\dot{v}_{BN}(m)$, according to (7)
    $\boldsymbol{i}_{dq,p3}(k+\varepsilon+1)\leftarrow \boldsymbol{i}_{dq,p2}(k+\varepsilon+1)+[B'_{12}\dot{v}_B(m)\ B'_{22}\dot{v}_B(m)]^T$
    for n=1: 3
      Compute $\dot{v}_{CN}(n)$, according to (7)
      $\boldsymbol{i}_{dq}(k+\varepsilon+1)\leftarrow \boldsymbol{i}_{dq,p3}(k+\varepsilon+1)+[B'_{13}\dot{v}_C(n)\ B'_{23}\dot{v}_C(n)]^T$
      Compute J, according to (14)
      if $J \leqslant J_0$
        $J_0\leftarrow J$
        $\boldsymbol{S}_{opt}(k+\varepsilon)\leftarrow [S_{A,11}(l)\ S_{A,13}(l)\ S_{A,21}(l)\ S_{A,23}(l)\ S_{B,11}(m)\ S_{B,13}(m)\ S_{B,21}(m)\ S_{B,23}(m)\ S_{C,11}(n)\ S_{C,13}(n)\ S_{C,21}(n)\ S_{C,23}(n)]$
      end if
    end for
  end for
end for
Apply $\boldsymbol{S}_{opt}(k+\varepsilon)$ to the system
end function

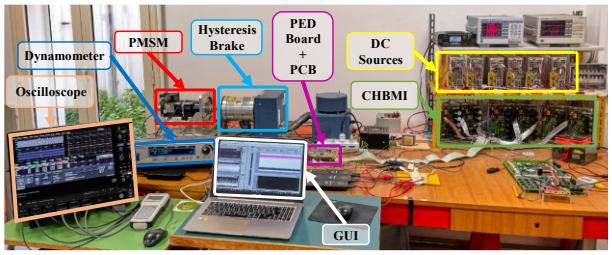

Fig. 7. Test bench.

Looking at Algorithm I, at first, all the operations which can be executed once per sampling period are carried out. In detail, $\boldsymbol{i}_{dq,p1}(k+\varepsilon+1)$ and $\boldsymbol{B}'(k)$ are computed, according to (22) and (27), respectively. Next, the set of available state functions at the instant $k+\varepsilon$ is defined, according to the two algorithm rules, which have been discussed in the previous section and summarized in Fig 4 and 5, respectively. In detail, these rules depend on the value at the previous iteration of the *enabling* variable M and on the set of optimal switching states at the previous iteration $\boldsymbol{S}_{opt}(k+\varepsilon-1)$. When the set of available switching states is defined, the predictions of the system state at instant $k+\varepsilon+1$ for every available switching state are carried out. In detail, 27 predictions must be carried out. However, since the three-phase voltages v_{AN}, v_{BN}, and v_{CN} are mutually independent, operations are organized into three nested *for* loops, thus, v_{AN} and $\boldsymbol{i}_{dq,p2}(k+\varepsilon+1)$ are computed only 3 times, v_{BN} and $\boldsymbol{i}_{dq,p3}(k+\varepsilon+1)$ are computed 9 times, and v_{CN}, $\boldsymbol{i}_{dq}(k+\varepsilon+1)$, and the cost function J are computed 27 times. At every iteration, the computed cost function J is compared with the last minimum J_0: if $J \leqslant J_0$, the value of J_0 and $\boldsymbol{S}_{opt}(k+\varepsilon)$ are updated. At the end of the 27 iterations, J_0 represents the minimum of the cost function and $\boldsymbol{S}_{opt}(k+\varepsilon)$ is the set of input variables that minimized J. The set $\boldsymbol{S}_{opt}(k+\varepsilon)$ is applied to the system. The presented algorithm is entirely implemented on the FPGA target of the adopted controller with single-precision floating point data. The Real-Time target has been adopted only for the implementation of the Graphical User Interface (GUI), for system monitoring purposes. In Table III, the required computational resources are presented. It must be underlined that the reported computational resources deal with not only the presented MPC algorithm but also with all the rest of the control, which includes the acquisition of currents and resolver signals with Analog to Digital Converters, Resolver to Digital Conversion (RDC) algorithm, resolver excitation and speed loop control with PI regulator. All these parts of the control are deeply discussed in [19] and [20]. The adopted sampling period T_s is equal to 100 µs, and the delay time T_d due to the control action processing is equal to 50 µs.

TABLE III. MPC ALGORITHM COMPUTATIONAL COST

Device Utilization	Available resources	Percent
Total slices	13300	86.9
Slice registers	106400	26.7
Slice LUTs	53200	68.2
Block RAMs	140	6.4
DSP48s	220	90.9

V. TEST BENCH

In this section, the test bench, whose picture is reported in Fig. 7, is discussed. The electrical drive consists of a DigiPower three-phase five-levels Cascaded H-Bridge Multilevel Inverter (CHBMI), composed of six MOSFET-based power H-Bridges, whose technical data are presented in

Table IV, and a and 6 poles, three-phase IPMSM (Magnetic S.r.l., type BLQ-40) with interior SmCo magnets, whose main features are summarized in Table V. The CHBMI is powered by six DC power supply RSO-2400 whose technical data are reported in Table VI. A MAGTROL HD-715 hysteresis brake is used to apply a load torque to the IPMSM, its maximum load torque is 6.2 Nm and the maximum speed is 30000 rpm. The hysteresis brake is controlled by a MAGTROL DSP6001 high-speed programmable dynamometer, which allows direct reading of the quantities of interest such as torque, speed, and mechanical power. The electrical quantities are acquired by Teledyne LeCroy MDA 8028HD oscilloscope, equipped with three high voltage differential probes Teledyne Lecroy HVD3106A 1 kV, 120 MHz, and three high sensitivity current probe Teledyne Lecroy CP030A AC/DC, 30 A rms, 50 MHz. In Table VII the FCS-MPC main parameters are summarized.

TABLE IV. CHBMI MOSFET IRFB4115PBF

Quantity	Symbol	Value
Voltage	V_{dss}	150 V
Resistance	R_{dSon}	9.3 mΩ
Current	I_D	104 A
Turn on delay	T_{Don}	18 ns
Rise time	T_R	73ns
Turn off delay	T_{Doff}	41 ns
Fall time	T_F	39ns
Reverse recovery	T_{RR}	86 ns

TABLE V. PERMANENT MAGNET BRUSHLESS SERVOMOTOR

Quantity	Symbol	Value
Nominal speed	N_{MAX}	4000 rpm
Back EMF	E_p	33 V/krpm
Rated Torque	T_N	1,8 Nm
Rated current	I_N	3,6 A
Maximum Torque	T_p	7,2 Nm
Maximum current	I_p	14.4 A
Pole pairs	p	3

TABLE VI. DC POWER SUPPLY RSO-2400

Quantity	Symbol	Value
Rated output voltage	V_{out}	48 V
Rated output current	I_{out}	50 A
Rated power	P_N	2400 W
Ripple	ΔV	200 mV_{p-p}
Input voltage range	V_{in}	180 ~ 264 VAC
Power factor	cosφ	0.95
Efficiency	η	91.5%
Input current	I_{in}	12 A

TABLE VII. FCS-MPC PARAMETERS

Quantity	Symbol	Value
DC LinkVoltage	V_{DC}	55 V
Pole pairs	p	3
Stator resistance	R	2.21 Ω
Direct inductance	L_d	0.0088 H
Quadrature inductance	L_q	0.0125 H
PM direct flux	λ_{PM}	0.0913 Wb
Sampling period	T_s	100 µs
Delay time	T_d	50 µs

VI. EXPERIMENTAL RESULTS

In this section, experimental results are presented to validate the proposed control algorithm. In detail, in order to analyze the system both in the steady-state and dynamic conditions, two sets of tests are carried out. For steady-state performance analysis, a set of working points have been defined as a function of IPMSM working conditions in terms of speed and load torque. The considered working points are summarized in Table V. For each identified working point, phase voltages v_{AN}, v_{BN}, and v_{CN} and phase currents i_A, i_B, and i_C are measured. The experimental investigations are carried out with an observation window of 1 s and a sampling frequency of 1MS/s, which guarantee a frequency resolution of 1 Hz and a Nyquist frequency of 500 kHz. As performance metrics, the switching frequency, which is correlated to the converter switching losses, the current THD, which is correlated to the load harmonic losses and to the torque ripple, and the voltage THD, which influences the iron losses, are considered.

TABLE VIII. ELECTRIC DRIVE WORKING POINTS

T [Nm]- ω_m [rpm]	1000	2000	3000	4000
1.8	WP4	WP3	WP2	WP1
1.35	WP8	WP7	WP6	WP5
0.9	WP12	WP11	WP10	WP9
0.45	WP16	WP15	WP14	WP13

With respect to the dynamic working condition analysis, a cycle composed by a 0-3000 rpm acceleration, including no-load and load operations, with rated-load torque application, has been applied. During dynamic analysis, the maximum allowed transitory currents were set to i_q=10 A and i_d =0, respectively. IPMSM phase voltages, phase currents, torque and speed signals are acquired with with MDA 8028HD oscilloscope by setting an observation window of 5 s and a sampling frequency of 500 kS/s.

A. Steady-state condition analysis

With respect to the steady-state condition analysis, phase voltages and currents and its spectra are reported in Fig. 8 when IPMSM drive operates in WP 2. It can be noted that, with respect to the voltage spectrum, harmonics amplitude, expressed in percent of the fundamental frequency, is always below 2%, except for the third harmonic (f_3=450 Hz). However, when IPMSM line-to-line voltages and phase voltages are considered, the third and its multiples are absent. For this reason, the third harmonic has a negligible amplitude in the current spectrum. It can be noted that current harmonics have an amplitude always lower than 0.5%. A very similar behavior can be observed in other working points. In Fig. 9(a), the converter switching frequency in the considered working range is reported. Switching frequency estimation has been carried out by counting the phase voltages level transitions N_t along the observation window and dividing by double the observation window T_w, according to (28):

$$f_{sw,m} = \frac{N_t}{2T_w} \tag{28}$$

It can be noted that, in the considered working range, the average switching frequency varies from 2400 to 1400 Hz, proposed algorithm guarantees good dynamic performance, with a reduced speed ripple.

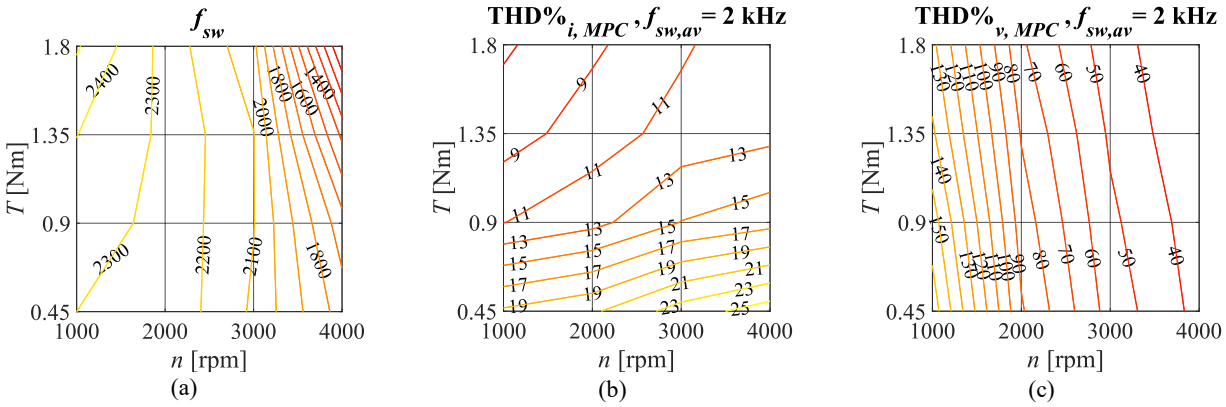

Fig. 10. (a) available H-B future states when rules 1 and 2 are complied, (b-e), available H-B future states when rules 1 and 2 are complied, taking into account the H-B current state (identified by the red circle).

which is much lower than the sampling frequency of 10 kHz. To show the effectiveness of the proposed control strategy for validation purposes, a period of the phase voltage A, expressed in p.u., and the respective gate signals are shown in Fig. 10. These signals have been sampled directly by the control software with the control sampling frequency of 10 kHz. As a way of example, sampling instants *k-1*, *k*, and *k+1* are analyzed. At the sampling instant *k-1*, the set of control signals $S_A(k\text{-}1)$ is equal to [1 1 0 1]. In detail, at the instant *k-1* the H-B_{A2} switches, therefore, according to the algorithm rules discussed in the previous sections, at the instant *k*, the state of H-B_{A2} is locked, and only H-B_{A1} is enabled to switch. The set of control signals $S_A(k)$ is equal to [1 0 0 1]. At the instant *k+1* the state of H--B_{A1} is locked and only HB_{A2} is enabled to switch, therefore, $S_A(k+1)$ = [1 0 1 1]. It must be underlined that, even if a certain H-B is enabled to switch, its state can remain the same of the previous sampling instant. In this case, the solution of the optimal control problem is the same of the previous iteration, which happens, as a way of example, at the sampling instant *k-6*. In Fig. 9 (b-c), the current THD and voltage THD trends in all the working range are reported, respectively. It can be noted that the current THD varies in the range 25-8%. In detail, for a fixed speed, the THD drastically decreases when the load torque increase. This behavior is linked with an increment of the fundamental frequency. Moreover, it can be noted a correlation between the current THD and the speed, such that the THD slowly increase when the speed increase. This behavior can be justified by a progressive decrement of the switching frequency when the speed increase. About the voltage THD, it varies in the range of 150 – 40%. It can be noted that the THD variation is strictly correlated to the speed. In detail, when the speed increases, the THD decrease. Moreover, the voltage THD is quite independent of the load torque. Looking at phase voltages reported in Fig. 8 and Fig. 10, it can be noted that the *dv/dt* is always equal to the DC link voltage V_{DC}, as expected by the imposed control rules, thus, condition (14) is verified.

B. *Dynamic analysis*

IPMSM phase currents, speed and torque trends during the adopted dynamic cycle are reported in Fig. 11. It can be noted that the speed transient ends in about 0.5 s. At the instant t_1=1.55 s, the rated load torque is applied to the motor. It causes a speed transient that ends after 0.35 s. At the instant t_2=3.18 s the load torque is removed and the speed transient ends after 0.18 s. The reported trends allow stating that the

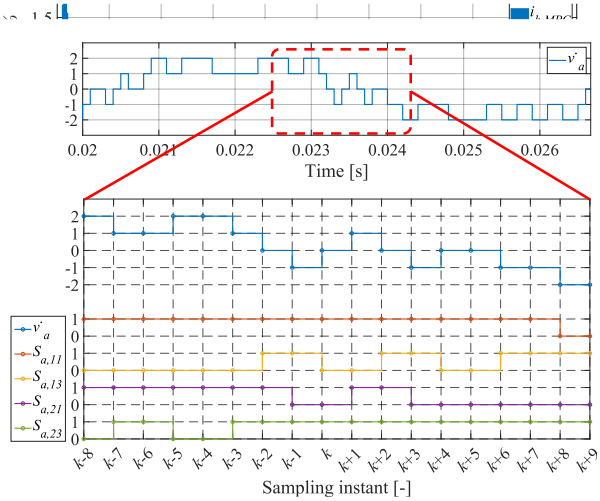

Fig. 9. Gate signals.

VII. Conclusions

In this work, an FCS-MPC for a 3P-5L-CHBMI-fed IPMSM electric drive with online candidate states selection is presented. In detail, the MPC mathematical formulation is presented and the proposed algorithm is discussed. The proposed algorithm is based on two rules which guarantee that only one H-B per phase can switch over a sampling instant and, with respect to the enabled H-B, only one H-B leg can switch over a sampling instant. These rules are complied by introducing the *enabling* variable *M* and by taking into account the current state of the system, such that the set of available transitions depends on the current H-B module state. The proposed algorithm allows for complying with several goals: the future candidate states are reduced from 4096 to 27, therefore the MPC computational cost is drastically reduced; the switching devices state transitions, which are strictly correlated to the converter switching losses, are minimized; the phase voltages *dv/dt* is minimized since it can reach the maximum value of V_{DC}. The proposed algorithm has been implemented on the sb-RIO 9651 SoM. The implementation process has been discussed: in detail, equations for the delay compensation process have been introduced and the algorithm optimization for an optimal implementation has been presented. Experimental results have been presented and discussed in order to validate the proposed control algorithm. In detail, a steady-state analysis and a dynamic analysis have

been carried out. Experimental results confirm that the proposed control goals have been reached. Moreover, the

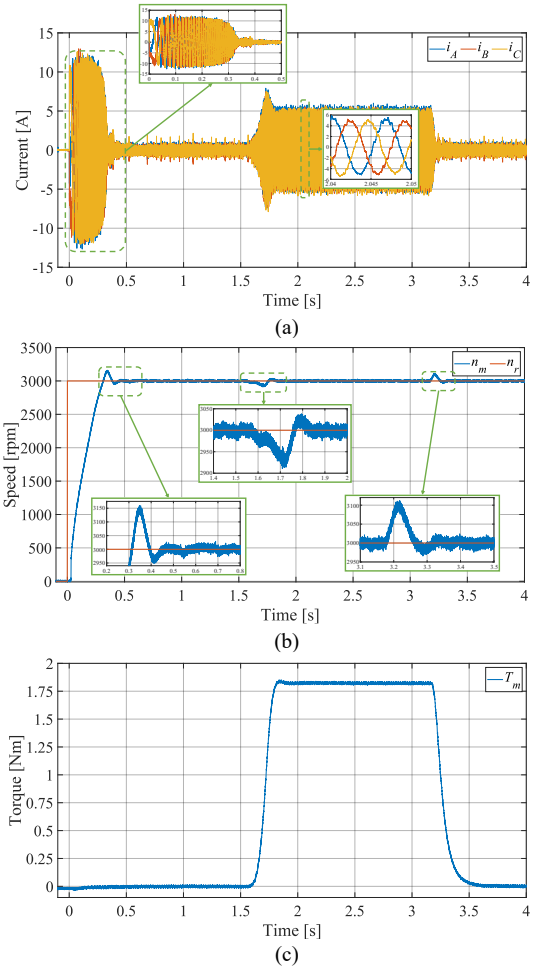

Fig. 11. Phase voltages and currents in steady-state conditions, WP2: (a) time domain, (b) frequency domain.

control guarantees good dynamic performance and low current THD with a very low switching frequency.

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