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# A Voltage-Controlled Split-pi Converter Interfacing a High-Voltage ESS with a DC Microgrid: Modeling and Experimental Validation

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**Abstract.** The Split-pi converter can be used for the bidirectional connection of an energy storage system (ESS) and a DC microgrid. It is common to have a DC bus voltage higher than the ESS voltage, but sometimes a high-voltage ESS is needed to satisfy current constraints and still reach high power levels. Therefore, in these scenarios, the grid-side voltage can be lower than the ESS voltage, for example, when the DC bus voltage is as low as 48 V. This paper presents a model of the Split-pi converter interfacing a high-voltage ESS to a low-voltage DC bus. In the three considered scenarios, the converter's output voltage is the main controlled variable. A state-space model is developed accounting for the parasitic elements. Compared to the case of a Split-pi working with a DC bus voltage higher than the ESS voltage, the controllers' design is more challenging due to the presence of the input LC filter. Finally, the proposed model is validated through simulations and experimental tests on a prototype implementation of the Split-pi converter.

## 1 Introduction

The advantages of DC microgrids, which allow for a simplification of electrical systems and enable high-efficiency operation, are stimulating a renewed interest in power electronic converters for energy storage systems (ESS) [1]–[3]. As for the converter topology, the dual active bridge (DAB) represents an advantageous solution to interface an ESS with a DC bus if an isolated DC/DC converter is needed [4]–[6]. However, bidirectional non-isolated DC/DC converters can improve efficiency, size, weight, and cost [4], [7]. Among them, the Split-pi topology is an interesting possibility. The Split-pi converter is formed by cascading two bidirectional power converters having a half-bridge topology. The two half-bridge converters (HBCs) share a bulk capacitor, as illustrated in the scheme of Fig. 1. The Split-pi has four operating modes depending on the direction of power flow and the relationship between the input and output voltages. The power flows from the storage side to the grid side in modes 1 and 3 and vice versa in modes 2 and 4. Furthermore, in modes 1-2, the ESS voltage is lower than the grid-side voltage, whereas the opposite relationship holds in modes 3-4.

Like the DAB converter, the Split-pi is characterized by high efficiency. In addition, it encompasses a lower number of power switches and presents smaller reactive components with respect to the DAB; finally, it is suitable for multiphase applications [8]–[16]. However, few papers have been published on the Split-pi so far, and only five analyzed the Split-pi converter controlled in a closed-loop scheme [14]–[18]. Particularly, [17] and [18] showed how to properly model and control a Split-pi that interfaces an ESS with a DC bus in a microgrid application. In such papers, each of the five possible DC microgrid operating scenarios was analyzed. Such scenarios stem from the diverse associations of the possible control modes for the storage and grid-side converters and the nature of the active load on the grid side of the Split-pi. It is worth noting that the storage converter can be controlled according to one of the following goals: 1. make the ESS behave as a stiff voltage generator, 2. make the ESS behave as a non-stiff voltage generator, or 3. make the ESS behave as a current generator subject to a higher-

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level control law imposed by an energy management system (EMS). At the same time, the DC microgrid can include a mix of droop-controlled voltage generators, current generators, and passive loads.

In [17] and [18], the operation of the Split-pi in modes 1-2 was considered. Although this condition is often met, the Split-pi can also operate in modes 3-4. In fact, a high-voltage ESS (higher than 200 V) is sometimes needed to satisfy current constraints descending from technical and safety considerations and still reach high power levels. In such situations, the grid-side voltage can be lower than the ESS voltage, for example, when the DC bus voltage is as low as 48 V.

The symmetry and bi-directionality of the Split-pi converter could lead one to think that no modification occurs with respect to the configuration considered in [17]-[18] if the relationship between the voltages of the ESS and the DC bus is exchanged. In fact, in modes 2-3 (i.e., with power flow from the high side to the low side), the converter can always be considered as a buck converter cascaded to an LC filter. Such a filter is formed by combining the high-side inductor and the bulk capacitor. Nevertheless, there is a significant difference that has an impact on the state-space model of the Split-pi. In mode 2, the current on the inductor of the buck's output LC filter (low-side inductor plus low-side capacitor) is regulated by the inner current loop, as shown in [17]. Conversely, in mode 3, the inner current loop is aimed at controlling the current on a different LC filter, i.e., the one formed by the high-side inductor plus the bulk capacitor. If this filter introduces a poorly damped resonance, the controllers' design gets more complex than for the Split-pi converter operating in modes 1-2. Furthermore, the bandwidth that the control system can achieve is more limited.

In this paper, the Split-pi converter studied in [17],[18] is once again considered as a case study, but the voltage levels of the DC microgrid and the ESS are swapped: the Split-pi converter now interfaces a 48 V DC microgrid with a 180 V ESS. Therefore, the converter is supposed to operate in modes 3-4, whereas it operated in modes 1-2 in [17]-[18]. As in [19], the study is carried out considering three common microgrid scenarios in which the output voltage of the Split-pi is the main controlled variable. The converter is modeled by a suitably devised state-space model that considers the parasitic elements. The control system is presented, and several details about the controller design are given. After showing the importance of the feed-forward action to keep the microgrid voltage within the allowed transient tolerance, several simulations are carried out to assess the performance in each scenario. Finally, experimental tests are performed on the prototype implementation of the Split-pi described in [18]. The obtained results show coherent behavior, thus validating the proposed study.

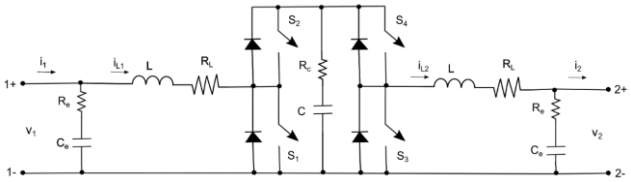


**Fig. 1** Electrical scheme of the Split-pi.

## 2 Brief Review of the Case Study

This Section briefly recalls the features of the case study described in [17], highlighting the differences between the operation in modes 3-4 vs. 1-2. In particular, the converter's rated parameters, the microgrid scenarios, and the control scheme architecture are recalled.

### *2.1. Case Study*

During the Split-pi's operation in modes 3-4, the voltage relationship is $V_1 > V_2$, and the four switches are driven with the following duty cycle values: {HBC1_top, HBC1_bottom, HBC2_top, HBC2_bottom} = {1, 0, d, 1-d}. The power flows from port 1 to 2 in mode 3 and vice versa in mode 4. For the present study, most of the converter's rated parameters are those reported in Tab. 3 of [17]. However, in modes 3-4, the input and output currents/voltages are exchanged; thus, some parameters are different: the maximum storage charging/discharging current is 5 A, the nominal duty cycle is $\bar{d}$=0.277, and the rated load resistance is $R_n$=3.333 Ω.

### *2.2. Microgrid Scenarios*

As explained in [17], five DC microgrid scenarios can be considered. They stem from the diverse associations of the three possible control modes for the storage and grid-side converters (non-stiff droop control, stiff droop control, and current control) and the nature of the active load on the grid side of the Split-pi. For the sake of clarity, an abbreviation in the form Sx-Gy is used to identify each scenario. In particular, x and y can vary as follows: D=non-stiff droop control; S=stiff droop control; C=current control; N=no grid-side generator is present or operated with droop control. As stated in the Introduction, the present study considers only the scenarios in which the Split-pi's output voltage is the main controlled variable:

- Scenario #1 (SS-GN): stiff microgrid formed by the Split-pi; passive load or external current generators controlled by the EMS
- Scenario #2 (SD-GN): non-stiff microgrid; droop control on Split-pi; passive load or external current generators controlled by the EMS
- Scenario #3 (SD-GD): non-stiff microgrid; droop control on Split-pi; at least one microgrid generator is droop controlled.

In the most general case, the Split-pi's load comprises the microgrid's passive loads, voltage generators, and current generators. In particular, in the three considered scenarios, it is possible to aggregate such devices and consider an equivalent current generator $I_{eq}$ connected in parallel to a load resistor $R$.

### *2.3. Control Scheme Architecture*

As discussed in [17], the control architecture for the Split-pi is based on a current loop to control the storage-side current $I_{L1}$ and a voltage loop to regulate the grid-side voltage $V_2$. In addition, a feed-forward (FF) action is included to keep the microgrid voltage within the allowed transient tolerance. Such a term equals $\bar{d}$ in modes 3-4, whereas it was $(1-\bar{d})^{-1}$ in modes 1-2. To show the importance of the FF action, besides the three scenarios, it is worth also considering a baseline scenario with the FF action disabled. Finally, it is worth recalling that scenarios #2 and #3 require a third voltage loop to implement the ESS's droop characteristic.

Fig. 2 shows the closed-loop control scheme for the voltage-controlled Split-pi, which is coherent with [17],[19]. The dependence of the input inductor current $I_{L1}$ on the duty cycle $d$ is expressed by the transfer function $G_{p1}(s)$. The relationship between the output current $I_2$ and $I_{L1}$ is described by $G_{p2}(s)$. Furthermore, the relationship between $I_{L1}$ and $V_2$ is $G_{p2}(s)\cdot R$. As for the current and voltage controllers, their transfer functions are $G_{ci1}(s)$ and $G_{cv2}(s)$, respectively. Finally, Fig. 2 shows that the equivalent current generator $I_{eq}$ generates a disturbance that is summed to the output of $G_{p2}(s)$. Regardless of the transfer function represented by an ellipsis, this disturbance must be suitably compensated for by the control system.

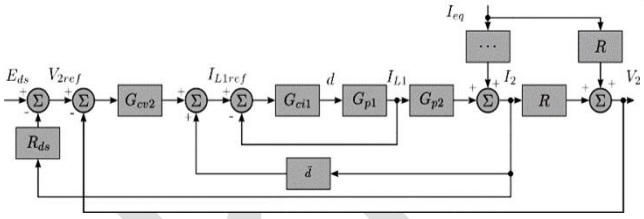


**Fig. 2** Control scheme for the voltage-controlled Split-pi.

## 3 Split-pi's State-Space Model

By using the approach presented in [20], the state-space model of the Split-pi converter operating in the considered scenarios was devised. The parasitic elements were properly considered. The state-space model could be expressed using matrix notation as in [19]:

$$\begin{cases}\dot{x} = Ax + Bu \\ y = Cx + Du\end{cases} \text{ with } \begin{cases}A = dA_{on} + (1-d)A_{off} \\ B = dB_{on} + (1-d)B_{off} \\ C = dA_{on} + (1-d)C_{off} \\ D = dD_{on} + (1-d)D_{off}\end{cases} \quad (1a,b)$$

assuming $R_{sum}=R+R_e$, $R_p=R\cdot R_e/R_{sum}$, $R_{tot}=R_p+R_L+R_c$, and:

$$x = [I_{L1},\ I_{L2}, V_c,\ V_e]' \quad (2)$$

$$u = [V_1, I_{eq}]' \quad y = [I_{L1}, V_2, I_2]' \quad (3a,b)$$

$$A_{on} = \begin{bmatrix} -\frac{R_L+R_c}{L} & \frac{R_c}{L} & -\frac{1}{L} & 0 \\ \frac{R_c}{L} & -\frac{R_{tot}}{L} & \frac{1}{L} & -\frac{R}{LR_{sum}} \\ \frac{1}{C} & -\frac{1}{C} & 0 & 0 \\ 0 & \frac{R}{R_{sum}C_e} & 0 & -\frac{1}{R_{sum}C_e} \end{bmatrix} \quad (4)$$

$$A_{off} = \begin{bmatrix} -\frac{R_L+R_c}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & -\frac{R_p+R_L}{L} & 0 & -\frac{R}{LR_{sum}} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{R}{R_{sum}C_e} & 0 & -\frac{1}{R_{sum}C_e} \end{bmatrix} \quad (5)$$

$$B_{on} = B_{off} = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{R_p}{L} \\ 0 & 0 \\ 0 & \frac{R}{R_{sum}C_e} \end{bmatrix} \quad (6)$$

$$C_{on} = C_{off} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & R_p & 0 & \frac{R}{R_{sum}} \\ 0 & \frac{R_e}{R_{sum}} & 0 & \frac{1}{R_{sum}} \end{bmatrix} \quad (7)$$

$$D_{on} = D_{off} = \begin{bmatrix} 0 & 0 \\ 0 & R_p \\ 0 & -\frac{R}{R_{sum}} \end{bmatrix} \quad (8)$$

## 4 Design of the Split-pi Controllers

According to [21], the state-space model was linearized in the neighborhood of the nominal working point corresponding to $\bar{d}$ and $\bar{x} = [I_{L10}, I_{L20}, V_{c0}, V_{e0}]' = [4.167, 15, 180, 50]'$. The linearization allowed deriving the transfer functions $G_{p1}(s)$ and $G_{p2}(s)$ that constitute the small-signal model. The controllers $G_{ci1}(s)$ and $G_{cv2}(s)$ were based on $G_{p1}(s)$ and $G_{p2}(s)$ and were obtained considering specific values of the phase and gain margins ($m_\varphi$ and $m_g$) and of the crossover frequency ($\omega_c$) [17], [22].

These three design parameters influence the transient behavior of the system. In fact, the phase margin affects the dynamic precision; in particular, low phase margin values imply low damping coefficients and, consequently, high overshoots. On the other hand, the crossover frequency influences the system response speed: a high value of $\omega_c$ implies a high bandwidth and, consequently, a short rise time. It is worth noting that a short rise time does not always

imply a short settling time since the latter also depends on the phase margin. In fact, a short settling time is obtained with simultaneously high values of crossover frequency and phase margin. Finally, a sufficiently high value of the gain margin is necessary to ensure system stability even in the presence of parameter variations. In this regard, relying only on the phase margin is not enough.

As said, the controllers were based on the small-signal transfer functions derived by linearizing the state-space model in the neighborhood of its nominal working point. However, if the stability margins are wide enough, the behavior of the controlled system is expected to be good with lower loads as well. Indeed, in scenarios baseline, #1, and #2, it is $R=R_n$; instead, in scenario #3, $R$ is very small due to the parallel connection between $R_n$ and the droop resistance $R_d$ of the voltage generator. Furthermore, in scenarios #2 and #3, the droop parameters of the ESS converter (i.e., $E_{ds}$=50 V and $R_{ds}$=0.2 Ω) were obtained by considering a 6% voltage reduction at the rated current. Instead, the droop parameters of the external voltage source in scenario #3 were $E_d$=55 V and $R_d$=0.666 Ω. With these values, the ESS converter was expected not to supply any power for half the nominal load power and to be charged/discharged below/above the nominal load power.

It is helpful to give further remarks on the controller design. First, a resonance at ω=1330 rad/s was determined by the LC filter before HBC1, and the corresponding damping coefficient was very low (ζ=0.1). Moreover, the bandwidth could not be increased by considering a simple PI controller due to the presence of the complex conjugate poles. Therefore, a PID regulator, whose transfer function is (9), was necessary. In any case, the maximum crossover frequency could not be higher than 1200 rad/s.

Furthermore, the gain at the switching frequency ($F_{sw}$=20 kHz) needed to be reduced by including a pole at $10^5$ rad/s in the current controller. However, this far pole had to be moved at $4\cdot10^4$ rad/s. In fact, the sampling frequency of the discrete-time controller was equal to $F_{sw}$; thus, a pole at $10^5$ rad/s could not be implemented.

In general, if the current reference varies, the current controller can attenuate the resonance. On the other hand, modifications of the load resistance are to be governed only by the voltage regulator. This regulator was a PI controller in conjunction with a pole at half the resonance frequency. Moreover, a phase margin of 85° was insufficient to compensate for the resonance, so it had to be increased to 120°.

The chosen controller parameters are shown in Tab. 1, which was extracted from [19]. The dynamics of $I_{L1}$ were similar in all the scenarios; therefore, similar parameters were obtained for the corresponding controllers. With regard to the voltage controller without the FF term, the dynamics of $V_2$ were sensitive to the resistance $R$; for this reason, it was necessary to use the right value of this parameter to design the system. Nevertheless, the FF term helped decrease the sensitivity. For this reason, comparable voltage regulators were obtained in scenarios #1, #2, and #3, even with different resistance values.

$$G_{PID}(s) = \left(K_p + \frac{K_i}{s} + sK_d\right)\frac{1}{1 + s\frac{K_d}{NK_p}} \qquad (9)$$

**Table 1** PI and PID Coefficients

| Loop Controller and Scenario | Values of $\omega_c$, $m_\varphi$, and $m_g$ | PI and PID Coefficients |
|---|---|---|
| $G_{ci1}$ for current $I_{L1}$<br>baseline, #1 (SS-GN), and #2 (SD-GN) | $\omega_c$=1200 rad/s<br>$m_\varphi$=94°<br>$m_g$=∞ | $K_{pi}$ = 4.507E-3<br>$K_{ii}$ = 31.2608<br>$K_{di}$ = 1.711E-5<br>$N$ = 37.9651<br>+ pole @ 4.0E4 rad/s |
| $G_{ci1}$ for current $I_{L1}$<br>#3 (SD-GD) | $\omega_c$=1200 rad/s<br>$m_\varphi$=89.8°<br>$m_g$=∞ | $K_{pi}$ = 3.207E-3<br>$K_{ii}$ = 26.6073<br>$K_{di}$ = 1.343E-5<br>$N$ = 41.876<br>+ pole @ 4.0E4 rad/s |
| $G_{cv2}$ for voltage $V_2$ w/o FF<br>baseline | $\omega_c$=100 rad/s<br>$m_\varphi$=120°<br>$m_g$=31 dB | $K_{pv}$ = 0.1275<br>$K_{iv}$ = 11.885<br>+ pole @ 666 rad/s |
| $G_{cv2}$ for voltage $V_2$ w/ FF<br>#1 (SS-GN) and #2 (SD-GN) | $\omega_c$=100 rad/s<br>$m_\varphi$=120°<br>$m_g$=29.4 dB | $K_{pv}$ = 0.076<br>$K_{iv}$ = 5.1286<br>+ pole @ 666 rad/s |
| $G_{cv2}$ for voltage $V_2$ w/ FF<br>#3 (SD-GD) | $\omega_c$=100 rad/s<br>$m_\varphi$=120°<br>$m_g$=43.9 dB | $K_{pv}$ = 0.097<br>$K_{iv}$ = 4.7315<br>+ pole @ 666 rad/s |

## 5 Simulations Results

The controlled Spit-pi converter was simulated in all the considered scenarios according to [19]. In the following subsections, the obtained results are presented and discussed.

### *5.1. Baseline Scenario and Scenario #1 (SS-GN)*

In the baseline scenario, the FF action was disabled, and the converter was used to create a stiff microgrid at 50 V. A passive load and an external current generator $I_d$ were also connected to the microgrid. During the first 200 ms, the converter reached a steady state after applying $R=R_n$ and $I_d=0$. Then, every 200 ms, step variations of $R$ and $I_d$ were applied as follows: $R=\{2,100,2,1,2,100,2\}\cdot R_n$ and $I_d=\{0,0,1,1,1,0,0\}\cdot I_n$. Accordingly, the storage system was first discharged, then charged, and finally discharged again. Fig. 3 shows the grid voltage variation expressed in percent of $V_{2n}$ (blue curve). The voltage was correctly regulated once the steady state was reached. However, the voltage variation exceeded the allowed tolerance (±20%), causing the intervention of the protection devices. As shown by the orange curve in Fig. 3, using the FF action in scenario #1 can reduce the voltage variation suitably. Specifically, the reduction was up to 39%.

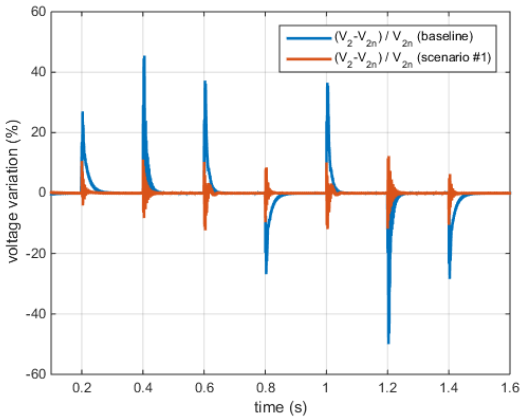


**Fig. 3** Voltage variation in baseline scenario and scenario #1 (SS−GN).

Although very large stepwise load variations such as $R_n \leftrightarrow 100 \cdot R_n$ could be tolerated during the operation in modes 1-2 [17][18], they lead to very high voltage variations in modes 3-4. For example, Fig. 4 shows the voltage variation profiles obtained without and with the FF action when the values of $R$ and $I_d$ were changed every 200 ms in a stepwise fashion according to the following sequences: $R=\{1,100,1,1,1\} \cdot R_n$ and $I_d=\{0,0,0,1,0\} \cdot I_n$. According to such profiles, the maximum voltage variations obtained while deactivating or activating the FF action would be +91% and +27.3%, respectively.

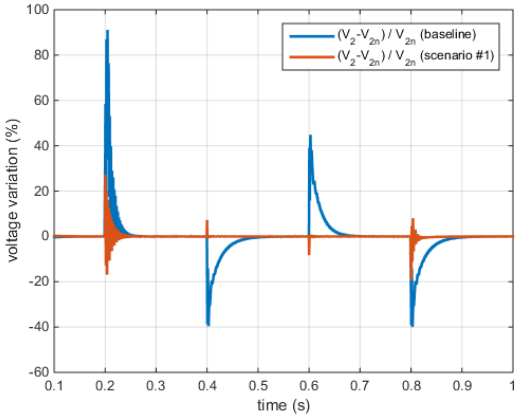


**Fig. 4** Voltage variation in baseline scenario and scenario #1 (SS−GN) with very large stepwise load variations.

Such very large stepwise load variations could be tolerated if the values of $L$ and $C$ were changed to increase the LC filter's resonance frequency and damping. However, the ripple on the inductor current and the capacitor voltage would increase too. For this reason, such large stepwise load variations (i.e., $R_n \leftrightarrow 100 \cdot R_n$) will not be considered in scenarios #2 and #3.

However, it is worth highlighting for completeness that the considered stepwise variations, although useful for control design, are never applied in real-world applications. In fact, the dynamics of real-world loads and generators are not instantaneous. Thus, such devices require a certain amount of time to exhibit the maximum variation of load resistance ($R_n \leftrightarrow 100 \cdot R_n$) or external current ($0 \leftrightarrow I_n$). This behavior can be simulated by including a rate limiter block in the simulation model. The parameters of such a block can be expressed as $\pm 100 \cdot R_n / t_{lim}$ for the load resistance and $\pm I_n / t_{lim}$ for the external current generator. Thus, it is worth determining the minimum value of $t_{lim}$ that allows keeping the microgrid voltage within the allowed transient tolerance of ±20% when the FF action is activated. The obtained value is $t_{lim}$=1.7 ms and is more than reasonable. Fig. 5 shows the voltage variation profiles obtained when the values of $R$ and $I_d$ were changed with and without the rate limiters according to the following sequences: $R=\{1,100,1,1,1\} \cdot R_n$ and $I_d=\{0,0,0,1,0\} \cdot I_n$. The corresponding maximum voltage variations are +19.9%/-16.2% with the rate limiters against +27.3%/-19.3% without the rate limiters.

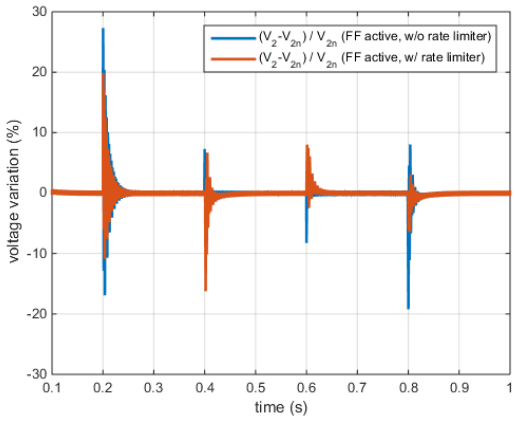


**Fig. 5** Voltage variation without and with rate limiter with very large stepwise load variations and FF enabled.

### *5.2. Scenario #2 (SD-GN)*

In scenario #2, the FF action was enabled, and the droop characteristic was implemented by closing the outer control loop. The simulation was performed as in scenario #1, i.e., considering $R=R_n$ and $I_d=0$ as the initial conditions and applying the following load sequence: $R=\{1,2,100,2,1,2,100,2\} \cdot R_n$ and $I_d=\{0,0,0,1,1,1,0,0\} \cdot I_n$. Fig. 6 shows the obtained voltage variation. The reference voltage was computed based on the droop characteristic and tracked by the converter's output voltage thanks to the control system. Specifically, considering the steady-state values in the waveform of Fig. 6, a -6% voltage variation was obtained during the storage system's discharge at the nominal power. Coherently, a +3% variation was exhibited when the storage system was charged at half the rated power. As for the transients, if the overshoots are also considered, the voltage variation did not exceed ±12.7%.

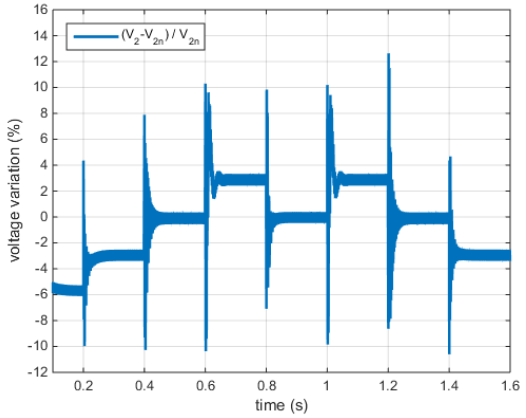


**Fig. 6** Voltage variation in scenario #2 (SD−GN).

*5.3. Scenario #3 (SD-GD)*

In scenario #3, droop control was used for both the storage converter and the microgrid's voltage generator. The microgrid also encompassed a current generator. During the first 200 ms, the converter reached a steady state after applying $R=100 \cdot R_n$ and $I_d=0$. The storage system was recharged at -5.65 A, and the microgrid voltage exhibited a +2% variation. Then, every 200 ms, step variations of $R$ and $I_d$ were applied as follows: $R=\{2,1,1,2,100\} \cdot R_n$, $I_d=\{0,0,0.457,0.457,0.457\} \cdot I_n$. Correspondingly, the storage system's current exhibited the following values: {0 A, 5.5 A, 0 A, -5.15 A, -10.8 A} (positive=discharging; negative=charging). Fig. 7 shows the obtained voltage variation, which did not exceed ±12.9%.

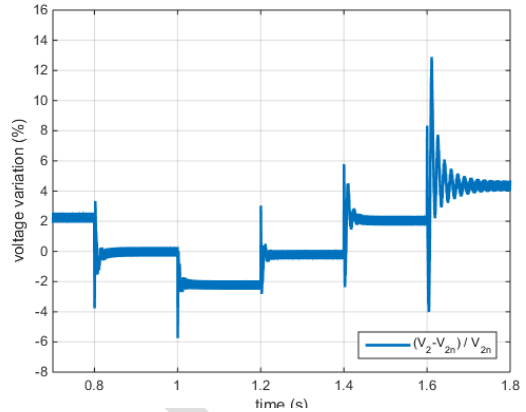


**Fig. 7** Voltage variation in scenario #3 (SD−GD).

## 6 Experimental Results

This Section presents the experimental results obtained on a prototype implementation of the Split-pi converter according to [19]. These results will serve as the experimental validation of the previous simulation results.

The prototype implementation of the Split-pi converter is the same as described in [18] and is based on an integrated 3-phase, IGBT-based H-bridge STGIPS10K60A. The storage system connected to port 1 was emulated with a TDK-Lambda GEN600-5.5 power supply set to 180 V. A Sorensen SLH-500-6-1800 programmable electronic load and a TDK-Lambda GEN60-40 power supply were used as an active load connected to port 2. The latter device can serve as both a voltage generator and a current generator, depending on the requirements of the test scenario. A dSPACE DS1103 board was used to control the converter and acquire the relevant electrical signals, which were then plotted in MATLAB.

*6.1. Baseline Scenario and Scenario #1 (SS-GN)*

The Split-pi converter was controlled to create a stiff microgrid with a lumped passive load. The FF action was disabled in the baseline scenario and enabled in scenario #1. As shown in Fig. 8, around t = 0 s, a sudden load variation was applied, i.e., an increase from 10 Ω to 20 Ω. Accordingly, the load power decreased from 250 W to 125 W, determining a transient in the output voltage $V_2$, shown as a percentage variation in Fig. 8. The adoption of the FF action significantly reduced the voltage overshoot, from 13.5% to around 5.5%, and allowed for higher dynamic performance. Similar results were obtained for the opposite load variation, for which the undershoot was reduced from -11.2% to -5.6%. It is reasonable to expect that even more pronounced voltage variation reductions can be obtained following larger load variations. Unfortunately, these conditions cannot be tested due to the limited power capability of the test rig.

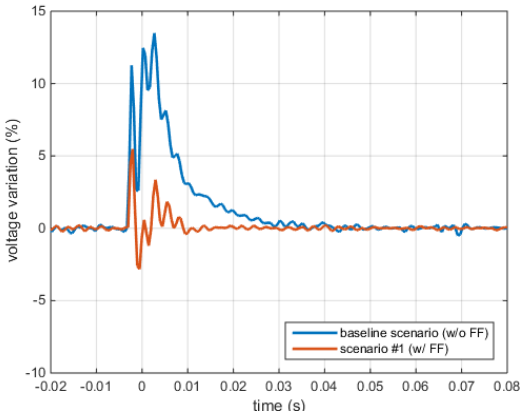


**Fig. 8** Experimental voltage variation in the baseline scenario and scenario #1 (SS−GN).

*6.2. Scenario #2 (SD-GN)*

In this scenario, the Split-pi converter was controlled in droop mode with a droop resistance set to 1.2 Ω and a no-load voltage of 50 V. The external current generator was set to give a constant current value of 1.25 A, and the passive load was set to a constant value of 20 Ω. In this configuration, while the current generator was on, the converter supplied the load with the remaining current quota needed to respect the droop characteristic, i.e., around 1.25 A, as shown in Fig. 9. Instead, when the current

generator was switched off at around t = 0 s, the load was entirely powered by the Split-pi converter, as expected. In both cases, the voltage reduction was equal to the value imposed by the droop characteristic: -3% and -5.66% when the generator was on and off, respectively.

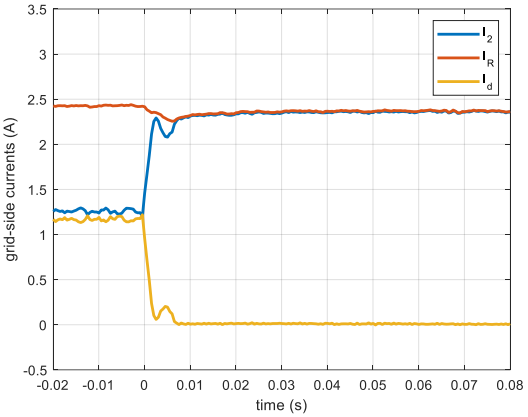


**Fig. 9** Experimental grid-side currents in scenario #2 (SD−GN).

*6.3. Scenario #3 (SD-GD)*

Fig. 10 shows the load current quotas given in scenario #3 by the microgrid's voltage generator ($I_d$) and the Split-pi converter ($I_2$), as well as the load current ($I_R$). In this case, both the converter and the voltage generator were controlled in droop mode with a droop resistance set to 1.2 Ω. The resulting non-stiff microgrid had a no-load voltage set to 50 V. In this test, at t = 0 s, the load was reduced from 20 Ω to 10 Ω, doubling the requested power. As expected, the converter and the voltage generator kept sharing the load demand equally. As in the previous test, the voltage variations were those entailed by the droop characteristics, i.e., -3% and -5.66%. The two values were equal to those of the previous test because the external generator's contribution $I_d$ was coincidentally identical.

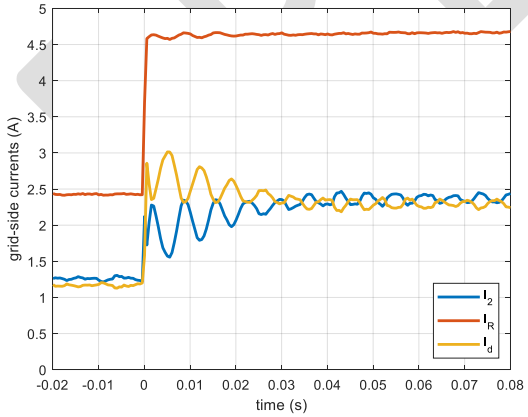


**Fig. 10** Experimental grid-side currents in scenario #3 (SD−GD).

## 7 Conclusions

In this work, a state-space model was devised for a Split-pi converter operated with a DC bus voltage lower than the storage voltage. The parasitic elements were taken into account. Three common microgrid scenarios were considered, and the output voltage of the Split-pi was the main controlled variable in all of them. Then, the state-space model was linearized around the rated operating point to design the current and voltage controllers. Furthermore, it was discussed how the input LC filter determines a resonance with very low damping, thus limiting the bandwidth that the control system can achieve. This resonance also made the controller design more challenging than in a Split-pi working with a DC bus voltage higher than the storage voltage. Simulation results showed the good behavior of the controlled system in all the scenarios. Then, the proposed approach was validated experimentally on a prototype converter connected to a 48 V DC microgrid and a 180 V ESS. This setup can be used as a laboratory-scale prototype of maritime and terrestrial microgrids. Finally, it should be noted that the presented method can also be applied to other bidirectional DC/DC converters.

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