Enhanced modulation strategy for 7-level voltage waveform in asymmetrical 5-level Cascaded H-Bridge Inverters

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Abstract— The CHBMI performance optimization can be reached both with hardware and software solutions. Generally, asymmetrical configurations allow the extension of the voltage levels number and the implementation of an innovative modulation strategy allows for improving the performance in terms of harmonic distortion and conversion efficiency. This work is devoted to the development of a modulation strategy that allows improving the performance of an asymmetrical single-phase five-level Cascaded H-Bridge Inverter generating a 7-level voltage waveform. Thus, a digital approach and corresponding digital functions are presented. Subsequently, the impact of the dead time and the influence on the voltage harmonic distortion have been discussed. Through simulation analysis, in the Matlab environment, the main benefits and drawbacks of the proposed approach have been discussed.

Keywords—Asymmetrical Cascaded H-Bridge Inverter, Modulation techniques, SHE or SHM algorithms, Dead time, THD.

I. INTRODUCTION

As well known, power electronics are going to increase in modern electrical systems [1]-[4]. Traditional two or three-level inverters are employed in several fields of applications. In particular, in the automotive field for Electrical Vehicles (EVs) or Hybrid Electrical Vehicles (HEVs) power inverter plays an important role due to their impact on electrical drive performance in terms of iron losses and torque ripple. In this context, Multilevel Power Inverters (MPIs) represent a promising solution in terms of lower total harmonics distortion (THD), higher efficiency, increased voltage/power handling capability, and reduced component stress, hence high reliability. According to [5], the authors have demonstrated that the MPI allows for increasing the efficiency of the electrical drive system. Moreover, the Cascaded H-Bridge (CHB) topology structure allows for obtaining other advantages such as modularity and fault-tolerant capability. By changing point of view, for CHB inverters are available several modulation strategies that allow obtaining different converter performances in terms of voltage harmonics and conversion efficiency. In all cases where high converter efficiency is required, Selective Harmonic Elimination (SHE) or Selective Harmonic Mitigation (SHM) algorithms allow for increasing the converter performance by reducing the switching losses [6]-[7].

Another interesting feature of CHB inverters regards the composition of the voltage waveform among the voltage levels. In this way, the asymmetrical configuration can be employed in order to increase the converter performance (harmonic distortion and converter efficiency), as investigated in [8]-[10] for electric drive applications. Indeed, by considering an asymmetrical configuration, where the DC sources amplitudes are properly chosen, it is possible to increase the voltage levels by maintaining the same topology structure. As suggested in [11] and [12], the authors have demonstrated that by maintaining a 5-level CHB topology structure it is possible to obtain a 7-level and 9-level voltage waveform. In this way, the converter performance can be improved without increasing the hardware complexity. Nevertheless, complete studies that propose a simple approach that take into account the implementation issue in the common electronic devices and that analyse the potentiality of the voltage waveform, in terms of harmonic content and converter efficiency, are missing.

This work aims to analyse an improved 7-level voltage waveform obtained with an asymmetrical configuration of a 5-level CHB inverter. The analysis is focused on the implementation issues by proposing a simple digital approach. For this purpose, SHE and SHM have been considered for comparative analysis with a conventional 7-level CHB inverter. Moreover, the main benefits of this approach have been investigated in terms of THD and the possibility to eliminate one more harmonic with respect to the traditional symmetric 7-level configuration.

Simulation results were compared with a traditional 7-level symmetrical configuration where three case studies

have been discussed. Thus, the advantages and drawbacks of the proposed method have been investigated.

II. IMPROVED STRATEGY FOR 7-LEVEL VOLTAGE WAVEFORM

As well known, a symmetrical 7-level CHB inverter is composed of three H-Bridge (HB) modules cascaded connected in which the output voltage $v(t)$ is the sum of the instantaneous voltage of each module with the same amplitude (V_{dc}):

$$v(t) = v_{HB1} + v_{HB2} + v_{HB3} \qquad (1)$$

where v_{HB1}, $v_{HB2,}$ and v_{HB3} are the output voltage of each H-Bridge module, respectively.

Figure 1 shows an asymmetrical topology structure of a 5-level CHB inverter where the DC voltage amplitudes of the HB$_1$ and HB$_2$ modules are V_{dc} and $2V_{dc}$, respectively.
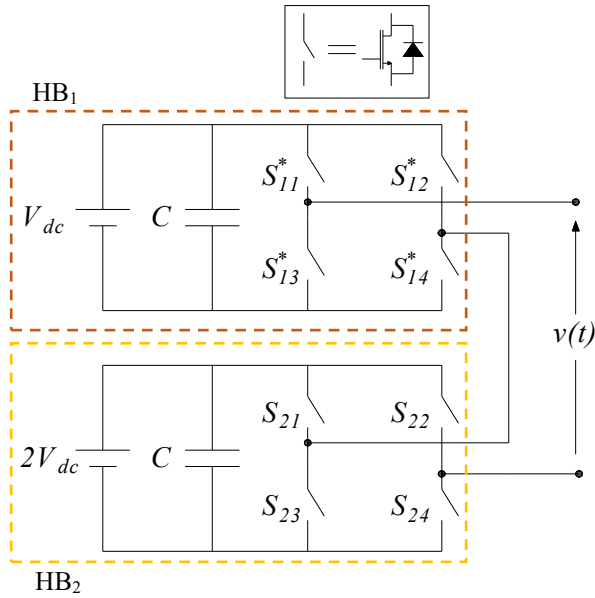

Fig. 1: Asymmetrical CHB inverter

By using the topology structure shown in Fig.1, it is possible to demonstrate that a 7-level voltage waveform can be obtained, as shown in Fig.2. It is interesting to note that the voltage waveform presents a staircase trend like in a symmetrical CHB inverter due to the chosen of the DC voltage amplitudes.

This improved performance can be obtained by implementing a traditional modulation strategy for a 7-level inverter and a proper combination of the gate signals.

In this work, in order to define a simple strategy that can be implemented in all common electronic devices, a digital approach has been used where a digital logic function and corresponding digital circuit have been defined. In detail, the gate signals of the HB$_2$ module are the same as a traditional 7-level scheme. Instead, it is necessary to manipulate the gate signals of the HB$_1$ module to generate the voltage trend depicted in Fig.2 (red voltage trend).
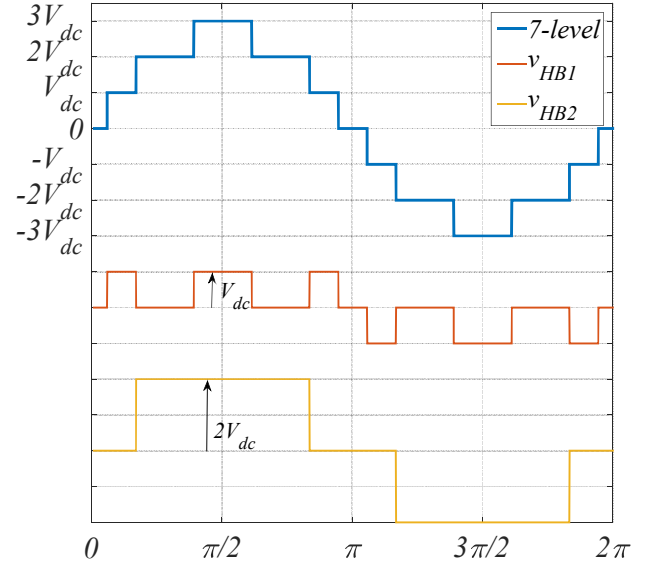

Fig. 2: Improved 7-level voltage waveform

By analysing the traditional 7-level voltage waveform and the desired voltage waveform of HB$_1$, illustrated in Fig. 2, the logic functions (2) can be obtained:

$$
\begin{aligned}
S_{11}^* &= \left(S_{11} \wedge S_{21} \wedge S_{31}\right) \vee \left(S_{11} \wedge \overline{S}_{21} \wedge \overline{S}_{31}\right) \\
S_{12}^* &= \left(S_{12} \wedge S_{22} \wedge S_{32}\right) \vee \left(S_{12} \wedge \overline{S}_{22} \wedge \overline{S}_{32}\right) \\
S_{13}^* &= \left(S_{13} \wedge S_{23} \wedge S_{33}\right) \vee \left(S_{13} \wedge \overline{S}_{23} \wedge \overline{S}_{33}\right) \\
S_{14}^* &= \left(S_{14} \wedge S_{24} \wedge S_{34}\right) \vee \left(S_{14} \wedge \overline{S}_{24} \wedge \overline{S}_{34}\right)
\end{aligned}
\qquad (2)
$$

where S_{1j}, $S_{2j,}$ and S_{3j} ($j=1...4$) are the gate signals of the traditional 7-level modulation scheme and S_{1j}^* are the improved gate signals of HB$_1$. For example, S_{11}^* is the gate signal of the high-side power components in HB$_1$ obtained by the digital combination of the traditional gate signals S_{11}, $S_{21,}$ and S_{31} obtained with a 7-level modulation scheme. Moreover, the improved gate signals S_{11}^* of the HB$_1$ module can be obtained by using the digital circuit shown in Fig. 3.
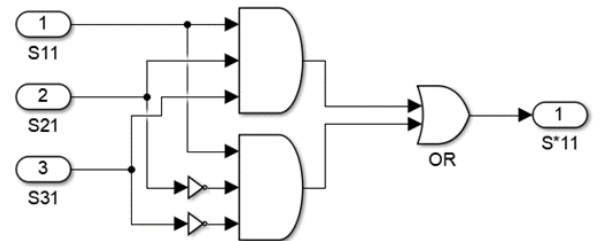

Fig. 3: Digital circuit to generate improved gate signals.

It should be noted that this digital approach allows a simple implementation in common electronic devices for power converters control (microcontrollers and FPGA). Moreover, the impact on computational costs of this approach is negligible with respect to the computational costs to evaluate the control angles.

III. DEAD-TIME IMPACT

The introduction of a dead time, between the gate signals of the same leg of each HB module, is necessary to avoid a short circuit and consequently module fault. The value of the minimum dead time depends on the power component adopted and, generally, the values are from 500ns to 2μs for traditional Mosfet and IGBT.

There are several strategies in literature to generate the dead time and some study investigates the impact of the dead time in terms of THD and conversion efficiency, as in [13] and [14]. Anyhow, a simple method to obtain a quarter-wave symmetry in the voltage waveform is shown in Fig. 4.
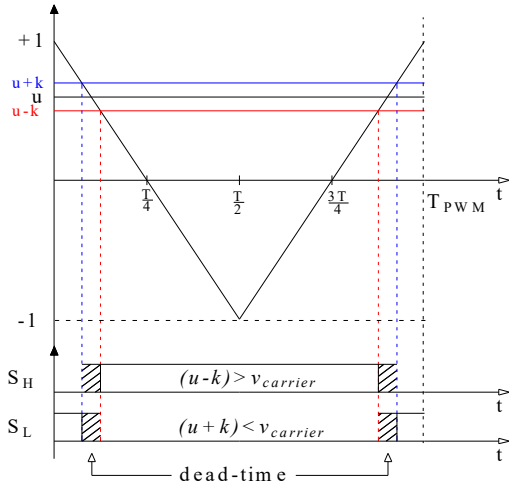

Fig. 4: Dead-time generation scheme.

As shown in Fig.4, the dead-time between high-side and low-side gate signals S_H and S_L is introduced by considering a k constant that must be added to the sample of modulation signal u. The constant k is proportional to the dead time desired and can be expressed as:

$$k = 2 \cdot dt \cdot f_{carrier} \quad (3)$$

where dt is the desired dead time and $f_{carrier}$ is the frequency of the reference triangle waveform. It should be noted that in this way k is an input variable of the modulation scheme adopted. It is clear that the minimum value of the dead time is a constraint on the k value. Thus, by using the dead-time method shown in Fig.4, the resulting gate signals for an asymmetric CHB are illustrated in Fig 5.

As depicted in Fig.5, the gate signals show the presence of the dead time and confirm quart-wave symmetry. Therefore, by taking into account the mathematical model of the output voltage of a 5-level CHB inverter, expressed in (4), Fig. 6 shows half cycle output converter voltage and corresponding voltage waveforms of the H-Bridge modules. As shown in Fig.6, the introduction of the dead time in the gate signals generates some voltage dips in the output voltage. Moreover, the time width of each voltage dip is equal to the value of the dead time.

$$
\begin{aligned}
v(t) &= v_{HB1} + v_{HB2} \\
v_{HB1} &= V_{dc}\left(S_{11}^* - S_{12}^*\right) \\
v_{HB2} &= 2V_{dc}\left(S_{21} - S_{22}\right)
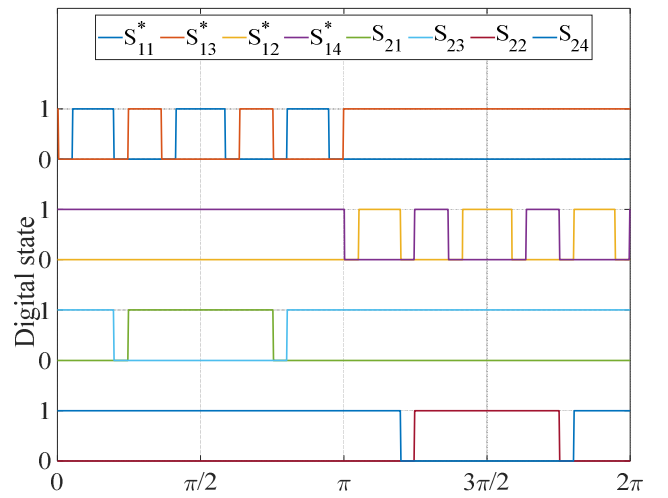\end{aligned}
\quad (4)
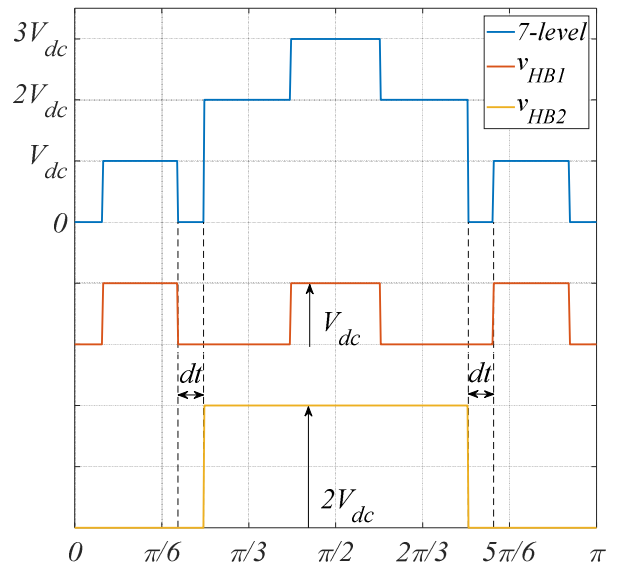$$

Fig. 5: Gate signals with dead time.

Fig. 6: A half cycle of the output converter voltage and corresponding output voltages of the H-Bridge modules.

$$v(t) = \sum_{h=1}^{N} \left[V_h \cdot \sin\left(h\omega t \right) \right]$$

$$V_h = \frac{4V_{dc}}{h\pi} \cdot \left\{ \cos\left[h\left(\frac{dt}{2} + \alpha \right) \right] + \cos\left[h\left(\frac{dt}{2} + \beta \right) \right] + \cos\left[h\left(\frac{dt}{2} + \gamma \right) \right] - 2\sin\left(h\frac{dt}{2} \right) \cdot \sin\left(h\beta \right) \right\} \tag{5}$$

Therefore, this phenomenon cannot be eliminated due to the necessary presence of dead time. From the distortion point of view, these voltage dips generate a different harmonic content in the output voltage with respect to the traditional 7-level voltage. Anyhow, it is possible to manipulate the time width of the voltage dips through the properly chosen dead time. In this way, the voltage harmonics can be controlled by using the traditional control angles and the dead time that can be used as a fourth variable. In the next section, the mathematical formulation and the impact of dead time are discussed.

IV. MATHEMATICAL FORMULATION

As previously described, the proposed method allows the generation of a symmetric 7-level voltage waveform maintaining a 5-level CHB topology structure. Nevertheless, by introducing the dead time in the gate signals has been demonstrated the presence of some voltage dips whit respect to the traditional 7-level voltage. In this section, the Fourier expansion of the voltage waveform is reported and the impact on the control angles constraint is discussed.

Fig. 5 shows a half-cycle of the obtained voltage waveform where α, β, and γ are the control angles to generate a traditional 7-level voltage waveform.
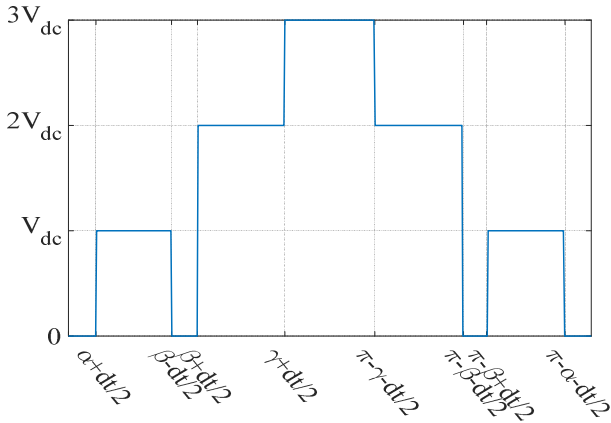

Fig. 7: A half cycle of the output converter voltage.

By applying the Fourier series expansion on the voltage waveform depicted in Fig. 7, the voltage $v(t)$ and the voltage harmonic amplitude V_h of h order are expressed in (5).

As expected, the dead time (dt) appears in the Fourier expansion in (5), valid only for odd values of h, in which it is clear that dt influences the voltage harmonics

amplitude V_h. Moreover, by eliminating the dt ($dt=0$) in (5), it is possible to demonstrate that the classical Fourier formulation for the 7-level staircase voltage waveform can be obtained.

Regarding the control angles constraints, the necessary constraints to obtain a 7-level voltage waveform are reported in (6). Moreover, to maintain the voltage level with amplitude V_{dc}, it is necessary to impose a further constraint expressed in (7).

By analysing the voltage harmonic amplitude in (5), it is evident the presence of four variables: α, β, γ, and dt. Thus, the expression (5) can be used to eliminate three harmonics or mitigate several harmonics.

$$\left(\frac{dt}{2} + \alpha \right) < \left(\frac{dt}{2} + \beta \right) < \left(\frac{dt}{2} + \gamma \right) < \frac{\pi}{2} \tag{6}$$

$$dt < (\beta - \alpha) \tag{7}$$

In the next section, simulation analysis of the proposed voltage waveform for different case studies has been presented where the performance has been compared with traditional 7-level voltage waveform.

V. SIMULATION ANALYSIS

This section deals with simulation analysis carried out in Matlab environment. In detail, this analysis is focused on the characterization of the improved 7-level voltage and the results have been compared with the converter performance obtained with a traditional 7-level CHB inverter. Therefore, the advantages and drawbacks of this approach are discussed. In order to investigate the performance of the proposed method, in terms of voltage harmonic distortion, several simulations analyses for different case studies have been carried out. The analysis has been conducted by using an especially designed search algorithm that allows to eliminate or mitigate, under a defined threshold, some harmonics. In detail, the search algorithm works by considering the control angles constraints and modulation index as input variables and allows obtaining the control angles and dt as output variables.

As a comparison tool, the Total Harmonic Distortion (THD) index has been used and evaluated as:

$$THD\% = \sqrt{\frac{\sum_{h=3}^{N} V_h^2}{V_1^2}} \cdot 100 \tag{8}$$

where V_h is the voltage harmonic of h order, V_1 is the first voltage harmonic and N is the number of considered harmonics that in this case is equal to 100. The values of the THD% have been evaluated for different working points of the modulation index (m) that is formulated as in (9).

In detail, in the expression (9) V_1 is the peak amplitude value of the first harmonic. Thus, the modulation index equal to 1 corresponds to a fundamental amplitude of the voltage square waveform with amplitude equal to $3Vdc$ that can be obtained by fixing the control angles α, β and γ equal to zero.

$$m = \frac{\pi \hat{V}_1}{12 V_{dc}} \qquad (9)$$

In the first case study, the performance of the traditional 7-level voltage and the proposed method has been compared by choosing three constant values of the dead time: 0.5 µs, 1 µs, and 2 µs. Thus, the search algorithm has been set to eliminate the first two harmonics: 3rd and 5th.

Figure 8 shows the comparison of THD% values vs. the modulation index obtained in the first case study. In detail, the blue curve represents the THD% values obtained with the traditional 7-level voltage waveform while red, yellow, and purple curves represent the THD% values obtained with the proposed method where the dead time is fixed equal to 0.5 µs, 1 µs and 2 µs, respectively.
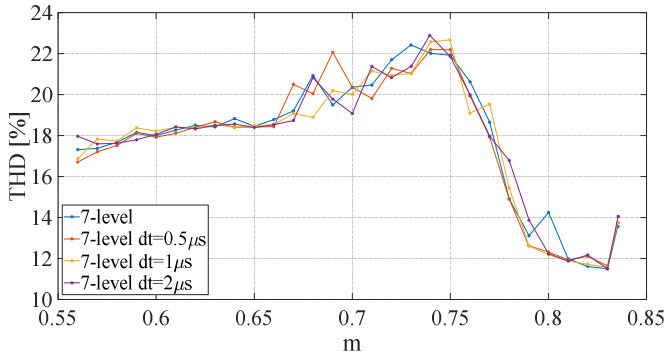

Fig. 8: Comparison of THD% trend vs. m between the 7-level and the proposed method.

It is interesting to note that similar values of THD% have been obtained in the range of modulation index considered. Thus, this result confirms that the asymmetrical structure of CHB and the proposed digital approach can generate a 7-level voltage waveform obtaining similar performance, in terms of the harmonic distortion, for different values of the dead time.

By observing the comparison of the harmonic spectra shown in Fig. 9 for m=0.82, it is evident that the 3rd and 5th harmonics are negligible in all cases as expected. Moreover, it is interesting to note that in the case where

the dead time is equal to 0.5µs (red bars) also the harmonic multiples of the 3rd and 5th results are mitigated.

In the second case study, by using the dead time as the fourth variable, the search algorithm has been set to eliminate three harmonics: 3rd, 5th, and 7th. Nevertheless, the search algorithm has found solutions around two working points of the modulation index equal to 0.6 and 0.8 where the selected harmonics are eliminated. Indeed, Fig.10 and 11 show the harmonic spectra relatively at modulation index values equal to 0.6 and 0.8, respectively.
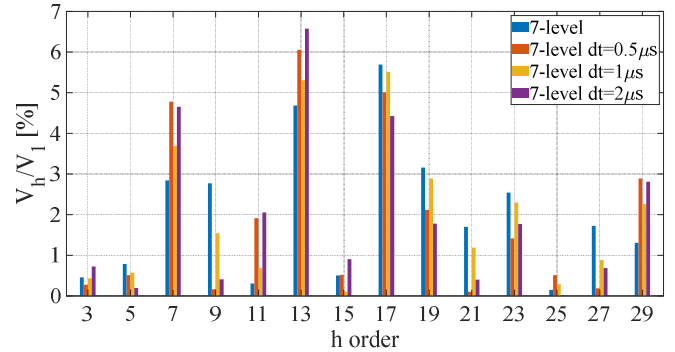

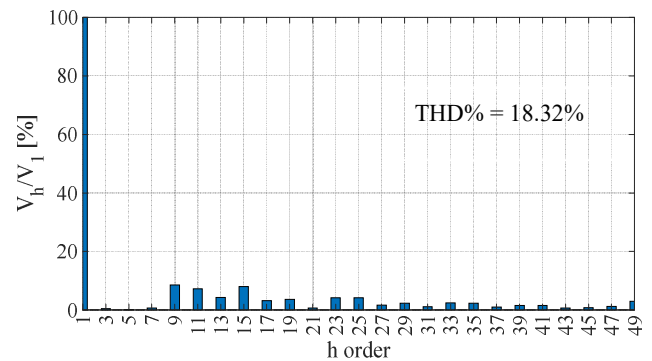Fig. 9: Harmonic spectra comparison between traditional 7-level voltage and proposed method for m=0.82.
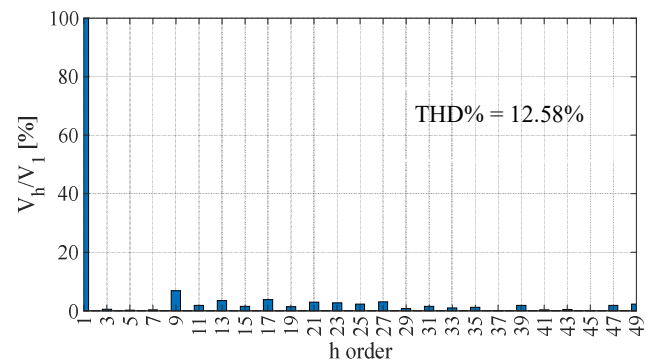

Fig. 10: Harmonic spectra for m=0.6.

Fig. 11: Harmonic spectra for m=0.8.

As shown in Fig. 10 and 11, the first three harmonics (3rd, 5th, and 7th) have been eliminated. In TABLE I, the control angles and dead time for m equal to 0.6 and 0.8 are reported. In detail, the dead time is expressed also in

microseconds considering a fundamental frequency equal to 50 Hz.

TABLE 1: CONTROL ANGLES AND DEAD TIME VALUES FOR THE CASE ILLUSTRATED IN FIG. 9 AND 10.

Modulation index	Control angles [rad]			Dead Time	
m	α	β	γ	dt [rad]	dt [μs]
0.6	0.1985	0.7023	1.4844	0.0102	32.50
0.8	0.1932	0.4483	0.9684	0.00778	24.79

In the third case study, the performance of the proposed voltage waveform, in terms of THD%, has been tested by using the selective harmonic mitigation (SHM) strategy. In detail, the search algorithm has been set to mitigate the first three harmonics (3rd, 5th, and 7th) and the first four harmonics (3rd, 5th, 7th and 9th). Moreover, the results have been compared with the THD% values of a traditional 7-level voltage waveform where the 3rd and 5th harmonics were eliminated. The comparison of THD% values vs. modulation index is shown in Fig. 12.
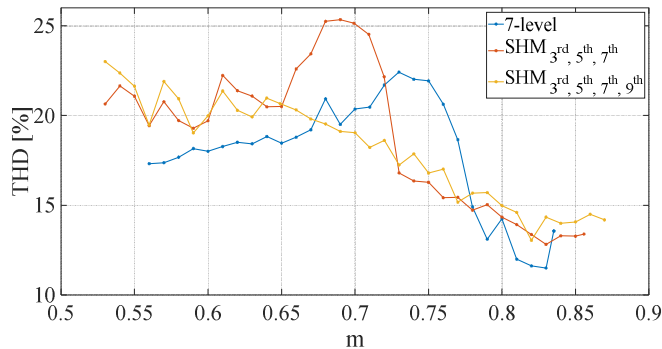

Fig. 12: Comparison of THD% values vs. m of the third case study.

As shown in Fig.12, the SHM strategy, where the first four harmonics (3rd, 5th, 7th and 9th) are considered, allows obtaining the lower values of THD% in the range of the modulation index from 0.67 to 0.78. Instead, for lower values of the modulation index up to 0.66, the lower values of the THD% have been obtained with a traditional 7-level voltage waveform. For modulation index values from 0.78 to 0.85 the THD% values are similar among the case considered.

VI. CONCLUSION

This work aims to propose a digital approach to generate a 7-level voltage waveform from an asymmetrical 5-level CHB inverter. In the first part of this work, the digital approach and corresponding digital function to combinate traditional gate signals have been presented and discussed. Subsequently, the impact of the introduction of the dead time, between two gate signals of the same H-Bridge leg, has been studied highlighting the presence of some voltage dips in the voltage waveform. Through the Fourier expansion analysis, the influence of the dead time on the voltage harmonics has

been demonstrated confirming the possibility of the use of the dead time as the fourth variable to eliminate or mitigate some harmonics in the voltage waveform. In this context, simulation analysis was focused on the characterization of the improved 7-level voltage and results have been compared with traditional 7-level voltage. From simulation analysis, emerged that the proposed method allows for obtaining similar results to the traditional 7-level voltage waveform (first case study). Subsequently, it has been demonstrated that the proposed method allows the elimination of three harmonics, by using the dead time as the fourth variable, only around two working points of the modulation index (second case study). Finally, by using an SHM strategy on the first three and first four harmonics interesting results have been obtained in terms of THD%.

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