Partial Discharge Behaviour Evaluation on MOSFET Employed in Automotive Applications

G. Akbar[1], A. Imburgia[1], G. Rizzo[2], Alessio Di Fatta[1], Sinda Kaziz[3,4], P. Romano[1], G. Ala[1], F. Viola[1]

[1]L.E.PR.E. HV Laboratory, Dipartimento di Ingegneria – University of Palermo, Palermo, Italy
[2]Prysmian Electronics, Palermo, Italy
[3]SI2E Laboratory, École nationale d'ingénieurs de Sfax, Université de Sfax, Tunisia;
[4]Faculté des sciences de Monastir, Université de Monastir, Tunisia;

Abstract- **This paper is focused on the measurement of partial discharges in the Silicon Carbide MOSFET. The latter represents a recent developed power electronics device, which has improved characteristics compared to the traditional Silicon MOSFET. The new technology has been conceived in order to satisfy the new market needs. With the ever-increasing development of the electric mobility sector, the need for ever more performing electronic power devices grows. The main features provided by the Silicon Carbide device were found in literature and concern a great thermal conductivity, wide bandgap, high power and high working temperature. However, considering the high voltage at which these devices work, also taking into account their small geometric dimensions, it is essential to evaluate the behavior from the partial discharges point of view. Based on the above, the aim of the present work is the measurement of partial discharges in ten different Silicon Carbide MOSFET devices in order to evaluate the electrical performances of the new proposed material as well as the quality of their manufacturing process. Experimental tests have been carried out by taking into account the Standard CEI EN 60270 for the realization of the measurement setup and the Standard CEI EN 61287 for the measurement procedure. In particular, the latter Standard provides the guidelines for the applied voltage waveform. Measurement results showed that no partial discharge phenomena occur in all the specimens under tests. Therefore, the SiC MOSFET passed the partial discharge test successfully.**

Keyword: MOSFET, partial discharge, automotive, power electronics, SiC.

I. Introduction

In recent decades, researchers from all over the world are engaged to reduce the global warming and pollution. For these aims, the transition from combustion engines to electric mobility constitutes one of the main actions [1-2]. With reference to the electric mobility, electrical and electronical engineers are engaged in the improvement of power electronic devices employed in the electric vehicles [3-6]. In particular, the MOSFETs, typically used in power converters [7], are the electronic devices investigated in this paper.

Recently, new efficient power devices realized with new materials and a new manufacturing process are leading to the replacement of the traditional Silicon (Si) power devices with the Silicon Carbide (SiC) ones [8-9].

The main features of this new generation of MOSFET concern a great thermal conductivity and wide bandgap, which in turn allow to reach high power and operate at high temperature.

Further advantages provided by the SiC MOSFETs can be summarized in very high operating junction temperature capability, a low on-state resistance, an extremely low gate charge and input capacitance and a limited size [10].

On the other hand, the cost of the SiC device compared to the traditional Si, is greater [11].

An investigation on SiC switching devices and a comparison with the conventional Si device was carried out in [12].

In [9] the evaluation was made in terms of power losses between the SiC and the Si, and it was found that at high frequencies they are lower in the SiC device.

In the present work, instead, the study has been made from the Partial Discharge (PD) behavior point of view.

Performances and duration of the new generation of high voltage power electronic components are dependent of the dielectric materials aiming to insulate their internal terminals. Therefore, the presence of defects, which may be due to faults appearing during the manufacturing process, but also to the internal design of layers and connections, can cause local enhancements of electric field. Consequently, possible appearance of PD phenomena or other effects (aging, tracking) that may result in reduction of device reliability. However, the purpose of the present work is the reliability evaluation of the new manufactured MOSFET devices, carried out by means of PD test.

The components under test have been subjected to their rated voltage with waveform and duration suggested by the standard CEI EN 61287.

The PD are acquired by means of the PryCam Grids instrument and elaborated by the PD Solver Software [13-14].

The paper is structured as follow. In the first part the measurement setup realized by follow the scheme proposed by the standard CEI EN 60270, is reported and analyzed. The specimen under test and its connection on the high voltage electrode of the measurement setup are also shown. In section III, the applied voltage waveform suggested by standard IEC 61287 (which provides the guidelines for measurements on static power converters such as inverters or rectifiers, and therefore also on components that are part of them, such as MOSFETs) is reported and described for the case study. The

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measurement results regarding the acquired PD patterns for the SiC MOSFETs under test are displayed and discussed in Section IV. While, in the final part, the related conclusions and the possible future development of the work are described.

II. Measurement Setup and Specimen Under Test

The PD behavior in the MOSFET devices has been measured by means of the test setup reported in Figure 1. In which the stress waveform proposed by the standards IEC 61287 has been realized by means of the Hipotronix generator. The arranged measurement setup has been realized in accordance to the electrical circuit suggested by the standard CEI EN 60270, that is reported in Figure 2. The setup is composed by the Hipotronix generator (*U* in Figure 2), the high voltage electrical connections realized with coppers pipes, the coupling capacitor C_k in series with the input impedance of the measuring system Z_{mi}, the PryCam Grids for the PD detection (*MI* in Figure 2) and the specimen under test represented by the MOSFET (C_a in Figure 2).
The others components present in the equivalent electrical circuit of Figure 2 but not highlighted in Figure 1 are the filter *Z*, the coupling device *CD* and the connecting cable *CC*.
For the measurement and elaboration of the PD signals, the PryCam Grids instrument and the PD Solver software have been used, respectively.

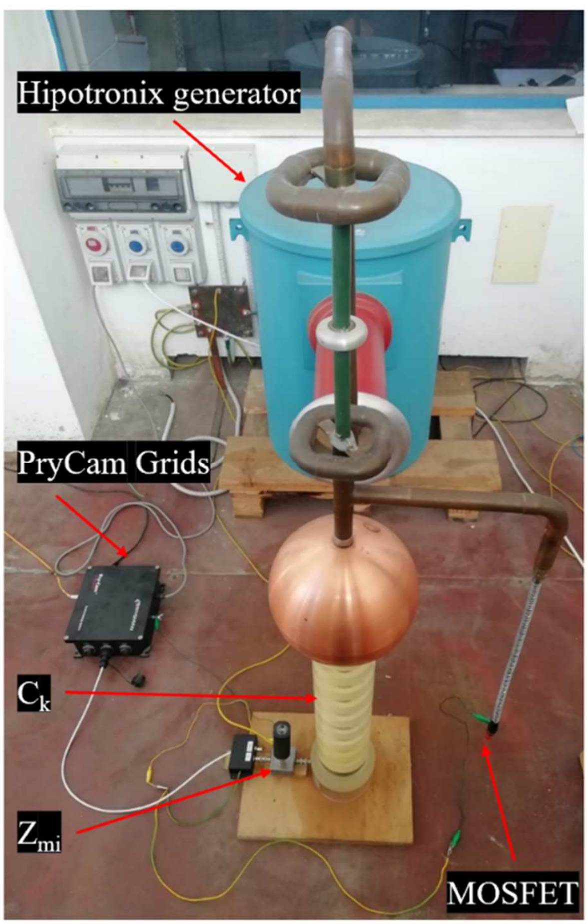

Fig. 1. PD Measurement setup.

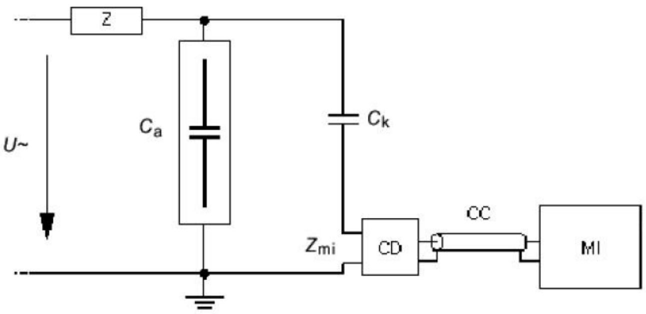

Fig. 2. Equivalent electrical circuit of the PD measurement setup proposed by the standard CEI EN 60270.

In Figure 3, the MOSFET under test (Figure 3a) and its connection into the partial discharge measurement setup (Figure 3b), are reported.
Further information regarding the specimens under test are given below.
The SiC Power MOSFET device has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature. This Surface Mounting Device (SMD) presents 7 pins and one tab: the gate pin is pin 1, the driver source pin is pin 2, the power source pins are 3,4,5,6,7, whereas the drain terminal is the tab.
As can be seen in Figure 3b, the pins of the specimen under test are short-circuited in order to apply the high voltage between them and the metallic screen connected to the ground by means of the green cable. In this way the entire dielectric material of the MOSFET is subjected to the high voltage and therefore the PD events can be measured.

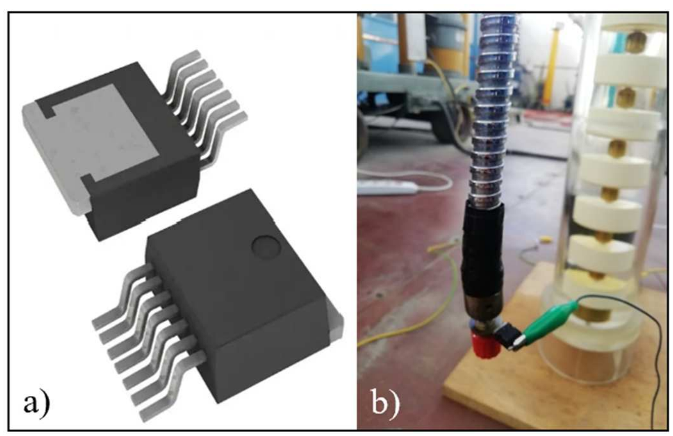

Fig. 3. Focusing on the specimen under test. 3a) the SiC MOSFET and 3b) its connection between high voltage and ground for the partial discharge measurement.

III. The Applied Voltage Waveform

In Figure 4, the trend of the 50 Hz sinusoidal voltage waveform applied to the specimens under test for the PD tests, proposed by the Standard CEI EN 60128, is reported. The sinusoidal voltage magnitude starts from 0 V and reaches the value equal to $1.5\ Um/\sqrt{2}$, after 10 s. In the latter equation Um is the MOSFET rated voltage, which for our specimens under test is 1200 V. After 10 s, the applied voltage magnitude remains constant for a time t_1 equal to 60 s. Subsequently, within 10 s, the voltage magnitude is reduced at $1.1\ Um/\sqrt{2}$. This last value is kept constant for a time t_2 equal to 30 s. In correspondence of the last 5 s of the time interval t_2, therefore from 25 to 30 s of $1.1\ Um/\sqrt{2}$ applied voltage, the measurement of PD is carried out. After that, the PD test ends by reducing the voltage magnitude at 0 V within 10 s.

In other words, the voltage stress is applied for a total time equal to 2 minutes. Starting from 0 V, the voltage magnitude increases and reaches 1273 V after 10 s. This voltage value is kept constant for 1 minute and after is reduced to 934 V. At this voltage level, which is applied for 30 s (t_2), the PD are monitored. However, as suggested by the reference Standard, only the PD observed in the last 5 s of the time interval t2 need to be considered.

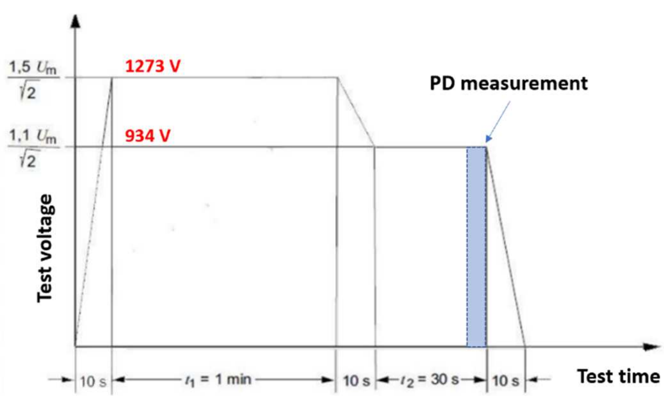

Fig. 4. Applied voltage waveform to the specimens under test. Trend of the 50 Hz voltage waveform suggested by the standard CEI EN 60128

IV. Measurement Results

After arranging the measurement setup and proceeding with the system calibration process, a set of PD measurements have been carried out in ten SiC MOSFET.

By applying the voltage stress of Figure 4 at the first specimen under test, no PD events have been detected, as can be seen in the very clear Phase Resolved PD (PRPD) pattern reported in Figure 5. For all ten specimens the same PRPD pattern has been obtained. Therefore, it is possible to confirm that the SiC MOSFET passed the PD test successfully.

In addition to the previous test, with measurements result shown in Figure 5, another test regarding the evaluation of the PD Inception Voltage (PDIV) has been carried out. This is useful for establishing the maximum voltage magnitude that can be applied to the SiC MOSFET without triggering PD phenomena.

For this test the sinusoidal voltage has been applied gradually increasing, without following the trend of Figure 4. Measurement result shows that at a voltage magnitude equal to 1500 V PD occurs and the related PRPD pattern is reported in Figure 6. Based on the pattern shape it is possible to confirm that only corona discharges are present. This type of discharge does not represent internal defect of the device, but they are emitted from the pins of SiC MOSFET.

To avoid this type of discharge, the connection between the high voltage and the SiC MOSFET pins should be improved. Therefore, we tried different possible solutions, such as the welding of all the pins in order to create a single rounded pin, and the immersion of the SiC MOSFET in a container of silicon oil. Both attempts were unsatisfactory as corona discharges continued to persist.

Also for this type of test, the obtained PRPD patterns for the 10 different MOSFET specimens were very similar to each other. The only difference concerns the ignition voltage magnitude of corona discharge. However, the detected ignition voltage level in the ten specimens was in the range between 1450 V and 1550 V.

Fig. 5. PRPD pattern obtained by stressing the SiC MOSFET with the voltage waveform suggested by standard CEI EN 60128.

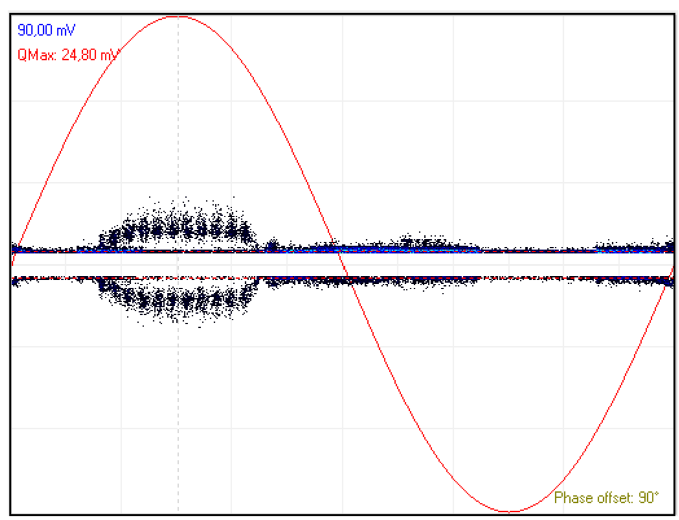

Fig. 6. Evaluation of the PDIV. PRPD pattern obtained by stressing the SiC MOSFET with a voltage magnitude equal to 1500 V.

V. Conclusions

The aim of the proposed work was to analyze the PD behavior on the new developed SiC technology employed in MOSFET devices. The proposed SiC MOSFET, thanks to its improved features compared to the traditional Si device, lends itself to being widely used in the near future. The main advantages provided by the SiC technology have been found in literature and summarized in this paper. However, the contribution of the authors on the validation of this new device concerns the evaluation of the PD behavior, this in order to provide useful information regarding the quality of the insulation among the internal terminals as well as the quality of the manufacturing process.

For these aims a PD measurement setup has been realized by following the Standard CEI EN 60270. While, for the measurement procedure, the Standard CEI EN 60128 has been taken into account. The latter proposes the trend of the 50 Hz voltage waveform that must be applied to the component under test for the PD measurements. In the carried out tests, with measurement results reported in this paper, the stress voltage waveform has been realized and applied by means of an high voltage generator manually controlled. Measurements results, carried out in 10 different SiC MOSFETs, showed the same PD behavior. Therefore, the same PRPD pattern has been obtained for all components and for this reason only one pattern regarding the PD detection has been reported. As it was possible to notice, no discharge has been detected during the application of the stress voltage. This confirms the good quality of the new SiC technology.

After that, with the aim to evaluate the voltage level that generates the ignition of PD, the voltage magnitude has been gradually increased. It was found that at an average value of 1500 V PD events occur. However, the observed PRPD pattern as well as the detected PD pulse confirms the presence of only corona discharges.

In order to avoid the triggering of corona discharge different possible solutions have been tried, such as the welding of all the pins in order to create a single rounded pin, but also the immersion of the specimen in a container of silicon oil. Both attempts were unsatisfactory as corona discharges continued to persist.

With the aim to overcome the issue related to the presence of corona discharge, which does not allow to easily evaluate the presence of other PD types, in future developments of this work further improvements of the measurement setup and of the connection between the MOSFET and the high voltage electrode will be made.

Moreover, future works will be also focused on the PD measurements in the SiC MOSFETs stressed with waveforms of square type with different frequencies and rise times, as well as stressed with the Pulse Width Modulation (PWM) waveforms.

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