



Article A Quasi-Z-Source-Based Inductive Power Transfer System for Constant Current/Constant Voltage Charging Applications

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Abstract: This article proposes a quasi-Z-source (qZS)-based Inductive Power Transfer (IPT) system for Electric Vehicles (EVs) charging applications. The IPT systems use the magnetic field to transfer power between two coils wirelessly, achieving improved reliability, safety and less environmental impact. Compared to the conventional IPT system, the proposed qZS-IPT system simultaneously achieves DC/DC regulation and DC/AC conversion through a single-stage conversion, thus lowering the cost and complexity of the system. Moreover, the reliability of the system is improved thanks to the qZS network shoot-though immunity and the reduced number of switches. To ensure the battery efficient charging and long service life, the constant current/constant voltage (CC/CV) method is considered. With the proposed innovative modulation scheme, the qZS can easily change between buck and boost modes, respectively, lowering or increasing the secondary side current. A theoretical analysis is presented for system design. Simulation results based on a 25 kW (200 V/135 A) low duty EV charger are presented to verify the effectiveness of the proposed scheme. Experimental tests are performed on a 150 W scale-down prototype to validate the analysis and demonstrate the effectiveness of the proposed qZS-IPT system for CC/CV chargers.

Keywords: battery charging; constant current/constant voltage (CC/CV) charging; Inductive Power Transfer (IPT); quasi-Z-Source (qZS)

1. Introduction

The growing need to reduce polluting emissions leads, in our days, to the rapid spread of Electric Vehicles (EVs) [1]. Thanks to high-performance electric motors and the use of "clean" energy sources for recharging EVs, the contribution of polluting gases caused by transportation could be drastically reduced. One of the most discussed topics in this area is the EVs charging mode [2–5]. Two different connection methods have been proposed for recharging the EVs: the classic one, which provides a cable connection (conductive or wired charging) [6], and the innovative one involving wireless power transmission (wireless charging) [7]. Wireless Power Transfer (WPT) systems use the electric field (Capacitive Power Transfer, CPT) [8–10] or magnetic field (Inductive Power Transfer, IPT) [11–13] to transfer power from a primary side to a secondary side. By removing the connection cable between the charging station and EV, the electrocution hazard is eliminated, the risk of short circuits and sparks is reduced, contact resistors are eliminated and the possibility of contact failures or breakage is then eliminated. Moreover, WPT systems are also unaffected by dirt, dust, and water. Thus, compared to wired systems, improved reliability, safety and less environmental impact are achieved [14].

The IPT systems have been preferred over CPT systems and have been developed and commercialized rapidly [15,16]. The general architecture of an IPT system for EV charging applications is shown in Figure 1 [17,18]. It consists of two sides, respectively, the transmitter side located in the charging station and the receiving side located in the vehicle.



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). The charging station can be supplied by the grid, as shown in Figure 1, or by a DC power source such as Photovoltaic (PV) or Fuel Cells (FC). In a typical IPT system, the input voltage is usually regulated by a boost DC/DC converter. To increase the coupling between the two coils, the DC/AC in the primary side and the AC/DC converter in the secondary side must work at high frequencies, in the order of hundreds of kHz. On the other hand, to keep the system efficient, switching losses limit the operating frequencies [19].



Figure 1. IPT system architecture for EV charging applications.

In order to overcome this problem, a second possible configuration has been proposed using Impedance Source (Z-Source) converters [20–27]. The main advantage of using these converters is the single-stage DC/AC conversion with a smaller number of switches [28]. In fact, it is possible to obtain the DC voltage boost and AC conversion simultaneously [29,30]. Moreover, the input impedance network (Z-network) ensures short circuit protection.

Another key element in IPT systems is the battery charging method [31,32]. Lithiumion (Li-ion) batteries are currently the most widely used in EV storage systems due to their high energy density [33,34]. The best Li-ion batteries charging method, which ensures efficient charging and long service life, is the constant current-constant voltage (CC/CV) [14] method. Different solutions have been adopted for the CC/CV charge implementation [35]. In [36], two different control loop are used to achieve the CC mode and the CV mode, measuring the battery voltage and current and controlling only the primary side inverter. In [37], a load identification approach is used to avoid the battery voltage and current sensing and the data communication between the primary and secondary side. In [38], the CC and CV modes are implemented using a reconfigurable IPT system. In [39], a decoupled control method is proposed, which enhances the transient response and the overall system performance compared to the traditional closed-loop control. It should be noted that the articles reviewed so far are all preferred for the classic IPT configuration, while there are still few works that consider the implementation of the CC/CV charging mode on Z-source converters-based IPT systems.

In [22,26], a Z-source converter with integrated Power Factor Correction (PFC) and load regulation for sinusoidal charging of batteries is proposed. The main problem of the Z-source converter is the discontinuous input current, which is not very suitable for renewable energy sources like PV and FCs. To achieve a continuous input current, the quasi-Z-source (qZS) converter is used in [20,27]. In [20], the performance comparison of the qZS and Z-source converters is carried out. In [27], the sliding mode predictive control is applied to the qZS converter, but the charging process of batteries is not taken into account. In [21], the qZS converter is controlled in the CC/CV mode to recharge the batteries, using two separated control schemes and a buck converter in the receiver side.

With the above, the main motivation of this article is to investigate impedance source converters in IPT systems for CC/CV charging of EV batteries. Among the different Z-source converter topologies, the qZS was chosen because of the continuous input current feature. The detailed schematic of the proposed qZS based inductive power transfer system (qZS- IPT) is shown in Figure 2. In contrast to the one proposed in [20,21,27], the Z-network diode is replaced by a switch to ensure the Continuous Conduction Mode (CCM) operation. The inductive coupling is realized by means of the series-series (SS) topology, which features a load independent characteristic during the CC mode. To achieve the CC/CV charging method, the control acts on the primary side qZS converter and with a proper modulation scheme, the converter can increase (boost mode) or decrease (buck mode) the voltage on the primary side. To summarize, the main contributions of this paper, compared to what is found in the literature, are underlined in the following:

- Unlike [21], the receiver side buck converter is removed to keep the design as simple as possible;
- Use of a single control scheme for the implementation of CC/CV phases, achieving a smooth transition between the two modes;
- Implementation of an innovative modulation scheme that allows the qZS converter to easily change between boost and buck modes.

This article has been divided into five sections. Section 2 describes the operating principle of the system and the basic theoretical analysis. Section 3 presents the CC/CV charge implementation. Section 4 describes the system operation with simulations in PLECS. A small-scale prototype is presented in Section 5 and the acquired waveforms and recorded CC/CV charging curves are provided, validating the proposed system with experimental results.



Figure 2. Circuit schematic of the qZS-based IPT system.

2. System Analysis and Modeling

The qZS converter has different states based on which switch is turned ON or OFF. In addition to the Active State (AS) and Zero State (ZS), normally used in traditional inverters, the Shoot-Through (ST) state is introduced. All the possible configurations of the converter are shown in Figure 3 and are described below.



Figure 3. Cont.



Figure 3. Circuit schematic of the qZS-IPT system in different states. (a) Active state S_1 , S_4 . (b) Active state S_2 , S_3 . (c) Zero state S_1 , S_2 . (d) Zero state S_3 , S_4 . (e) Shoot-through state.

- 1. Active State: During the AS, the diagonal switches (S_1 and S_4 or S_2 and S_3) are ON and the switch S_5 is ON (see Figure 3a,b). The capacitors C_1 and C_2 are connected in series through S_5 and supply current to the load along with the DC source.
- 2. Zero State: During the ZS, the upper (S_1 and S_2) or lower (S_3 and S_4) switches are ON and the switch S_5 is ON (see Figure 3c,d). The transmitter current is freewheeling, the Z-network inductors and the source charge the Z-network capacitors.
- 3. Shoot-Through State: During the ST state, the switches S_1 to S_4 are ON and S_5 is OFF (see Figure 3e). The inductors are charged both by the DC source and the Z-network capacitors. Thanks to this ST state, the Z-network output voltage is boosted. Using the voltage-second balance across one of the Z-network inductors, the DC-link peak voltage can be obtained as:

$$\hat{v}_{DC} = \frac{1}{1 - 2D} V_{in} \tag{1}$$

where *D* is the duty cycle.

Combining the previous three states, different operating modes can be achieved. In particular, the system can operate both in boost mode, increasing the DC-link voltage with respect to the input voltage, in buck mode, decreasing the AC output voltage or in buck-boost mode.

2.1. Buck Mode

In buck mode operation, only the AS and ZS are used.

The first harmonic of the inverter output voltage, denoted with $v_{p,1}$, can be expressed as:

$$v_{p,1} = \frac{4V_{DC}}{\pi} \cos\left(\frac{\pi}{2}D\right) \sin\left(\omega_0 t\right).$$
⁽²⁾

The DC-link voltage V_{DC} during the buck mode operation is equal, neglecting the voltage drops across the Z-network components to:

L

$$V_{DC} \cong V_{in} \tag{3}$$

thus, the amplitude of the first harmonic is:

$$\hat{v}_{p,1} = \frac{4V_{in}}{\pi} \cos\left(\frac{\pi}{2}D\right) \tag{4}$$

and it will be maximum when the duty cycle is 0 and minimum when the duty cycle is 1. The output current in this operation mode can be calculated as:

$$I_o = \frac{8}{\omega_0 M} \frac{V_{in}}{\pi^2} \cos\left(\frac{\pi}{2}D\right).$$
(5)

2.2. Boost Mode

In boost mode operation, only the AS and the ST state are used. The inverter output voltage first harmonic expression is the same in (2). However, thanks to the boosting action during the ST state, the DC-link peak voltage will be increased as reported in (1). Thus, the amplitude of the first harmonic during the boost mode can be calculated, replacing (1) in (2) as:

$$\hat{v}_{p,1} = \frac{4V_{in}}{\pi} \frac{1}{1-2D} \cos\left(\frac{\pi}{2}D\right)$$
 (6)

and it will be minimum for *D* equal to 0 and theoretically infinite for *D* equal to 0.5.

The output current in this operation mode can be calculated as

$$I_o = \frac{8V_{in}}{\omega_0 M \pi^2 (1 - 2D)} \cos\left(\frac{\pi}{2}D\right). \tag{7}$$

2.3. Buck-Boost Mode

In order to achieve a smooth transition between buck and boost mode and to use a single modulator for both operation modes, a new control logic was implemented. In particular, the duty cycle has been allowed to vary not between 0 and 1 for the buck mode and between 0 and 0.5 for the boost mode, as normally happens, but between -1 and 0 for buck mode and between 0 and 0.5 for boost mode. In this way, when the control circuit tries to decrease the current, the duty cycle may become negative by switching to buck operation. The control signals S_1 , S_2 and S_5 are generated in the same way for both operation modes. The S_3 and S_4 signals remain to be generated differently, so we introduce a variable *T* that indicates whether the duty cycle is greater (T = 0) or smaller (T = 1) than 0. Thus, the following relationship and truth Table 1 can be written:

$$S_{3} = \begin{cases} S_{2}, & D > 0 \to T = 0\\ \bar{S}_{1}, & D < 0 \to T = 1' \end{cases}$$
(8)

$$S_4 = \begin{cases} S_1, & D > 0 \to T = 0\\ S_2, & D < 0 \to T = 1 \end{cases}.$$
(9)

. .

Т S_1 S_3 Т S_1 S_2 S_2

Table 1. Thruth tables of S_3 control signal and S_4 control signal.

Considering all	the minterms in	the truth tables	s, the following	combinatorial	expres
sions are obtained			Ũ		
biolis die obtailied.					

$$\bar{T}\bar{S}_{1}S_{2} + \bar{T}S_{1}S_{2} + T\bar{S}_{1}S_{2} + T\bar{S}_{1}\bar{S}_{2} = \bar{T}\bar{S}_{1}S_{2} + \bar{T}S_{1}S_{2} + T\bar{S}_{1}S_{2} + T\bar{S}_{1}\bar{S}_{2} = \bar{S}_{1}S_{2} + \bar{T}S_{1}S_{2} + T\bar{S}_{1}\bar{S}_{2}$$
(10)

$$\bar{T}S_1S_2 + \bar{T}S_1\bar{S}_2 + T\bar{S}_1\bar{S}_2 + TS_1\bar{S}_2 = (\bar{T} + T)(S_1\bar{S}_2) + \bar{T}S_1\bar{S}_2 + T\bar{S}_1\bar{S}_2 = S_1\bar{S}_2 + \bar{T}S_1\bar{S}_2 + T\bar{S}_1\bar{S}_2$$
(11)

The combinational logic circuit associated to (10) and (11) is shown in Figure 4. This circuit is implemented in the FPGA-based control board to realize the PWM modulator.



Figure 4. Combinatorial logic circuit for the proposed modulator.

3. CC/CV Charging Implementation

In order to ensure fast and safe charging of the battery, the CC/CV charging method was considered. It consists of two phases: in the CC phase, the battery charging current is kept constant and equal to I_{max} until the battery voltage reaches its maximum allowable value V_{max} .

In the CV phase, the battery voltage is kept constant to V_{max} until the battery charge current reaches a minimum value I_{min} .

The CC/CV charge was implemented using a double-loop control scheme: the external loop, which controls the battery voltage V_o , and the internal loop which controls the battery current I_o . An interesting feature of the proposed control method is the possibility

 S_4



Figure 5. Closed–loop control scheme for CC/CV charging implementation.

The battery voltage V_o is measured and compared to the reference value V_o^* , set to the maximum allowable voltage for the battery. The error is sent to a Proportional-Integral (PI) controller to generate the reference charging current I_o^* , which is compared to the actual battery current I_o and processed by the second PI controller to generate the reference duty cycle D^* . To the first PI controller output, a saturation block is added. The upper limit of the saturation block is set to be equal to the maximum battery charging current, while the lower limit is set to 0.

To the second PI controller output, another saturation block is added to limit the duty cycle, with the upper saturation limit set to 0.4 and the lower saturation limit set to -1. In this way, when the battery voltage is low, the PI controller tries to increase the charging current, which will be saturated to the maximum permissible value by the battery. During the CC phase, the converter usually works in boost mode, with duty cycle in the range of 0 to 0.4. As the battery charges, the charging current will be kept constant until the maximum voltage is reached. At this point, the system automatically switches to the CV phase, during which the charging current is reduced to a minimum value. In this phase, the converter will switch to the buck mode when the duty cycle becomes negative in the range of 0 to -1. When the charging current reaches the minimum value, the charging process is completed.

4. Simulation Results

The proposed system was designed and simulated in PLECS. The simulation parameters are summarized in Table 2. The simulation is carried out to demonstrate the system behaviour during the CC-CV charge. Figure 6 shows the steady- state voltage and current waveforms during boost mode (a) and buck mode (b) operation of each stage of the proposed system. From top to bottom the input voltage V_{in} and current i_1 , the DC-link voltage v_{DC} and current i_{DC} , the primary side voltage v_p and current i_p , the secondary side voltage v_s and current i_s and the battery voltage V_o and current I_o are represented.

Figure 6a shows the waveforms during boost mode and CC phase. The battery charging current reference is set to 125 A (red dashed line), corresponding to a duty cycle of 0.18. During the shoot-though state, the DC-link current reaches almost 200 A, charging the Z-network inductors. It can be noticed that the DC-link voltage is boosted from 330 V to almost 500 V.

Figure 6b shows the waveforms during buck mode and CV phase. The battery maximum voltage reference is set to 225 V, corresponding to a duty cycle of -0.57. It can be noticed that the DC-link voltage in this case is practically constant and equal to the input voltage apart from voltage drops on components.

In CC phase, the closed-loop control maintains the battery charging current to 125 A while the battery voltage is increasing. As the battery voltage reaches the maximum value $V_{o,max} = 225$ V, the CV phase is activated. To maintain a constant voltage, the charging current is proportionally decreased until its value reaches the minimum battery charging current $I_{o,min} = 5$ A. Thanks to the improved control algorithm, no voltage and current transients are observed during the transition from CC to CV phase.



Figure 6. Steady-state voltage and current waveforms for (**a**) boost mode operation (D = 0.18) and (**b**) buck mode operation (D = -0.57).

Parameter	Unit	Symbol	Value
Output power	(kW)	Po	25
Input DC Voltage	(V)	V _{in}	330
Nominal Battery Voltage	(V)	V_o	200
Maximum Battery Voltage	(V)	V _{o,max}	225
Maximum Battery Current	(A)	I _{o,max}	125
Minimum Battery Current	(A)	I _{o,min}	5
Coil Inductance	(µH)	L_s, L_p	13.6
Compensation Capacitance	(nF)	C_s, C_p	286

Table 2. Cont.

Parameter	Unit	Symbol	Value
Coil ESR	(Ω)	r_p, r_s	0.1
Z-Network Inductance	(µH)	L_1, L_2	100
Z-network Capacitance	(mF)	C_s, C_p	1.5
Output Capacitance	(mF)	Co	2
Duty Cycle	(-)	D	-1 to 0.4
Switching Frequency	(kHz)	f_0	85

5. Experimental Results

Experimental tests have been performed on a scaled-down prototype to validate the simulation results and prove that the system achieves the CC-CV charge. The test-bench, shown in Figure 7, is composed of:

- A PED-board, used to acquire voltages and currents, implement the control algorithm and generate the control signals for the inverter;
- The proposed qZS-IPT system, whose parameters are summarized in Table 3;
- An Agilent 6672A DC Power Supply (0–20 V/0–100 A, 2 kW), used as the input source;
- An Agilent 6060B Single Input Electronic Load (3–60 V/0–60 A, 300 W), used as a load in voltage mode for open-loop tests;
- A lithium-ion battery, whose parameters are reported in Table 4, used for the CC-CV charging demonstration;
- A Lecroy WavePro 7200A oscilloscope with two differential voltage probe and two current probe.

Table 3. Laboratory Prototype Parameters.

Parameter	Unit	Symbol	Value
Output power	(W)	Po	250
Input DC voltage	(V)	V _{in}	20
Coil inductance	(µH)	L_s, L_p	13.6
Compensation capacitance	(nF)	C_s, C_p	286
Coil ESR	(Ω)	r_p, r_s	0.1
Z-Network inductance	(µH)	L_1, L_2	10
Z-network capacitance	(mF)	C_s, C_p	150
Output capacitance	(μF)	Co	200
Duty cycle	(-)	D	$-1 \div 0.4$
Switching frequency	(kHz)	f_0	85

Table 4. Battery Parameters.

Parameter	Unit	Symbol	Value
Nominal battery voltage	(V)	V_o	14.8
Maximum battery voltage	(V)	V _{o,max}	16.8
Maximum battery current	(A)	I _{o,max}	8
Minimum battery current	(A)	I _{o,min}	0.2
Maximum capacity	(Ah)	Q _{max}	6
Configuration	-	-	4S2P
Cell brand	-	-	LGHG2
Format	-	-	186520



Figure 7. Setup of the laboratory prototype for the proposed qZS-IPT system.

Figures 8–11 show the key waveforms of the proposed system in open-loop configuration with the electronic load, in voltage mode, set to 12 V. A critical aspect of the experimental realization of the laboratory prototype is the lack of a proper DC-link capacitor to suppress the sharp transients and possible overvoltage due to high di/dt. For this reason, in order to protect the power switches, a RC snubber circuit is used, in parallel to each inverter MOSFET.

Figures 8 and 9 show the waveforms obtained in boost mode, with D = 0.1 and D = 0.2, respectively. Figures 8a and 9a show the Z-network input and output voltage and current. The theoretical DC-link peak voltage can be calculated using (1), obtaining 25 V for D = 0.1 and 33 V for D = 0.2. The practical DC-link peak voltage was 22 V and 30 V, respectively, due to the component voltage drops. Figures 8b and 9b show the inverter output voltage and current and the rectifier input voltage and current. The theoretical secondary current is equal to 9.8 A for D = 0.1 and 12.6 A for D = 0.2. The practical secondary current amplitude was 9.2 A and 12 A. Figures 8c and 9c show the input and output voltage and current. The theoretical output current value can be calculated by using (7) to be 6.25 A for D = 0.1 and 8 A for D = 0.2. The measured value was 5.9 A and 7.6 A, respectively.

Figures 10 and 11 report the key waveforms of the system in buck mode operation obtained with D = -0.2 and D = -0.4, respectively. Figures 10a and 11a show the Z-network input and output voltage and current. As expected, the DC-link voltage in this case is constant and equal to the input voltage, hence 20 V. Figures 10b and 11b show the inverter output voltage and current and the rectifier input voltage and current. The theoretical secondary current amplitude is equal to 7.5 A for D = -0.2 and 6.4 A for D = -0.4. The practical secondary current amplitude was 7 A and 6 A. Figures 10c and 11c show the input and output voltage and current. The theoretical output current value can be calculated by using (4) to be 4.4 A for D = -0.2 and 3.77 A for D = -0.4. The measured value was 3.9 A and 3.2 A, respectively.

The experimental results are in accordance with the mathematical analysis carried out in Section 2, demonstrating the correct operation of the modulator by switching from boost operation, for positive duty cycle values, to buck operation, for negative duty cycle values. Moreover, the measured values of voltages and currents in the various stages of the system agree with the theoretical ones, demonstrating the correct operation of the prototype.

To demonstrate the CC/CV charge process for the proposed system, the control scheme shown in Figure 5 was implemented in the control board, using LabVIEW. The control board interfaces with a control PC, on which a graphic interface has been realized to control the various parameters of the system. The battery was first discharged to the minimum voltage $V_{o,min} = 12$ V and was then connected to the qZS-IPT system. The maximum current for the CC phase was set to $I_{o,max} = 8$ A, the maximum voltage for the CV phase was set to $V_{o,max} = 16.8$ V and the minimum current to stop the charging process was set to $I_{o,min} = 0.2$ A. Figure 12 shows the acquired battery voltage and current during the entire process and the estimated capacity using the Coulomb counting method. As predicted by the simulations, the system was able to perform CC/CV charging, without transients during the transition between the two phases.



Figure 8. Cont.



Figure 8. Experimental waveforms of the qZS-IPT system in boost mode with D = 0.1. (a) Input voltage V_{in} and current i_1 , DC-link voltage v_{dc} and current i_{dc} . (b) primary side voltage v_p and current i_p , secondary side voltage v_s and current i_s . (c) Input voltage V_{in} and current i_1 , output voltage V_o and current I_o .



Figure 9. Cont.



Figure 9. Experimental waveforms of the qZS-IPT system in boost mode with D = 0.2. (a) Input voltage V_{in} and current i_1 , DC-link voltage v_{dc} and current i_{dc} . (b) primary side voltage v_p and current i_p , secondary side voltage v_s and current i_s . (c) Input voltage V_{in} and current i_1 , output voltage V_o and current I_o .



Figure 10. Cont.



Figure 10. Experimental waveforms of the qZS-IPT system in buck mode with D = -0.2. (a) Input voltage V_{in} and current i_1 , DC-link voltage v_{dc} and current i_{dc} . (b) primary side voltage v_p and current i_p , secondary side voltage v_s and current i_s . (c) input voltage V_{in} and current i_1 , output voltage V_o and current I_o .



Figure 11. Cont.



Figure 11. Experimental waveforms of the qZS-IPT system in buck mode with D = -0.4. (a) Input voltage V_{in} and current i_1 , DC-link voltage v_{dc} and current i_{dc} . (b) Primary side voltage v_p and current i_p , secondary side voltage v_s and current i_s . (c) Input voltage V_{in} and current i_1 , output voltage V_o and current I_o .



Figure 12. Experimental battery voltage and current during a complete CC/CV charge cycle.

6. Conclusions

This article has presented a quasi-Z-source-based IPT system for EV battery charging applications. Thanks to the Z-network the qZS-IPT system is immune to short-circuiting and taking advantage of the shoot-through states the simultaneous DC voltage regulation and DC/AC conversion is possible. A new modulator has been proposed, capable of making the transition between buck and boost modes in a simple and effective way. Among the different charging methods, the CC/CV charge was chosen. Unlike many other papers that propose two separate control loops, one for the CC phase and one for the CV phase, a single double-loop control was proposed improving the transition between the two phases This article validated the theoretical analysis by means of simulations and

experimental results, verifying proper system operation in both buck and boost modes, and ensuring the system ability to perform CC/CV charging.

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Abbreviations

The following abbreviations are used in this manuscript:

V_{in} [V]	input voltage
<i>i</i> ₁ [A]	input current
L_1, L_2 [H]	Z-network inductors
$C_1, C_2 [F]$	Z-network capacitors
v _{dc} [V]	DC-link voltage
<i>i_{dc}</i> [A]	DC-link current
$S_1 \dots S_5$	qZS converter switches
v _p [V]	Primary side voltage
<i>i</i> _{<i>p</i>} [A]	Primary side current
L_p [H]	Primary self-inductance
C_p [F]	Primary compensation capacitor
$R_p[\Omega]$	Primary coil resistance
<i>M</i> [H]	Mutual inductance
L_s [H]	Secondary self-inductance
C_s [F]	Secondary compensation capacitor
$R_s \left[\Omega \right]$	Secondary coil resistance
v_s [V]	Secondary side voltage
<i>i</i> _s [A]	Secondary side current
$D_1 \dots D_4$	Rectifier diodes
C_o [F]	Output capacitor
$R_o [\Omega]$	Load resistance
V_o [V]	Output voltage
I_0 [A]	Output current

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