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***Abstract*—In the scenario of a more and more sustainable society, an increasing electrification in different fields, such as mobility and industrial applications, is foreseen in the next decades. As far as power electronics is concerned, a challenging perspective is represented by achieving higher and higher switching frequencies while maintaining high voltage and low power losses. To do that, emerging semiconductor technologies are supposed to be increasingly employed, as well as innovative topologies of connections among switching devices. Among them, the cascode configuration can notably contribute to achieve high levels of dV/dt without losing efficiency. In this paper, a 3-phase Pulse Width Modulated (PWM) inverter based on a cascode connection for each of its six switches is proposed and some promising experimental results are provided. SiC technology has been used for each power device, while a normally-off/normally-on combination of switching devices has been selected to implement the cascode-based switch.**

Keywords—traction inverter, SiC devices, cascode connection.

I. Introduction

In the scenario of a greener and more sustainable future, a capillary electrification of essential goods and services is going to occur in the years to come.

In the recent years an increasing attention has been addressed particularly to electric mobility (E-Mobility), due to the disastrous effects in terms of greenhouse gases emission and global warming arising from the oil exploitation for use in transportations. This urgency will be strengthened by the rapid and imminent growth of the world population [1].

Great efforts have to be still addressed towards an actually sustainable E-Mobility, so that renewable energies are essential for this purpose [2-5].

Therefore, design optimization of power electronics will increasingly play a major role for an actually efficient and sustainable operation in several fields, including E-Mobility [6-8].

One of the most challenging requirements the modern means of transportation need to satisfy is the high power density, in order not to add weight to the vehicles despite the high power needed for traction.

In order to reduce size and weight of components, higher and higher switching frequencies are required, but at the cost of high power losses. To limit switching power losses even at the highest voltage and frequency levels, new semiconductor technologies of power devices, such as Wide Band Gap (WBG) devices, are capable of providing a major contribution. Particularly Silicon-Carbide (SiC) features high breakdown electrical field and thermal conductivity. Therefore, compared to the traditional Silicon Field Effect Transistors (FETs) and Insulated Gate Bipolar Transistors (IGBTs), Silicon-Carbide (SiC) power switching devices are particularly promising in terms of voltage rating and thermal management, keeping high reliability and low energy losses in several fields, including mobility applications [9-11].

In [12], a simulation analysis shows the notable advantages brought by SiC devices in comparison with the Silicon ones especially at the highest switching frequencies.

SiC devices turn out therefore to be attractive solutions for implementing traction DC-AC converters (traction inverters). In fact, traction inverters would benefit from the use of SiC MOSFETs in terms of reachable energy density, due to a higher maximum switching frequency if compared to IGBTs, which on the other side are cheaper.

In addition to emerging switching devices, even alternative connections are being investigated in order to comply with challenging specifications in terms of voltage levels and transient times.

Among them, the cascode connection is greatly attractive, in particular for traction inverters, for what previously mentioned.

The cascode topology consists of the series connection between a switching device which is commanded by an external driving signal and a self-driven switching device whose state depends on the state of the first one.

A convenient solution of cascode connection is based on a normally-off switch as pilot device and a normally-on switch as self-driven device, so that the whole connection is equivalent to a normally-off switch, which is comfortable to drive with common gate driver ICs for low-voltage devices [13].

Cascode configuration provides benefits particularly whenever the converter has to operate in reverse conduction [14]. By using a SiC MOSFET as normally-off device gives advantages in terms of fast switching transients, as experimentally tested in [15] for a DC-DC converter.

[16] reports an investigation on the paralleling suitability of SiC MOSFETs and SiC/Si cascode devices by theoretical

analysis and experimental verifications. Applications of GaN devices in cascode topologies have been investigated in [17]. GaN-based solutions are particularly challenging due to the significant package-related issues, as addressed in [18].

An experimental investigation on the impact of emerging 650/900 V cascode GaN devices on bidirectional DC-DC converters that are suitable for energy storage and distributed renewable energy systems has been reported in [19].

Repetitive surge energy robustness of a 650-V rated cascode GaN HEMT in the unclamped inductive switching test has been investigated in [20].

Regarding GaN/SiC cascode devices, short-circuit characteristics and single-pulse avalanche capability, using an unclamped inductive switching testing setup, have been studied in [21] and [22] respectively.

The failure mode of SiC Cascode JFETs and GaN/SiC cascode devices under short circuit conditions has been investigated respectively in [23] and [24].

Applications of cascode solutions in inverters are investigated in [25-26] for electrical machines driving.

In this paper, an interesting solution of cascode switch is proposed, presenting a normally-on JFET as self-driven device and a normally-off MOSFET as pilot device. JFET devices are convenient in terms of equivalent resistance and capacitance but they do not have body-diode, which is however provided by MOSFETs. Therefore, an equivalent normally-off switch with high blocking voltage and reverse conduction capability is obtained. Moreover, the chosen devices are in SiC in order to aim at extremely fast switching transients.

The use of cascode solution for traction inverters turns out to be promising, especially considering the exploitation of SiC devices, due to the notable potential in terms of reliability at high voltage and frequency levels.

The selected application is a 3-phase inverter supplying an induction motor.

The target power level of the current experimental prototype of cascode-based 3-phase inverter here presented is equal to 5 kW, whereas the target voltage level is 1000 V, which is compliant with some typical E-Mobility traction applications, such as electric vehicles (e.g. considering a 400 V battery) or tramway trolleys (e.g. considering a 750 V DC-grid).

II. THE PROPOSED 3-PHASE INVERTER

A single cascode configuration consists of the series connection between two switching devices, driven by an external control signalin order to obtain the behaviour of a switch with notable performances in terms of voltage rising/falling time, that is the dV/dt, even for high voltage levels. One of the two switching devices is referenced as the pilot device, meaning that it is externally driven but it drives itself the other switching device, which is therefore self-driven.

Two different solutions of cascode connection have been investigated in simulation, both implying the use of an enhancement n-MOS as pilot device and another n-MOS (in one case) or a n-channel JFET (in the other case) as self-driven device.

The disadvantage of the first solution, based on two series-connected n-MOSFETs, lies in the need of a further voltage supply between them to implement the correct switching operation, whereas the second one is more convenient since it is based on a totally self-driven JFET, due to the short-circuit connection between the source of the pilot MOSFET and the gate of the JFET, which is enough to turn the JFET on, due to its negative threshold gate-source voltage, as shown in Fig. 1 and Fig. 2, reporting the MOS/MOS cascode and the MOS/JFET cascode respectively. The floating node at the gate of each pilot MOSFET in the schematics means that an external driving signal is applied between the gate itself and the corresponding source node.

In order to guarantee that a proper gate-source signal is applied to each of the three high-side switches, which are characterized by a floating source node, the MOSFET drivers' output high-side channels are supplied in a way that is electrically isolated from the low-side channels.

The MOS/JFET solution has been considered in this paper, where a 3-phase inverter based on cascode-connected switching devices is proposed. The inverter has been designed and realized by using a cascode connection as each of its 6 switches. For the implementation of the cascode switch, the MOS-JFET solution has been preferred as aforementioned, being more easily controllable since only one external gate signal is required for each switch and being the JFET a convenient high-voltage device in terms of conductivity.

The power MOSFET and the JFET that have been used are reported in Table I, along with their main features in terms of voltage-current rating and dynamic performances. High-voltage SiC FETs have been chosen, as highlighted by their maxima drain-source voltage levels.

TABLE I. MAIN PARAMETERS OF THE CASCODE DEVICE

FET	$V_{ds,max}$ [V]	$I_{d,max}$ [A]	C_{iss} [pF]	C_{oss} [pF]	C_{rss} [pF]
SiC MOS C3M0280090D	900	10.2	204	26	3
SiC JFET UJ3N120070K3S	1200	33.5	985	100	96

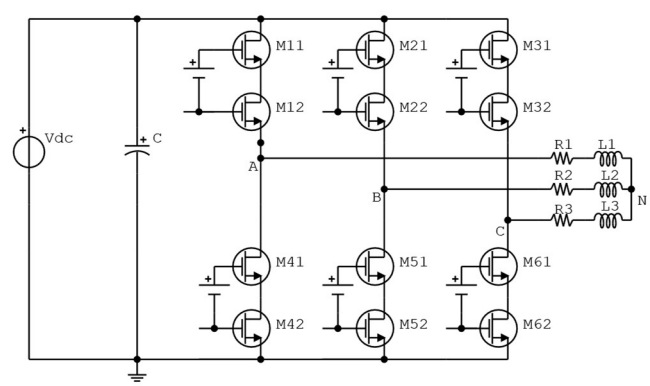


Fig. 1. Schematic of the 3-phase inverter based on nMOS/nMOS cascode.

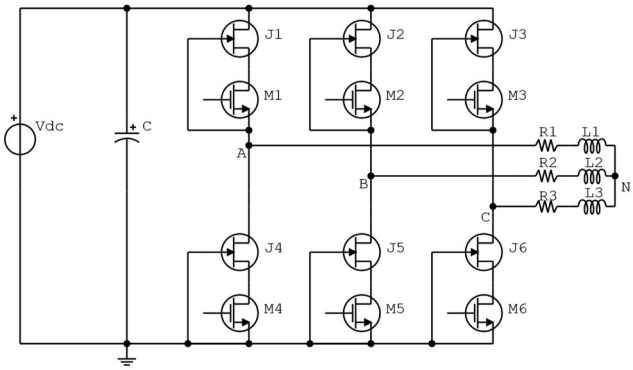


Fig. 2. Schematic of the 3-phase inverter based on nMOS/JFET cascode.

The proposed solution aims therefore to be even more performant dynamically than a single high-voltage SiC MOSFET, due to the fast switching of the of the pilot nMOS body-diode if compared to the switching of a high-voltage SiC body-diode.

The target power level of the current experimental prototype of cascode-based 3-phase inverter here presented is equal to 5 kW, whereas the target voltage level is 1000 V.

Therefore, particular care has been addressed to the layout design of the realized electronic board, as explained in the following section.

The voltage and current waveforms concerning the load and arising from power electronics simulation, as highlighted in both the schematics, are shown in Fig. 3, in order to report the proper operation of the converter in any of the two proposed solutions (either nMOS-nMOS or nMOS/JFET).

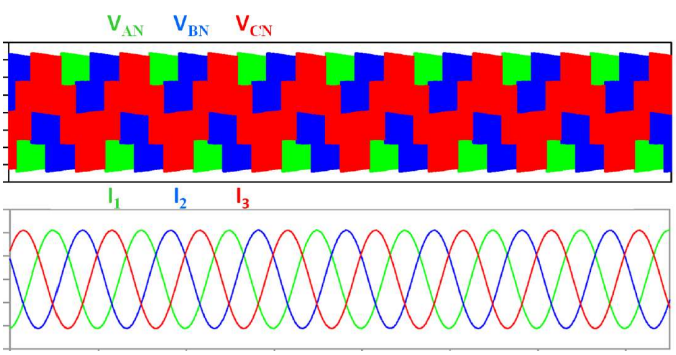


Fig. 3. Simulation of the three load voltage and current waveforms for any of the two above-mentioned cascode-based solutions of inverter.

III. Experimental Setup and Tests

The proposed 3-phase inverter has been realized in order to experimentally investigate its operation while supplying an induction motor.

Due to the high-voltage levels and short switching transients that are foreseen, particular care has been addressed to the design of the printed circuit board (PCB) layout, aiming at smoothing high-frequency ringing and at avoiding electric arcs.

The PCB layout design has been appropriately carried out to minimize the stray inductances, by placing the electronic devices close to each other and by making the copper traces as short and as wide as possible.

Fig. 4. Top view of the experimental prototype of 3-phase inverter based on nMOS/JFET cascode.

Moreover, as for the current paths with high di/dt, the ground paths have been kept separated from the ground plane.

To prevent the risk of electric arcs, a minimum clearance has been adopted considering a 1000 V maximum voltage as safety margin.

An experimental prototype of the proposed inverter has been realized at the Rapid Prototyping Laboratory (RP Lab) of the University of Palermo and it is shown in Fig. 4.

The experimental setup for the test of the 3-phase inverter using cascode switches is shown in Fig. 5, highlighting the PCB of the inverter, a 3-phase induction motor employed as load and a DC voltage supply used to power the inverter, as well as the measurements instrumentation.

Fig. 6 shows the measured 3-phase load current, proving the proper operation of the proposed converter, which correctly supplies the induction motor. The measured peak-to-peak current is equal to 4 A in the specific case.

In Fig. 7 the voltage across a single cascode-connected switch (in green) is shown, under a switching frequency of around 40 kHz and a DC-link voltage of 150 V, along with the drain-source voltage of the pilot MOSFET (in yellow), highlighting that most of the DC supply voltage is applied across the JFET, as foreseen.

The 3-phase sinusoidal PWM strategy consists in a proper gate signals' generation based on the comparison between a 3-phase sinusoidal control signal at a given modulation frequency and a carrier triangular waveform which determines the cascode switching frequency.

In Fig. 8a), the three phase voltage waveforms are shown for a 250 V DC-link voltage and a 50 W power level, as arising from experimental tests, considering a PWM based on a 3.9 kHz carrier frequency and a 100 Hz modulation frequency.

In Fig. 8b) the rise transient of one of these voltage waveforms is highlighted.

The result in terms of dV/dt, arsing from a rise time Δt of about 62 ns, is around 4 V/ns, which is promising if a higher DC voltage will be considered in the future.

A further improvement of the dV/dt is supposed to occur if the DC-link voltage is increased, as in the objective of the present work.

Therefore, due to the decrease of the equivalent capacitance of the switching devices due to a higher applied voltage, the rise transient times should be faster.

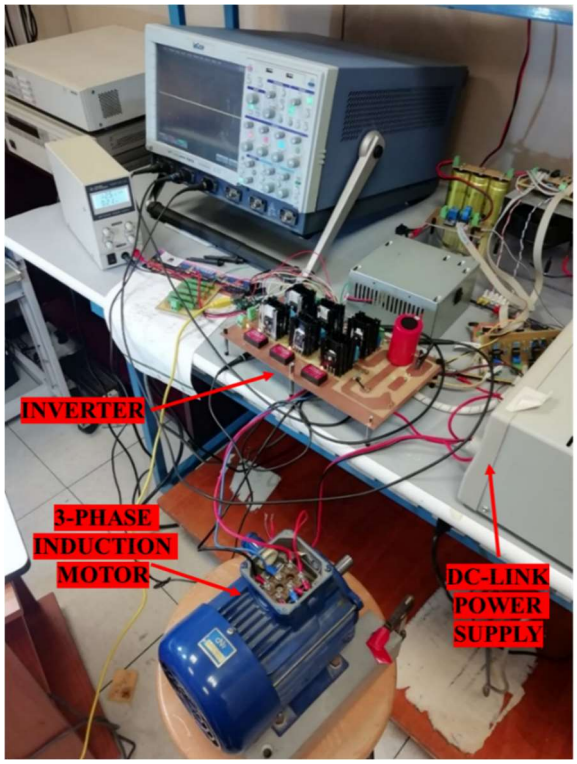


Fig. 5. Experimental setup for the measurements on the 3-phase inverter.

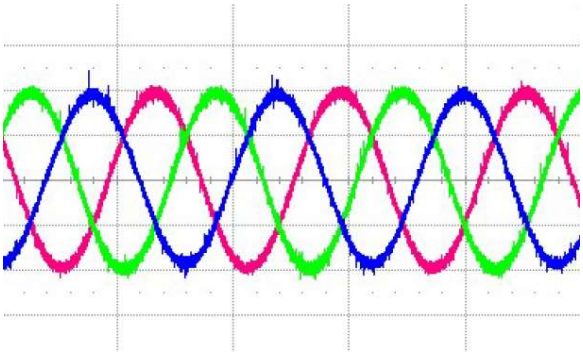


Fig. 6. 3-phase load current measured in the induction motor: current division = 1A/div; time division = 50 ms/div.

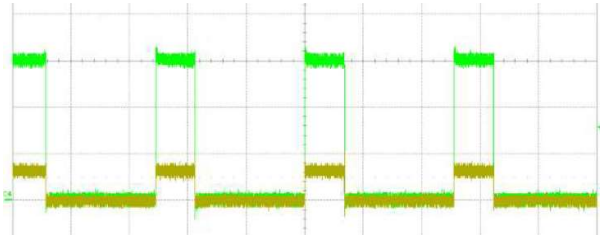
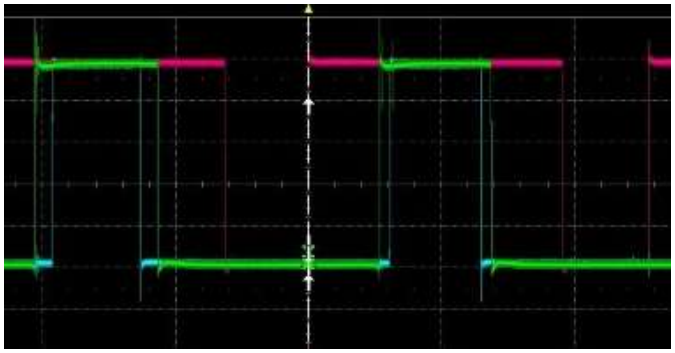
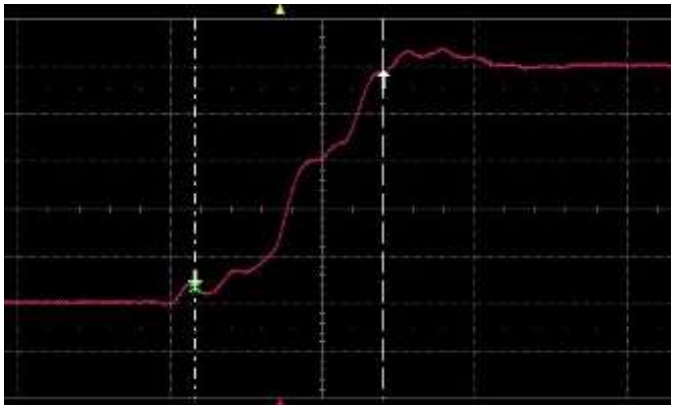


Fig. 7. The cascode switch voltage (green: voltage division = 50 V/div) and the corresponding pilot MOSFET V_{DS} (yellow: voltage division = 20 V/div): time division = 10 μs/div.



(a)



(b)

Fig. 8. (a) V_A (pink), V_B (red), V_C (light blue) voltage waveforms (time division=100μs/div; voltage division=50V/div); (b) rise time of Δt (around 62 ns) of V_A (time division=50ns/div; voltage division=50V/div).

IV. Conclusions

In this paper, a 3-phase inverter with cascode-based switches has been proposed and some experimental results have been shown.

The inverter has been controlled through a sinusoidal PWM and the here shown waveforms concern a switching frequency of around 4 kHz and a modulation frequency of around 100 Hz. A 3-phase induction motor is properly supplied by the proposed prototype, and a dV/dt of around 4 V/ns has been obtained.

Future work implies the investigation of higher voltage levels and switching frequencies, of at least 300 V and 100 kHz, in order to better evaluate the switching performances of the converter, since the case study is at high voltage and frequency.

An improvement of the dV/dt is foreseen, due to the decrease of the equivalent capacitance of the switching devices by increasing the applied voltage.

The use of cascode solution for traction inverters turns out to be promising, especially considering the exploitation of SiC devices, due to the notable potential in terms of reliability at high voltage and frequency levels.

A more detailed investigation concerning the effects of the proposed solution in terms of power density and efficiency of power converters represents the future development of this work, together with the analysis of other possible areas of application and of other significant figures of merit, such as Total Harmonic Distortion (THD).

It will also represent a challenging application to test innovative control algorithms, e.g. concerning the harmonic mitigation in inverters.

Other future developments concern also the exploitation of other emerging technologies for semiconductor devices, like the GaN FETs.

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