Comparative Detailed Analysis of a 7-Level Cascaded H-Bridge Inverter in Symmetric and Asymmetric Configurations

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***Abstract*—This paper discusses the advantages of asymmetric multilevel inverters over traditional inverters and presents a comparative analysis between symmetric and asymmetric cascaded H-bridge multilevel topologies. The use of multilevel inverters is gaining importance in sectors such as electric transportation and renewable energy integration due to their ability to generate high-quality waveforms with lower harmonic content. However, the cost associated with multilevel inverters is a challenge due to the large number of required components. The paper focuses on a single-phase 7-level binary asymmetrical Cascaded H-Bridge Multilevel Inverter (CHBMIs) and compares its performance with the symmetrical counterpart in terms of both harmonic content and total harmonic distortion. In addition, the percentage of power absorbed by both bridges of the asymmetric converter is also analyzed. The results presented in this work show demonstrate the effectiveness of the proposed asymmetrical converter.**

Keywords—Multilevel power converters, modulation techniques, asymmetric cascaded H-bridge multilevel inverter, harmonic analysis.

I. INTRODUCTION

Over the last decades, environmental issues have been compelling significant changes in several areas of industry, particularly in the production, management and utilization of electrical energy. Therefore, there is an increasing interest among the scientific and political communities in addressing environmental issues, with a particular focus on the development of full-electric transportation and the greater utilization of renewable energy sources for energy production. In this context, MultiLevel Inverters (MLIs) can play a crucial role in improving the electrification of transportation and facilitating the integration of renewable energy into the electricity grid [1].

Compared to traditional inverters, the MLIs are capable to generate voltage waveforms with a greater number of levels, which allows a more accurate approximation to the ideal sinusoidal trend. Moreover, MLIs overcome the operative limits of traditional inverters, providing several advantages such as lower harmonic content in the output voltages, reduced voltage stress on the power components in terms of *dv/dt* and decreased ElectroMagnetic Interference (EMI) [1], [2]. Therefore, MLIs are applied in many fields such as high-power and high-voltage systems to build Static Synchronous Compensator (STATCOM) [3], in high-voltage DC applications [4] and e-mobility applications [5], [6].

Among the MLIs topologies reported in the literature [7], the CHBMI is widely adopted due to its modularity and fault-tolerant capability. Thus, the CHBMI is a flexible solution to increase the voltage levels by adding H-Bridge modules [8]. Nevertheless, the CHBMI needs separated DC sources and, therefore, it can be used in all applications where separated DC sources are easily available like PV systems [9], hybrid energy storage systems [10] and automotive [11]. Finally, the CHBMI is particularly suitable for grid-connected applications to regulate the voltage as STATCOM [12].

On the other hand, the cost associated with MLIs is high due to the large number of required components [13]. Several studies propose innovative MLIs topologies to improve efficiency and generate a greater number of output voltage levels while limiting the number of required components [1]. A promising approach is the use of Asymmetrical MultiLevel Inverters (AMLI) that allows to reduce the number of power components.

AMLI structures are obtained by using different voltage amplitudes across the DC-link capacitors. In this way, it is possible to increase the voltage levels while maintaining the same hardware configuration, compared to the symmetric approaches, and reducing the overall cost. Many researchers have proposed innovative asymmetric topologies. For instance, the authors in [14] describe the working principle of an innovative structure of MLI, able to generate an output voltage with 13levels in symmetric configuration, whereas, in the asymmetric configuration, it can generate an output voltage wave of 17-levels achieving a 3% of Total Harmonic Distortion (THD) for the 17-levels and an efficiency of 97%. The AMLI reported in [15] reaches the highest experimental efficiency of 96,74%, whereas the THD of output voltage without filters is 5,3%. Boora et al describe the topology of modular inverters. These converters are composed of multiple cascade-connected cells. generating 57 voltage levels with a voltage THD of 2% [16].

Among the AMLI proposed in the recent literature, an interesting and simple solution is the Asymmetrical Cascaded H-Bridge Multilevel Inverter (ACHBMI) [17], which inherits all the advantages of the CHBMI structure and allows to increase the voltage levels by properly choosing the DC voltage amplitude, without adding H-Bridge modules and by maintaining a reduced hardware complexity. Thus, the main challenge of this topology structure regards the choice of DC voltage amplitudes.

In literature, there are two ways to choose the DC voltage amplitudes: the binary method, where the voltage ratio among the DC source is 1:2:4…; and the tertiary method, with a voltage ratio equal to 1:3:9… [12]. An interesting improvement is discussed in [18], where the ratio among the three sources is 1:2:6.

According to [18], staircase modulation is the best solution to control an ACHBMI converter. This modulation strategy allows to obtain a staircase voltage waveform employing a simple real-time algorithm that can be implemented in common electronic devices. Nevertheless, the main drawback of this approach is the presence of low-order voltage harmonics that increase as the modulation index decrease. Thus, this aspect limits the application fields of this technique. Moreover, a detailed analysis to evaluate the ACHBMI performance in terms of voltage harmonics, conversion efficiency, power distribution among the voltage levels and dead-time effects on the output voltages with MultiCarrier Pulse-Width Modulation (MC PWM) strategies is still missing in the recent literature.

In this work, a comparative analysis between CHBMI and ACHBMI topology structures is reported. In detail, the analysis is focused on the evaluation of the converter performance, in terms of voltage harmonics and power distribution among the voltage levels, by using a multicarrier PWM strategy (Sinusoidal Phase Disposition PWM – SPD PWM). Simulations are carried out in the Matlab/Simulink® environment. Different working points are considered in terms of modulation index and switching frequency and the results between single-phase 7-level CHBMI and ACHBMI in binary configuration are compared.

The paper consists of the following sections: Section II describes the ACHBMI and mathematical model of simulated inverters, Section III reports the implementation of the modulation technique and Section IV discusses the simulation results.

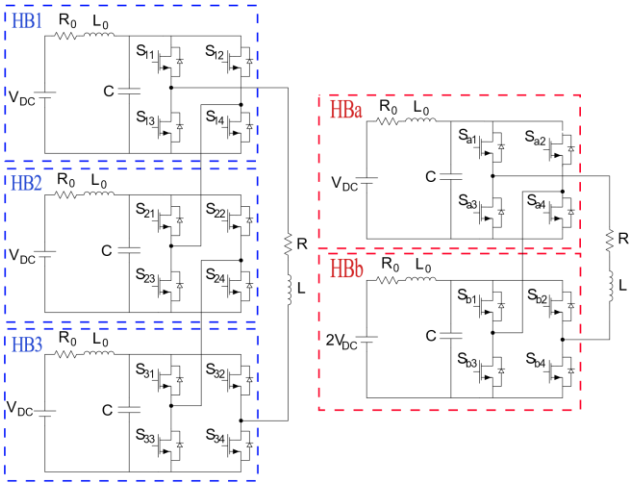

Fig. 1. Single-phase 7-level inverter: (a) CHBMI and (b) ACHBMI.

II. Asymmetric Converter Topology

As well known, the number of the voltage levels N_s for a CHBMI can be expressed as:

$$N_s = 2n_c + 1 \tag{1}$$

where n_c is the number of the cascaded connected H-bridges.

As discussed in [12], the number of the voltage levels for a binary ACHBMI is expressed as:

$$N_a = 2^{n_c+1} - 1. \tag{2}$$

Therefore, it is interesting to note that only two H-bridge modules are needed in the binary ACHBMI configuration to generate 7 voltage levels.

Fig. 1 shows a single-phase 7-level CHBMI and an ACHBMI for comparative purposes. As shown in Fig. 1, an asymmetrical multilevel inverter is capable to generate the same number of voltage levels, but with fewer components and with more compactness concerning the symmetrical topology.

The mathematical model in a symmetrical configuration, shaken in Fig. 1 (a), is described as follows:

$$\begin{cases} V_{HBj} = V_{Cj}(S_{j1} - S_{j2}) \\ \dfrac{di_{0j}}{dt} = -\dfrac{R_0}{L_0} i_{0j} - \dfrac{V_{Cj}}{L_0} + \dfrac{V_{DC}}{L_0} \\ \dfrac{dV_{Cj}}{dt} = -\dfrac{1}{C} i_{load}(S_{j1} - S_{j2}) + \dfrac{1}{C} i_{0j} \\ V_{load} = \sum_{j=1}^{n_C} V_{HBj} \\ \dfrac{di_{load}}{dt} = -\dfrac{R}{L} i_{laod} + \dfrac{V_{load}}{L} \end{cases} \tag{3}$$

where V_{HBj} is the output voltage of the generic H-bridge, S_{ji} ($j = 1 \dots 4$) are the traditional gate signals for 7-level CHBMI, V_{load} is the voltage across the load, i_{load} is load current, V_{DC} refers to the voltage of the DC generator, i_{0j} represents the input current of the *j-th* H-bridge, V_{Cj} denotes the voltage across the *j-th* DC-link capacitor. The circuit parameters are as follows: R_0 is the power supply circuit resistance, power supply circuit resistance is L_0, DC-link capacity C, load inductance is L and R is the load resistance. The mathematical model of the converter in asymmetric configuration is described as follows:

$$\begin{cases} V_{HBa} = V_{Ca}(S_{a1} - S_{a2}) \\ \dfrac{di_{0a}}{dt} = -\dfrac{R_0}{L_0} i_{0a} - \dfrac{V_{Ca}}{L_0} + \dfrac{V_{DC}}{L_0} \\ \dfrac{dV_{Ca}}{dt} = -\dfrac{1}{C} i_{load}(S_{a1} - S_{a2}) + \dfrac{1}{C} i_{0a} \\ V_{HBb} = V_{Cb}(S_{b1} - S_{b2}) \\ \dfrac{di_{0b}}{dt} = -\dfrac{R_0}{L_0} i_{0b} - \dfrac{V_{Cb}}{L_0} + \dfrac{2V_{DC}}{L_0} \\ \dfrac{dV_{Cb}}{dt} = -\dfrac{1}{C} i_{load}(S_{b1} - S_{b2}) + \dfrac{1}{C} i_{0b} \\ V_{load} = V_{HBa} + V_{HBb} \\ \dfrac{di_{load}}{dt} = -\dfrac{R}{L} i_{laod} + \dfrac{V_{load}}{L} \end{cases} \tag{4}$$

where V_{HBa} and V_{HBb} are the output voltage respectively of HBa and HBb, S_{aj} and S_{bj} are the generic signals of switches of the asymmetric inverter, while i_{0a} and i_{0b} represent the input current of the H-bridges, and V_{Ca} and V_{Cb} are the voltage across the respective DC-link capacitor. It is important to highlight that, as seen from the mathematical model in (4), the DC-link voltage of HBb is twice that of HBa.

The current conduction of the diode is taken into account by incorporating Generalized Switching Functions in the mathematical model. The following are the Generalized Switching Functions related to generic HB*j*:

$$\begin{cases} S_{j1} = [(i_{load} \geq 0)\ G_{j1}] + [(i_{load} < 0)\ G_{j3}] \\ S_{j3} = [(i_{load} \leq 0)\ G_{j1}] + [(i_{load} > 0)\ G_{j3}] \\ S_{j2} = [(i_{load} \leq 0)\ G_{j2}] + [(i_{load} > 0)\ G_{j4}] \\ S_{j4} = [(i_{load} \geq 0)\ G_{j2}] + [(i_{load} < 0)\ G_{j4}] \end{cases} \quad (5)$$

Where G_{ji} represents the generic signals generated by the block where the modulation technique is implemented.

III. Implmentation of SPD for ACHBMI

The MC PWM technique is employed to obtain a 7-level waveform using a CHBMI. Specifically, among the various MC PWM patterns available, the SPD pattern is chosen [19]. Fig. 2 shows the SPD modulation scheme. This technique utilizes six carrier signals and one modulating signal to generate the gate signals.

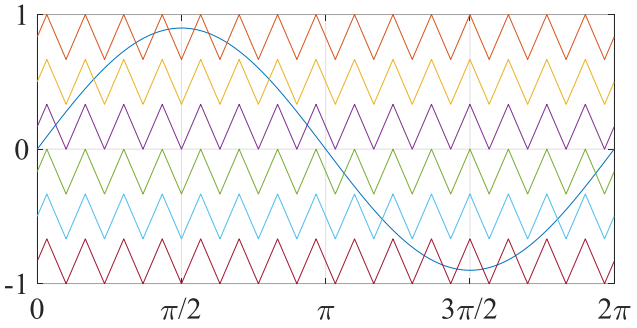

Fig. 2. The PD PWM signals pattern for a 7-level asymmetric inverter.

In MC PWM control, the amplitude of the modulating signal and the frequency of the carriers are not fixed. Therefore, it is important to define the frequency modulation index m_f, which is defined as:

$$m_f = \frac{f_s}{f_1} \quad (6)$$

where f_s represents the carrier frequency and f_1 is the modulating frequency. Instead, the amplitude modulation ratio m_a is:

$$m_a = \frac{V_{mod}}{6V_{car}} \quad (7)$$

where V_{mod} represents the amplitude of the modulating signal, and V_{car} is the amplitude of the carrier signal.

To generate the gate signals for ACHBMI, it is necessary to implement a proper strategy. In detail, the signals of the upper H-bridge HBa need to be modified. In this particular work, a digital approach was employed to achieve this modification, allowing the simplification of the implementation in the common electronic devices, as described in [20].

The gate signals of HBa were obtained by using the following logic functions:

$$\begin{aligned} S_{a1} &= (S_{11} \wedge S_{21} \wedge S_{31}) \vee (\overline{S_{11}} \wedge \overline{S_{21}} \wedge S_{31}) \\ S_{a2} &= (S_{12} \wedge S_{22} \wedge S_{32}) \vee (\overline{S_{12}} \wedge \overline{S_{22}} \wedge S_{32}) \\ S_{a3} &= (S_{13} \wedge S_{23} \wedge S_{33}) \vee (\overline{S_{13}} \wedge \overline{S_{23}} \wedge S_{33}) \\ S_{a4} &= (S_{14} \wedge S_{24} \wedge S_{34}) \vee (\overline{S_{14}} \wedge \overline{S_{24}} \wedge S_{34}) \end{aligned} \quad (8)$$

where S_{ij}, S_{2j} and S_{3j} $(j = 1 \ldots 4)$ are the traditional gate signals for 7-level CHBMI, while S_{aj} are the new gate signals of the HBa. In detail, the control signals for the HBa were generated by comparing the modulating signal with the carrier signal, similar to a standard MC PWM. Subsequently, as depicted in Fig. 3, the logic circuit processes all these signals to determine the control signals for the HBa. While, the signals of the module HBb (with the DC-link voltage equal to $2V_{DC}$) do not need any changes.

These signals are then processed through the logical circuits depicted in Fig. 3. The logical circuits generate the signals for HBa, while the signals from HBb are not processed through logical functions and are directly sent to the inverter model.

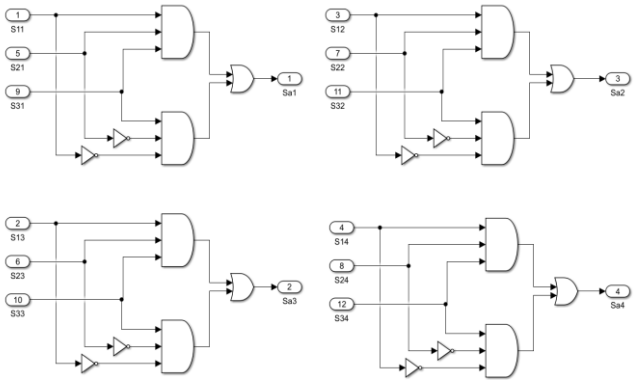

Fig. 3. Logic circuits of the signals of HBa.

A graphical representation of the implemented mathematical model is shown in Fig. 4, where m_a and m_f are the input quantities of the PD PWM modulator.

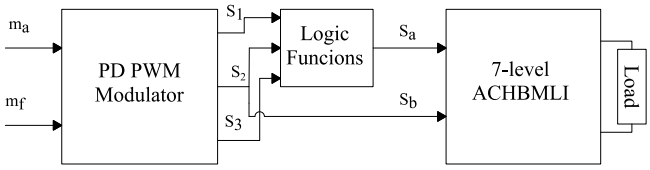

Fig. 4. Block diagram of 7-level ACHBMI.

The modulator generates the signals and implements the dead times between the complementary switch signals.

IV. Simulation Results

The performances of a single-phase 7-level ACHBMI with a traditional single-phase 7-level CHBMI are compared by analyzing the voltage harmonics and the DC power distribution. The mathematical model of Section II has been implemented in the Matlab/Simulink® environment, where the analysis was carried out by considering several working points.

The quality of the generated voltage is evaluated through the spectral analysis and the THD, which can be calculated as follows:

$$THD = \sqrt{\frac{\sum_{h=1}^{\infty}(V_h^2 - V_1^2)}{V_1^2}} \cdot 100 \quad (9)$$

where V_1 represents the amplitude of the fundamental frequency (in this case, 50 Hz), and V_h is the amplitude of the generic harmonic multiple of the fundamental.

Both symmetrical and asymmetrical inverters are controlled with the SPD PWM modulation technique; other circuit parameters such as the capacitors of the DC-link and the load are maintained at the same value to provide comparable results between the two topologies. TABLE I summarizes this analysis.

TABLE I. SIMULATION PARAMETERS

Quantity	*Symbol*	*Value*
Input voltage [V]	V_{DC}	100 V
Power supply circuit resistance [Ω]	R_0	0.1 Ω
Power supply circuit resistance [H]	L_0	10^{-6} H
DC-link capacity [F]	C	$2.2 \cdot 10^{-3}$ F
Fundamental frequency [Hz]	f_1	50 Hz
Load inductance [H]	L	10^{-3} H
Load resistance [Ω]	R	10 Ω
Dead time [s]	t_d	10^{-6} s
Frequency modulation index	m_f	200
Amplitude modulation index	m_a	0.9

A. Harmonic spectra comparison

The main purpose of this analysis is to compare the harmonic distribution in the frequency domain of the voltage. Fig. 5 shows a voltage trend generated by the ACHBMI with m_a=0.9; m_f=200 and f_1=50 Hz.

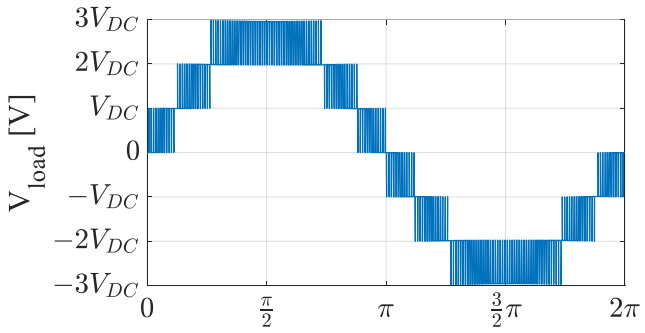

Fig. 5. The voltage waveform on the load over one period.

As shown in Fig. 5, it can noted that the 7-level ACHBMI simulated can generate a step waveform with 7-levels

Fig. 6 shows the comparison between the voltage harmonics in the frequency domain (expressed as a percentage of the fundamental amplitude) for both the symmetrical and asymmetrical configurations at the same working conditions (m_a=0.9; m_f=200 and f_1=50 Hz).

It can be observed that the harmonic spectra are very similar in both configurations, resulting in the same harmonic distribution in the frequency domain. Indeed, in both spectra are detected only harmonics around the multiples of the switching frequency and the predominant component is at switching frequency (h=200) with amplitude 23.83% and 23.79% for ACHBMI and CHBMI, respectively. Additionally, the THD values are equal to 22.63% and 22.81% for ACHBMI and CHBMI, respectively.

B. THD analysis

In this subsection, the performance of CHBMI and ACHBMI have been analyzed by using the THD as a comparison tool, which has been evaluated for different values of modulation index m_a and switching frequency.

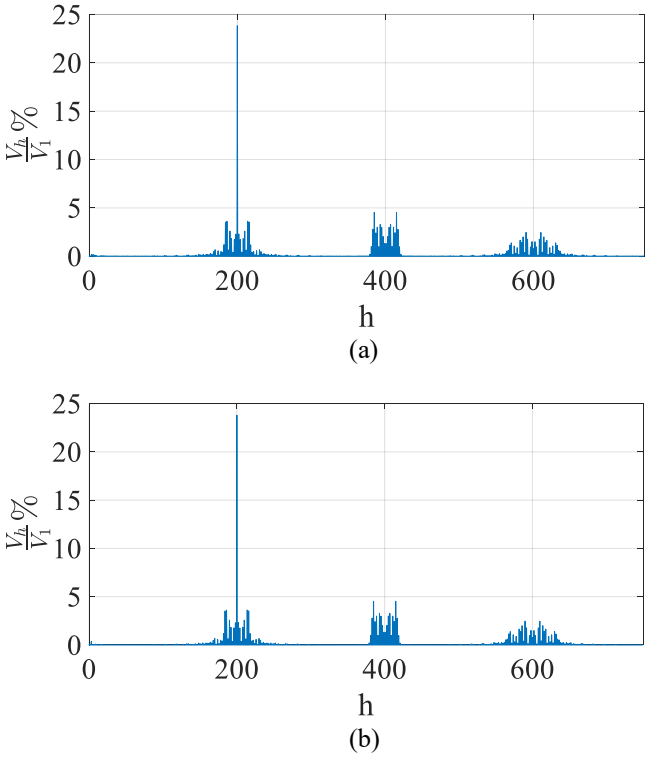

Fig. 6. Harmonic spectrum of the load voltage wave (a) ACHBMI; (b) CHBMI.

The simulations were done for switching frequencies ranging from 5 kHz to 70 kHz and, for each frequency, the modulation index m_a was increased from 0.2 to 1.5. Therefore, the number of voltage levels in the output will vary based on the value of m_a. In both cases, for m_a less than 0.3, the inverters generate 3-level voltages. For m_a equal to 0.4 and 0.5, the inverters produce 5-level voltages. For m_a between 0.7 and 1, the inverters generate 7-level voltages. For even higher values of m_a, the inverters operate in overmodulation.

Fig. 7 shows the THD results vs. modulation index for each of the considered switching frequencies. It can be observed that as m_a increases, increasing the number of levels, the THD decreases even more rapidly. This is because the output waveform more closely approximates the ideal sinusoidal waveform.

The minimum THD value was obtained at m_a equal to 1.2, corresponding to 15.46% and 15.56% for ACHBMI and CHBMI, respectively. Furthermore, in the overmodulation range, the THD increases as m_a increases.

Regarding the impact of the switching frequency on the harmonic content of the alternating voltage, it can be observed that the trends are very close to each other. This suggests that the switching frequency has minimal influence on the value of THD.

Finally, it can be said based on Fig. 7 and to the simulations that the ACBHMI and the CHBMI have the same performance in terms of THD. However, the ACBHMI offers greater hardware simplicity because it is composed of only two H-bridges.

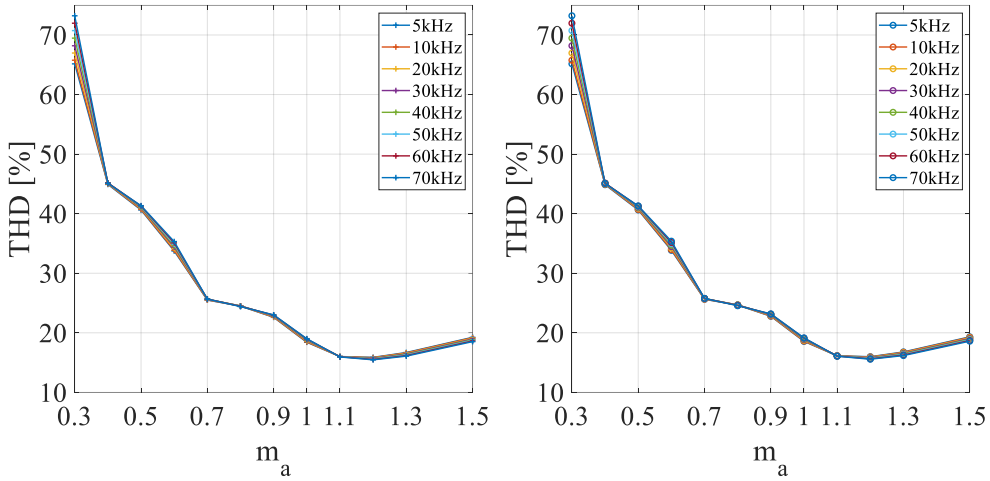

Fig. 7. Variation of load voltage THD for different ma and m_f values: (a) 7-level ACHBMI; (b) 7-level CHBMI

In particular, Fig. 8 shows the THD values of the load voltage for both inverters, with m_a values ranging from 0.3 to 1.5 and a switching frequency of 10 kHz. As observed, the values taken by both curves are almost identical, and the two characteristics are nearly overlapping. Therefore, an enlargement portion of the same graph is also presented in Fig. 8 to highlight the subtle difference between the two curves.

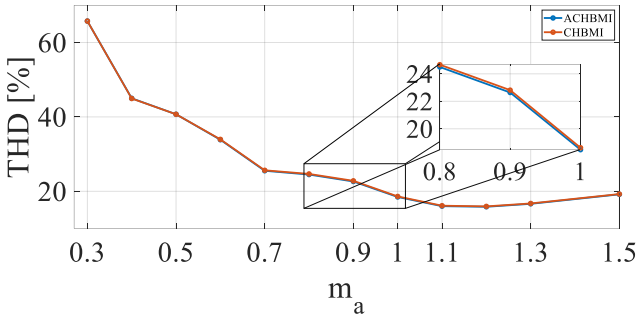

Fig. 8. The THD of the load voltage varies for different values of m_a and a $m_f = 200$.

C. *Power analysis*

Further simulations were conducted to evaluate the percentage of power absorbed by both bridges of the 7-level ACHBMI under different operating conditions, and the results are shown in Figure 9.

Regarding HBa, for $m_a = 0.3$, it absorbs 100% of the power consumed by the ACHBMI, because HBb is not active under these conditions. As m_a increases, the percentage of power absorbed by HBa decreases until reaching a minimum at m_a equal to 0.8, after which it starts to increase again. While the percentage of power absorbed by HBb is zero for $m_a = 0.3$. However, as m_a increases, the percentage of power absorbed by HBb also increases until $m_a = 0.8$. Beyond this point, the percentage of power absorbed by HBb decreases.

In conclusion, it can be said that in this case, the modulation frequency does not have a significant impact on the percentage of power absorbed by both H-bridges. Indeed, the characteristics of different modulation frequencies are very close to each other.

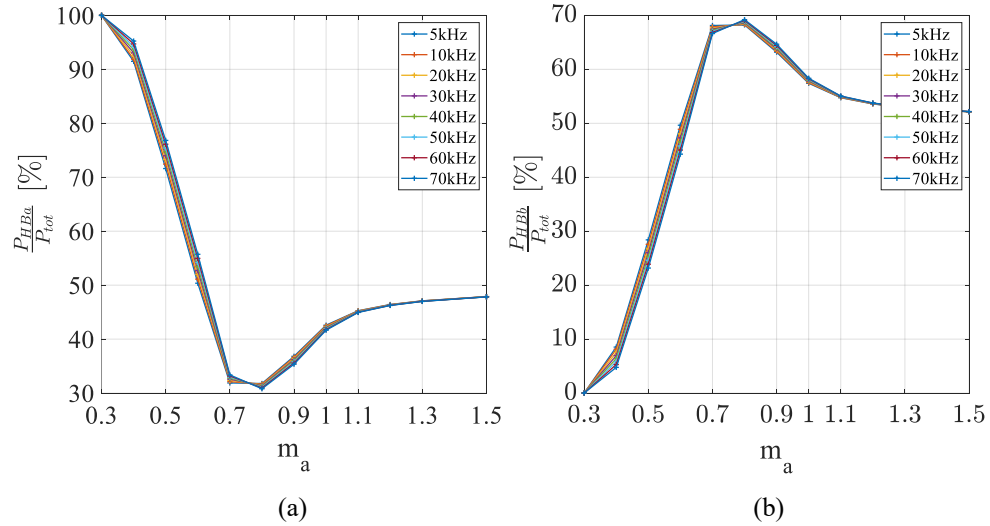

Fig. 9. The average total power absorbed: (a) the average power absorbed by HBa, (b) the average power absorbed by HBb.

V. CONCLUSIONS

This paper presents a performance analysis of the ACHBMI. The focus was on a single-phase, 7-level ACHBMI model, which was evaluated and compared with its symmetric counterpart. Simulations based on the mathematical model were conducted in MATLAB/Simulink® to obtain data for comparison.

It was concluded that the asymmetric 7-level model owns similar performance to the symmetric model but with a reduced number of components and a simpler hardware structure. In addition, simulations were implemented to determine the percentage of power absorbed by each H-bridge of the ACHBMI under various operating conditions.

Based on the simulations, it was concluded that the 7-level ACHBMI offers comparable performance to the symmetric counterpart while having a simpler hardware complexity. The reduced number of components in the asymmetric configuration provided advantages such as increased reliability, compactness, and lightweight characteristics, making it a suitable choice for applications where these features are important, such as the automotive industry.

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