

Virtual EMF-Based Current Limiting Control for Grid-Forming Inverters Under Symmetrical and Asymmetrical Faults

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Abstract—This article proposes a novel current-limiting strategy for grid-forming inverters under symmetrical and asymmetrical faults. The method enables fault ride-through while providing grid support in compliance with grid code requirements. During faults, the power references prescribed by the grid code are imposed, and the virtual EMF is modified accordingly through amplitude and phase feedforward terms in the power loops. These terms are derived from the space-vector diagram of the synchronous machine emulated in the synchronous power control, enabling effective current limitation while preserving grid-forming behavior and avoiding windup in both inner and outer control loops. Such a methodology is first developed for symmetrical grid faults and then extended to asymmetrical faults, where positive- and negative-sequence grid-current injection is prescribed. In this regard, the former is regulated by modifying the positive-sequence virtual EMF, while the latter is limited by a variable virtual reactance. The inner current loop relies on finite-control-set model predictive control to ensure fast dynamic and transient overcurrent limitation. The effectiveness of the proposed method is assessed on a controller hardware-in-the-loop platform and verified on an experimental test bench, both in strong and weak grid scenarios.

Index Terms—Fault current limitation, fault ride-through, grid code, grid faults, grid-forming (GFM) control, model predictive control, multilevel inverters.

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I. INTRODUCTION

GRID-FORMING (GFM) control strategies allow the inverter-based resources (IBRs) to contribute to frequency and voltage regulations by emulating the behavior of traditional synchronous generators (SGs) [1], [2], thus representing a promising solution towards the green transition [3], [4]. In case of a grid fault, GFM inverters are expected to satisfy two fundamental requirements, i.e., actively support the grid, contributing to voltage regulation, and limit the inverter current within the semiconductor ratings. Regarding the first requirement, transmission system operators (TSOs) from different countries are continuously updating grid codes providing proposals and future provisions related to grid support requirements in case of both symmetrical faults, namely three-phase faults [5], [6], [7], and asymmetrical faults, namely single line ground (SLG), double line ground (DLG), and Line–Line (LL) [7], [8], [9]. In particular, they require fast fault current injection (FFCI) capability, i.e., the injection of reactive current for voltage support both at positive- and negative-sequence components according to the severity of the grid voltage reduction and with specified dynamic performance. The second requirement arises from the reduced overcurrent that power electronics devices can withstand during a grid fault (from 1.2 to 1.5 p.u.), if compared to their SGs counterparts [10]. Consequently, including an effective fault-current limiting strategy in GFM inverters control is mandatory to guarantee the fault ride-through (FRT) capability. A significant body of literature focuses on developing current-limiting strategies, which can be mainly classified into: Current limiter-based (CLB), virtual-impedance based (VIB), and voltage-limiter based (VLB) strategies [11].

CLB strategies consist of constraining the current reference supplied to the inner current loop. This task can be implemented by ignoring the current references generated by the GFM controller and imposing limited current references in grid-following (GFL) mode. Although it can be easily adopted both for symmetrical [12] and asymmetrical faults [13], switching from GFM to GFL operation requires a backup phase-locked-loop (PLL) with loss of GFM capability during the fault, which may lead to a slow postfault recovery and instability under weak grid scenarios [14]. The approach proposed in [15] allows for overcoming the described limitation with the use of a reference current circular limiter, which preserves the phase of the reference

current space-vector, thus maintaining the GFM behavior during the fault. In any case, CLB strategies constrain the current references rather than the actual inverter currents. Consequently, the fault-current transient remains dependent on the closed-loop dynamics and potentially dangerous current overshoots may still occur. Moreover, the adoption of a saturator may lead to the windup of the outer power loops, with consequent recovery failure once the fault is cleared [16].

VIB strategies rely on increasing the virtual impedance value to limit the reference current magnitude [17], [18]. Unlike the CLB methods, they do not cause windup of the outer control loops. However, the design of the virtual impedance is challenging since the worst-case scenario must be considered to avoid system instability, thus limiting the actual inverter power capability. Moreover, increasing the virtual impedance leads to transient overcurrent at the fault occurrence and clearance, which can still damage the inverter switches [19]. Most relevant works in the literature address symmetrical faults [17], [18], [19], and only recent works address both symmetrical and asymmetrical faults [20], [21], [22]. However, they lack in effectiveness validation with both strong and weak grid scenarios, and newest grid codes compliance is not considered.

VLB techniques achieve indirect current limitation by limiting the virtual electro motive force (VEMF) generated in the outer control loop. Similarly to CLB strategies, voltage limitation is carried out by saturating both the magnitude and phase of the VEMF, thus requiring appropriate antiwindup schemes, which causes a worsening of the current harmonic distortion. Moreover, the adoption of a PLL is required to carry out proper voltage saturation, resulting in unstable operation under weak grid scenarios. Even in this case, most of the works available in the literature are designed for symmetrical faults [23], [24] and only a poor minority addresses asymmetrical faults, as in [25], where the proposed algorithm is validated in the simulation environment by considering voltage dips only in one phase and in a strong grid scenario. In addition, the negative-sequence current is not controlled and overcurrents occur during the faults, resulting in reduced FRT capability.

This literature review reveals the following research gaps.

- 1) The literature focuses on FRT capability, ignoring newest grid code requirements related to voltage support.
- 2) Existing methods are affected by outer loop windup, complex impedance design, need for backup PLL, and poor dynamic performance.
- 3) Most of the works focus on symmetrical faults and only a few papers address asymmetrical faults.
- 4) The effectiveness of current limiting strategies under a weak grid scenario is poorly investigated.

Given the above, this work proposes a novel indirect fault current limiting strategy for GFM inverters, namely variable VEMF (VVEMF), aimed at addressing the identified literature gaps, by enabling the inverter to ride-through both symmetrical and asymmetrical grid faults while supporting the grid through the FFCI capability. The key novelty of the proposed algorithm lies in updating the active and reactive power loops set points at the fault occurrence based on the grid code prescriptions, and modifying the VEMF space-vector correspondingly through

VEMF amplitude and phase feedforward terms. Such a novel approach does not fall into any of the previous categories and exhibits the following key merits.

- 1) Effective grid current reference limitation without requiring an explicit saturation stage, thus avoiding windup in the outer power control loops.
- 2) Continuous GFM operation also during the fault without any backup PLL, as the outer power loop is never disabled or ignored.
- 3) Grid current control at the positive and negative sequences, enabling voltage regulation under symmetrical and asymmetrical faults and complying with the most up-to-date grid codes.
- 4) Excellent performance even under a weak grid scenario, i.e., short circuit ratio (SCR) = 1.9.

The outer loop is based on the synchronous power controller (SPC) proposed in [26], a power-synchronization-based GFM control strategy that integrates inertia emulation, damping, and droop characteristics through the active power loop. The SPC regulates the positive-sequence grid current by modifying the positive-sequence VEMF through the virtual admittance (VA). An additional outer loop based on a variable virtual reactance is adopted in case of an asymmetrical fault to control the negative-sequence currents. The inner current loop is based on a modified version of the finite control set – model predictive control (FCS-MPC) proposed in [27]. Its multiobjective capability enables the indirect control of the grid currents through the direct regulation of the inverter currents and *LCL*-filter capacitor voltages, allowing simultaneous compliance with grid-code current requirements and inverter current limitation for FRT operation. Unlike conventional current-limiting approaches, inverter current constraints are directly incorporated into the cost function, thereby limiting the actual inverter currents rather than only their references. Moreover, capacitor-voltage control improves the converter behavior under weak-grid conditions by mitigating the oscillations of the voltage at the point of common coupling (PCC). These features, together with the fast dynamic response of MPC, overcome limitations of conventional proportional-integral (PI) and proportional-resonant (PR) controllers related to their single-input single-output structure [27], [28], while addressing the main shortcomings of existing fault-current limiting strategies, namely transient inverter overcurrents and poor performance under weak-grid conditions.

The proposed current limiting strategy is validated under symmetrical and asymmetrical grid faults on a controller-hardware-in-the-loop (C-HIL) platform and on an experimental test bench, composed of an *LCL*-filtered grid-tied three-phase five level (3P-5L) cascaded h-bridge multilevel inverter (CHBMLI), in both strong and weak grid scenarios. The fault current limiting algorithm proposed in [15] has been selected as a comparison target due to its improved postfault recovery capability and continuous GFM operation. The rest of this article is organized as follows. Section II presents the proposed fault current limiting strategy for symmetrical faults. Section III extends the proposed strategy to asymmetrical faults. Section IV describes the C-HIL and experimental setup. Sections V and VI present the control

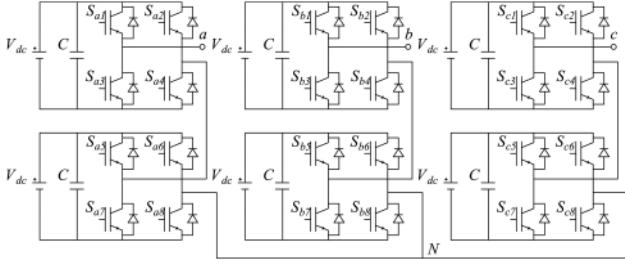


Fig. 1. 3P-5L-CHBML scheme used in the GFM inverter.

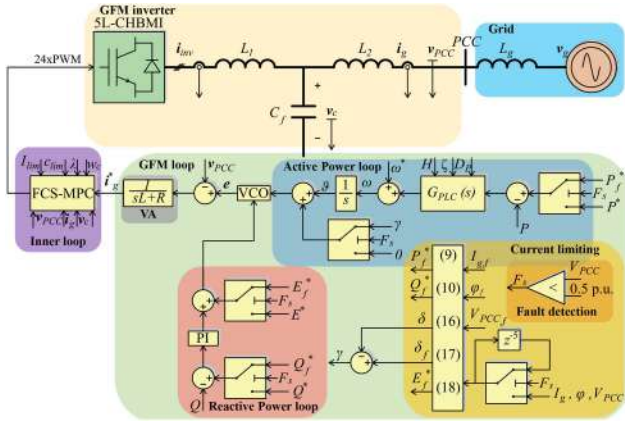


Fig. 2. Block diagram of the adopted GFM control with the proposed fault current limiting strategy for symmetrical faults.

validation under symmetrical and asymmetrical faults, respectively. Finally, Section VII concludes this article.

II. DESIGN OF THE PROPOSED CURRENT LIMITING STRATEGY FOR SYMMETRICAL GRID FAULTS

In this section, the proposed indirect fault current limiting strategy is designed for a three-phase grid short circuit. The GFM inverter is an LCL -filtered grid-tied 3P-5L-CHBML, whose circuit diagram is reported in Fig. 1. Fig. 2 shows the GFM control scheme. The outer loop is based on the SPC [26], empowered by the proposed fault current limiting strategy. The inner control loop is based on FCS-MPC.

According to Fig. 2, $\mathbf{v}_{inv} = [v_{inv,a}, v_{inv,b}, v_{inv,c}]^T$ and $\mathbf{i}_{inv} = [i_{inv,a}, i_{inv,b}, i_{inv,c}]^T$ are the three-phase inverter-side voltages and currents, respectively, $\mathbf{v}_c = [v_{c,a}, v_{c,b}, v_{c,c}]^T$ is the three-phase capacitor voltage, $\mathbf{v}_g = [v_{g,a}, v_{g,b}, v_{g,c}]^T$ and $\mathbf{i}_g = [i_{g,a}, i_{g,b}, i_{g,c}]^T$ are the three-phase grid-side voltages and currents, respectively, and $\mathbf{v}_{PCC} = [v_{PCC,a}, v_{PCC,b}, v_{PCC,c}]^T$ is the three-phase PCC voltage. Moreover, L_1 is the inverter-side inductor, C_f is the filter capacitor, and L_2 is the grid-side inductor, and L_g is the equivalent grid inductance.

The whole control is formulated in the stationary orthogonal $\alpha\beta$ reference frame. Thus, the three-phase quantities $\xi = [\xi_a, \xi_b, \xi_c]^T$ are transformed to $\xi_{\alpha\beta} = [\xi_\alpha, \xi_\beta]^T$ through the transformation matrix T reported as follows:

$$T = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}. \quad (1)$$

It is also recalled that, in the adopted notation, an uppercase symbol $\Xi_{\alpha\beta}$ denotes the amplitude of the space-vector $\xi_{\alpha\beta}$, expressed as

$$\Xi_{\alpha\beta} = \sqrt{\xi_\alpha^2 + \xi_\beta^2}. \quad (2)$$

Finally, it is worth mentioning that the active and reactive powers P and Q at the PCC can be easily computed in the stationary $\alpha\beta$ reference frame from measured $\mathbf{v}_{PCC}$ and $\mathbf{i}_g$ components as

$$P = \frac{3}{2} (v_{PCC,\alpha} i_{g,\alpha} + v_{PCC,\beta} i_{g,\beta}) \quad (3)$$

$$Q = \frac{3}{2} (v_{PCC,\beta} i_{g,\alpha} - v_{PCC,\alpha} i_{g,\beta}). \quad (4)$$

For the sake of notation simplicity, the $\alpha\beta$ subscript is omitted in the remainder of the article, unless otherwise specified.

A. Synchronous Power Controller

The adopted GFM control is based on the SPC [26], a power-synchronization-based GFM strategy that integrates inertia emulation, damping, and droop characteristics within the active power control loop, enabling PLL-less GFM operation.

The active power loop outputs the inverter frequency ω by processing the active power error, i.e., the difference between the active power set point P^* and the measured active power P , through the transfer function, $G_{PLC}(s)$, that emulates the behavior of an SG, expressed in the Laplace domain as

$$G_{PLC}(s) = \frac{sK_P + K_I}{s + K_G} \quad (5)$$

where K_P , K_I , and K_G are the active power loop transfer function gains, which depend on the desired values of virtual inertia H , damping coefficient ζ and active power droop coefficient D_P [26]. One of the main advantages of the SPC is that inertia, damping, and droop characteristics can be designed independently, thus avoiding the coupling between damping performance and droop behavior. In this regard, Zhang et al. [29] provided guidelines for the SPC parameter tuning. In detail, the damping coefficient ζ is chosen equal to 0.707 as it maximizes the SPC phase margin, while the design of the virtual inertia H and the active power droop coefficient D_P depend on the TSO requirements and on the available power reserve of the GFM inverter. Given the above, in this work, H and D_P are set equal to 1 s and to 1 kW/Hz, respectively.

The inverter frequency ω is obtained by adding a frequency feedforward term ω^* to the output of $G_{PLC}(s)$. It is then integrated in time to obtain the VEMF angle ϑ . The reactive power loop computes the reactive power error, i.e., the difference between the reactive power set point Q^* and the measured reactive power Q , using a PI controller, whose transfer function $G_{PI}(s)$ is reported as follows:

$$G_{PI}(s) = k_{P,Q} + \frac{k_{I,Q}}{s} \quad (6)$$

where $k_{P,Q}$ is the proportional gain and $k_{I,Q}$ is the integral gain. These gains are tuned according to [15]. The VEMF magnitude E is computed by adding a feedforward VEMF term E^* to the PI

output. Then, the VEMF magnitude E and angle ϑ are combined in a voltage controlled oscillator to generate the VEMF signal $\mathbf{e} = [e_\alpha, e_\beta]^T$, as follows:

$$\mathbf{e} = E \begin{bmatrix} \cos \vartheta \\ \sin \vartheta \end{bmatrix} \quad (7)$$

The grid current reference signal $\mathbf{i}_g^* = [i_{g,\alpha}^*, i_{g,\beta}^*]^T$ is obtained by feeding the difference between the VEMF $\mathbf{e}$ and the PCC voltage $\mathbf{v}_{PCC}$ to a VA block, whose transfer function $G_{VA}(s)$ is

$$G_{VA}(s) = \frac{\mathbf{i}_g^*}{\mathbf{e} - \mathbf{v}_{PCC}} = \frac{1}{sL + R} \quad (8)$$

where L and R are the virtual inductance and resistance, respectively. According to [26], the virtual inductance L is set to 0.3 p.u., which is a typical value of a grid-connected SG, while the virtual resistance R is set to 0.1 p.u., to guarantee sufficient damping.

B. Indirect Fault Current Limitation Strategy

The indirect fault current limitation strategy must achieve the following objectives during symmetrical grid faults: maintain the GFM behavior and ensure FRT operation.

To maintain the GFM behavior, the structure of the SPC must not be altered, i.e., the current reference $\mathbf{i}_g^*$ must be computed based on the active and reactive power set points through (5), (6), (7), and (8). To this end, such set points must be recomputed at the fault occurrence according to the grid code specifications. In this regard, it is possible to express the active and reactive power references as a function of the PCC voltage amplitude V_{PCC} , and of the desired grid fault current amplitude $I_{g,f}$ and power factor $\cos \varphi_f$, as

$$P_f^* = \frac{3}{2} V_{PCC} I_{g,f} \cos \varphi_f \quad (9)$$

$$Q_f^* = \frac{3}{2} V_{PCC} I_{g,f} \sin \varphi_f. \quad (10)$$

In this application, the grid code [5] is adopted, as it specifies the behavior that the GFM inverter must follow to perform voltage support during symmetrical grid faults. In detail, when the voltage amplitude at the PCC V_{PCC} decreases more than 50% of its rated value $V_{PCC,r}$, the GFM inverter must inject zero fault active power P_f and the maximum available reactive power Q_f so that the resulting fault current amplitude $I_{g,f}$ is equal to the rated current I_r . According to (9), obtaining a zero fault active power with nonzero V_{PCC} and $I_{g,f}$ requires a null power factor $\cos \varphi_f$. Moreover, although the grid code [5] prescribes a fault current equal to the rated current, (10) shows that for a given $\cos \varphi_f$ and V_{PCC} , any reactive power value can be injected by setting the magnitude of the desired grid fault current $I_{g,f}$. This guarantees one extra degree of freedom, allowing for adapting the proposed strategy to different grid codes. Prescriptions of the grid code [5] are adopted to drive the SPC during the fault. In detail, according to the control scheme in Fig. 2, when the PCC voltage magnitude V_{PCC} drops below 0.5 p.u., the fault detection signal F_s is set to high and switches the power set points, P^* and Q^* , from the normal operating conditions to the

fault operating conditions, P_f^* and Q_f^* , computed according to (9) and (10), by imposing a null power factor and the desired grid fault current amplitude $I_{g,f}$. It must be underlined that different fault detection criteria may be adopted according to the requirements of a specific application, utility, or grid code, without affecting the formulation or operation of the proposed control strategy.

However, updating the power set-points according to the grid code prescriptions is not sufficient to guarantee fault current limiting and FRT operation. Indeed, due to the slow dynamic of the SPC loop, at the fault occurrence, the VEMF almost coincides with its prefault value. Looking at (8), it is clear that, for fixed VEMF and VA, a decrease in the PCC voltage due to a grid fault causes an increase in the grid current reference $\mathbf{i}_g^*$, potentially leading to inverter switch damage. Equation (8) also suggests that the current reference $\mathbf{i}_g^*$ can be directly limited through the adoption of a current saturator, or indirectly, by acting on the virtual impedance or on the VEMF. Indeed, the indirect fault current limitation strategy proposed in this work acts on the VEMF to avoid switches damage and preserve the GFM behavior. According to the control scheme in Fig. 2, when the fault is detected, some additional feedforward terms are introduced in the active and reactive power loops to instantaneously adjust the VEMF value. These feedforward terms prevent slow fault VEMF variations that would otherwise lead to undesired transient overcurrent, effectively accelerating the response of the outer active and reactive power loops during the fault. Specifically, in the reactive power loop, the feedforward VEMF magnitude E^* used in normal operating conditions is replaced by its fault feedforward counterpart E_f^* . Similarly, in the active power loop, the null feedforward VEMF angle associated with the normal operating condition is replaced, at the fault occurrence, by a non-null feedforward VEMF angle γ , which modifies the VEMF phase ϑ into ϑ_f . It is worth emphasizing that this mechanism does not ignore nor disable the outer power control loops, but rather assists their dynamics, thereby preserving the GFM behavior of the inverter during fault conditions.

To calculate the fault VEMF feedforward terms E_f^* and γ , the voltage balance equation of the emulated SG connected to the grid under generic operating conditions is considered

$$\mathbf{e} = R\mathbf{i}_g + j\omega L\mathbf{i}_g + \mathbf{v}_{PCC} \quad (11)$$

with

$$\mathbf{j} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}. \quad (12)$$

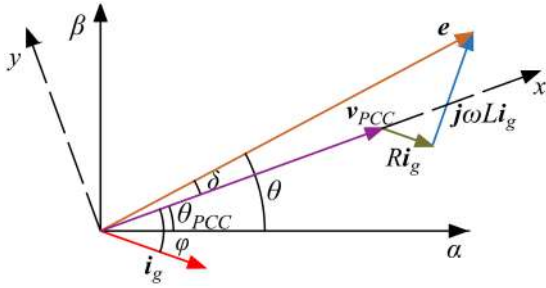
Equation (11) can be represented in the form of a space-vector diagram in the $\alpha\beta$ frame, as shown in Fig. 3.

Looking at the space-vector diagram, the VEMF can be decomposed along the x and y axes, parallel and orthogonal to the voltage space-vector $\mathbf{v}_{PCC}$, respectively, as follows:

$$E \cos \delta = V_{PCC} + RI_g \cos \varphi + \omega LI_g \sin \varphi \quad (13)$$

$$E \sin \delta = \omega LI_g \cos \varphi - RI_g \sin \varphi \quad (14)$$

where δ is the power angle, i.e., the angular displacement between the VEMF and the PCC phase voltage. Combining (13)


$$\begin{aligned}
A &= \begin{bmatrix} -\frac{R_1+R_d}{L_1} \mathbf{I}_2 & \frac{R_d}{L_1} \mathbf{I}_2 & -\frac{1}{L_1} \mathbf{I}_2 \\ \frac{R_d}{L_2} \mathbf{I}_2 & -\frac{R_2+R_d}{L_2} \mathbf{I}_2 & \frac{1}{L_2} \mathbf{I}_2 \\ \frac{1}{C_f} \mathbf{I}_2 & -\frac{1}{C_f} \mathbf{I}_2 & \mathbf{0}_{2 \times 2} \end{bmatrix} \\
B &= \begin{bmatrix} \frac{1}{L_1} \mathbf{I}_2 & \mathbf{0}_{2 \times 2} \\ \mathbf{0}_{2 \times 2} & -\frac{1}{L_2} \mathbf{I}_2 \\ \mathbf{0}_{2 \times 2} & \mathbf{0}_{2 \times 2} \end{bmatrix} \quad (23)
\end{aligned}$$

where $\mathbf{I}$ and $\mathbf{0}$ are the identity and zero matrices, respectively, and R_d is the filter damping resistance. The inverter voltage vector $\mathbf{v}_{inv}$ is expressed as a function of the GCSs state variables through the 3P-5L CHBML control model. In detail, the inverter phase voltage v_{xN} referred to the neutral point N can be expressed as

$$v_{xN} = V_{dc}(S_{x1} - S_{x2} + S_{x5} - S_{x6}) \quad (24)$$

where $x \in \{a, b, c\}$ denotes the inverter phase, V_{DC} is the HB module DC-link voltage, and $S_{xj} \in \{01\}$ are the GCSs related to the upper and lower HB modules when $j \in \{1, 2\}$ and $j \in \{5, 6\}$, respectively. For future system state prediction purposes, the continuous-time state-space model (22) is discretized through an exact discretization method, as follows:

$$\mathbf{A}_d = e^{\mathbf{A}T_s} \quad (25)$$

$$\mathbf{B}_d = \mathbf{A}^{-1}(\mathbf{A}_d - \mathbf{I}_6)\mathbf{B} \quad (26)$$

where $\mathbf{A}_d$ and $\mathbf{B}_d$ are the discrete dynamic matrix and input matrix, respectively, and T_s is the sampling time. To compensate for the computational delay that can lead to steady-state error, a double-step prediction strategy is implemented. Thus, the predicted state can be expressed as

$$\mathbf{x}(k+2) = \mathbf{A}_d^2\mathbf{x}(k) + \mathbf{A}_d\mathbf{B}_d\mathbf{u}_{opt}(k) + \mathbf{B}_d\mathbf{u}(k+1) \quad (27)$$

where k denotes the k th sampling instant and $\mathbf{u}_{opt}(k) = [\mathbf{v}_{inv,opt}(k)^T \mathbf{T}^T, \mathbf{v}_{PCC}(k)^T \mathbf{T}^T]^T$ is the previous optimal control action. The control goals are synthesized into a multiterm cost function, which aims at controlling the grid currents $\mathbf{i}_g(k+2)$ and the switching frequency. In this regard, the grid-current reference $\mathbf{i}_g^*(k)$ generated by the GFM loop must be projected two steps forward, according to the double-step prediction carried out for the system state. Such a projection coincides with rotating the grid-current space-vector by an angle $\Delta\theta = 2\omega T_s$ in the $\alpha\beta$ frame, as follows:

$$\mathbf{i}_g^*(k+2) = \mathbf{T}_{DC}\mathbf{i}_g^*(k) \quad (28)$$

with

$$\mathbf{T}_{DC} = \begin{bmatrix} \cos(2\omega T_s) & -\sin(2\omega T_s) \\ \sin(2\omega T_s) & \cos(2\omega T_s) \end{bmatrix}. \quad (29)$$

Then, the grid currents $\mathbf{i}_g$ are indirectly controlled through the inverter currents $\mathbf{i}_{inv}$ and the capacitor voltages $\mathbf{v}_c$ by calculating their reference values $\mathbf{i}_{inv}^*(k+2)$ and $\mathbf{v}_c^*(k+2)$ from the grid current reference $\mathbf{i}_g^*(k+2)$, as follows:

$$\mathbf{v}_c^*(k+2) = \frac{L_2}{T_s}\Delta\mathbf{i}_g^*(k+2) + R_2\mathbf{i}_g^*(k+2) + \mathbf{v}_{PCC}(k+2) \quad (30)$$

$$\mathbf{i}_{inv}^*(k+2) = \frac{C_f}{T_s}\Delta\mathbf{v}_c^*(k+2) + \mathbf{i}_g^*(k+2) \quad (31)$$

where $\Delta\mathbf{i}_g^*(k+2) = \mathbf{i}_g^*(k+2) - \mathbf{i}_g^*(k+1)$ and $\Delta\mathbf{v}_c^*(k+2) = \mathbf{v}_c^*(k+2) - \mathbf{v}_c^*(k+1)$. It must be underlined that also the PCC voltage space-vector $\mathbf{v}_{PCC}$ must be projected two steps forward accordingly.

In case of a grid fault, although the VEMF is updated instantly through the feedforward terms E_f^* and γ , the current reference $\mathbf{i}_g^*$

still exhibits an overshoot at the fault occurrence and clearance caused by the inductive behavior of the VA. Such an overshoot is reflected through relations (30) and (31) in the inverter current reference $\mathbf{i}_{inv}^*$ and capacitor voltage reference $\mathbf{v}_c^*$. Among them, the overshoot in the inverter current reference $\mathbf{i}_{inv}^*$ is the most dangerous as it is directly responsible of the switch damage. To face this issue, the tracking of this transient reference overcurrent can be avoided by adopting an additional cost function term, which penalizes the predicted overcurrent $\Delta I_{inv}(k+2)$, defined as

$$\Delta I_{inv}(k+2) = \begin{cases} I_{lim} - I_{inv}(k+2), & I_{inv}(k+2) > I_{lim} \\ 0, & I_{inv}(k+2) \leq I_{lim} \end{cases} \quad (32)$$

where I_{lim} is the maximum transient current, and I_{inv} is the predicted inverter current amplitude. In detail, $\Delta I_{inv}(k+2)$ is nonzero only when the predicted inverter current amplitude is higher than the maximum transient current. It must be underlined that penalizing the predicted current amplitude ΔI_{inv} allows for directly limiting the actual converter current evolution within the converter ratings, instead of its reference, representing a fundamental difference with respect to conventional current limiting strategies. This avoids the need for a reference current saturator or circular limiter, thus preventing windup in the active and reactive power loops and guarantees GFM behavior under all operating conditions.

Given the above, the cost function J is formulated as

$$J = \|\mathbf{i}_{inv}^*(k+2) - \mathbf{i}_{inv}(k+2)\|_2^2 + c_{lim}\Delta I_{inv}^2(k+2) + w_c\|\mathbf{v}_c^*(k+2) - \mathbf{v}_c(k+2)\|_2^2 + \lambda\|\Delta\mathbf{v}_{inv}(k+1)\|_1 \quad (33)$$

where w_c , λ , and c_{lim} are weighting factors that allow for penalizing the capacitor voltage reference tracking, the switching frequency, and the predicted overcurrent, respectively. The cost function (33) is then minimized over a prediction horizon $N_p = 1$ to find the optimal control action $\mathbf{v}_{inv,opt}(k+1)$ to be applied at the sampling instant $k+1$. Since the 3P-5L-CHBML phase voltage $v_{xN} \in \{-2V_{DC}, -V_{DC}, 0, V_{DC}, 2V_{DC}\}$, 125 voltage vectors (VVs) should be investigated to find the optimal VV that minimizes the cost function J . Considering the CHBML GCSs redundancies, the control problem computational complexity grows easily, making the control implementation unfeasible. Thus, the computational complexity is reduced through an offline optimization process and online switching constraints [30]. The former is aimed at eliminating VV and GCSs redundancies: the VVs selection criterion lies in minimizing the common mode voltages, while the GCSs selection criterion lies in minimizing the switching transitions. The latter aims to restrain the set of online investigated VVs $\mathcal{U}(k+1)$ to minimize the cost function. In details, only the previous optimal VV and its adjacent VVs are investigated to find the solution of the optimal control problem. In this way, only seven predictions are required, making the FCS-MPC implementation feasible and computationally cheap. A more detailed discussion concerning the offline optimization process, the online switching constraints, and implementation details is provided in [27] and [30].

Finally, the optimal control problem is formulated as follows:

$$\begin{aligned} v_{inv,opt}(k+1) &= \arg \min J(i_{inv}(k), v_c(k), v_{inv}(k)) \\ \text{s.t. } \begin{cases} x(k+2) = A_d^2 x(k) + A_d B_d u_{opt}(k) + B_d u(k+1) \\ |\Delta v_{xN}(k+1)| \leq V_{DC} \\ |i_{inv}(k+2)| \leq I_{lim} \\ v_{inv}(k+1) \in \mathcal{U}(k+1). \end{cases} \end{aligned} \quad (34)$$

III. EXTENDING THE PROPOSED CURRENT LIMITING STRATEGY TO ASYMMETRICAL GRID FAULTS

In this section, the indirect current limiting strategy designed previously for three-phase short-circuit is extended to address asymmetrical grid faults. Throughout the text, the superscripts “+” and “−” denote a positive- and a negative-sequence electric quantity, respectively, while the superscripts “+,” “−” denote that the considered equation is valid for both positive- and negative-sequence.

A. Grid Code Requirements for Asymmetrical Faults

To account for asymmetrical faults, the grid code [9] is adopted to impose the positive- and negative-sequence current references. It prescribes a null active current and a linear relation between the PCC voltage reduction $\Delta V_{PCC}^{+,-} = V_{PCC,f}^{+,-} - V_{PCC}^{+,-}$ due to the grid fault and the reactive grid current increment $\Delta I_{g,Q}^{+,-} = I_{g,Q,f}^{+,-} - I_{g,Q}^{+,-}$ to support the grid during the fault

$$\Delta I_{g,Q}^{+,-} = r I_r \frac{\Delta V_{PCC}^{+,-}}{V_{PCC,r}}. \quad (35)$$

Supposing that during normal operation null positive- and negative-sequence reactive current is injected, then $\Delta I_{g,Q}^{+,-} = I_{g,f}^{+,-}$. In this regard, the parameter r is a coefficient representing an overcurrent factor, i.e., the ratio between the injected reactive fault current and the rated current required to provide adequate voltage support during asymmetrical faults. The grid code [9] prescribes values of r in the range 2–6, depending on the country in which the grid code is applied. It is worth emphasizing that the requirement of injecting a reactive fault current 2–6 times higher than the rated current appears highly demanding from a converter design perspective. Indeed, power electronics devices are designed with respect to their rated current capability, with only limited and time-constrained overload margins [10]. Such prescriptions, although currently proposed rather than formally adopted, would imply either operating the GFM inverter beyond its safe operating area or significantly oversizing the semiconductor devices, with evident penalties in terms of cost, efficiency, and power density. Considering that grid faults are rare and short-duration events, enforcing $r > 1$ at the hardware level may lead to a disproportionate design effort with respect to the expected operational benefit. For this reason, in this work, r is set equal to 1, meaning that the inverter provides voltage support up to its rated current capability. A broader critical assessment of these emerging grid code requirements, however, lies beyond the scope of this article. Given the above,

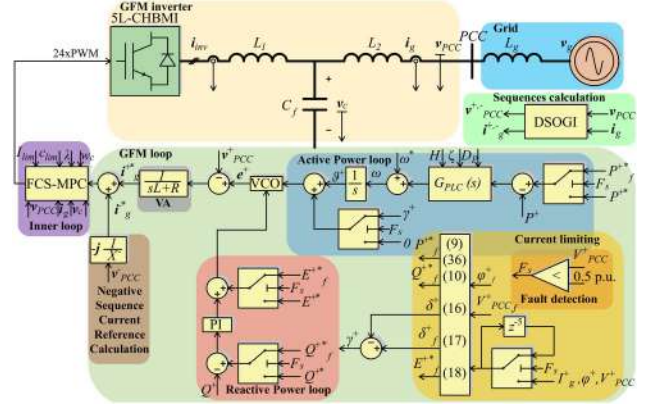


Fig. 4. Block diagram of the adopted GFM control with the proposed fault current limitation strategy for asymmetrical faults.

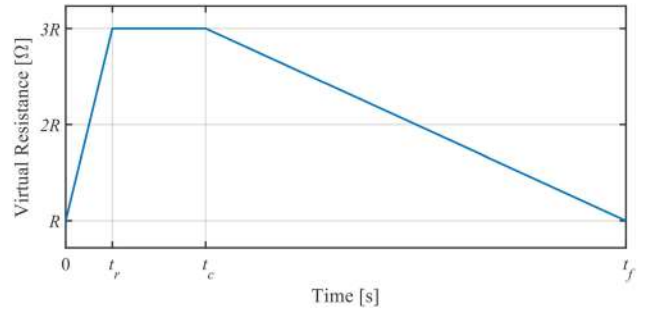


Fig. 5. Postfault variable virtual resistance trend.



Fig. 6. Test bench: 1) Six DC sources; 2) 3P-5L-CHBMI; 3) LCL filter; 4) Grid connection switch; 5) Grid emulator; 6) Master and slave oscilloscopes; 7) PC with GUI; and 8) PED-Board with measurement shield.

(35) is updated as follows:

$$I_{g,f}^{+,-} = I_r \frac{\Delta V_{PCC}^{+,-}}{V_{PCC,r}}. \quad (36)$$

B. Improved GFM Control With positive- and Negative-Fault Current Limiting Control Capability

As the grid code [9] prescribes the injection of both positive- and negative-sequence reactive current during asymmetrical faults, the key improvement to maintain GFM behavior and ensure FRT operation deals with calculating the symmetrical components of the PCC voltage and grid current for control purposes. In this regard, the improved GFM control scheme with positive- and negative-sequence control capability is shown in Fig. 4. To calculate the positive- and negative-sequence

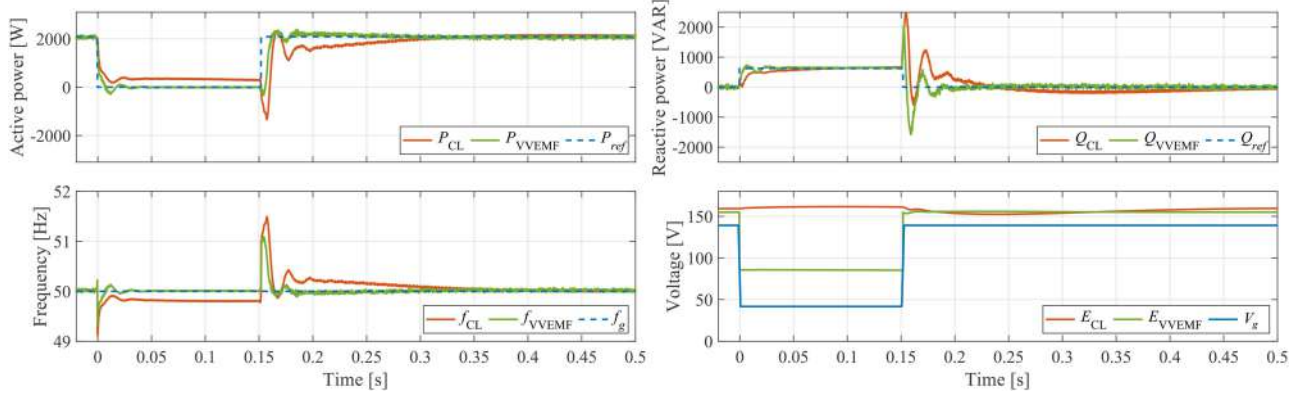


Fig. 7. C-HIL outer loops response comparison during a symmetrical fault obtained with the CL method (orange) and the proposed VVEMF method (green), $V_{PCC,f} = 0.3$ p.u., and an $SCR = \infty$.

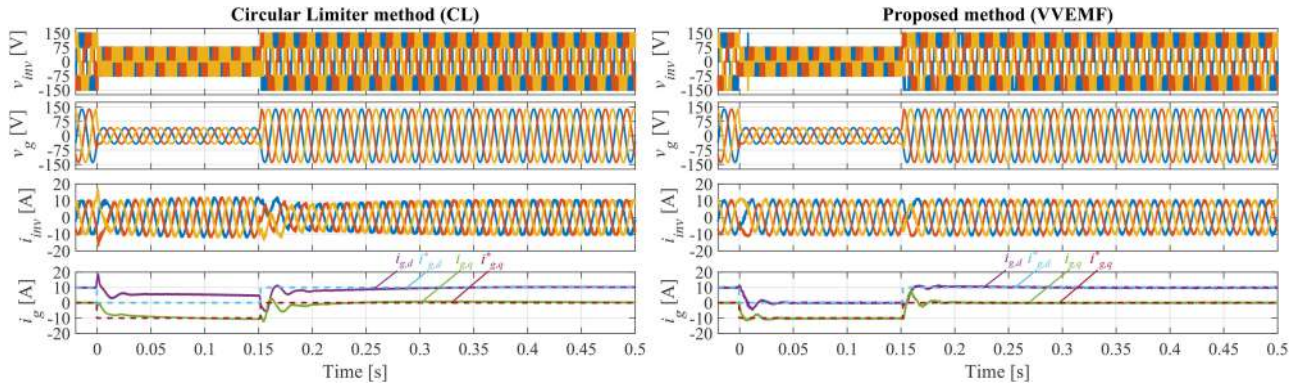


Fig. 8. C-HIL main electrical quantities during a symmetrical fault obtained with CL method (left) and the proposed method VVEMF strategy (right), $V_{PCC,f} = 0.3$ p.u., and an $SCR = \infty$.

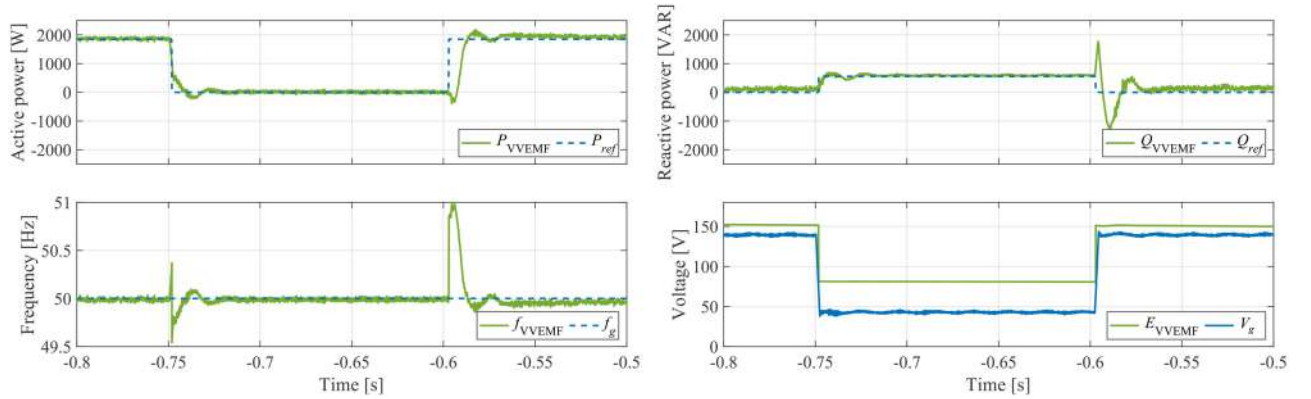


Fig. 9. Experimental outer loops response comparison during a symmetrical fault obtained with the CL method (orange) and the proposed VVEMF method (green), $V_{PCC,f} = 0.3$ p.u., and an $SCR = \infty$.

space-vectors $i_g^{+,-}$, and $v_{PCC}^{+,-}$, a double second-order generalized integrator (DSOGI) with frequency locked loop (FLL) is adopted, as shown in Fig. 4. The interested reader can find more details on the employed block scheme and transfer function of the DSOGI-FLL in [31].

It must be underlined that, regarding the calculation of the positive sequence grid-current reference i_g^{+*} , the adopted control scheme is identical to that designed for symmetrical grid faults discussed in Section II. In detail, the fault is detected by

investigating the PCC voltage amplitude at the positive sequence V_{PCC}^{+} . This choice provides a unified fault detection criterion between symmetrical and asymmetrical fault events.

At the fault occurrence, the positive-sequence grid current reference i_g^{+*} is computed through the SPC (5), (6), (7), and (8) by switching the power references from normal operation to fault operation. Positive sequence active and reactive power set points P^{+*} and Q^{+*} are, respectively, computed through (9), characterized to guarantee a null positive-sequence active

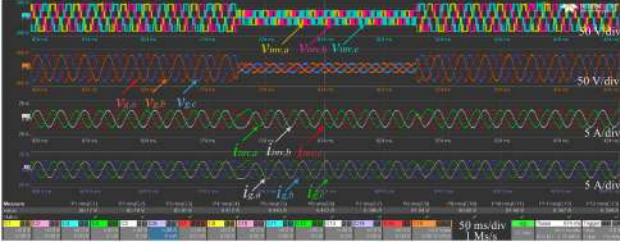


Fig. 10. Experimental results obtained with the proposed VVEMF during a 3PF, $V_{PCC,f} = 0.3$ p.u., $SCR = \infty$, $I_f = 1$ p.u.

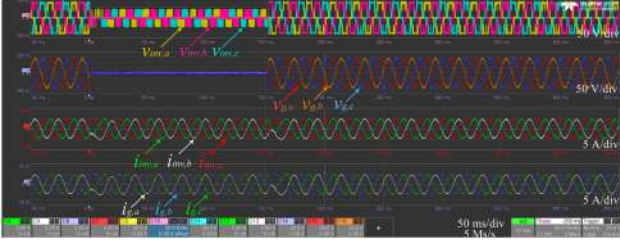


Fig. 11. Experimental results obtained with the proposed VVEMF during a 3PF, $V_{PCC,f} = 0$ p.u., $SCR = \infty$, $I_f = 1$ p.u.

power, and by replacing the positive-sequence of (36) in (10). Even in this case, the methodology behind the indirect fault current limiting strategy for asymmetrical faults is identical to that discussed in Section II. Indeed, it is based on updating the feedforward terms E_f^{+*} and γ^+ in the active and reactive power loops to instantaneously adjust the positive-sequence VEMF. With this aim, (16), (17), (18), and (21) are adopted. The negative-sequence grid current reference i_g^{-*} is calculated by imposing that such current must be in quadrature lagging the negative-sequence PCC voltage v_{PCC}^- . This implicitly imposes the negative-sequence current component to be purely reactive, according to [9]. Thus

$$i_g^{-*} = -j \frac{v_{PCC}^-}{X^-} \quad (37)$$

where $X^- = V_{PCC,r}/I_r$ is a negative-sequence virtual reactance, computed by considering the negative-sequence grid current injection requirement (36).

Finally, it has been observed in the simulation environment that, at the asymmetrical fault clearance, severe oscillations in the PCC voltage are recorded in the weak grid scenario. Such oscillations occur as the PCC is strongly correlated to the grid-current trend in weak grid scenarios. To face this issue, a variable postfault virtual resistance is implemented according to [15]. The postfault resistance trend has been designed by trial-and-error fashion, and it is depicted in Fig. 5. At the fault clearance, the virtual resistance is tripled within a sampling interval T_s , equal to 50 μ s in this work. Then it is maintained at a value of $3R$ for six subsequent sample intervals, and, finally, it decreases to the prefault value in 20 ms (i.e., 400 sampling instants).

Once the references i_g^{+*} and i_g^{-*} are obtained, they must be projected two-steps forward to account for the delay compensation strategy adopted in the FCS-MPC through (28). In this

regard, since positive-sequence space-vectors rotate counter-clockwise in the $\alpha\beta$ frame, then $T_{DC}^+ = T_{DC}$, and the matrix reported in (29) can be used to compute the projected positive-sequence grid-current reference $i_g^{+*}(k+2)$. The projected negative-sequence grid-current reference $i_g^{-*}(k+2)$ is obtained by considering that the negative-sequence space-vectors rotate in the $\alpha\beta$ frame in the opposite direction with respect to their positive-sequence counterparts. Thus, the argument of sine and cosine functions in matrix (29) must be inverted, which leads to $T_{DC}^- = T_{DC}^T$. Projected positive- and negative-sequence grid-current references are composed to obtain the total grid-current reference $i_g^*(k+2)$, as follows:

$$i_g^*(k+2) = i_g^{+*}(k+2) + i_g^{-*}(k+2). \quad (38)$$

At this point, the remaining operations regarding the inner FCS-MPC, i.e., inverter-side current and the capacitor voltage references calculation, future system state predictions, and cost function minimization are unchanged.

Overall, the FRT methodology proposed in Section II for symmetrical faults can be extended to asymmetrical grid faults with only minor modifications. In practice, the only addition consists of a control loop for computing the negative-sequence current reference, while the rest of the control structure remains essentially unchanged. This highlights the versatility of the proposed approach, which allows the fault current to be shaped according to the desired operating objective. It is also worth noting that different grid codes have been adopted for symmetrical and asymmetrical faults to demonstrate the capability of the proposed method to adapt to different requirements, since its formulation relies on fundamental electrotechnical relations rather than on a specific grid code prescription. Finally, also in the asymmetrical case, the proposed strategy preserves the GFM behavior, enabling both FRT capability and active grid support during the fault.

IV. C-HIL AND EXPERIMENTAL SETUP DESCRIPTION

The proposed indirect fault current limiting strategy is validated both in a C-HIL environment and on an experimental setup. In both cases, the control algorithm runs on a sbRIO-9651 controller. In the C-HIL environment, the power stage is emulated in real time on a Typhoon HIL 404, replicating the experimental setup shown in Fig. 6, consisting of a 3P-5L-CHBMI prototype, six 75 V DC sources, an LCL filter, and a grid emulator. This approach allows verifying the correct functionality and real-time feasibility of the algorithm before proceeding to experimental validation. Moreover, it enables safe testing under potentially critical operating that could be harmful to the real hardware conditions (e.g., weak grid or zero voltage at the PCC). The main system parameters are reported in Table I. More details on the experimental setup can be found in [27].

V. CONTROL VALIDATION UNDER SYMMETRICAL FAULTS

In this section, the proposed strategy is validated under symmetrical grid faults. To prove the benefits of the proposed

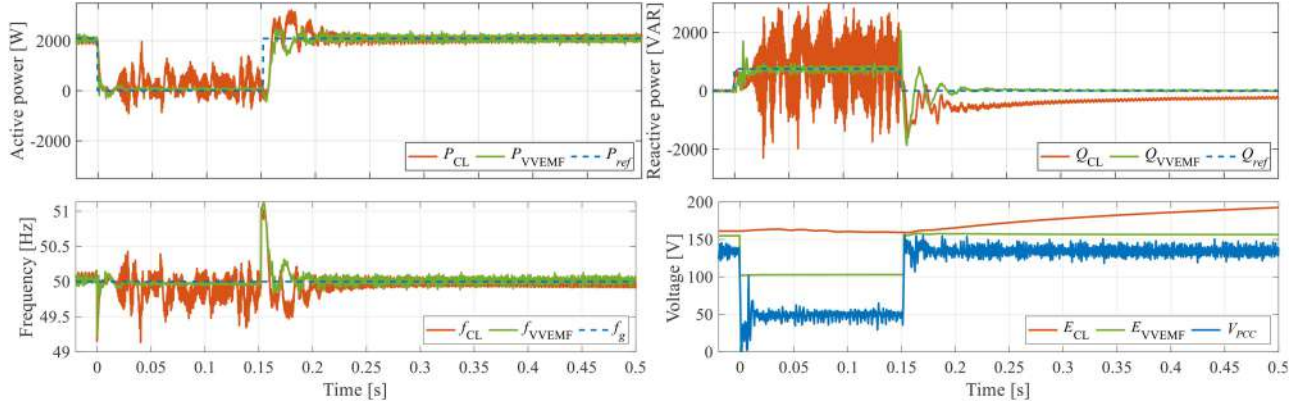


Fig. 12. C-HIL outer loops response comparison during a symmetrical fault obtained with the CL method (orange) and the proposed VVEMF method (green), $V_{g,f} = 0.3$ p.u., and an SCR = 4.

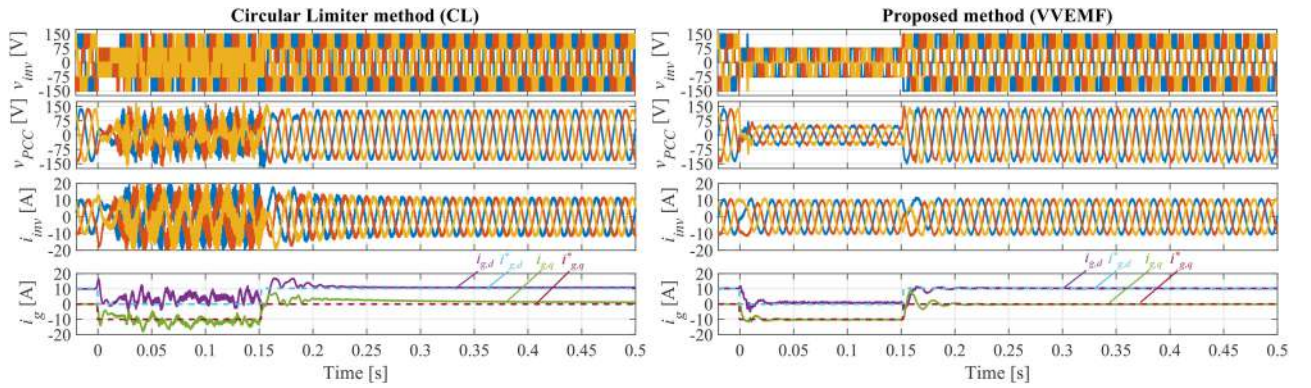


Fig. 13. C-HIL main electrical quantities during a symmetrical fault obtained with CL method (left) and the proposed VVEMF strategy (right), $V_{g,f} = 0.3$ p.u., and an SCR = ∞ .

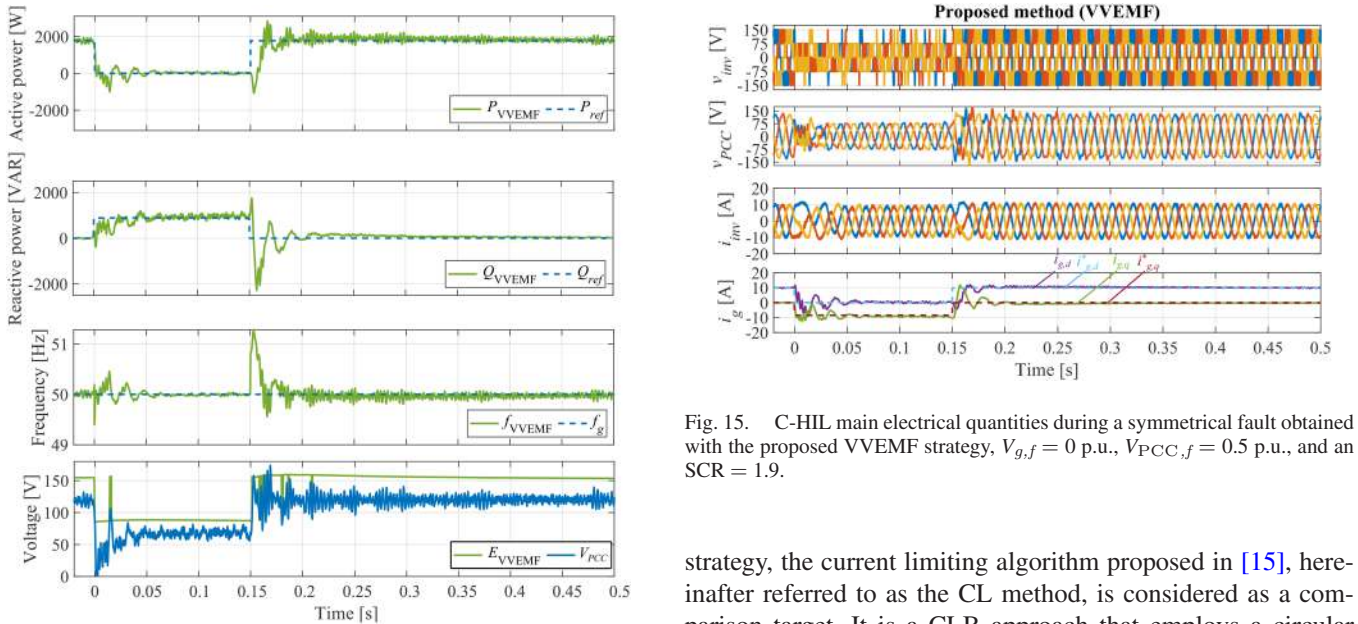


Fig. 14. C-HIL outer loops response during a symmetrical fault obtained with the proposed VVEMF strategy, $V_{g,f} = 0$ p.u., $V_{PCC,f} = 0.5$ p.u., and an SCR = 1.9.

Fig. 15. C-HIL main electrical quantities during a symmetrical fault obtained with the proposed VVEMF strategy, $V_{g,f} = 0$ p.u., $V_{PCC,f} = 0.5$ p.u., and an SCR = 1.9.

strategy, the current limiting algorithm proposed in [15], hereinafter referred to as the CL method, is considered as a comparison target. It is a CLB approach that employs a circular limiter to constrain the grid current reference while preserving the GFM behavior during the fault. Moreover, also the CL method employs the SPC as GFM structure, and incorporates

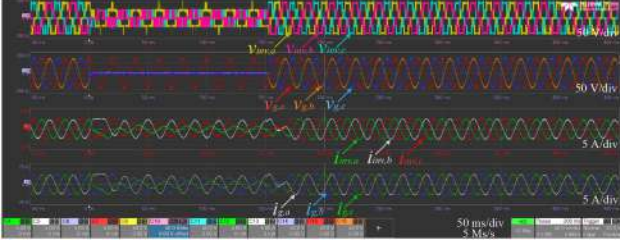


Fig. 16. Experimental main electrical quantities during a DLG fault ($v_{g,b}$ and $v_{g,c}$ go to zero) with an SCR = ∞ .

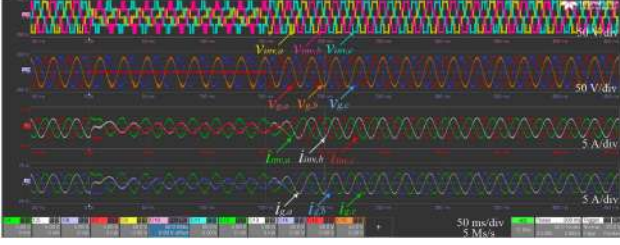


Fig. 17. Experimental main electrical quantities during a SLG fault ($v_{g,a}$ goes to zero) with an SCR = ∞ .

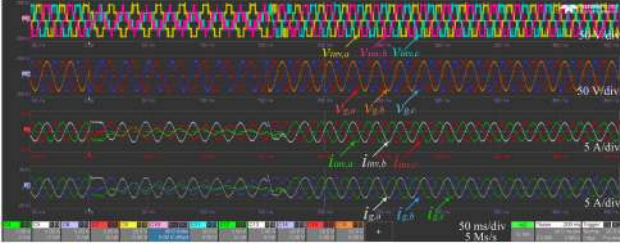


Fig. 18. Experimental main electrical quantities during a LL fault ($v_{g,b}$ becomes equal to $v_{g,c}$) with an SCR = ∞ .

power set-point adjustment to comply with grid-code requirements and a variable virtual impedance to improve the postfault recovery performance. Therefore, the CL method shares most of the key features of the proposed VVEMF strategy and the main difference is related to the current limiting mechanism. For this reason, the CL method represents an ideal benchmark for assessing the effectiveness of the proposed current limiting approach. It employs standard PR controllers in the inner current loop with a PWM stage and is tuned according to the zero-pole cancellation strategy [32]. To verify the FRT and FFCI capability of the compared strategies, a grid voltage reduction up to 0.3 p.u., which lasts 0.15 s, is investigated in the case of both strong and weak grid scenarios. The comparison is performed in terms of current, power, and frequency overshoot, settling time, and steady-state error. In particular, settling time and steady-state error quantify the compliance with grid-code dynamic requirements, whereas the current overshoot represents a key indicator of the fault current limiting effectiveness and the resulting FRT capability. Since the injected fault current depends on the maximum transient current I_{lim} with its weight c_{lim} and on the fault current magnitude $I_{g,f}$, to inject the rated current as specified by the grid code, these parameters are set to

TABLE I
SYSTEM PARAMETERS

Symbol	Quantity	Value ^a
S_r	Rated apparent power [kVA]	2
V_g	Rated line grid voltage RMS [V]	170
f_g	Rated grid frequency [Hz]	50
V_{DC}	DC voltage input of each H-Bridge [V]	75
f_{sw}	Switching frequency [kHz]	3.2
L_1	Converter-side inductance [mH]	2.2
L_2	Grid-side inductance [mH]	2.2
C_f	Filter capacitance [μ F]	10
R_d	Damping resistance [Ω]	1
f_{res}	Resonance frequency [kHz]	1.5
f_s	Sampling frequency [kHz]	20
λ	Switching effort weighting factor [-]	$1 \cdot 10^{-4}$
w	Capacitor voltage tracking weighting factor [-]	0.03
c_{lim}	Overcurrent penalization weighting factor [-]	50
I_{lim}	Maximum transient current [A]	11
H	Virtual inertia constant [s]	1
D_P	Active power droop coefficient [kW/Hz]	1
ζ	Active power loop damping coefficient [-]	0.707
K_P	Active power loop gain [Hz/W]	0.0028
K_I	Active power loop gain [Hz/J]	0.0188
K_G	Active power loop gain [Hz]	2.9939
$k_{p,Q}$	Reactive power loop proportional gain [-]	0
$k_{i,Q}$	Reactive power loop integral gain. [-]	0.25
L	Virtual inductance [p.u.]	0.3
R	Virtual resistance [p.u.]	0.1
k_p	Current loop proportional gain [-]	4.69
k_i	Current loop integral gain [-]	213.39
SCR	Short Circuit Ratio [-]	$1.9 \sim \infty$
$I_{g,f}$	Fault current magnitude [A]	10 A

11 A (1.1 p.u.), 50 and 10 A (1 p.u.), respectively, as reported in Table I.

A. Strong Grid Scenario (SCR = ∞)

The comparison between the outer loop responses to the grid voltage reduction produced by the proposed VVEMF strategy and by the CL strategy, in terms of active and reactive power, inverter frequency, and main electrical quantities, is carried out in the C-HIL environment and it is depicted in Figs. 7 and 8, respectively. It should be noted that the frequency depicted in Fig. 7 is an inner control quantity; thus, it is not directly measured. It is obtained through the active power loop transfer function (5), based on the active power error. Looking at the active power trends shown in Fig. 7, although both strategies impose the same active and reactive power references variations, the proposed VVEMF strategy guarantees a much more precise and fast response. Indeed, at the fault occurrence, the proposed VVEMF strategy allows for reaching the active power reference within 40 ms with a reduced power overshoot (about 12%), while the CL strategy never reaches the active power reference over the fault duration of 150 ms and an almost constant active power error of about 500 W is recorded. At the fault clearance, the proposed VVEMF strategy allows for injecting the reference active power in about 40 ms with an overshoot of 12%; on the contrary, the CL strategy exhibits a relevant active power overshoot (about 65%) at the reference variation and reaches the active power reference after about 150 ms. Similar considerations are valid for the frequency trends: even in this case, only the proposed VVEMF allows for following the grid frequency of 50 Hz with a frequency overshoot of

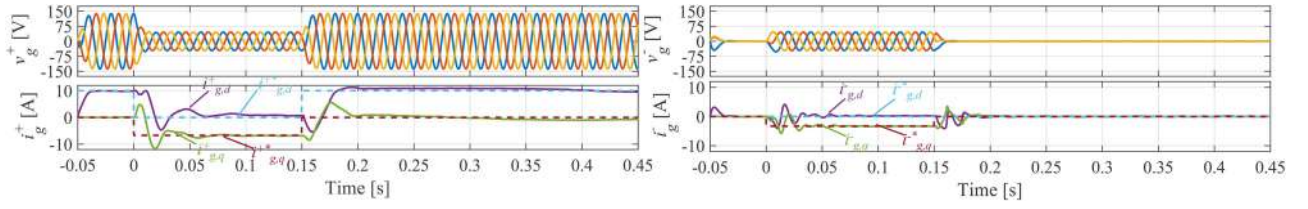


Fig. 19. Experimental positive and negative sequence electrical quantities during a DLG fault ($v_{g,b}$ and $v_{g,c}$ go to zero), $SCR = \infty$.

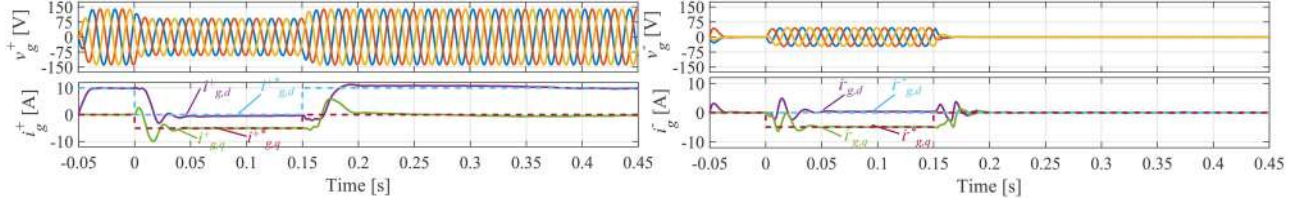


Fig. 20. Experimental positive and negative sequence electrical quantities during a SLG fault ($v_{g,a}$ goes to zero), $SCR = \infty$.

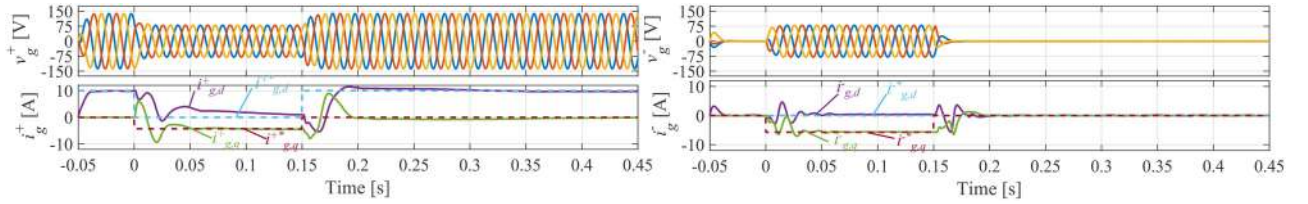


Fig. 21. Experimental positive and negative sequence electrical quantities during a LL fault ($v_{g,b} = v_{g,c}$), $SCR = \infty$.

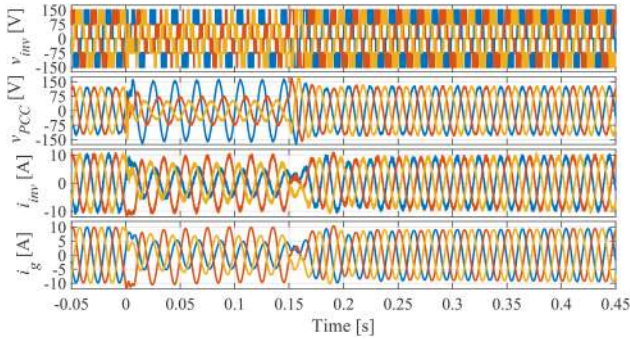


Fig. 22. C-HIL main electrical quantities during a DLG fault ($v_{g,b}$ and $v_{g,c}$ go to zero) with an $SCR = 1.9$.

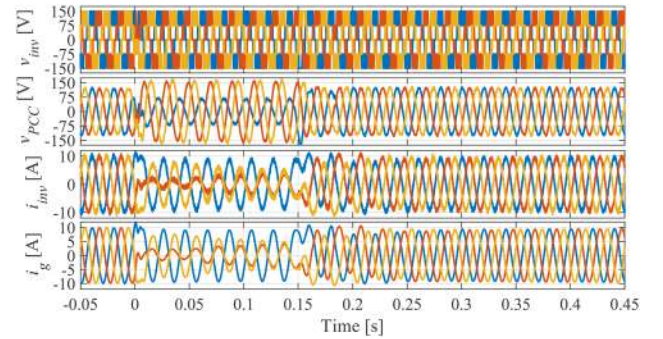


Fig. 23. C-HIL main electrical quantities during a SLG fault ($v_{g,a}$ goes to zero) with an $SCR = 1.9$.

about 1 Hz, while the CL strategy maintains a frequency error of about 0.2 Hz. At the fault clearance, the VVEMF strategy exhibits a lower frequency overshoot (about 1 Hz), compared to the CL method, and nulls the frequency error in about 40 ms. On the contrary, the CL method reaches the grid frequency much more slowly, in about 150 ms. Moreover, looking at the active power and frequency trends, it is evident that the frequency dynamic is always driven by the active power error. Indeed, the proposed method preserves the GFM behavior even during the fault, as expected. Regarding the reactive power trends, at the fault occurrence, the proposed strategy allows for following the reference in about 40 ms, while the CL method reaches the reference in about 100 ms with comparable overshoots. Indeed, only the proposed VVEMF strategy allows for meeting the 50 ms requirement imposed by the grid codes in [5] and [7]. At the fault

clearance, both strategies exhibit similar overshoot. However, the proposed VVEMF strategy exhibits a faster step response, similar to the active power and frequency trends discussed so far. The comparison between the VEMF magnitude trends reported in Fig. 7 clearly explains the main difference between the compared current limiting methods. Indeed, at the fault occurrence, the CL method produces a very slow VEMF amplitude increase, causing a huge increase of the current reference, according to (8), and the adoption of the reference current limiter leads to the windup of the outer loops. Such behavior is evident by looking at the current trends reported in Fig. 8. In detail, although the current references (identified by the dotted lines) are saturated, the outer control loop windup produces a severe inverter- and grid-current overshoot (almost double of the rated current) at the fault occurrence. Moreover, the CL strategy maintains a relevant

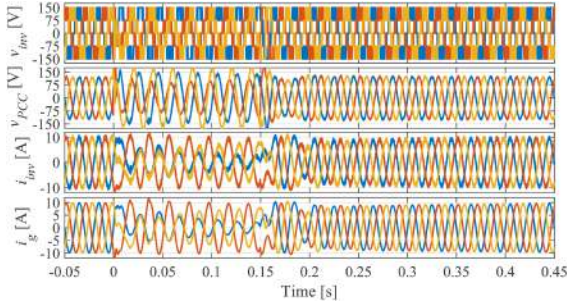


Fig. 24. C-HIL main electrical quantities during a LL fault ($v_{g,b}$ becomes equal to $v_{g,c}$) with an SCR = 1.9.

d -current error during the fault (about 0.5 p.u.) and determines a slow recovery at the fault clearance. Conversely, the proposed strategy instantaneously updates the VEMF through magnitude and phase feedforward terms from the normal to fault operating conditions, as shown in Fig. 7, coherently with the fault active and reactive power reference values. This allows for preventing the outer loop windup, intrinsically limiting the current reference while preserving the GFM behavior and enabling the injection of reactive power during the fault to support the grid. Such features are evident by looking at the inverter- and grid-current trends reported in Fig. 8. With the VVEMF strategy, the dq -currents follow the updated references with a settling time of 40 ms and a negligible overshoot (lower than 1.1 p.u.), while the CL method determines the inverter overcurrent up to 2 p.u. The VVEMF strategy also guarantees good performance at fault clearance. Finally, under strong grid conditions, both compared strategies exhibit good current THD. The same grid voltage reduction is replicated on the experimental setup to validate the real-time simulation results. In this sense, the experimental trends of the active power, reactive power, frequency, and VEMF shown in Fig. 9 reveal nearly identical results in settling time, overshoot, and steady-state error, both at the fault occurrence and clearance, if compared to the C-HIL results shown in Fig. 7. The main electrical quantities, namely the converter-side and grid voltages and the converter-side and grid-side currents, are depicted in Fig. 10. Experimental results show that the proposed VVEMF strategy properly limits the inverter currents during the fault. Moreover, the grid-side current is updated fast enough to follow the new fault power references, and no current distortion worsening is recorded during the fault.

Finally, the proposed VVEMF method is tested by performing a three-phase bolted fault, which represents the worst-case scenario to test the fault current limiting capability of the proposed algorithm. According to Fig. 11, the proposed method exhibits superb current limiting capability, constraining the inverter current to the rated current with an almost null overshoot and extinguishing the transient within 50 ms as prescribed by the grid code. Thus, the proposed current limiting strategy is independent of the voltage amplitude at the PCC.

B. Weak Grid Scenarios (SCR = 4 and SCR = 1.9)

The performance comparative analysis between the proposed VVEMF strategy and by the CL strategy at the grid voltage reduction is replicated under weak grid scenario (SCR = 4),

and main power and electrical quantities are shown in Figs. 12 and 13.

Looking at such figures, it can be noted that the proposed VVEMF strategy still guarantees excellent system performance under weak-grid conditions, with fast and precise current and power step responses. Thus, no relevant differences are highlighted in comparison to the strong grid scenario. Conversely, the CL strategy exhibits a significant performance degradation. In detail, Fig. 13 shows that the CL strategy determines pronounced voltage and current distortion during the fault, resulting in severe overcurrent that goes above 2 p.u. and, consequently, a failure in accomplishing the fault current limiting task. Moreover, Figs. 12 and 13 show a much slower postfault recovery in terms of reactive power and VEMF, whose amplitude continues growing.

To further prove the effectiveness of the proposed strategy, it is tested in an even weaker grid scenario (SCR = 1.9). In detail, the test is performed by reducing the grid voltage to 0 V. Under this condition, the voltage at the PCC drops to approximately 0.5 p.u., which corresponds to the voltage drop across the grid impedance when the rated current flows. This value also represents the minimum voltage at the PCC for such a high grid inductance ($L_g = 23$ mH). Even in this case, the proposed method effectively limits the inverter-side current to the rated value and supports the grid by injecting only reactive power, as shown in Figs. 14 and 15. By comparing frequency and power trends obtained for SCR = 4 and SCR = 1.9, no significant differences in terms of settling time and overshoot are recorded. This behavior is explained by the multiobjective capability of the FCS-MPC, which simultaneously controls the inverter-side current and the capacitor voltage, providing several benefits. In detail, since the capacitor voltage closely approximates with the PCC voltage, regulating this variable allows for effectively shaping the PCC voltage. This feature is particularly beneficial under low SCR conditions, where the PCC voltage strongly depends on the grid current due to the high grid impedance, and the interaction between the injected current and the PCC voltage may lead to oscillatory behavior. Moreover, a high grid inductance due to the grid weakness affects the LCL filter resonance frequency, potentially compromising the GFM inverter stability. However, since the LCL filter dynamic is captured in the control model, the FCS-MPC guarantees intrinsic active damping capability [27], thereby mitigating voltage and current oscillations. These features demonstrate that the proposed control strategy ensures excellent dynamic performance and FRT capability independently of the grid weakness.

VI. CONTROL VALIDATION UNDER ASYMMETRICAL FAULTS

In this section, the current limitation performance and grid code compliance of the proposed fault current limiting strategy are validated under DLG, SLG, and LL faults, which last 0.15 s. Tests are conducted on the experimental setup in a strong grid scenario (SCR = ∞) and in the C-HIL environment under a weak grid scenario (SCR = 1.9).

A. Strong Grid Scenario (SCR = ∞)

Figs. 16–18 show the main electrical quantities during DLG ($v_{g,b}$ and $v_{g,c}$ go to zero), SLG ($v_{g,a}$ goes to zero), and LL

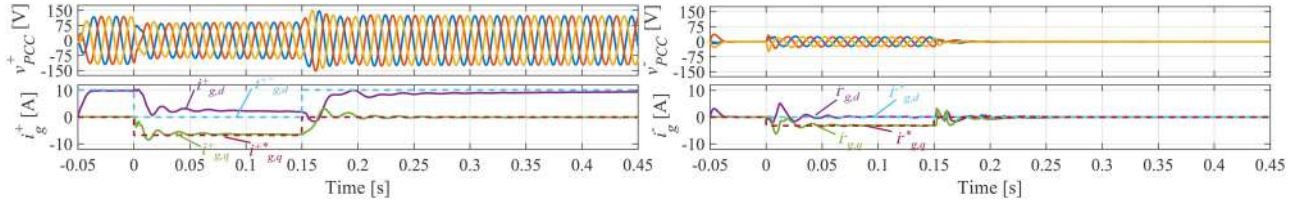


Fig. 25. C-HIL positive and negative sequence electrical quantities during a DLG fault ($v_{g,b}$ and $v_{g,c}$ go to zero) with an SCR = 1.9.

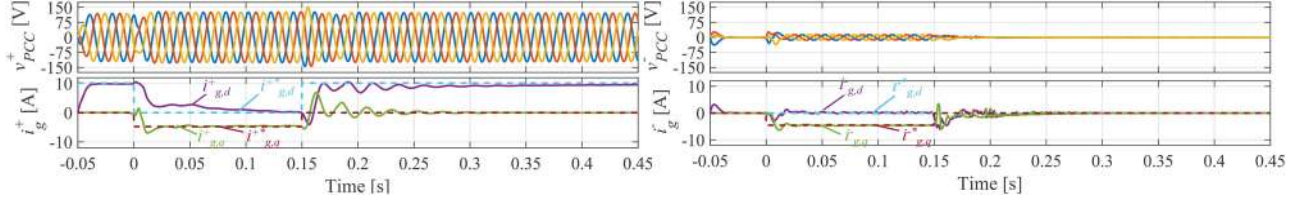


Fig. 26. C-HIL positive and negative sequence electrical quantities during a SLG fault ($v_{g,a}$ goes to zero) with an SCR = 1.9.

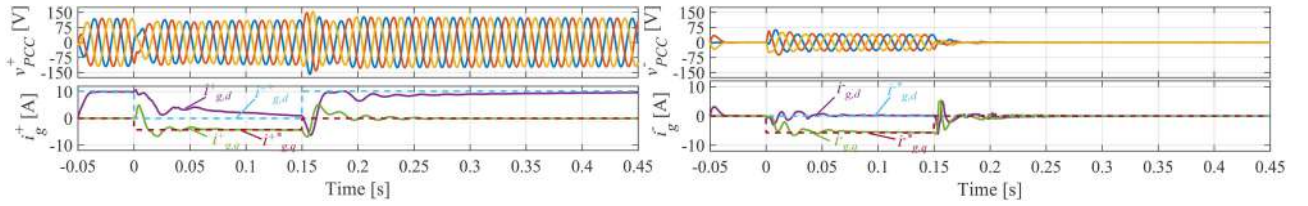


Fig. 27. C-HIL positive and negative sequence electrical quantities during a LL fault ($v_{g,b} = v_{g,c}$) with an SCR = 1.9.

($v_{g,b}$ becomes equal to $v_{g,c}$) faults, respectively. Independently of the considered fault, the proposed method effectively limits the inverter-side current, always being lower than 1.2 p.u. Positive- and negative-sequence grid voltages and currents during the previously mentioned faults are depicted in Figs. 19–21, respectively.

To better investigate the symmetric components dynamic response, the grid side currents and their references are reported in terms of their dq components. It can be noticed that, in all three investigated cases, the proposed method injects the positive- and negative-sequence reactive current prescribed by the grid code in about 50 ms, complying with the settling time grid code requirements of 60 ms [9]. Thus, the proposed method exhibits an excellent FRT capability even under asymmetrical fault conditions, guaranteeing inverter current limitation and positive and negative sequence reactive current injection according to the grid code prescriptions.

B. Weak Grid Scenario (SCR = 1.9)

The same analysis for the strong grid scenario is repeated in the case of the weak grid. In Figs. 22–24 the main electrical quantities in case of DLG, SLG, and LL faults are depicted, respectively. It can be noticed that, although one or more of the phase voltages drop to zero, a nonzero voltage at the PCC is measured. This corresponds to the voltage drop across the line inductance L_g and, therefore, depends on the grid fault current.

Looking at the inverter-side currents, the proposed method can effectively limit the current in all three fault cases, even in a weak grid scenario. The trends of related positive and negative

sequence quantities are depicted in Figs. 25–27 for each fault, respectively. The overall dynamic behavior closely resembles that observed in the strong grid scenario. The only noticeable difference concerns the positive-sequence current, which exhibits a slightly slower transient response due to the lower grid stiffness. However, the reactive current dynamic still complies with grid code specifications, which prescribe a settling time of 60 ms with a tolerated delay of 20 ms. Another difference appears in the positive-sequence postfault operation, where oscillations arise due to the interaction between the injected current and the PCC voltage in the weak grid condition. Nevertheless, these oscillations are effectively damped by the variable postfault virtual resistance introduced in the control strategy.

C. Comparison With Other Existing FRT Strategies

Table II provides a comparative assessment between the proposed VVEMF strategy and existing fault current limiting methods. The comparison shows that most available approaches address only a subset of the requirements of modern GFM converters. While GFM operation preservation and FRT capability under symmetrical faults are commonly achieved, asymmetrical fault management, negative-sequence current control, voltage support according to grid codes, and operation under weak-grid conditions are only rarely addressed. Moreover, several methods exhibit significant transient overcurrents during fault occurrence and clearance (up to 2 p.u.). Conversely, the proposed VVEMF strategy successfully combines all these features while maintaining excellent dynamic performance under both symmetrical and asymmetrical fault conditions.

TABLE II
COMPARISON WITH STATE-OF-THE-ART FAULT CURRENT LIMITING STRATEGIES

	CLB			VIB			VLB			Proposed VVEMF		
	[12]	[13]	[15]	[17]	[18]	[20]	[21]	[22]	[23]	[24]	[25]	
Voltage support during short circuits	NO	NO	YES	NO	NO	NO	YES	YES	NO	NO	NO	YES
GFM behavior during the fault	YES	NO	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
Overcurrent limitation performance	X	X	–	X	XX	XX	X	XX	✓	✓	✓	✓✓
FRT capability under symmetrical faults	✓	✓	✓✓	✓	✓	✓	✓	✓	✓	✓	✓	✓✓
FRT capability under asymmetrical faults	–	✓	–	–	–	✓	✓	✓	–	–	✓	✓✓
Negative-sequence current control	NO	NO	NO	NO	NO	YES	YES	YES	NO	NO	NO	YES
Experimental validation	NO	YES	YES	YES	NO	NO	NO	NO	YES	YES	NO	YES
Performance in weak grid scenarios	✓	–	✓	–	–	–	✓	–	–	–	–	✓✓

Scaled from best (✓✓) to worst (XX), (–) not addressed

VII. CONCLUSION

This article proposes a novel indirect fault current limiting strategy for GFM inverters operating under both symmetrical and asymmetrical grid faults. The proposed approach is based on the coordinated update of the active and reactive power references, computed according to grid-code prescriptions, and the corresponding modification of the VEMF through dedicated feedforward terms. In this way, the inverter current is effectively limited without requiring explicit current-reference or voltage saturation stages, while preserving continuous GFM operation, providing effective voltage support during the fault, and avoiding outer-loop windup phenomena. The effectiveness of the proposed strategy has been validated through C-HIL and experimental tests under symmetrical and asymmetrical grid faults, both in strong- and weak-grid conditions.

The obtained results demonstrate that the proposed method enables the inverter to successfully ride-through symmetrical and asymmetrical grid faults while simultaneously providing the voltage support required by the most up-to-date grid codes through FFCI capability. Moreover, the proposed strategy guarantees effective current limitation, stable operation, and fast dynamic performance even under severe weak-grid conditions, confirming its suitability for future power systems with high penetration of IBRs.

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