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Evaluation of Dynamic On-Resistance and Trapping Effects in GaN on Si HEMTs Using Rectangular Gate Voltage Pulses

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Abstract

Dynamic on-resistance (R_{ON}) of commercial GaN on Si normally off high-electron-mobility transistor (HEMT) devices is a very important parameter because it is responsible for conduction losses that limit the power conversion efficiency of high-power switching converters. Due to charge trapping effects, dynamic R_{ON} is always higher than in DC, a behavior known as current collapse. To study how short-time dynamics of charge trapping and release affects R_{ON} we use rectangular 0–5 V gate voltage pulses with durations in the 1 µs to 100 µs range. Measurements are first carried out for single pulses of increasing duration, and it is found that R_{ON} depends on both pulse duration and drain current I_D, being higher at shorter pulse durations and lower I_D. For a train of five pulses, R_{ON} decreases with pulse number, reaching a steady state after a time interval of 100 µs. The response to a five pulses train is compared to that of a square-wave signal to study the time evolution of R_{ON} toward a dynamic steady state. The DC R_{ON} is also measured, and it is a factor of ten smaller than dynamic R_{ON} at the same I_D. This confirms that a reduction in trapped charges takes place in DC as compared to the square-wave switching operation. Additional off-state stress tests at V_{DS} = 55 V reveal the presence of residual surface traps in the drain access region, leading to four times increase in R_{ON} in comparison to pristine devices. Finally, the dynamic R_{ON} is also measured by the double-pulse test (DPT) technique with inductive load, giving a good agreement with results from single-pulse measurements.

Keywords: GaN on Si high-electron-mobility transistors (HEMTs); dynamic on-resistance; charge trapping and release; current collapse; double-pulse test (DPT); DC stress test

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1. Introduction

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are a hot topic for scientific research and industrial applications due to their capability to drive high current with low dynamic on-resistance (R_{ON}) and to withstand high voltages [1,2]. They are used for high power switching circuits in the electric vehicles automotive industry or for RF applications [3]. However, to cut production cost and to exploit the advantages of integration these GaN HEMTs are grown on Si wafers. As Si and GaN have a 17% lattice mismatch, this leads to a significant concentration of crystal defects in the heterostructure, acting as trap centers for charge carriers [4]. These trapping centers and their relevant effects play an important role in the degradation of dynamic performance and limit long-term reliability of these HEMTs through peculiar failure modes. Updated and comprehensive

reviews on charge carrier trapping and release mechanisms in GaN on Si heterostructure can be found in [5,6].

Figure 1 illustrates the simplified cross-section of a typical normally off p-GaN gate [7] HEMT device with traps distribution and their effects on dynamic electrical parameters. For simplicity, the details of the necessary buffer layer to aid Si to GaN transition and reduce crystal defects concentration during the epitaxial growth are not indicated.

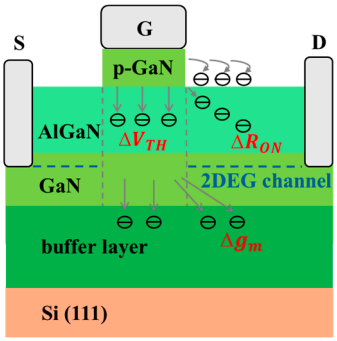


Figure 1. Schematic representation of surface and bulk traps in a normally off p-GaN HEMT affecting threshold voltage V_{TH}, dynamic R_{ON}, and transconductance g_m.

In a hard switching operation at relatively low drain to source blocking voltages V_{DS} (less than 100 V) and drain currents I_D (less than 1 A), as is the case of our study, the horizontal electric field during the off-time and the off-time itself are not sufficient to induce barrier surface/interface trapping in the drain access region [8]. For the same reason, during the off-to-on transition and the on-time, accelerated electrons in the two-dimensional electron gas (2DEG) channel cannot acquire sufficient kinetic energy to overcome the potential barrier and become trapped in the AlGaN barrier of the drain access region, i.e., the generation of hot electrons [9,10] can be ruled out. Hence the main contributions to the observed changes in R_{ON} must be attributed to electrons of the 2DEG channel that become trapped within the channel itself during the on-time together with electrons trapped in the buffer layer during the off-time, both under the gate and in the drain access region [11]. In fact, trapped electrons in the channel are responsible for scattering, decreasing free electrons mobility and leading to an increase in R_{ON}. Trapped electrons in the buffer layer under the channel during off-time can be considered as being located uniformly in the whole device's active area. They also affect the R_{ON}, as well as the threshold voltage V_{TH} and the transconductance g_m, because they act as a back gate that negatively biases the device giving an increased R_{ON} [11].

Of course, during the switching operation, the reverse process also takes place, i.e., the electric field-assisted trapped charge release mostly during the off-time and a dynamic steady state must be established in the device through a dynamic balance between charge trapping and release. Understanding charge trapping and release dynamic mechanisms and their influence on R_{ON} is critical for ensuring long-term reliability and performance stability of these devices.

Datasheets of commercial GaN HEMT devices usually report the DC or static R_{ON} only, but in a switching operation, the dynamic on-resistance R_{ON} is more relevant because it determines conduction losses that limit the power conversion efficiency of high-power switching converters. Dynamic R_{ON} is invariably higher than the static one, leading to an increase in switching and conduction losses and longer switching times. This behavior is also known as a current collapse [12].

In this paper we address the time evolution of R_{ON} of commercial normally off GaN HEMT devices operated in hard switching mode with resistive load using rectangular gate voltage pulses. Measurements are first conducted for single pulses of increasing duration

from 1 µs to 100 µs and then for a train of five pulses to analyze short-time transient switching behavior and to check if and how dynamic R_{ON} evolves with pulse number trough trapped charge accumulation. These results are compared to those of steady-state switching with a square-wave gate voltage at much longer times, and to the DC R_{ON} measured over a time interval of 30 min. To check the possible influence on dynamic R_{ON} of trapped electrons at surface/interface traps in the drain-side access region DC, off-state stress tests are conducted, resulting in an appreciable increase in R_{ON} in comparison to the one of pristine device. Finally, we use the double-pulse test (DPT) method with inductive load to measure R_{ON} and compare results to those for single-pulse measurements. The presented results give useful insights into the short timescale dynamic and steady-state behavior of R_{ON}.

The main advantage of our method, compared to more complex circuits as half and full bridge topologies used in switching converters, is simplicity. However, the latters give more accurate results because the HEMT devices are operated under real load conditions, like those found in electric vehicles with batteries or electric motors.

The paper is organized as follows: Section 2 introduces the materials and methods used for the measurements. Section 3 presents the experimental results discussing their analysis and explanation. Finally, Section 4 highlights some conclusions.

2. Materials and Methods

The circuit used for the measurements is shown in Figure 2. The drain load can be a simple resistor R_D, or an air core inductor shunted by a fast power Schottky diode (MBRS1100) for the measurements conducted by the DPT method. The transistor is a commercial normally off GaN HEMT device produced by ST (SGT120R65AL, 650 V, R_{ON} = 75 mΩ typ., 15 A). The typical threshold voltage is 1.8 V and the absolute maximum rating for the positive V_{GS} is 7 V. Hence, to drive it deeply into the ohmic region without risk of gate junction breakdown, we use rectangular gate voltage pulses having amplitude 0–5 V.

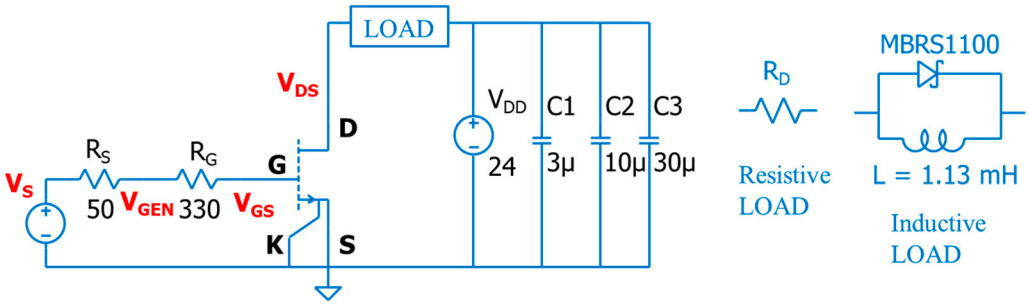
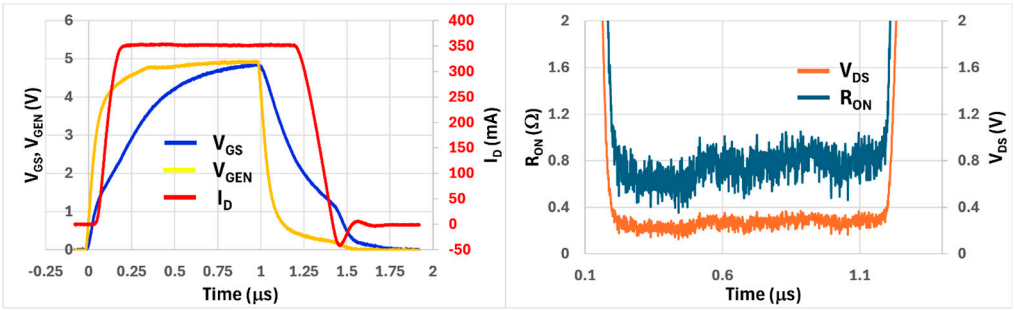


Figure 2. Circuit schematic used for measurements. The drain load can be resistive or inductive for the DPT method.

The rectangular voltage pulses for driving the gate are provided by an arbitrary signal generator (Digilent Analog Discovery 2 multi functions programmable board, recommended output current of 10 mA at ±5 V and maximum absolute rating of 50 mA at ±5.8 V of analog output voltage). The free software WaveForms, which can be downloaded from the Digilent website at https://digilent.com/reference/software/waveforms/waveforms-3/start (accessed on 8 June 2025), is used to generate the rectangular voltage pulses. The gate series resistor is added to comply with the current limit of the arbitrary signal generator. The chosen 330 Ω value ensures a good trade-off between the gate charge/discharge peak current required to the driver and the fast switching time of the GaN HEMT in response to a rectangular gate voltage. We check in advance that even for the minimum rectangular

pulse duration of 1 µs, the V_{GS} reaches 5 V, and the drain current reaches its steady-state value, as shown in Figure 3a.



(**a**) (**b**)

Figure 3. Response to a single rectangular pulse of 1 µs duration for a drain current of 350 mA. (**a**) gate-source voltage V_{GS}, generator voltage V_{GEN}, and drain current I_D. (**b**) dynamic R_{ON} and drain-source voltage V_{DS}.

For the case of resistive drain load, the voltages across the gate and drain resistors, whose value is accurately measured in advance, are acquired by a four channels oscilloscope (Tektronix MSO54) through 1X accurately compensated probes. The drain current is calculated as $I_D(t) = [V_{DD}(t) - V_{DS}(t)]/R_D$. The dynamic on-resistance R_{ON} is calculated as $V_{DS}(t)/I_D(t)$, giving the time evolution during the on-time. Where single values of R_{ON} are quoted, these are the nominal resistance values taken, for convenience, in correspondence to 90% of the on-time pulse duration. The switched drain current can be set by changing V_{DD} (6 V or 24 V) and R_D to obtain I_D ranging from 100 mA to 750 mA.

For the case of the DPT method with inductive load, the drain current $I_D(t)$ and the inductor current $I_L(t)$ are measured by means of two current probes, Teledyne LeCroy T3CP100-2, whose output is connected to the Tektronix MSO54 oscilloscope. The dynamic on-resistance R_{ON} is again calculated as $V_{DS}(t)/I_D(t)$.

As during the on-state of the device V_{DS} can be in the hundreds of mV range, the oscilloscope is set to high-resolution mode, exploiting the maximum available bit depth (16 bits). Furthermore, to reduce noise, the bandwidth is limited for all four channels of the oscilloscope. For practical convenience, the measurement circuit is implemented on a breadboard, ensuring the wire connections are as short as possible to minimize parasitic effects. Before each measurement, the gate and drain terminals of the device are shorted to the ground for two minutes to release any trapped charge leftover from the previous measurement and re-establish pristine condition avoiding the presence of any form of 'memory effect.' Measurements are conducted on several SGT120R65AL devices but for consistency the reported results are for the same single device. The voltage measurement errors can be assumed to be 5%, but for better clarity, error bars are not indicated in the graphs, displaying single numerical values. A picture of the measurement setup and further practical details are given in [8].

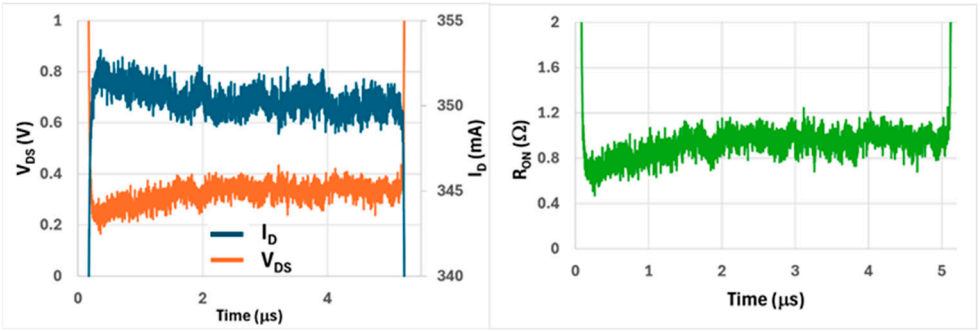
3. Results and Discussion

The response to a single rectangular voltage pulse of 1 µs duration, that is, the minimum duration used for the measurements, for resistive load and I_D = 350 mA is shown in Figure 3a.

The Vs (see Figure 2) rise/fall times under no load can be assumed to be 100 ns and its R_S = 50 Ω internal output series resistance, set by an external jumper on the Analog Discovery 2 board, adds to the 330 Ω gate resistor. Hence the total resistance seen by the gate capacitance is 380 Ω. The 50 Ω internal output resistance gives V_{GEN} smoothed out

rise and falling edges. It can be noticed that V_{GS} still reaches 5 V at the end of the pulse and that the I_D trace switches very abruptly and has a flat top meaning that I_D can reach its steady-state value. The ringing on the falling edge of I_D is due to unavoidable parasitic inductive effects, but its maximum amplitude of about 50 mA is small in comparison to the switched I_D = 350 mA. This demonstrates that by keeping wire connections on the breadboard as short as possible, parasitic effects are kept to a minimum. Figure 3b shows that V_{DS} also switches quite abruptly and has an almost flat bottom. The ratio $V_{DS}(t)/I_D(t)$ gives the dynamic $R_{ON}(t)$ trace that has a slightly increasing trend and exhibits some noise. The quoted value for R_{ON} is the average value taken at 90% of $R_{ON}(t)$ duration, that in this case, is 0.8 Ω.

Figure 4 shows the time evolution of R_{ON} together with I_D and V_{DS} for a longer 5 µs pulse duration and again I_D = 350 mA. An initial increasing trend with time for R_{ON} is evident and then it reaches a steady state. This behavior can be explained with the fact that a 5 µs pulse duration is comparable to the short timescale for trapping effects of electrons in the 2DEG channel to take place and be effective.



(**a**) (**b**)

Figure 4. Response to a single rectangular pulse of 5 µs duration for a drain current of 350 mA. (**a**) drain-source voltage V_{DS} and drain current I_D and (**b**) dynamic R_{ON}.

In fact, trapping of electrons in trap centers located in the 2DEG channel are responsible for scattering, decreasing free electrons mobility and channel conductivity and resulting in current collapse with an associated increase in R_{ON}. On the other hand, the release of electric field-assisted electrons from these centers must be associated with a current collapse reduction and a decrease in R_{ON}. When an equilibrium between trapping and release is established, then R_{ON} should remain constant with time. In addition, the ratio of empty to filled traps must be higher at low I_D current, because electron trapping is proportional to the free charge carrier concentration while electron release is not dependent on it [13].

The values of R_{ON} as a function of pulse duration and for different drain currents are reported in Figure 5. It can be noticed that at low currents of 100 mA and 350 mA, trapping effects with increasing R_{ON} prevail for short pulse durations (1 µs and 5 µs) and then for longer pulse durations, R_{ON} decreases steadily. However, for a high current of 750 mA, R_{ON} decreases steadily with pulse duration. This behavior can be explained by the fact that with a finite concentration of traps in the 2DEG channel, the capture probability increases with increasing free carrier concentration [13], i.e., drain current, and hence the average trapping time, becomes shorter than 1 µs. R_{ON} at 750 mA reaches a constant value at 10 µs pulse duration, while for lower currents it takes 50 µs, which is five times longer. This means that the average release time is longer for a lower I_D. R_{ON} at 100 mA has the lowest constant value, because the ratio of empty to filled traps is higher at low current. When the device is operated at much higher switching currents, these effects are less evident because the drain current plays an important role in the trapping process, leading to higher R_{ON} values.

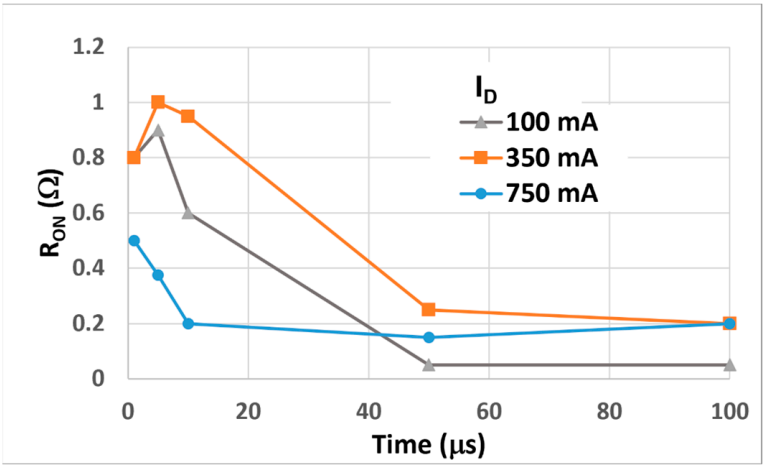
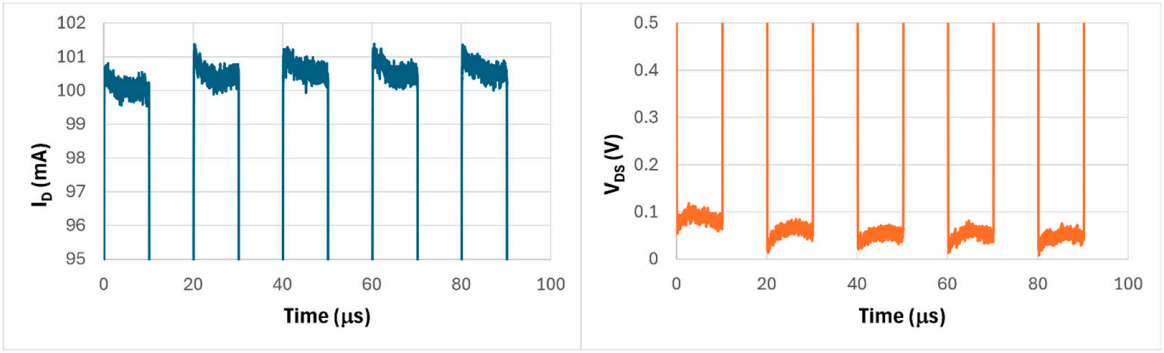


Figure 5. Dynamic R_{ON} as a function of pulse duration for I_D = 100 mA, 350 mA, and 750 mA.

To study the cumulative effect of the traps on drain current conduction and R_{ON}, we use a train of five gate voltage pulses with 50% duty cycle. An important difference with the single-pulse case is that during each on-to-off transition, electrons in the channel are pushed towards the buffer layer where they become trapped by bulk traps. When the device is driven back to the on-state by the next pulse of the train, these trapped electrons act as a "back gate" with negative bias, affecting threshold gate voltage V_{TH}. Bulk traps in the buffer layer can be assumed to be distributed in the whole device active area; hence, the "back gate" is extended in the gate-to-drain region as well, and this affects also dynamic R_{ON} [11].

The time evolution of I_D and V_{DS} during a train of five pulses of 10 µs duration each, corresponding to a 50 kHz square wave, is shown in Figure 6 for a nominal drain current of 100 mA. The expanded vertical scale reveals that the drain current increases and the drain voltage decreases with pulse number, both reaching a sort of steady-state regime starting from the third pulse. Similar behavior is observed at I_D = 350 mA but not at I_D = 750 mA. The dynamic R_{ON} vs. pulse number reported in Figure 7 for comparison at I_D = 100 mA, 350 mA, and 750 mA is almost constant with the pulse number for I_D = 750 mA. At lower currents, R_{ON} is decreasing with pulse number, a behavior like the case of single voltage pulses reported previously in Figure 5.



(**a**) (**b**)

Figure 6. Response to a train of five pulses of 10 µs duration each for nominal I_D = 100 mA. (**a**) Drain current I_D, (**b**) drain-source voltage V_{DS}.

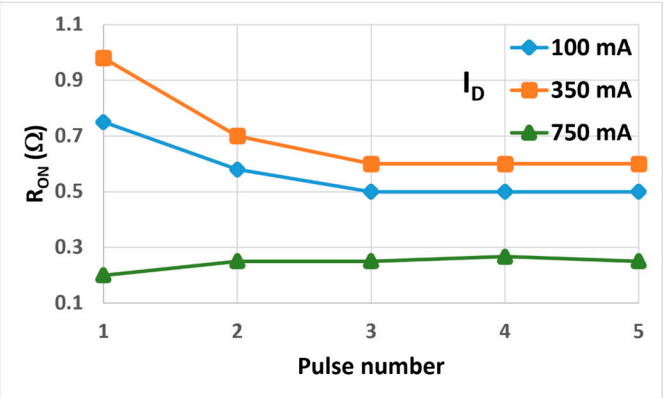
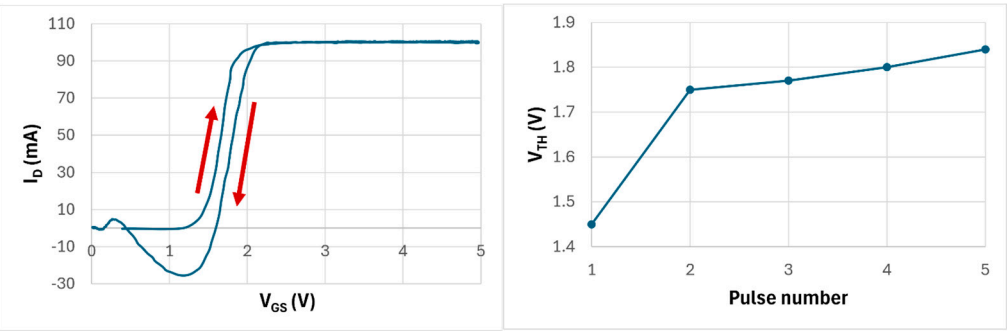


Figure 7. Dynamic R_{ON} vs. gate voltage pulse number for I_D = 100 mA, 350 mA, and 750 mA. The pulse duration is 10 µs.

It is worth noticing from comparing Figures 5 and 7 that R_{ON} for the fifth pulse of the train is always higher than the one for an equivalent single pulse with 100 µs duration. This means that the release of electrons is less effective during a switching operation at higher repetition frequency.

The effect of the traps on the threshold gate voltage V_{TH} vs. the pulse number is also investigated. By plotting the drain current as a function of the gate voltage for the same pulse, the corresponding graph shows a sort of hysteresis between the rising and falling edges of the drain current, as shown in Figure 8a for I_D = 100 mA, where the negative values of I_D during the falling edge are due to parasitic inductive effects.



(**a**) (**b**)

Figure 8. (**a**) Current hysteresis I_D vs. V_{GS} between rising (up arrow) and falling (down arrow) edges at 100 mA, (**b**) threshold voltage V_{TH} for the rising edge at 10 mA vs. pulse number.

The threshold gate voltage V_{TH} taken at I_D = 10 mA during a rising edge vs. the pulse number is reported in Figure 8b and shows an increase from 1.45 V to 1.84 V with the pulse number. This behavior is to be expected and can be explained by the electrons that, during the off-time between pulses, are pushed down towards the substrate where they become captured by traps in the buffer layer under the channel. These can act as a lower back gate equivalent to a negative bias, ultimately increasing the V_{TH} needed for I_D = 10 mA during the falling edge of each pulse. These traps can be considered filled after the fourth pulse.

When used in real switching applications, the GaN HEMT device is driven by a square-wave voltage and reaches a dynamic steady-state equilibrium between on and off states. In this situation a different ratio of empty to filled traps can be expected, resulting in different R_{ON} values as compared to the ones reported in Figure 7 for the case of a five pulses train. To check this, we drive the gate with a 50 kHz square wave (same period and duty cycle as the five pulses train) and evaluate R_{ON} after 1, 10, and 30 min after the application of

the driving gate voltage and for different nominal I_D. The measured R_{ON} values, shown in Figure 9, are pretty much constant with time. This means that the dynamic steady state is reached at most after 1 min with a new ratio of empty to filled traps established both in the 2DEG channel and in the buffer layer underneath.

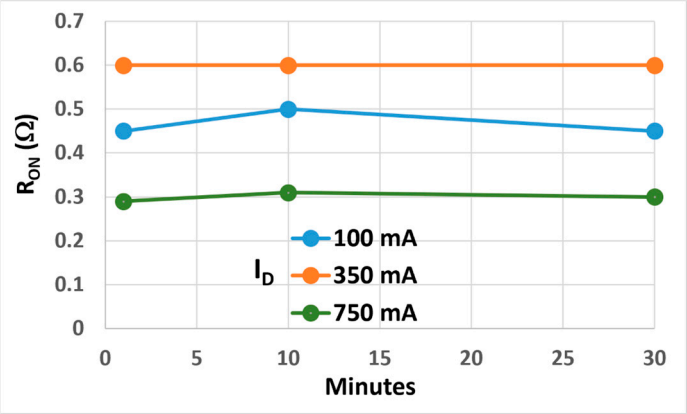


Figure 9. Dynamic R_{ON} for a square-wave gate voltage measured at for different I_D values.

It is worth noticing that the R_{ON} values are different than the ones reported in Figure 7 for the fifth pulse of the five pulses train case. In comparison to Figure 7, R_{ON} is lower (higher empty to filled traps ratio) at I_D = 100 mA, almost the same at 350 mA, and higher (trapping by traps in the channel is stronger) at 750 mA. Moreover, dynamic R_{ON} values at the steady state reported in Figure 9 are at least four times higher than the DC values reported in the SGT120R65AL datasheet (0.075 Ω at low I_D and V_{GS} = 5 V). This proves that the dynamic R_{ON} is always higher than in DC, with associated switching losses that are more than expected from calculation based on DC R_{ON} values.

As a further check we measure the DC R_{ON} using a single long pulse of 30 min duration. The influence of thermal effects due to Joule heating of the drain power resistor load are minimized by mounting the resistor on a suitable heatsink. $R_{ON}(t)$ for 100 mA and 350 mA drain current is reported in Figure 10. The trace for 100 mA is affected by noise but shows an almost zero average, the exact, very small DC R_{ON} value below the sensitivity that can be achieved by the oscilloscope. At 350 mA the average DC R_{ON} is below 0.1 Ω, a factor of six smaller than the square-wave dynamic R_{ON} value at the same drain current. This is due to an increased ratio of empty to filled traps in the channel, another evidence that electrons release increases with pulse duration.

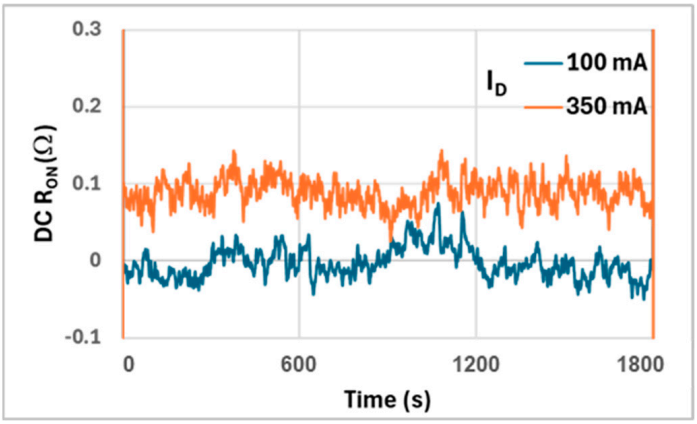


Figure 10. DC R_{ON} vs. time for a single pulse of 30 min duration at I_D = 100 mA and 350 mA.

To check whether surface/interface traps are present in the gate to drain region of the HEMT device under study, off-state DC stress tests are conducted at V_{DS} = 55 V for 1 min, 10 min, and 30 min, with the gate terminal left floating. The small off-state leakage drain current flowing together with the high, horizontal electric field generated by V_{DS} on the drain side of the gate can promote trapping of electrons coming in the barrier layers and interfaces in the drain access region [14]. These off-state stress tests are non-destructive and repeatable with no creation of permanent defects, such as those caused by the inverse piezoelectric effect at very high V_{DS} when applied, even for relatively short times [15–17]. A subsequent single square pulse applied immediately after the stress test finds these trapped charges giving an increased and hence degraded dynamic R_{ON}.

For 1 min and 10 min off-state stress durations, no appreciable difference in dynamic R_{ON} with the pristine device is observed. On the contrary, after 30 min, the stressed device exhibits an appreciable degradation in its dynamic R_{ON}, as shown in Figure 11 for the same off-stressed and pristine (unstressed) device at a drain current of 750 mA, probed with a single pulse of 50 µs duration. It can be noted that the R_{ON} of the stressed device is about four times higher than the one of the unstressed devices. This result confirms the presence of residual surface/interface traps in the barrier layers and highlights that the adopted passivation techniques are unable to fully neutralize these traps.

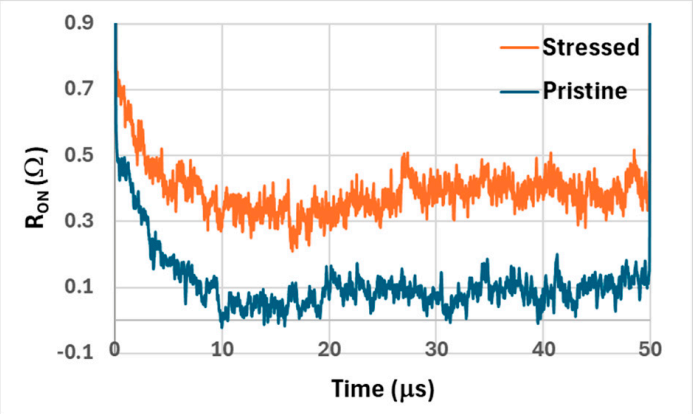
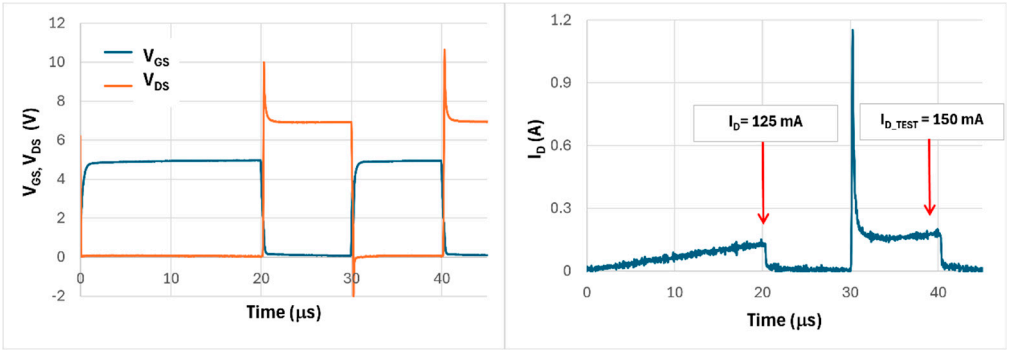


Figure 11. Dynamic R_{ON} of the same device before (pristine) and after 30 min of off-state stress at V_{DS} = 55 V, using a 50 µs single pulse and I_D = 750 mA.

The double-pulse test (DPT) is a technique useful for testing high power switching devices driving inductive loads, as in the case where the load is made up of the windings of an electric motor. The circuit schematic for the DPT is the same as the one shown in Figure 2 but with inductive load on the drain terminal. The method has established itself as an industry standard, to the point that dedicated software programs for the oscilloscope are available to extract and measure all the switching parameters of the transistor device with a single measurement [18].

In the DPT, the gate of the HEMT is driven by two rectangular voltage pulses (0–5 V in our case) separated by an off-time interval, as shown in Figure 12a. During the first pulse, also called "storage pulse", which is usually the longer one, the inductor is charged at constant voltage, hence, linearly increasing the current and storing magnetic energy in its internal volume. The second one is the "test pulse" and it is usually shorter than the storage pulse. The measurement and extraction of all the relevant switching parameters of the HEMT device are relative to the test pulse [19,20].



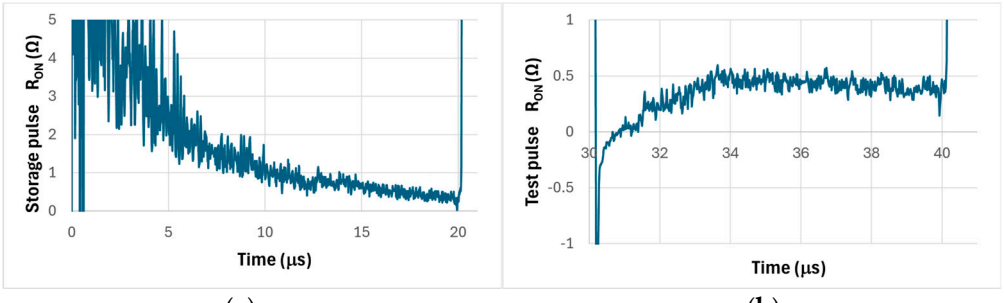
(**a**) (**b**)

Figure 12. Relevant voltages and drain current traces for the DPT method at nominal I_{D_TEST} = 150 mA. (**a**) Double pulse of the gate voltage V_{GS} and drain-source voltage V_{DS} and (**b**) drain current I_D.

In the DPT circuit schematic shown in Figure 2, the flyback power Schottky diode, connected in parallel with the inductor, reduces voltage overshoot across the inductor load during the on-to-off transitions, limiting the V_{DS} across the switching device during the off-time and providing also a very short reverse recovery time. To prevent magnetic saturation, we use an air core inductor whose value is chosen for the desired drain current at the end of the storage pulse. The DPT measurements are conducted for drain current I_{D_TEST} of the test pulse, ranging from 150 mA to 600 mA by changing the storage pulse duration and the drain supply voltage. The off-time and test pulse durations are both kept at 10 µs. The inductor value is accurately measured in advance as being L = 1.13 mH with an R_{series} = 1.4 Ω.

The relevant traces of V_{GS}, V_{DS}, and I_D for 20 µs storage pulse, 10 µs off-time, and 10 µs test pulse durations are reported in Figure 12. The spikes in the V_{DS} trace are a signature of a time derivative effect due to a parasitic series capacitive coupling. The drain current in Figure 12b linearly increases with time during the storage pulse and it goes to zero during the off-time interval. At the rising edge of the subsequent test pulse there is a pronounced drain current spike. It is caused by the parasitic capacitive coupling of the current probe. These parasitic effects do not affect the accuracy of the DPT measurement, as we limit the R_{ON} extraction to the final part of the charging and test pulses.

The dynamic R_{ON} during the storage pulse, shown in Figure 13a, decreases with time, attaining a value of about 0.4 Ω at the end of the pulse. The dynamic R_{ON} for the test pulse, shown in Figure 13b, also obtains a very close value to 0.4 Ω at the end of the pulse.



(**a**) (**b**)

Figure 13. R_{ON} vs. time in the DPT measurement. (**a**) R_{ON} during the storage pulse, (**b**) R_{ON} during the test pulse.

The dynamic R_{ON} vs. I_D measured with the DPT method for the test pulse at 90% of its duration is compared to a 10 µs duration single-pulse measurement in Figure 14. It can be noted that the R_{ON} measured by the DPT method decreases with I_D, a further proof

that the ratio of trapped to free electrons in the channel becomes smaller at higher drain currents. In addition, the R_{ON} values are lower than the ones for 10 µs single rectangular pulses at the same I_D (see Figure 5) because the DPT method is equivalent to the application of two V_{GS} pulses. Only at high I_D = 750 mA, where the ratio of trapped to free electrons in the channel becomes smaller, does the R_{ON} for the single pulse and DPT become quite close to each other.

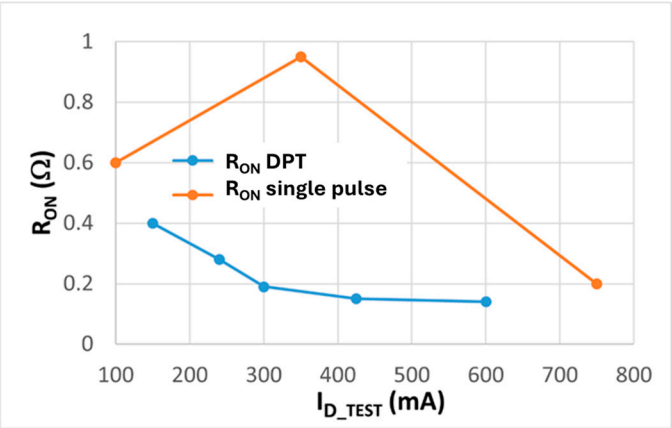


Figure 14. Dynamic R_{ON} vs. I_D measured for 10 µs test pulse of the DPT method compared to 10 µs single-pulse measurements.

4. Conclusions

Time domain measurements at relatively low I_D and blocking voltage V_{DS} allow us to study the degradation mechanisms of dynamic R_{ON} in commercial, normally off GaN on Si HEMT devices due to electron traps located in the 2DEG channel and in the buffer layer underneath. With single rectangular voltage pulses, the release of trapped electrons that is responsible for a decreased R_{ON} depends on the pulse duration as well as the drain current. At I_D = 750 mA, trapping effects are dominant on a time scale below 1 µs, while for lower I_D, the time scale is up to five times longer at 5 µs. Measurements of dynamic switching with a train of five pulses and a square wave show the role of cumulative effects with lower dynamic R_{ON} values as compared to the ones for single pulses. Measurements with longer pulses up to 30 min duration operate the HEMT in DC, where release mechanisms are at their maximum, giving a very low R_{ON} of about 100 mΩ at I_D = 350 mA.

Devices subjected to an off-state stress test have an increased R_{ON} up to four times the one of pristine device, demonstrating the presence of surface/interface traps in the drain access region.

Finally, the values of R_{ON} measured by the DPT method show a decrease with I_D with values of about 150 mΩ for currents above 350 mA, demonstrating good agreement with results from single-pulse measurements.

In summary, the presented results give useful insights into the short timescale dynamic and steady-state behavior of R_{ON} during a hard switching operation but highlight a limited device ability to maintain operational performance after prolonged off-time electrical stress. To improve the reliability and performance stability of GaN on Si HEMT devices for high-frequency and power applications, a reduction in defects and traps concentration of the GaN heterostructure, together with advanced device structures and processing techniques, is crucial and must be pursued.

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Abbreviations

The following abbreviations are used in this manuscript:

HEMT	High-Electron-Mobility Transistor
R_{ON}	Dynamic Conduction Resistance
DC R_{ON}	Static Conduction Resistance
DPT	Double-Pulse Test
2DEG	Two-dimensional Electron Gas

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