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Advanced Model Predictive Control of Cascaded H-Bridge-fed Drives for E-Mobility Applications

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Preface

This research activity is aimed at obtaining the academic degree of Philosophiæ Doctor (Ph.D.) in Energy and was carried out at the Sustainable Development and Energy Saving Laboratory (SDESLAB) and at the Laboratory of Electrotechnical Applications (LEAP) of the University of Palermo, Palermo (PA), Italy, from November 1, 2021, to October 31, 2024.

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The author of this work thereby declares that this thesis represents his unaided work, Parts of this dissertation have been published in international journals and/or conference articles (see list of the author publications at the end of the thesis).

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Introduction

1. Electric Vehicles: Potentialities, Limits, and Market Trends

Energy conservation and sustainable development are indispensable pillars in addressing the climate emergency. In this context, the transportation sector holds a pivotal role. Electric Vehicles (EVs) and Hybrid Electric Vehicles (HEVs) represent the future of the transportation sector; it is predicted that 54% of new vehicles sold by 2040 will be electric [1]-[2]. In particular, electric vehicles are going to replace internal combustion engine vehicles due to the several advantages they offer, i.e., reduction in greenhouse emissions, reduced reliance on fossil fuels, and benefits for both the electric grid and the customers [3]. In detail, a full-electric vehicle does not produce emissions during its use, and energy production to charge its battery systems determines greenhouse gas emissions about 50% lower than those produced by an internal combustion vehicle.

On the other hand, long charging time and low maximum driving range of battery-powered electric vehicles, trucks, and buses before recharging are still the biggest challenges that are impeding the fast growth of transportation electrification [4]. To overcome these limits, the market trend is to increase the battery pack-rated voltage from 400 V to 800 V, up to 1.2 kV [5]-[6]. Such a choice enables Extreme Fast Charging (XFC) and implies advantages such as the reduction of the cable cross-sections and weight, and the reduction of the inverter conduction losses. On the other hand, considering a standard Two-Level Voltage Source Inverter (2L-VSI)-based powertrain, whose block scheme is shown in Fig. 1, higher DC-link voltage implies higher dv/dt on the inverter voltage waveforms and higher Common Mode Voltages (CMVs), that produce electromagnetic interferences (EMIs) and can reduce the motor lifetime by damaging the windings, insulation, bearing balls, or rollers [7]. Concerning the switching device, a higher DC link voltage determines an increase in their cost and a reduction in their maximum switching frequency; moreover, it implies higher switching losses that usually outweigh the reduced conduction losses, thus reducing the

overall inverter efficiency [8]. Finally, to increase system reliability, multiple power switching devices are connected in parallel for each switch [1]-[2]. As a consequence, although a high number of power switches are employed in the inverter topology, the 2L-VSI carries out non-optimal voltages and currents harmonic content and Total Harmonic Distortion (THD).

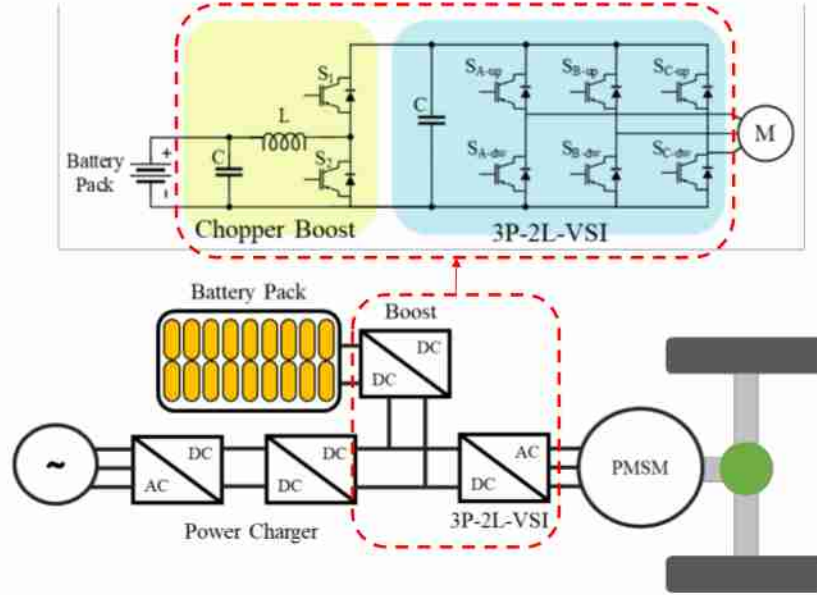


Fig. 1: Standard electric powetrain block scheme.

2. Multilevel Inverters in the E-Mobility Sector

In this context, Multilevel Inverters (MIs) represent a valid solution that allows for overcoming the limits related to traditional 2L-VSIs and maximizing the powertrain performance. According to [9]-[11], MIs can be considered a mature and proven technology, that successfully entered the industry. They are commercialized in standard and customized products that power a wide range of applications, such as compressors, extruders, pumps, fans, grinding mills, rolling mills, laminators, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, reactive power compensation, marine propulsion, High-Voltage Direct-Current (HVDC) transmission, hydro pumped storage, wind energy conversion, and railway traction.

Due to the higher number of available voltage levels, MIs can generate voltages with very low harmonic distortion and very low dv/dt . This leads to numerous benefits in the powertrain: it is possible to drastically reduce the switching frequency while ensuring low voltages and currents harmonic content. Moreover, the reduced dv/dt allows a drastic reduction of e EMI issues and also increases the reliability of the powertrain by reducing the stress on motor windings and on the bearing balls and rollers.

The higher number of voltage levels is achieved by employing more complex inverter topologies that require a higher number of power switches. This could potentially increase the cost of the inverter. However, since each power switch is subject to a portion of the DC link voltage, it is possible to employ low-voltage power switches, which are less expensive and subject to reduced voltage stress. This eliminates the need for complex series-parallel configurations, enhancing reliability and extending component lifespan. This feature also impacts the inverter efficiency: in detail, although the number of employed power switches is higher than a 2L-VSI topology, the reduced voltage applied to each power switch, together with the possibility of reducing the switching frequency, allows for reducing conduction and switching losses on the device, leading to an increase in the converter efficiency. Finally, as mentioned in [12], adopting an MI topology also impacts the battery pack design, leading to an overall reduction in the powertrain cost.

3. Cascaded H-Bridge Inverter: Features and Current Applications

According to [13]-[14], MIs are classified into single and multiple DC source topologies. The former group includes the Neutral-Point Clamped (NPC), the Flying Capacitor Inverters (FCI), and the Modular Multilevel Converter (MMC); the latter includes the Cascaded H-Bridge (CHB) inverter. The previously discussed MI topologies represent the most commonly adopted ones in both the industrial and academic sectors.

Among them, CHB seems the most interesting and promising MI topology for electric traction and e-mobility applications. Its distinctive feature, if compared to other MI topologies, deals with its modular structure. Indeed, it is composed of several H-Bridge (HB) modules, connected in a cascaded fashion per each phase. Its modular structure enables the generation of high-output voltages from a low-voltage DC link and power switches. For the same reason, many voltage levels can be easily achieved, significantly reducing both voltage and current THD, and avoiding bulky and expensive filters. Moreover, unlike other multilevel topologies, CHB inverters do not require complex voltage balancing mechanisms for the DC link capacitors, since each HB cell operates independently, simplifying the control and reducing the risk of capacitor voltage imbalances [9]-[11]. For a given number of voltage levels, all the discussed MI topologies require the same number of power switches. However, the CHB requires no passive components (i.e., floating capacitors and diodes). Last but not least, CHB exhibits a high degree of redundancy, that enables fault-tolerant operation, through the proper design of fault-tolerant control algorithms.

Its modularity and scalability make the CHB inverter the preferred choice in high-voltage high-power applications, such as Flexible AC Transmission Systems (FACTS), Static Compensators (STATCOM), Dynamic Voltage Restorers (DVRs), Unified Power Flow Controllers (UPFC) and photovoltaic energy generation [15]-[22].

CHB is being adopted also in medium-voltage high-power industrial electric drives [23]-[25]. In detail, in the range of 4.16-13.8 kV, CHB-based electric drives result in being the most efficient, if compared with other MI topologies, regardless of the adopted semiconductor technology.

4. Cascaded H-Bridge Benefits in the E-Mobility Sector

By analyzing the scientific literature reported so far, it emerges that the main drawback related to the CHB inverter in most of the discussed applications is linked with the necessity of isolated DC sources. Indeed, a transformer with multiple secondary windings is required to guarantee HB module DC links galvanic insulation. Such a solution drastically affects the system bulk, weight, and cost. On the contrary, when modular voltage sources are available, as in the electric mobility sector where a battery pack is used, the CHB inverter offers some new and unique possibilities: firstly, by splitting the battery pack into several submodules, as it is illustrated in Fig. 2, the CHB can be integrated with the powertrain without adopting bulky transformers or intermediate DC-DC conversion stages, reducing the system cost and complexity, and increasing the powertrain efficiency. Moreover, the CHB topology can be exploited to realize an active battery submodules State of Charge (SoC) control, facilitating the voltage equalization of each source. Extending this concept, isolated DC sources allow the exploitation of different energy sources (e.g., batteries, supercapacitors, fuel cells), thus obtaining a hybrid energy storage system characterized by both high energy and power density [26]. This would guarantee excellent powertrain performance and at the same time extend the useful life of the battery pack, which would no longer have to deal alone with the power peaks required by the load. In addition, the CHB easy maintenance related to its modular structure and its fault-tolerant capability related to its states redundancies represent attractive features in the e-mobility sector. In detail, the presence of redundant states in the converter can justify the transition from a 2L-VSI to MIs, acquiring a smaller number of redundant devices but achieving the same reliability objective through a control logic capable of identifying the fault condition and reconfiguring the system. According to the discussion carried out so far, CHB inverter represents an appealing alternative to the traditional 2L-VSI also in the e-mobility sector, especially for military combat vehicles and heavy-duty trucks, since it facilitates using higher voltage motors with low-voltage power

switches and facilitates the management of the large number of battery cells. Despite the advantages and unique possibilities that CHB inverters offer, CHB-based powertrains are poorly investigated in the scientific literature.

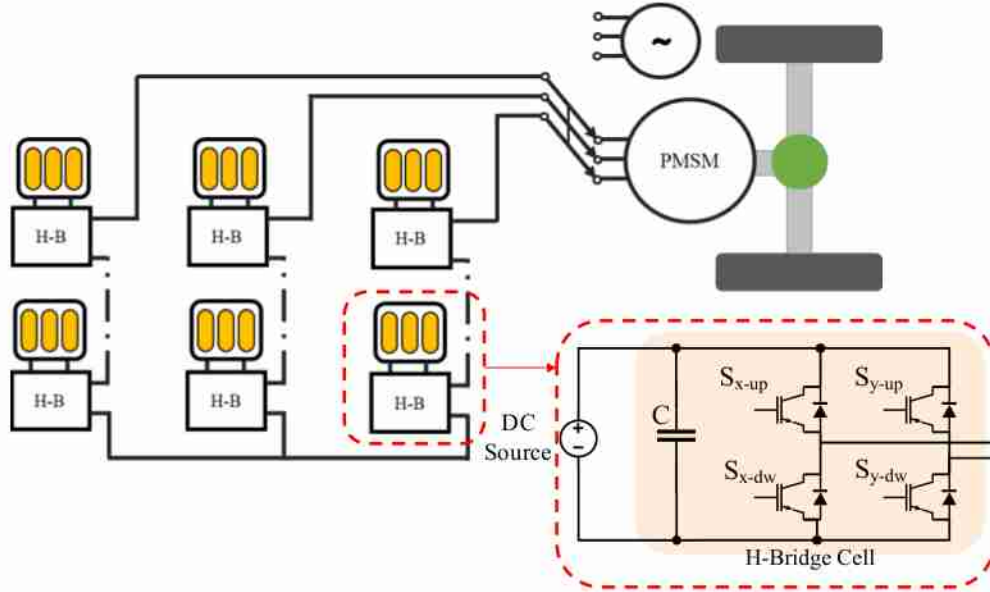


Fig. 2: CHB-based electric powertrain block scheme.

Authors of [26] present a CHB-based motor drive system with integrated segmented energy storage. In detail, it can achieve an effective real power voltage balancing distribution between the energy storage and the electric motor, by an autonomous power regenerative control system. The proposed energy storage voltage balancing enables not only the voltage harmonic compensation but also real power compensation during the acceleration and deceleration modes of the motor. In [27], a hybrid CHB motor drive direct torque control scheme for EVs or HEVs is proposed. Its main achievements are a significant reduction in the torque ripple, sinusoidal output voltages and currents, lower switching losses, and high-performance torque and flux regulation. In [12], a detailed comparison between traditional 2L-VSI, both with IGBT and SiC MOSFET power switches, and a SiC-MOSFET-based CHB inverter for EVs applications is presented. In detail, the comparison is carried out both in terms of converter efficiency and cost. It emerges that the traditional 2L-VSI efficiency drastically decreases at partial load working conditions, considerably deteriorating the overall efficiency, due to the fluctuating power demand of vehicles over the driving cycle. On the contrary, the CHB inverter guarantees a very high efficiency almost in every working condition. In terms of cost, the cost of the CHB inverter is in the middle between the IGBT-based and the SiC MOSFET-based 2L-VSIs. However, if the cost of the overall powertrain is considered, the CHB-base powertrain results in being the cheapest, since the CHB

topology drastically affects the battery pack design, which is the most expensive part of the whole powertrain.

A similar analysis is carried out in [28]: in detail, the optimal number of cascaded HB modules is investigated, finding that four cascaded modules per phase results in the most economical solution, independently of the adopted power switch technology.

In [29], a review of the latest research contributions regarding the evolution of circuit topologies, operational challenges, control schemes, and fault-tolerant strategies of the MMCs in the field of electric transportation is presented. In detail, most of the discussed applications deal with rail power supplies such as static frequency converters and railway power conditioners. On the contrary, it is underlined that the adoption of MMC and CHB inverters in traction drive applications is an open topic, regarding both the adoption of the optimal MI topology and the control and modulation strategy design, especially considering that the employed power electronics can be reutilized to implement an on-board power charger.

Scientific literature underlines some challenges to be faced: first, the converter weight and volume, and, as a consequence, the necessity of integration with the battery pack, to minimize the powertrain volume; second, the control complexity with respect to a traditional 2L-VSI; third, the converter impact on the battery module lifetime. In detail, the lack of an intermediate DC-DC converter between the inverter and the battery on a side can reduce the powertrain cost, weight, volume, and hardware complexity, but on the other side, can accelerate the reduction of the State of Health (SoH) of the battery, however, this is an open topic. In this analysis, it is necessary to consider that an increment in the CHB number of voltage levels, which results in better performances in terms of harmonic behavior and reliability, requires a huge increase in hardware resources. Therefore, for the aforementioned applications, the five-level three-phase CHB topology represents the most suitable topology in terms of the ratio between hardware resources and reachable benefits.

5. Modulation and Control Strategies Impact on Electric Drive Performance and Efficiency

According to [1] and [2], EVs and HEVs are characterized by some specific control requirements such as fast dynamic response to the change in speed and torque reference, a wide range of operating speeds including zero speed, low torque ripple, voltage balancing, and equal power switches utilization. Such control goals are typically fulfilled through the implementation of four control stages: outer control loop, inner control loop, modulator, and

a mid-stage which mostly deals with voltage balancing and CMV minimization. The outer control loop is devoted to the speed control and usually PI or PID controllers are employed. The inner control is devoted to the torque (current) control. The most commonly adopted current control strategies are voltage-frequency (V/f) control, Field Oriented Control (FOC), and Direct Torque Control (DTC). Among them, the FOC is a well-established vector control strategy that allows for controlling independently the motor flux and torque by representing them as functions of the stator currents. Typically flux and torque control is carried out through two independent PI-based control channels. The control action is converted into power switches Gate Control Signals (GCSs) through a modulation stage. The modulation stage allows for adapting the FOC block scheme to almost every inverter topology. It guarantees fast dynamic response and low current ripple almost in every electric drive working conditions. Its simplicity and versatility, together with guaranteed good electric drive performance made it the most commonly adopted control strategy almost in every field of applications where electric drives are employed. In this context, it is evident that the modulation stage plays a key role in determining MI performance. Indeed, although MIs represent an already proven technology, they offer a great deal of challenges and a wide range of possibilities, especially in the modulation and control fields. Modulation strategies can be classified into hard-switching and soft-switching strategies, depending on the inverter switching frequency. Multicarrier Pulse Width Modulation (MC-PWM) strategies are the most adopted modulation strategies for MIs control purposes [30]-[33]. They are the evolution of conventional PWM modulation strategies employed for traditional 2L-VSIs. Their widespread adoption is related to their simple implementation on common controllers and control flexibility thanks to the simple adaptation in closed-loop controls. Moreover, the MC-PWM schemes guarantee reduced voltage and current harmonic distortion thanks to their ability to shift harmonics in the high frequency range, and good electric drive dynamic response. Indeed, there are several kinds of MC-PWM strategies characterized by different harmonic behaviours and impacts on CHB performance in terms of harmonic content and conversion efficiency.

The Space Vector Modulation (SVM) is particularly adopted in electric drives and traction applications due to its excellent DC-link voltage utilization, flexibility in switching states selection, and lower THD, as discussed in [34]. However, its main drawback is computational complexity, which drastically increases when MIs are employed. Indeed, a similar behaviour to SVM can be obtained with carrier-based modulation strategies [35].

In high-power and medium-high voltage applications, low-switching frequency modulation schemes such as Selective Harmonic Elimination (SHE) and Selective Harmonic Mitigation (SHM) algorithms are used to obtain high converter efficiency [36]-[39]. These algorithms allow for eliminating or mitigating low-order voltage harmonics by using a set of non-linear transcendental equations systems whose order depends on the number of the inverter voltage levels. They provide good steady-state performance when a high number of voltage levels is reached since it is possible to eliminate or mitigate a greater number of the harmonics. However, they are poorly adopted in electric drive applications due to their high computational cost and their poor dynamic performance.

6. Potentialities of Model Predictive Control in the E-Mobility Sector

To maximize the electric drive performance in terms of power losses and control flexibility, the scientific literature efforts focus on new control software solutions such as the Model Predictive Control (MPC). It represents a promising solution for power electronics and drives control, surpassing the limitations of traditional control strategies. In detail, FOC simplifies complex Multi-Input Multi-Output (MIMO) control problems into Single-Input Single-Output (SISO) control loops, affecting the system performance during transients and faults due to loop interactions and bandwidth limitations. Additionally, the use of PWM modulation, while enabling linear control, introduces delays that reduce system bandwidth. On the contrary, MPC allows for obtaining the optimal control action by solving a state-space model-based optimal control problem over a prediction horizon. The adoption of the controlled system state space model allows for considering system non-linearities, which are typically correlated to converter switching behaviour in power electronics and electrical drive fields [40]-[41]. The control objectives are synthesized into a cost function, which allows for fulfilling several conflicting goals. Such a feature is extremely attractive even in the e-mobility sector, due to the numerous control goals that must be faced in the powertrain control implementation, especially when MIs are employed, i.e., speed and torque reference tracking, battery state of charge management, voltage balancing, and switching equalization. Its principal merit deals with drastically reducing the inverter switching frequency but guaranteeing a reduced current harmonic distortion [42]. This feature makes the MPC one of the most appealing control strategies in the e-mobility sector since it allows for maximizing the electric drive efficiency, which implies an increase in the driving range.

MPC can be mainly classified into direct MPC and indirect MPC. Over the rest of this work, the direct MPC, also named Finite Control Set (FCS) MPC, will be considered. Indeed, the solution to the optimal control problem is found by predicting the future system state several

times, according to the number of available inverter Voltage Vectors (VVs). It follows that, currently, its main drawback is related to its high computational cost. Indeed, solving the optimal control problem online is a challenging task, especially when MIs are employed. Moreover, designing a FCS-MPC for a CHB-fed electric drive exhibits another layer of difficulty, due to its high degree of state redundancies.

7. Goal and Contents of This Thesis Work

According to the analysis of the scientific literature carried out so far, which will be further expanded and detailed over the rest of this work according to the specific topic taken into consideration, the following considerations can be stated:

- Although MIs and specifically CHB inverters offer several advantages in the field of the e-mobility sector, implementation and analysis of CHB-based electric drives is poorly faced in the scientific literature. In particular, a detailed analysis of the modulation strategies impact both on the CHB and motor in terms of harmonic behaviour and efficiency is missing.
- Regarding advanced control strategies such as the MPC, most of the applications related to CHB control are focused on grid-connected applications and the implementation and analysis of CHB-based drive controlled by MPC for e-mobility applications is missing. Moreover, the practical implementation of MPC for a CHB inverter is currently an open topic due to its high computational cost and issues related to state redundancies management and CHB modules power balancing [44]-[47].

Given the arguments presented so far, the present research project, named “*Development of an innovative electric drive with multilevel inverter for e-mobility applications*” aims to design, implement, and analyze a Three Phase Five Level (3P-5L) CHB-fed IPMSM drive for e-mobility applications. In detail, the CHB inverter topology is adopted for this application due to the previously discussed advantages and opportunities it can provide in the e-mobility sector. The adopted electrical motor is the Interior Permanent Magnet Synchronous Machine (IPMSM), since it is nowadays the most common and appreciated electrical machine in EV applications, due to its high power density, high efficiency, and low vibration and noise [1]-[2], [48]-[50]. The 3P-5L-CHB-fed IPMSM drive hardware and software design and implementation is carried out at the Sustainable Development and Energy Saving Laboratory of the University of Palermo. The thesis work is structured as follows:

- ❖ Chapter I is devoted to the performance analysis of the CHB inverter. In detail, performance analysis is carried out experimentally on the 3P-5L-CHB inverter prototype present at the SDESLAB of the University of Palermo and aims to investigate the impact of the numerous MC-PWM strategies on the CHB performance, both in terms of harmonic distortion and converter efficiency. Then, five MC-PWM strategies, i.e., Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD), Phase Shifted (PS), and Suppressed Carrier Arrangement Modulation (SCAMOD), and two kinds of modulating signals, i.e., Sinusoidal (S) and Switching Frequency Optimal (SFO), are considered and their implementation on the adopted controller is carefully described. In detail, software that allows for switching in real time between the previously mentioned MC-PWM strategies is implemented on the System on Module (SoM) sbRIO 9651 controller, composed of an Field Programmable Gate Array (FPGA) and a Digital Signal Processor (DSP). Comparative analysis is carried out over a wide working range, defined in terms of the converter amplitude modulation index and the switching frequency. In this way, the switching frequency impact on the inverter harmonic distortion and efficiency is investigated, allowing for accurately defining each MC-PWM strategy behaviour and for properly choosing the MC-PWM strategy depending on the specific application. Based on the experimental results, such analysis is further extended considering also the Dead Time (DT) as a modulation parameter. In detail, the second part of this analysis aims to identify a generalized mathematical model that allows for estimating the DT impact on the fundamental voltage drop. The proposed mathematical model is generalized for every MC-PWM strategy and every switching frequency value. Such a model is experimentally validated by comparing the estimated and the measured voltage drop.
- ❖ Chapter II is devoted to the 3P-5L-CHB-fed IPMSM drive implementation. The implementation is carried out both from the hardware and software side, describing the design and realization of conditioning circuits for current and speed measurement, and describing the control software implementation. In detail, the FOC is adopted as the main control strategy and it is integrated with the modulation stage described in Chapter I. The 3P-5L-CHB-fed IPMSM drive implementation is experimentally validated through some dynamic and steady-state condition tests. Finally, MC-PWM strategies impact on the IPMSM current harmonic distortion and power losses is investigated. Even in this case, tests are carried out over a wide operative range, defined in terms of motor speed and torque. Power loss analysis is

carried out through the harmonic segregation losses approach. It allows for identifying the fundamental power losses and harmonic power losses. Moreover, a comparison with a traditional 2L-VSI-fed IPMSM drive is carried out, to highlight the strong improvement in terms of current harmonic distortion and IPMSM efficiency related to the adoption of the CHB inverter.

- ❖ Chapter III is devoted to the design and implementation of novel FCS-MPC strategies for the CHB-fed IPMSM drive. Firstly, the control computational complexity issue is faced by developing a control algorithm named V^2B -MPC. In detail, such an algorithm allows for drastically reducing the control computation complexity by reducing the number of predictions to find the optimal control action from 4096, i.e., the total number of GCSs combination for a 3P-5L-CHB inverter, to only 7. Such a control algorithm is based on an offline optimization process devoted to discarding the redundant VVs and maintaining a subset of VVs that satisfy some design constraints that deal with the CMV minimization, the dv/dt minimization, and the GCSs transition minimization. The offline optimization process gives as output a subset of 61 non-redundant VVs and each one can be synthesized by only one GCSs combination. The proposed V^2B -MPC solves the optimal control problem by identifying online a subset of 7 VVs, composed of the previous optimal VV and its adjacent VVs, and looking for the current optimum among this subset. Indeed, only 7 predictions are required. The proposed V^2B -MPC is validated through experimental analysis. The CHB-fed IPMSM drive performance are investigated in steady state and dynamic working conditions over a torque-speed working area and the proposed control algorithm is compared with another control algorithm selected from the scientific literature, named Cell-by-Cell-Based (CBCB) MPC [47]. Subsequently, the proposed algorithm is improved to realize the CHB Sub-Modules (SMs) power equalization. In detail, the updated control algorithm, named Split Space Vector Based (S^2VB) MPC guarantees the SMs power balancing through the emulation of the PS-PWM, that is the only MC-PWM strategy, among the previously mentioned ones, that guarantees such a desired behaviour. With this aim, the 3P-5L-CHB topology can be seen as two independent cascaded 3P-3L-CHB, each one composed of a triplet of SMs. Then, the CHB VV is split into two VVs, each one related to one of the two SMs triplets. In order to guarantee SMs power balancing, one of the two triplets named slave triplet, must repeat the optimal switching pattern related to the other triplet, named master triplet. The effectiveness of the proposed

control is proven experimentally, and its behaviour, both in steady state and dynamic working conditions, is compared to the V^2B -MPC.

- ❖ Finally, Chapter IV investigates the potentialities of MPC applied to multiphase drives. Indeed, multiphase machine drives are gaining attention due to their advantages over traditional three-phase drives, such as lower magnetic induction field space harmonics, power splitting among phases, and fault-tolerant capability [51]-[52]. Such features make multiphase drives particularly appealing for EV applications. Moreover, MPC is particularly suitable for multiphase machine drives, although the higher number of phases increases the computational complexity if compared to the three-phase drives, even if the traditional 2L-VSI is employed. For this reason, this activity is focused on designing an FCS-MPC for a Six-Phase Asymmetric IPMSM (6P-AIPMSM) with reduced computational complexity. In detail, the proposed algorithm, named Voltage-Vector-Subset-Based (V^2SB)-MPC, allows for reducing the number of required predictions from 64 to 14 by selecting online a subset of adjacent and non-adjacent VVs to the previous optimal one. Such subsets are previously identified offline and stored in a Look-Up Table (LUT) by emulating the traditional FCS-MPC switching pattern. The proposed algorithm is tested in the MATLAB-Simulink environment and compared with other restrained search MPCs selected from the scientific literature. This activity was carried out in collaboration with the Institute of Power Electronics System (ELSYS) of the Technische Hochschule Nürnberg Georg-Simon Ohm during the PhD visiting period.

8. References

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Chapter I Cascaded H-Bridge Multilevel Inverter: Open-Loop Control and Experimental Performance Analysis

I.1 Introduction

The CHB inverter has been widely adopted in grid-connected application as STATCOM and PV inverter [I,1]-[I,8], in industrial electric drive applications [I,9]-[I,10], and in the e-transportation sector [I,11]-[I,14]. In almost every application previously mentioned, the CHB is driven by MC-PWM strategies due to their simple implementation on FPGA and DSPs and to their good response in terms of voltage harmonic distribution over the spectrum [I,15]. MC-PWM strategies have been widely investigated in the literature: according to [I,16] they can be classified in LS and PS, depending on the mutual carriers disposition. Several improved MC-PWM strategies have been proposed: in [I,17], a modified PS-PWM scheme with clamped modulating signals for a 3P-5L-CHB aimed to improve the inverter lifetime and reliability is proposed. In [I,18], a modified LS-PWM to improve the fault-tolerant capabilities is proposed. Although most of the contributions in the literature are focused on the study and definition of new modulation schemes to improve the performance of multilevel converters, there are few comparative studies focused on multilevel converters performance as a function of modulation technique and its parameters such as switching frequency and DT, especially regarding the CHB circuit topology. In [I,19] the authors compare the performance of a modular multilevel Single-Delta Bridge-Cell (SDBC) inverter, for utility-scale grid-tied photovoltaic applications, in terms of power-balancing capability and harmonic performance by using PS-PWM and LS-PWM. Also, in this case, the analysis is carried out for different load conditions but without varying the switching frequency. In [I,20] the authors study the main difference between Space Vector modulation and carrier-based PWM schemes by analyzing the output voltage harmonic content of a 3P-

5L NPC inverter. Also, in this work, the study is focused on the harmonic distortion while a comparison between the conversion efficiency in different operation conditions is missing. Conference papers [I,21]-[I,23] address the effect of switching frequency on multilevel inverter performance in terms of harmonic content but not extensively and they do not investigate the effects on inverter efficiency. In [I,24], CHBMI efficiency and voltage waveforms THD are evaluated varying the switching frequency for fixed amplitude modulation index; only two MC-PWM schemes are compared and the analysis is performed in simulation.

Regarding the DT effects on converter performance, it has been widely investigated in the literature only for conventional 2L-VSI, and just a few papers discuss its effect on MIs. A new Repetitive Control is proposed in [I,25]: it can suppress selected low-frequency harmonics below the Nyquist frequency without bringing the system into instability. In [I,26], an alternative compensation scheme to minimize the zero-current clamping is proposed. The compensation voltage signal is piecemeal and has a trapezoidal wave shape. In [I,27] a VSI small-signal model including the dead time effects in DQ-frame is proposed: taking into account a three-phase RL passive load in DQ-frame, Z_{qq} impedance results to be more resistive than the Z_{dd} impedance due to the dead time, especially at low frequency. In [I,28], a comparison between the output voltage waveforms of a Unipolar PWM-controlled H-Bridge and a PS-PWM-controlled CHB inverter is carried out in the simulation environment. CHB is less afflicted by the DT effects since a lower THD is evaluated when the DT increases. In [I,29]-[I,31], new DT compensation algorithms for CHB and NPC are proposed.

As can be seen, regarding the converter efficiency, several analyses have been carried out on inverter losses and voltage THD, however, on one side switching frequency and DT are treated only such a fixed parameter, and on the other, only a small number of PWM control strategies are taken into account and compared in the same conditions. In addition, most of the cited works are carried out only in the simulation environment.

In this chapter, an extended experimental performance analysis of the 3P-5L-CHB inverter, situated at the SDESLAB of the University of Palermo is carried out. In detail, the analysis is devoted to investigating the switching frequency impact on voltage harmonic distortion and converter efficiency when MC-PWM strategies are employed. Such MC-PWM strategies are classified depending on the carriers mutual disposition and phase shift, and depending on the harmonic content of the modulating signals. Investigation is carried out over a working range identified by the amplitude and modulation index and the converter

switching frequency. The experimental analysis is subsequently extended by investigating the DT impact. In detail, a generalized mathematical model that allows for estimating the DT impact on the fundamental voltage drop is provided. The proposed mathematical model is generalized for every MC-PWM strategy and every switching frequency value. Then, DT impact on the voltage harmonic distortion and converter efficiency is investigated. Indeed, the previously defined working range is extended by considering a set of DT values.

I.2 Cascaded H-Bridge Inverter Mathematical Model

The CHB is a MI topology characterized by several H-Bridge (HB) modules connected in a cascaded fashion. Each HB module can be controlled independently and it can provide a number of voltage levels equal to 3. Thus, the number of CHB voltage levels n_l depends on the number of cascaded HB modules n_{HB} , according to the following relation:

$$n_l = 2n_{HB} + 1 \quad (\text{I},1)$$

Due to the modularity that characterizes the CHB, it is convenient to build its mathematical model starting with the model of one HB module, whose circuit diagram is reported in Fig. I. 1.

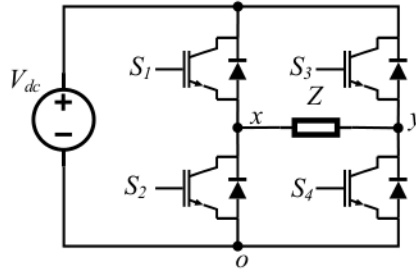


Fig. I. 1: H-bridge module circuit diagram.

In detail, each power switch and its anti-parallel diode are modeled as an ideal bidirectional switch with zero switching time, and zero conduction and switching losses. Then, each bidirectional switch state is represented by a state function $S_z \in \{0, 1\}$, where $z \in \{1, 2, 3, 4\}$ identifies the HB bidirectional switches. With respect to the x -leg, the voltage v_{xo} is equal to:

$$v_{xo} = \frac{V_{dc}}{2} (1 + S_1 - S_2) \quad (\text{I},2)$$

Where V_{dc} is the HB module DC-link voltage. To avoid leg short circuits, switching devices on the same HB leg must work in a complementary way. Therefore, the following relation is introduced:

$$S_2 = \overline{S_1} \quad (\text{I},3)$$

where $\overline{S_1}$ is the negative of S_1 . Then, the equation (I,2) can be rewritten as:

$$v_{xo} = V_{dc} \cdot S_1 \quad (\text{I},4)$$

Then, according to equation (I,4), the output voltage $v_{xo} \in \{0, V_{dc}\}$. The same considerations are valid for the voltage v_{yo} , related to leg y . The voltage v_{xy} is defined as:

$$v_{xy} = v_{xo} - v_{yo} \quad (\text{I,5})$$

By replacing (I,4) in (I,5), it follows:

$$v_{xy} = V_{dc}(S_1 - S_3) \quad (\text{I,6})$$

According to (I,5), $v_{xy} \in \{-V_{dc}, 0, V_{dc}\}$. Table I. 1 shows the HB available states and related output voltage.

Table I. 1: HB available states and related output voltage.

S_1	S_3	v_{xy}
0	0	0
0	1	$-V_{dc}$
1	0	V_{dc}
1	1	0

Once the HB state model is defined, it can be used to build the state model of a generic n_l -level single-phase CHB, whose schematic is reported in Fig. I. 2.

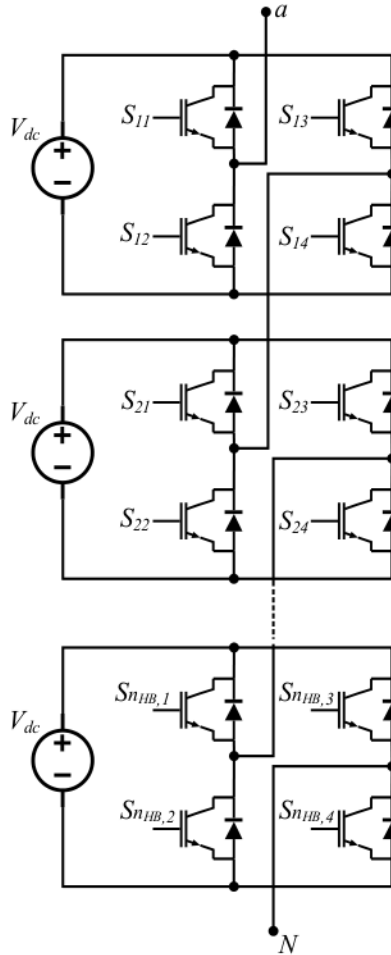


Fig. I. 2: Single phase CHB schematic with n_{HB} cascaded H-Bridge modules.

The phase voltage v_{aN} is defined as:

$$v_{aN} = \sum_{i=1}^{n_{HB}} v_{xy,i} \quad (I,7)$$

where i identifies the i^{th} cascaded HB module per phase. By considering a symmetric configuration, i.e., every HB module is characterized by the same DC link voltage V_{dc} , replacing (I,6) in (I,7), it follows:

$$v_{aN} = V_{dc} \sum_{i=1}^{n_{HB}} (S_{a,i1} - S_{a,i3}) \quad (I,8)$$

As a way of example, Table I. 2 summarizes the available states of a 5L-CHB and related output voltage v_{aN} .

Table I. 2: Available states of a 5L-CHB and related output voltage v_{aN} .

S_{11}	S_{13}	S_{21}	S_{23}	v_{aN}
1	0	1	0	$2V_{dc}$
0	1	0	1	$-2V_{dc}$
1	0	0	0	V_{dc}
1	0	1	1	V_{dc}
0	1	1	1	$-V_{dc}$
0	1	0	0	$-V_{dc}$
1	1	1	0	V_{dc}
0	0	1	0	V_{dc}
1	1	0	1	$-V_{dc}$
0	0	0	1	$-V_{dc}$
0	0	0	0	0
0	0	1	1	0
1	1	1	1	0
1	1	0	0	0
1	0	0	1	0
0	1	1	0	0

Finally, the 3P-CHB topology is considered. By considering a star-connected three-phase load, where n is the star center, it is possible to model each CHB phase as an independent waveform generator, as illustrated in Fig. I. 3. Phase voltage equation (I,8) referred to the converter star center N is valid for the j^{th} phase, with $j \in \{a, b, c\}$.

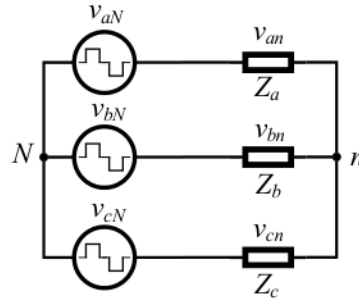


Fig. I. 3: 3P-CHB inverter powering a symmetric load.

Then, it is possible to express the load voltages v_{an} , v_{bn} , and v_{cn} , referred to the load star center n , as a function of the phase voltages v_{aN} , v_{bN} , and v_{cN} , and the voltage between the star centers v_{nN} , i.e., the CMV, as follows:

$$\begin{cases} v_{aN} = v_{an} + v_{nN} \\ v_{bN} = v_{bn} + v_{nN} \\ v_{cN} = v_{cn} + v_{nN} \end{cases} \quad (I,9)$$

Imposing that $v_{an}+v_{bn}+v_{cn}=0$, is it possible to express the CMV v_{nN} as:

$$v_{nN} = \frac{v_{aN} + v_{bN} + v_{cN}}{3} \quad (I,10)$$

Then, the load voltages v_{an} , v_{bn} , and v_{cn} can be expressed as:

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} \quad (I,11)$$

In a compact form:

$$\mathbf{v}_n = \mathbf{M} \cdot \mathbf{v}_N \quad (I,12)$$

Finally, the 3P-5L-CHB circuit diagram is reported in Fig. I. 4. The complete circuit diagram is reported since it is the MI topology that will be adopted over the rest of this work.

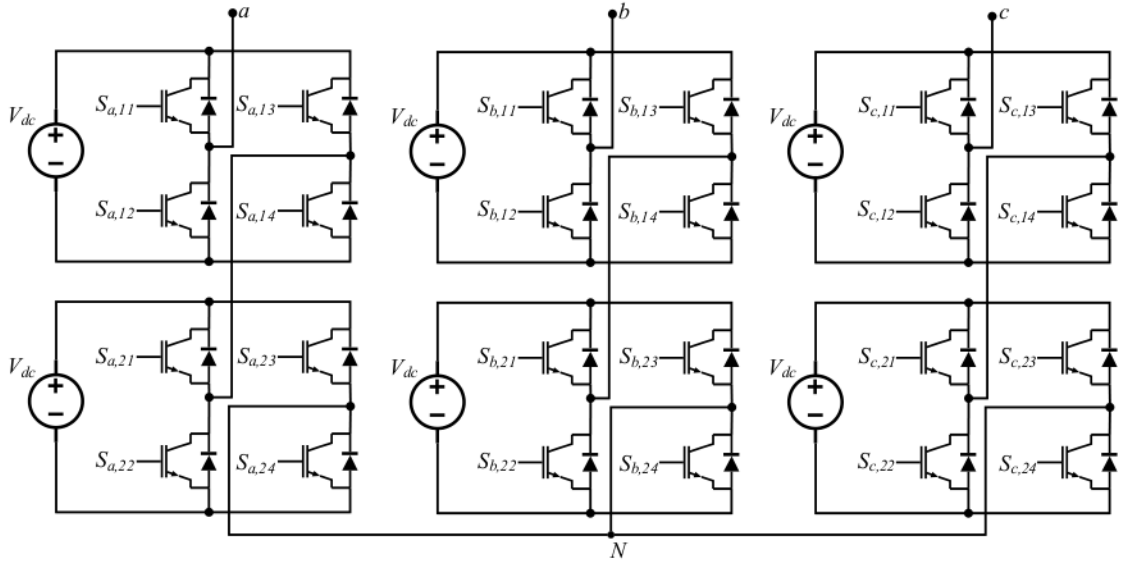


Fig. I. 4: Three Phase Five-Level CHB circuit diagram.

I.3 Multi-Carrier Pulse Width Modulation Strategies

Generally, the performance of the converter depends on the modulation schemes in terms of harmonic distortion. MC-PWM represents the natural evolution of the classical PWM scheme for 2L-VSIs. They are commonly used in many fields of applications due to their simple implementation in common controllers (microcontroller or FPGA) and due to their good response in terms of the harmonic content that allows easy voltages and current filtering [I,15]-[I,16].

The number of modulating signals depends on the number of phases m , and the number of carriers n_c depends on the number of MI phase voltage levels n_l , according to the relation:

$$n_c = n_l - 1 \quad (\text{I,13})$$

By replacing (I,1) in (I,13), it is possible to link the number of required carriers to the number of CHB modules per phase, as follows:

$$n_c = 2n_{HB} \quad (\text{I,14})$$

Thus, for a five-level converter, four carrier signals are required. GCSs are generated through the comparison of modulating signals and carrier triangular signals. Taking into account the hypothesis related to the power switches and their anti-parallel diode introduced in the previous section, it is possible to state that the CHB state functions and the GCSs coincide and they can be indicated with the same symbol $S_{j,iz}$. The MC-PWM modulating schemes and relations for GCSs generation are discussed for the 3P-5L CHB, since it is the MI topology adopted over the rest of this work, without losing generality. Relations for GCSs generation for a 3P-5L CHB are reported below:

$$S_{j,11} = \begin{cases} 1 & \text{if } u_j \geq T_1 \\ 0 & \text{if } u_j < T_1 \end{cases} \quad (\text{I,15})$$

$$S_{j,13} = \begin{cases} 1 & \text{if } u_j < T_4 \\ 0 & \text{if } u_j \geq T_4 \end{cases} \quad (\text{I,16})$$

$$S_{j,21} = \begin{cases} 1 & \text{if } u_j \geq T_2 \\ 0 & \text{if } u_j < T_2 \end{cases} \quad (\text{I,17})$$

$$S_{j,23} = \begin{cases} 1 & \text{if } u_j < T_3 \\ 0 & \text{if } u_j \geq T_3 \end{cases} \quad (\text{I,18})$$

Where u_j is the modulating signal related to phase j and T_1 , T_2 , T_3 , and T_4 are the carrier signals. Carriers are assigned to each HB leg according to relations (I,15), (I,16), (I,17), and (I,18) such that these relations are valid independently by the adopted MC-PWM strategy. It must be underlined that GCSs to the lower power switches ($S_{j,i2}$ and $S_{j,i4}$) of each HB leg are derived by the higher power switches ($S_{j,i1}$ and $S_{j,i3}$), according to (I,3).

It is possible to define the amplitude modulation index M as the ratio between the modulating signal amplitude U and the total DC link voltage U_{dc} , as follows:

$$M = \frac{U}{U_{dc}} \quad (\text{I,19})$$

where the total DC link voltage U_{dc} for a symmetric n_{HB} -level CHB is defined as:

$$U_{dc} = n_{HB} \cdot V_{dc} \quad (\text{I,20})$$

The formulation of the amplitude modulation index M provided in (I,19) is valid for any number of inverter voltage levels and for every adopted MC-PWM strategy.

Before discussing the MC-PWM strategies in detail, the apparent switching frequency f_a must be introduced. In detail, as will be shown later, each MC-PWM strategy displaces harmonics over the spectrum differently, depending on the mutual carriers level- or phase-shift. Such a behaviour is justified in the time domain by the fact that MC-PWM strategies produce a different number of the CHB state transitions, for a fixed carriers frequency. Thus, the switching frequency f_{sw} is linked to the carriers period T_{PWM} and provides information about the switching rate of the individual power device undergoing a state change. Conversely, the apparent switching frequency f_a indicates the total number of switching events within a modulation period.

MC-PWM strategies are classified as Level Shifted (LS) and Phase Shifted (PS).

I.3.1 Level Shifted MC-PWM

About LS-PWM strategy, carriers are characterized by the same peak-to-peak amplitude, a mutual amplitude shift such that no carriers superpositions occur, and a mutual phase shift. Depending on the mutual phase shift, LS-PWM can be classified as:

- Phase Disposition (PD): all carriers are in phase;
- Phase Opposition Disposition (POD): carriers are in phase two-by-two
- Alternative Phase Opposition Disposition (APOD): adjacent carriers are in phase opposition.

LS-PWM modulation schemes are reported in Fig. I. 5.

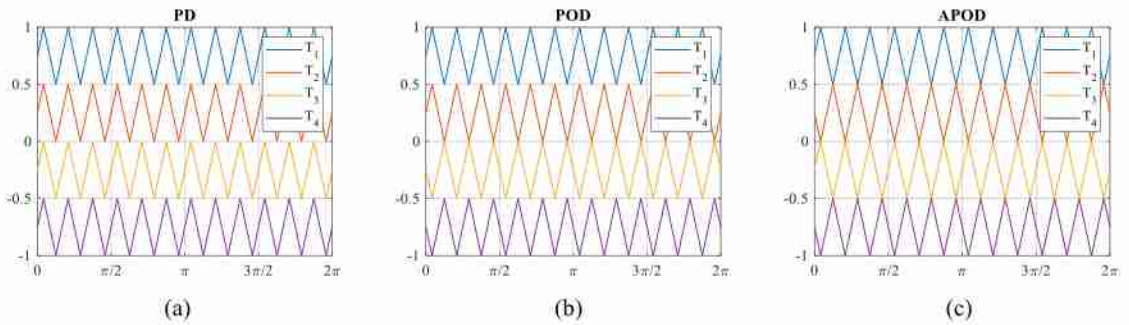


Fig. I. 5: LS-PWM modulation schemes for a 5L-CHB inverter: (a) PD, (b) POD, (c) APOD.

LS-PWM strategies present the same harmonic distribution in the frequency domain: in detail, voltage harmonics are centered around the switching frequency and its integer multiples, according to the following relation:

$$f_h = k \cdot f_{sw} \quad (I,21)$$

where f_h is the frequency where each group of voltage harmonics is centered, and $k=1, 2, 3 \dots$. Looking at relation (I,21), the apparent switching frequency f_a can be computed by setting $k=1$. Then, it can be stated that, for LS-PWM strategies, the switching frequency f_{sw} and the apparent switching frequency f_a coincide. It must be underlined that the distribution

of harmonics in the frequency domain does not depend on the number of inverter voltage levels. Moreover, the carriers mutual level shift implies an uneven power distribution among the HB modules, depending on the carriers assigned to each HB and depending on the amplitude modulation index M . In detail, when the amplitude modulation index is lower than 0.5, the HB controlled by an external couple of carriers (T_1 and T_4) does not switch at all.

I.3.2 Phase Shifted MC-PWM

About the PS-PWM strategy, carriers are characterized by the same peak-to-peak amplitude, the same average value equal to zero, and a mutual phase shift that depends on the number of cascaded HB modules per phase n_{HB} . In detail, supposing to consider carriers assigned to x -legs of each HB module (T_1 and T_2 for a 5L-CHB) as a reference, the phase φ_i to assign to the i^{th} reference carrier is computed with the following relation:

$$\varphi_i = \frac{(i-1) \cdot \pi}{n_{HB}} \quad (I,22)$$

where i is the i^{th} considered HB module per phase. Carriers assigned to the y -legs of each HB module (T_4 and T_3 for a 5L-CHB) are in phase opposition to the related reference carriers. Then, the modulation scheme shown in Fig. I. 6 (a) is obtained: it can be noted that each HB in the same phase is controlled with a classical Unipolar PWM strategy, whose GCSs are phase-shifted by φ_i . As a consequence, all the HB modules on the same phase lead the same active power independently of the CHB working conditions, allowing a uniform utilization of each HB module and DC sources. Phase voltage harmonics are centered around multiples of switching frequency f_{sw} as a function of the number of inverter voltage levels n_l , according to the following relation:

$$f_h = k(n_l - 1)f_{sw} \quad (I,23)$$

In a 3P-5L CHB inverter, harmonics are centered around $4f_{sw}$ and its multiples and, by setting $k=1$, the apparent switching frequency $f_a=4f_{sw}$. It follows that, for fixed carriers frequency, PS-PWM guarantees an easier voltage and current harmonic filtering, due to the harmonic shift in the high-frequency range, but it causes higher switching losses.

I.3.3 Suppressed Carrier Arrangement Modulation

SCAMOD is a hybrid scheme between LS and PS, characterized by stacked couples of carriers that have the same peak-to-peak amplitude and a mutual phase shift equal to 180° . SCA modulation scheme for a 3P-5L-CHB is reported in Fig. I. 6 (b). Output voltage harmonics are centered around multiples of switching frequency, according to the following relation:

$$f_h = k2f_{sw} \quad (I,24)$$

It must be underlined that SCA modulation produces a shift over the spectrum that does not depends on the number of voltage levels or, equivalently, by the cascaded HB modules per phase. Thus, the apparent switching frequency f_a is constant and equal to $2f_{sw}$. Moreover, SCAMOD produces an even power distribution among HB cells only when the number of cascaded HB modules n_{HB} is strictly lower than 3.

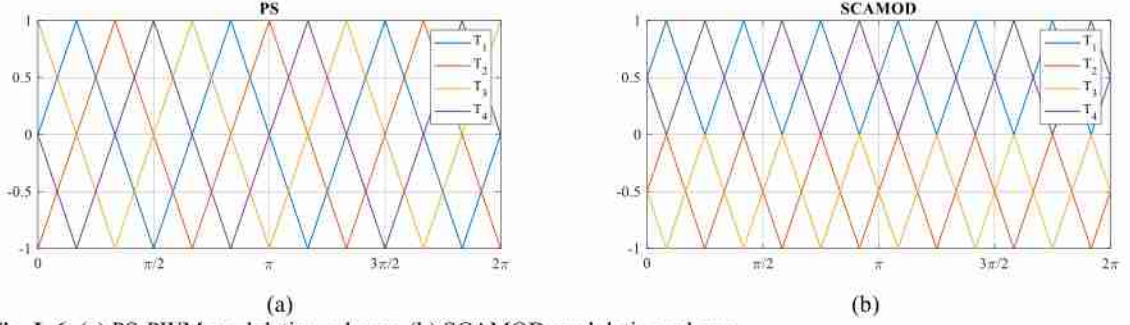


Fig. I. 6: (a) PS-PWM modulation scheme, (b) SCAMOD modulation scheme.

I.3.4 Switching Frequency Optimal Modulation

The performance of the converter is affected by the modulating signals. Usually, Sinusoidal (S) and Switching Frequency Optimal (SFO) modulating signals are commonly adopted in grid-connected and electric drive applications, respectively. In detail, SFO modulating signals u_a^* , u_b^* , and u_c^* are obtained from the sinusoidal modulating signals u_a , u_b , and u_c according to the following relation:

$$\begin{cases} u_a^* = u_a - u_{offset} \\ u_b^* = u_b - u_{offset} \\ u_c^* = u_c - u_{offset} \end{cases} \quad (I,25)$$

where u_{offset} is a triangular waveform whose fundamental frequency is equal to three times the sinusoidal modulating signals frequency. It can be obtained as follows:

$$u_{offset} = \frac{\max(u_a, u_b, u_c) + \min(u_a, u_b, u_c)}{3} \quad (I,26)$$

According to [I,1], the SFO modulation signals allow for obtaining the same overall harmonic content of a SVM and the modulation index can be extended up to 1.15. Sinusoidal modulating signals, offset signal, and SFO modulating signals are shown in Fig. I. 7 (a), (b), and (c), respectively.

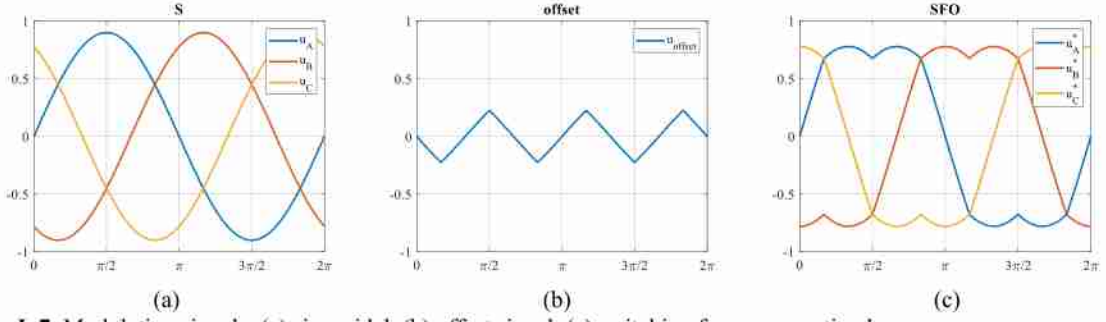


Fig. I. 7: Modulating signals: (a) sinusoidal, (b) offset signal, (c) switching frequency optimal.

I.4 Dead Time Generation Strategies

As discussed in the previous section, the relation (I,3) is adopted to prevent power devices on the same leg from being in a conducting state simultaneously, causing the leg to short-circuit. However, since power devices are characterized by a non-zero switching time, which depends on the technology of the adopted devices, the DT in the GCSs is introduced. The DT generation is commonly carried out by the software that executes the modulation algorithm. In this work, two simple DT generation strategies are presented. The former method consists of generating the GCSs through the logic circuit shown in Fig. I. 8.

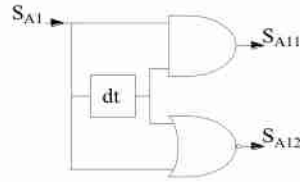


Fig. I. 8: Dead time generator logic circuit.

In detail, according to Fig. I. 8, the GCS S_{A1} generated by the modulator is delayed according to the desired DT, and the signal S_{A1d} is generated. Then, signals S_{A1} and S_{A1d} input into the AND and NOR gates, and the GCSs S_{A11} and S_{A12} are generated, according to the truth table reported in Table I. 3.

Table I. 3: Truth table of the dead time generation logic circuit.

S_{A1}	$S_{A1,d}$	S_{A11}	S_{A12}
0	0	0	1
0	1	0	0
1	0	0	0
1	1	1	0

The latter method deals with manipulating the modulating signal u in a PWM period, according to the modulation scheme reported in Fig. I. 9.

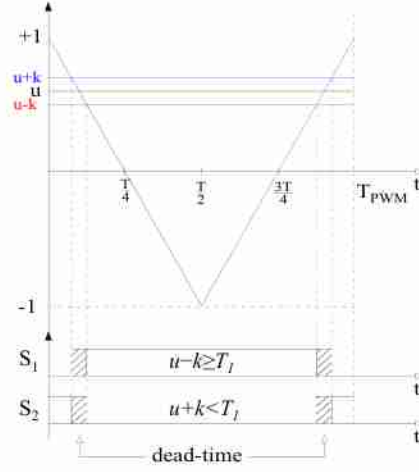


Fig. I. 9: Dead-time generation in a PWM period with the k constant.

In detail, the modulating signal u is split into two signals $u+k$ (blue horizontal line) and $u-k$ (red horizontal line), where k is a DT factor. The split modulating signals $u-k$ and $u+k$ are assigned to the upper and lower devices of each HB leg, respectively. Then, relations for GCSs generation reported in (I,15), (I,16), (I,17), and (I,18) must be modified. In detail, as a way of example, relations (I,15), (I,16) are split into (I,27), (I,28), (I,29), and (I,30), reported below.

$$S_{j,11} = \begin{cases} 1 & \text{if } u_j - k \geq T_l \\ 0 & \text{if } u_j - k < T_l \end{cases} \quad (\text{I,27})$$

$$S_{j,12} = \begin{cases} 1 & \text{if } u_j + k < T_l \\ 0 & \text{if } u_j + k \geq T_l \end{cases} \quad (\text{I,28})$$

$$S_{j,13} = \begin{cases} 1 & \text{if } u_j + k < T_4 \\ 0 & \text{if } u_j + k \geq T_4 \end{cases} \quad (\text{I,29})$$

$$S_{j,14} = \begin{cases} 1 & \text{if } u_j - k \geq T_4 \\ 0 & \text{if } u_j - k < T_4 \end{cases} \quad (\text{I,30})$$

Similar relations are valid for generations of GCSs $S_{j,21}$, $S_{j,22}$, $S_{j,23}$, and $S_{j,24}$, replacing T_l and T_4 with T_2 and T_3 , respectively. GCSs generated for an HB leg are shown in Fig. I. 9. In detail, the ideal GCSs (with $DT=0$) are identified with a dashed line, and the real GCSs are identified by the continuous line. For a fixed desired DT, the coefficient k is evaluated through a graphical approach based on triangle similarity. However, this approach must be customized for each specific MC-PWM strategy. In detail, for PS PWM strategy, looking at Fig. I. 10 (a), by observing the similarity between the dotted black triangle and the solid red triangle, the following relationship can be defined:

$$\frac{u+k-(u-k)}{t_{dt}} = \frac{1-(-1)}{T_{PWM}/2} \quad (I,31)$$

Isolating k in one member, the following relation is obtained:

$$k_{PS} = 2t_{dt}f_{sw} \quad (I,32)$$

By carrying out the same procedure for PD and SCAMOD, relations (I,33) and (I,34) are obtained.

$$\frac{u+k-(u-k)}{t_{dt}} = \frac{1-0.5}{T_{PWM}/2} \quad (I,33)$$

$$\frac{u+k-(u-k)}{t_{dt}} = \frac{1-0}{T_{PWM}/2} \quad (I,34)$$

Then, isolating k in one member, it follows respectively:

$$k_{PD} = \frac{1}{2}t_{dt}f_{sw} \quad (I,35)$$

$$k_{SCA} = t_{dt}f_{sw} \quad (I,36)$$

Comparing equations (I,32), (I,35), and (I,36) it follows that, for fixed DT value, modulating signal u must be shifted differently, according to the adopted MC-PWM strategy. This result is correlated to the different carrier signals slope. In other words, by shifting u by the same quantity, independently by the MC-PWM strategy, three different DT values are obtained, as can be seen in Fig. I. 10. Finally, it must be underlined that coefficient k for POD- and APOD-PWM strategies are the same as k_{PD} , since carriers for LS strategies are characterized by the same slope.

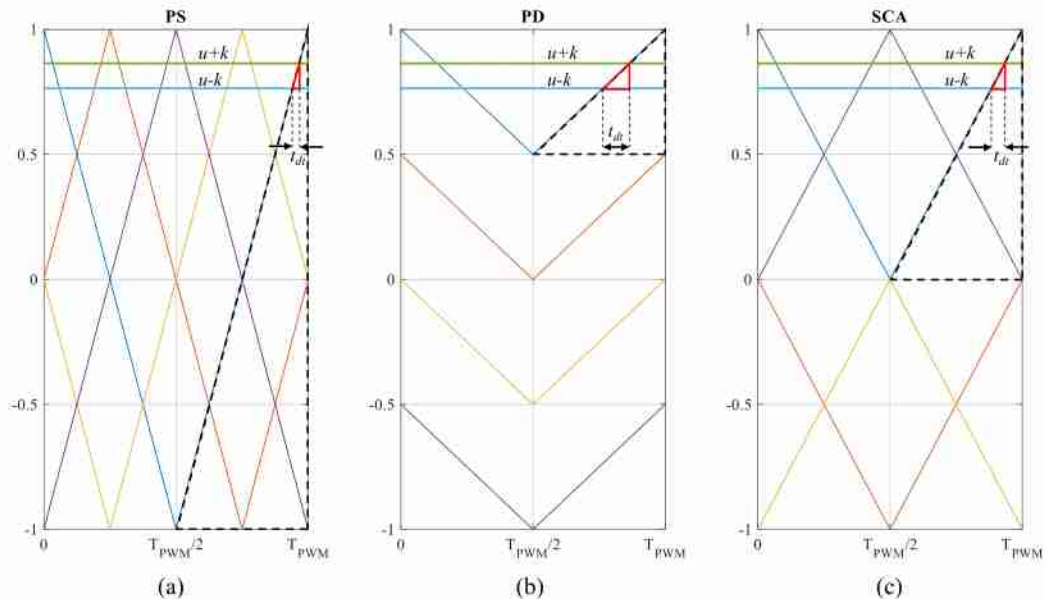


Fig. I. 10: Graphical method to define the DT coefficient k : (a) PS, (b) PD, (c) SCAMOD

I.5 CHB Inverter Mathematical Model Update Considering the Dead Time Effect

According to the discussion carried out in Section I.2, the CHB mathematical model is based on the assumption that each power switch and its anti-parallel diode are modeled as an ideal bidirectional switch with zero switching time and zero conduction and switching losses. As a consequence, the CHB state functions and the GCSs coincide and they are indicated with the same symbol $S_{j,iz}$. However, once the DT between each leg GCSs is introduced, it is mandatory to distinguish whether the power switches or their anti-parallel diodes are conducting, depending on the phase currents. For this purpose, the generalized CHB state functions $\hat{S}_{j,iz}$, are introduced. Considering the pair of anti-parallel devices at positions $j,i1$ and $j,i2$: if the phase current i_j is positive and if the GCS $S_{j,i1}=1$, then the power device at position $j,i1$ is actually in conducting state; if instead i_j is negative, the condition for the diode at position $j,i1$ to conduct is that the GCS $S_{j,i2}=0$. Indeed, the diode at position $j,i1$ can conduct both when GCS $S_{j,i1}=1$ and i_j is negative, and also when the i_j is negative and GCSs $S_{j,i1}=0$ and $S_{j,i2}=0$. This last operating condition occurs during DT. Similar considerations are valid for other CHB anti-paralleled devices and the following generalized CHB state functions $\hat{S}_{j,iz}$ are obtained:

$$\begin{cases} \hat{S}_{j,i1} = S_{j,i1} \wedge (i_j \geq 0) \vee \overline{S_{j,i2}} \wedge (i_j < 0) \\ \hat{S}_{j,i2} = S_{j,i2} \wedge (i_j \leq 0) \vee \overline{S_{j,i1}} \wedge (i_j > 0) \\ \hat{S}_{j,i3} = S_{j,i3} \wedge (i_j \leq 0) \vee \overline{S_{j,i4}} \wedge (i_j > 0) \\ \hat{S}_{j,i4} = S_{j,i4} \wedge (i_j \geq 0) \vee \overline{S_{j,i3}} \wedge (i_j < 0) \end{cases} \quad (I,37)$$

Once the generalized CHB state functions are introduced, the CHB phase voltage equation (I,8) is updated as follows:

$$v_{jN} = \frac{V_{dc}}{2} \sum_{i=1}^{n_{HB}} (\hat{S}_{j,i1} - \hat{S}_{j,i2} - \hat{S}_{j,i3} + \hat{S}_{j,i4}) \quad (I,38)$$

I.6 Control Software Design and MC-PWM Implementation

The MC-PWM strategies discussed in the previous section are implemented on the SoM sbRIO 9651 controller by National Instrument. It is based on the Xilinx Zynq 7000 System on a Chip (SoC) and consists of a Xilinx Zynq FPGA and an ARM Cortex A9 DSP module. Both modules can be programmed independently in the LabVIEW environment with Graphical (G) language by choosing the proper target, named FPGA and Real-Time (RT) targets, respectively. SoM sbRIO 9651 is equipped with a commercial control board designed for fast prototyping purposes, named Power Electronics and Drives (PED) Board.

A picture of the PED Board is shown in Fig. I. 11. The sbRIO 9651 and PED Board technical data are reported in Table I. 4 and Table I. 5, respectively.

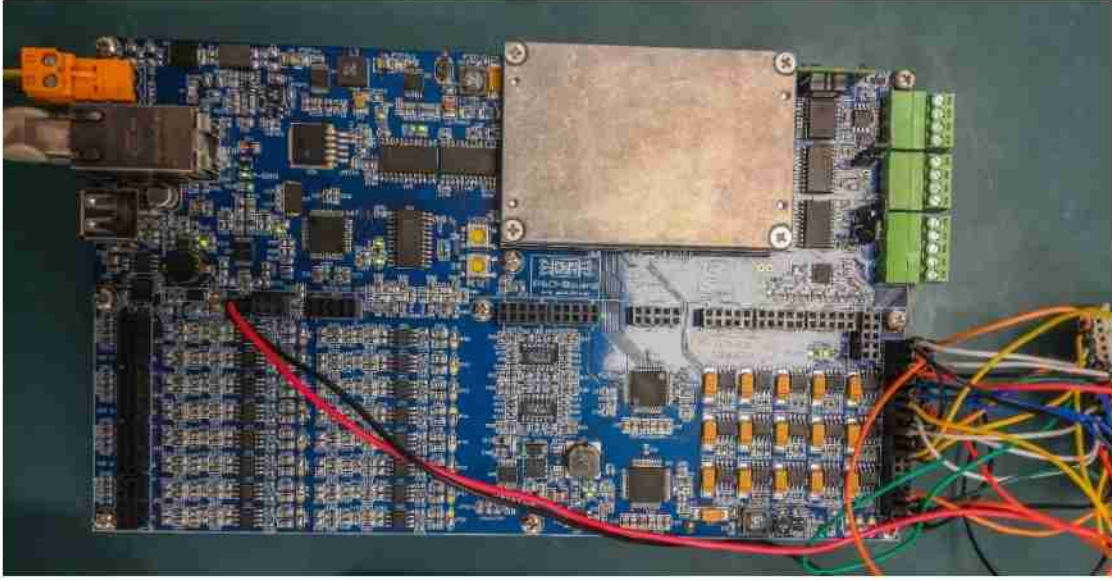


Fig. I. 11: Picture of the PED Board

Table I. 4: sbRIO 9651 technical data

Quantity	Value
Type	Xilinx Zynq-7000 SoC
Architecture	ARM Cortex A-9
Speed	667 MHz
Cores	2
Logic Cells	85000
Flip-flops	106400
LUTs	53200
DSP slices	220

Table I. 5: PED-Board technical data.

Hardware	Features
PWM Channels	30x, 0-5V or 0-15 V selectable voltage
14 bit-ADC,	2x8 Channels, Simultaneous Sampling up to 600 kS/s, -5 - +5V or 0-10V
10 bit- ADC,	1x8 Channels, Up to 200 kS/s, 0-5 V inputs
12 bit-DAC,	1x4 Channels, 10 μ s settling time
Digital I/O	46x3.3V standard
Ethernet	1x RS485

The implemented control algorithm allows for switching between the discussed MC-PWM strategies and modifying in real-time the main modulation parameters, such as the switching frequency f_{sw} , the amplitude modulation index M , and the DT, allowing for easy CHB inverter performance comparative analysis. In Fig. I. 12, the block diagram of the control algorithm is shown. Both the FPGA and RT targets are adopted for the control implementation.

I.6.1 FPGA Target

The FPGA target is adopted to implement time-critical operations.

With respect to the block diagram in Fig. I. 12, a Flat Sequence Structure (FSS) with two frames is placed. It allows for defining operations sequences by placing them into specific frames.

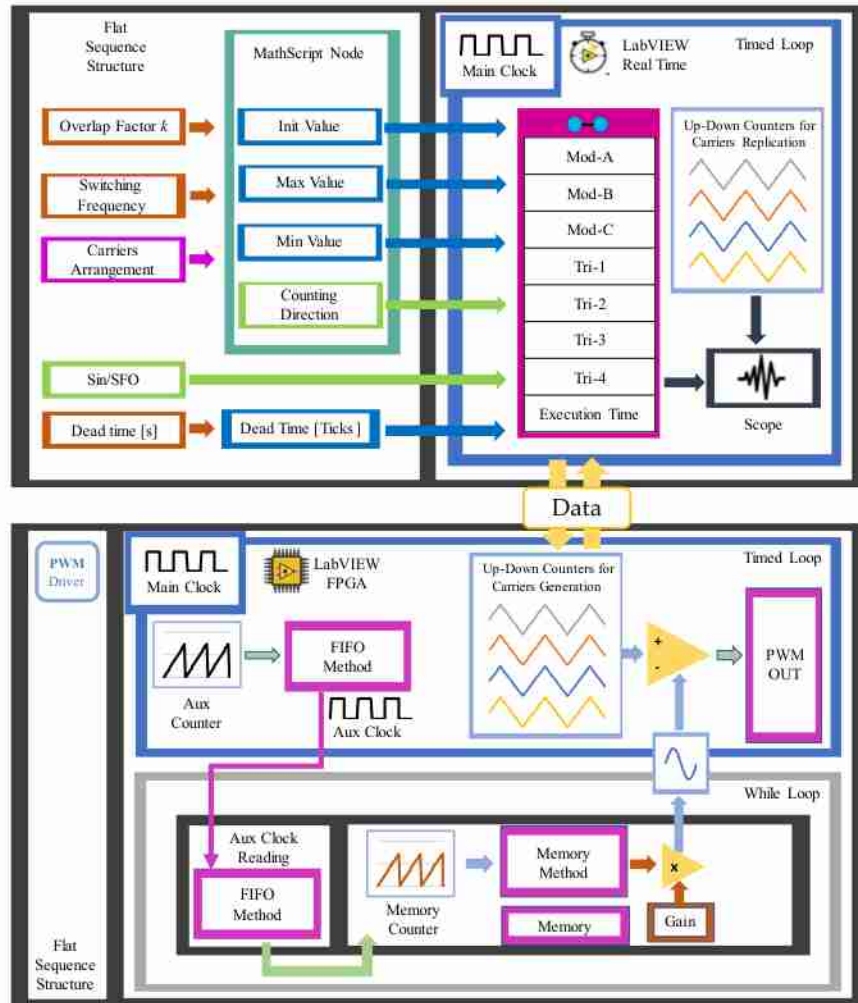


Fig. I. 12: Control block diagram implemented in the FPGA and Real-Time Targets.

In the first frame, the initialization of PWM I/O nodes is implemented, placing in there the PWM I/O Driver. The second frame contains two structures running in parallel, i.e., a Timed Loop (TL) and a While Loop (WL). The TL is a WL with a hard constraint on the maximum execution time. In detail, the user can set the maximum execution time that, in this application, is equal to 8.33 ns. Due to the hard time restriction, only Boolean or Integer variables, identified by the colors green and blue, respectively, can be adopted. Within the TL, the following operations are arranged:

- Carriers generation: this operation is realized by the implementation of modular up-down counters; in detail, the main counters parameters, i.e., the counter initial value, maximum counting value, minimum counting value, and counting direction (increasing or decreasing) can be modified to obtain the desired MC-PWM strategy;

- GCSs generation: this operation is carried out by the comparison of carriers and modulating signals, according to the relations (I,15), (I,16), (I,17), and (I,18);
- Aux Clock generation: Aux clock is required for the coordination between the operation inside the TL and WL. Aux Clock is realized by the sawtooth counter; in detail, when the counter reset occurs, a Boolean signal is generated and sent to the WL by a First Input First Output (FIFO) register, which triggers the WL.

Operations inside the WL are triggered by the Boolean signal from the TL and are executed with the default 40 MHz clock. The WL does not have time constraints, unlike the TL. This means that the WL processing time depends on the number of operations to be performed and their complexity. However, to guarantee real-time operation, the operations must be completed within the WL receives the next trigger signal. The following operations are arranged inside the WL:

- Aux clock reading: this operation is realized by another FIFO in reading mode. The Boolean signal is sent in other FSS frames to mark all other operations;
- Modulating signals generation: modulating signals are generated by extracting elements from a pre-allocated vector of 1000 elements representing one sinewave signal period. Element extraction is carried out through three sawtooth counters, one per phase, which are employed as memory addresses;
- Scaling and SFO generation: the sinewave amplitude is matched with the carriers amplitude and, if required, SFO modulating signals are generated, according to (I,25) and (I,26).

A way to simplify the programming workflow is to save and recall recursive structures, such as up-down counters, logic circuits for DT generation, and so on. As a way of example, the frame of an FSS including a TL and a WL for the generation of the modulating signals is reported in Fig. I. 13. The up-down counters and DT generation structures are shown in red and green squares, respectively.

I.6.2 Real-Time Target

In the RT target, operations related to the counters parameter computation, and Graphical User Interface (GUI) management are implemented. Therefore, the FPGA target contains only the control main structure, and it is completed by the complementary operations executed in the RT target. In particular, in RT target another two frames FSS is placed. The first frame contains all operations to be executed only once, i.e. DT conversion from seconds to clock ticks and carriers parameters calculations. To realize parameters calculation, the

MathScript Node is used: it allows for implementing operations with a textual language instead of linking blocks. Parameters calculation has been generalized, for each MC-PWM strategy.

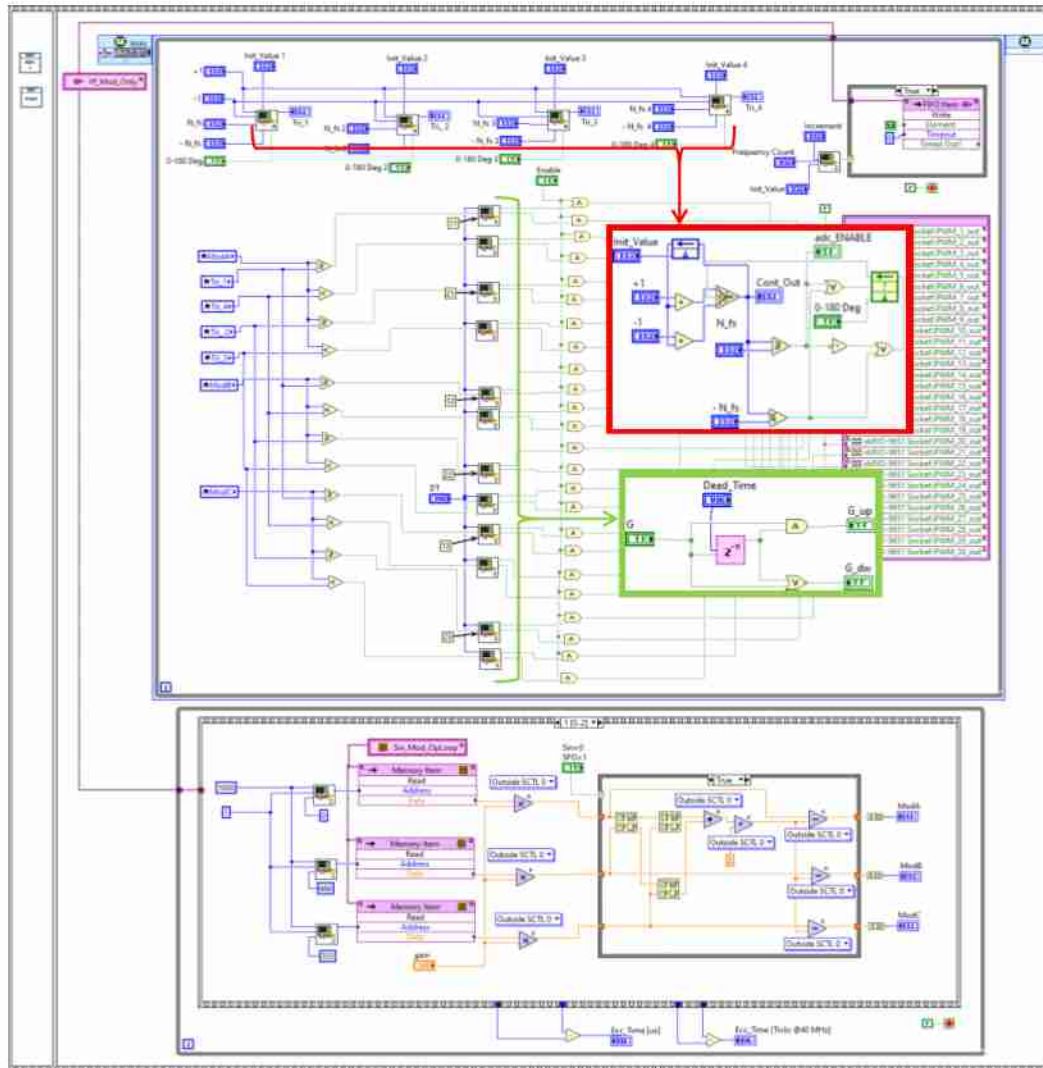


Fig. I. 13: Block Diagram of FPGA Target including generation of carriers, modulating signals, and PWM signal.

The second frame contains the TL that addresses the signal transmission between the FPGA and RT targets and the signals monitoring. The GUI is shown in Fig. I. 14. There, carriers signals, modulating signals, and relative parameters can be monitored; modulation index amplitude M , switching frequency f_{sw} , and modulating signals frequency f , can be set by the user thanks to the related sliders; desired carriers arrangement can be set, introducing in the text box the related symbol (PD, POD, APOD, SCA, PS). The enable button allows for setting the PWM outputs to zero value.

Indeed, splitting the code between the RT and FPGA targets allows for a drastic reduction in the FPGA resource utilization. In Table I. 6 the comparison between the FPGA resource utilization when the control algorithm is implemented entirely in the FPGA target and when

it is split among FPGA and RT targets is reported. In detail, It can be noted that the number of total slices in percentage used is reduced from 88.5% to 38.2%. Then, it is possible to notice that moving the non-time-critical operation to the RT target allows for drastically reducing the FPGA resource utilization.

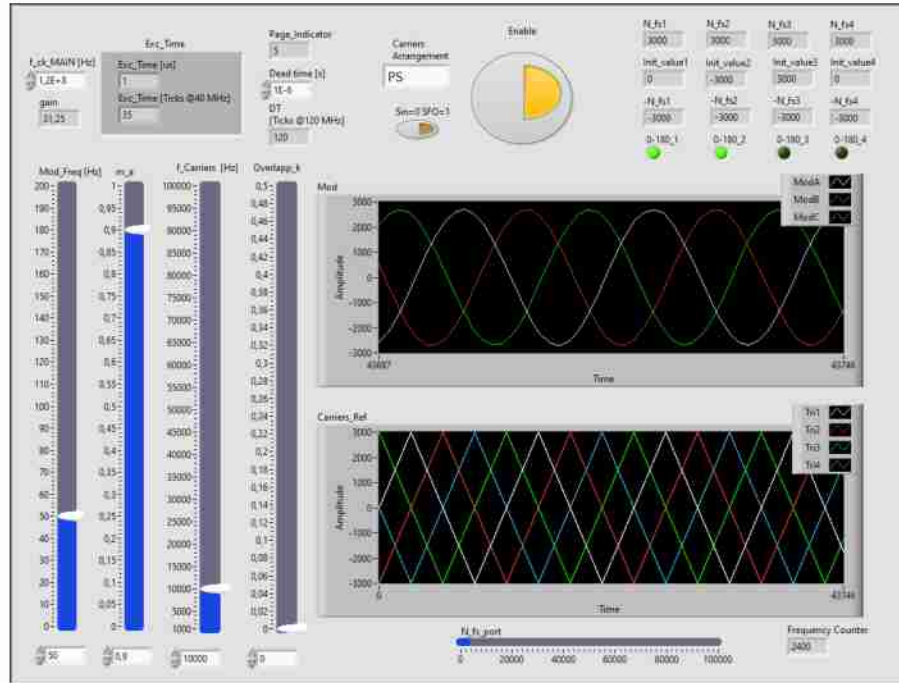


Fig. I. 14: Graphical User Interface implemented in LabVIEW Real-Time front panel.

Table I. 6: Control algorithm computational cost when it is implemented entirely in the FPGA target and when it is split between FPGA and RT targets.

Device Utilization	Available Resources	FPGA only [%]	FPGA + RT [%]
Total slices	13300	88.5	38.2
Slice registers	106400	31.9	12.4
Slice LUTs	53200	72.9	27.8
Block RAMs	140	5	5
DSP48s	220	7.7	2.7

I.7 Test Bench Description

In Fig. I. 15, a picture of the test bench housed at the SDESLAB at the University of Palermo is shown. In detail, it is composed of:

- a MOSFET-based 3P-5L-CHB inverter prototype, composed of six 5 kW HB modules, whose main nameplate data are reported in Table I. 7;
- six programmable DC power supplies RSP-2400 with rated DC voltage equal to 48 V, whose nameplate data are reported in Table I. 8;
- the PED-board equipped with SoM sbRIO 9651 described in the previous section;
- three constantan rheostats and a three-phase inductive load series connected with resistance and inductance equal to 20 Ω and 3 mH, respectively;

- a Teledyne LeCroy WaveRunner Oscilloscope 640Zi, equipped with two Yokogawa 700924 differential voltage probes and two Yokogawa 701933 current probes;
- two Yokogawa power meters (WT 330 and WT 130).

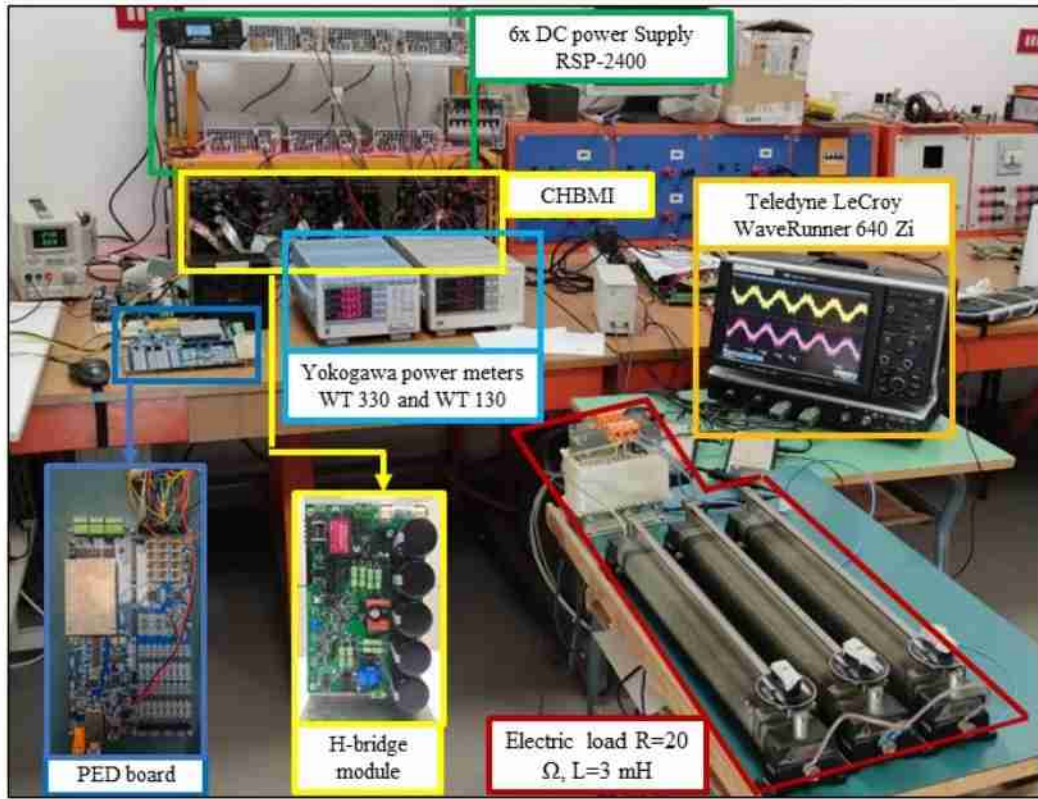


Fig. I. 15: Test bench at the Sustainable Development and Energy Saving Laboratory.

Table I. 7: CHBMI MOSFET IRFB4115PBF technical data.

Symbol	Quantity	Value
V_{dss}	Voltage	150 V
R_{dSon}	Resistance	9.3 m Ω
I_D	Current	104 A
T_{Don}	Turn on delay	18 ns
T_R	Rise time	73 ns
T_{Doff}	Turn off delay	41 ns
T_F	Fall time	39 ns
T_{RR}	Reversal Recovery	86 ns

Table I. 8: DC POWER SUPPLY RSP- 2400 technical data.

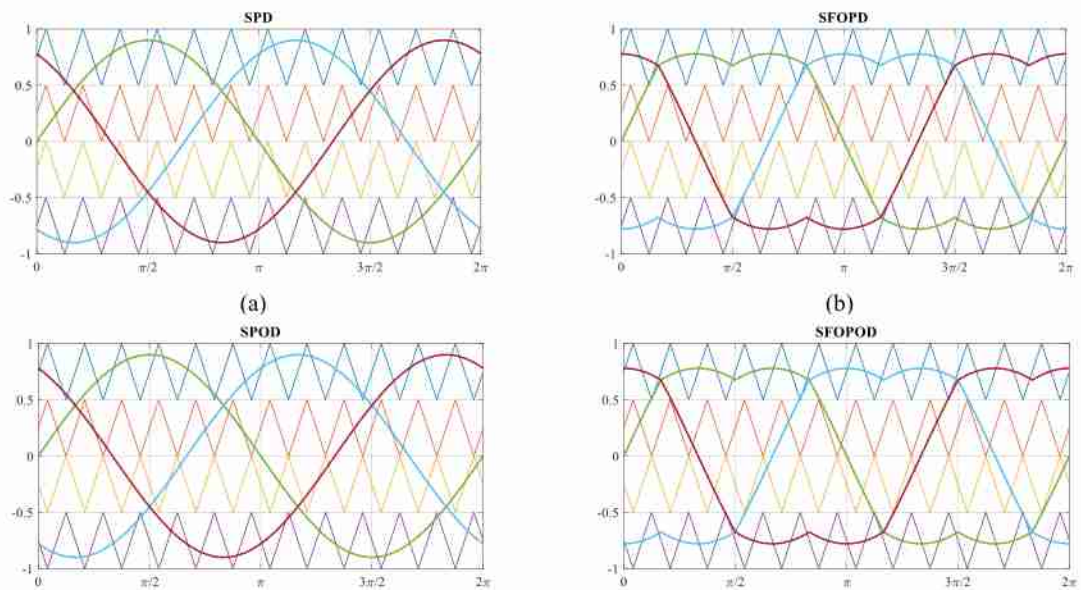
Symbol	Quantity	Value
V_{out}	Rated output voltage	48 V
I_{out}	Rated output current	50 A
P_N	Rated power	2400 W
ΔV	Ripple	200 mV _{p-p}
V_{in}	Input voltage range	180 ~ 264 VAC
$\cos\phi$	Power factor	0.95
η	Efficiency	91.5 %
I_{in}	Input current	12 A/230 Vac

The experimental investigation is carried out by acquiring both input and output electrical quantities of CHB inverter supplying a fixed RL load, resulting in a fixed value of Displacement Power Factor (DPF). Since the input CHB electrical quantities present

continuous waveforms with negligible harmonic content, the input CHB power is measured by two conventional power analyzers (Yokogawa WT 330 and WT 130) with a sampling frequency equal to 100 kS/s. Whereas, the CHB output electrical quantities exhibit a larger harmonic content, then the CHB output quantities are acquired and analyzed by a Teledyne LeCroy WaveRunner Oscilloscope 640Zi equipped with Yokogawa 701933 current and Yokogawa 700924 voltage probes. The international standards IEC 61800-9-1 and IEC 61800-9-2, for accurate active power measurement, recommend a measurement bandwidth range from 0 to 10 times the switching frequency f_{sw} for traditional 2L-VSIs. Therefore, a sampling frequency equal to 10 MS/s is adopted, with an observation window of 0.1 s. In detail, this choice allows for performing an accurate analysis in the frequency domain of electrical quantities and accurate CHB output power measurement with switching frequency values up to 1 MHz, and with a frequency resolution of 10 Hz.

I.8 Experimental Evaluation of the Switching Frequency Impact on CHB Performance

In this section, an extended experimental analysis that aims to evaluate the switching frequency impact on the MC-PWM-driven CHB performance is carried out. In detail, the experimental tests are conducted by supplying an RL load. By combining the previously discussed MC-PWM strategies and modulating signals, 10 different modulation schemes, reported in Fig. I. 16, are obtained. CHB inverter performance, in terms of voltage THD and inverter efficiency η , are evaluated for every modulation scheme over a working range identified by the amplitude modulation index $M \in \{0.3, 0.6, 0.9, 1.15\}$ and the switching frequency $f_{sw} \in \{10, 20, 30, \dots, 70 \text{ kHz}\}$. Table I. 9 summarizes the main system under test parameters and the analyzed working range.



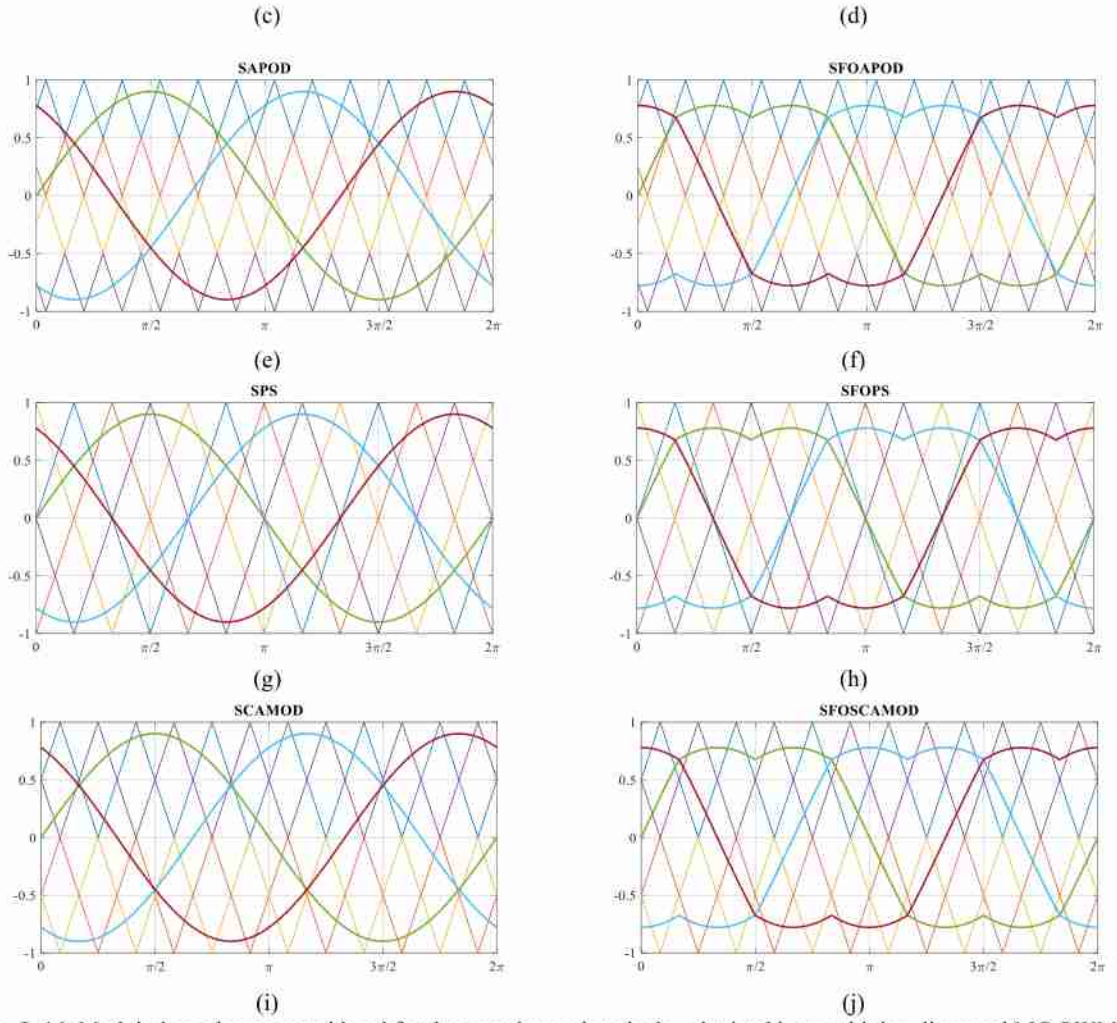


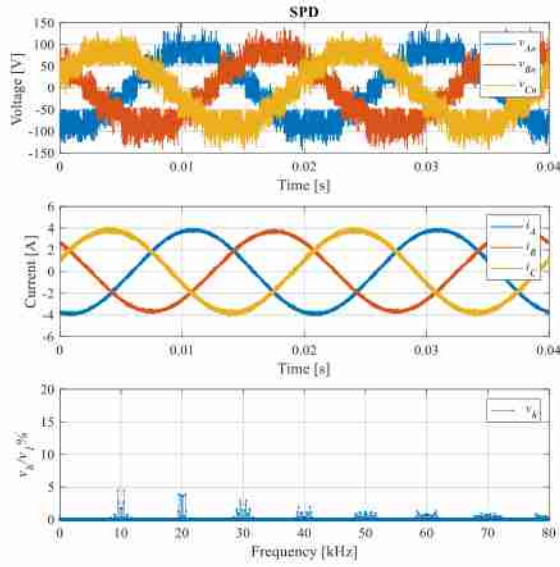
Fig. I. 16: Modulation schemes considered for the experimental analysis , obtained by combining discussed MC-PWM strategies and modulating signals: (a) SPD, (b) SFOPD, (c) SPOD, (d) SFOPD, (e) SAPOD, (f) SFOAPOD, (g) SPS, (h) SFOPS, (i) SCAMDOD, (j) SFOSCAMOD.

Table I. 9: Main system under test parameters and the analyzed working range

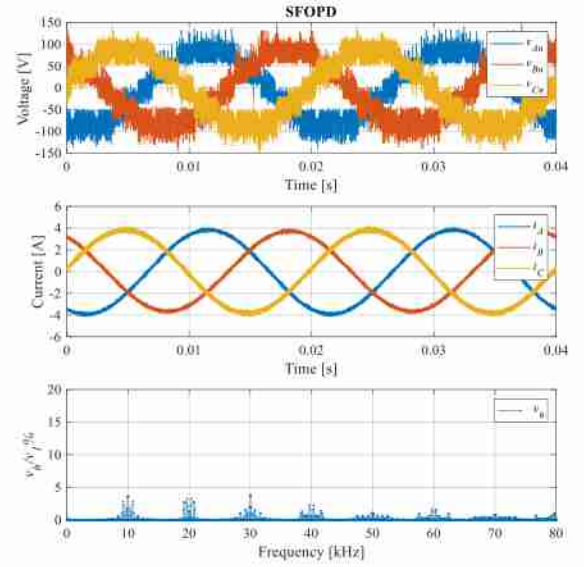
Quantity	Symbol	Value
DC voltage	V_{DC}	48 V
Fundamental frequency	f	50 Hz
Load resistance	R	20 Ω
Load inductance	L	3 mH
Switching frequency range	f_{sw}	10 kHz – 70 kHz
Modulation index range	M	0.3 – 1.15
Dead-time	t_{dt}	1 μ s

I.8.1 AC and DC Side Electric Quantities Analysis

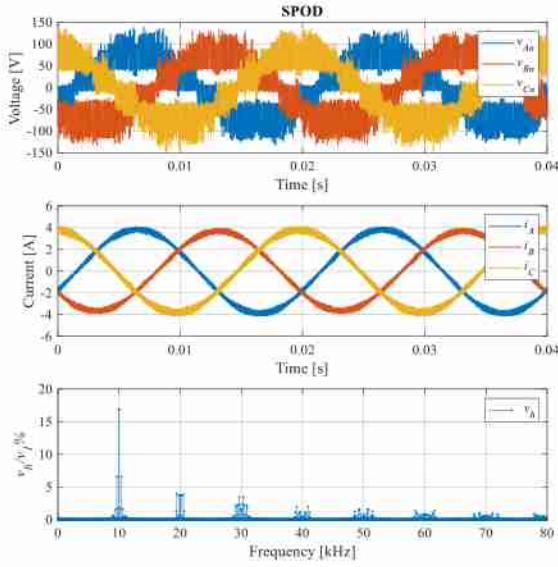
In Fig. I. 17, measured load voltages v_{An} , v_{Bn} , and v_{Cn} , the phase currents i_A , i_B , and i_C , and the voltage spectra, obtained by the 10 modulation schemes when $f_{sw}=10$ kHz and $M=0.9$, are reported.



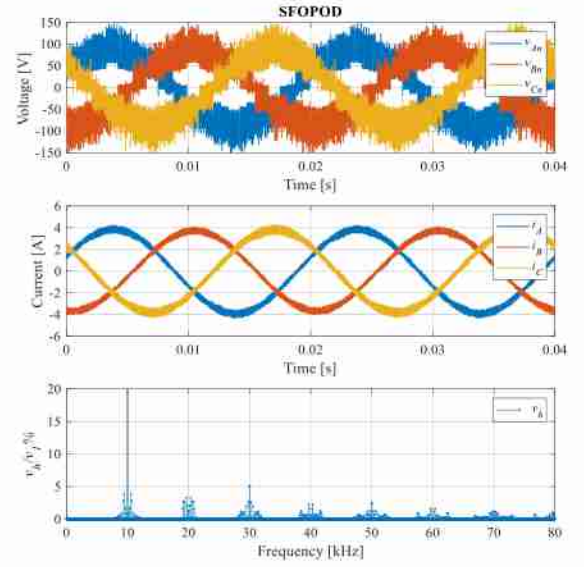
(a)



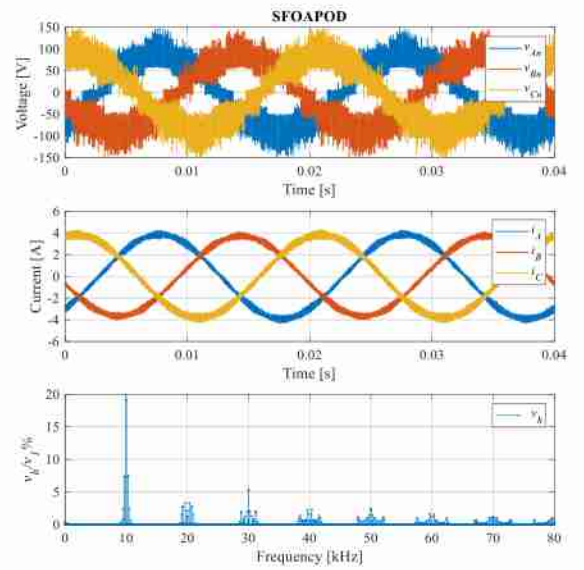
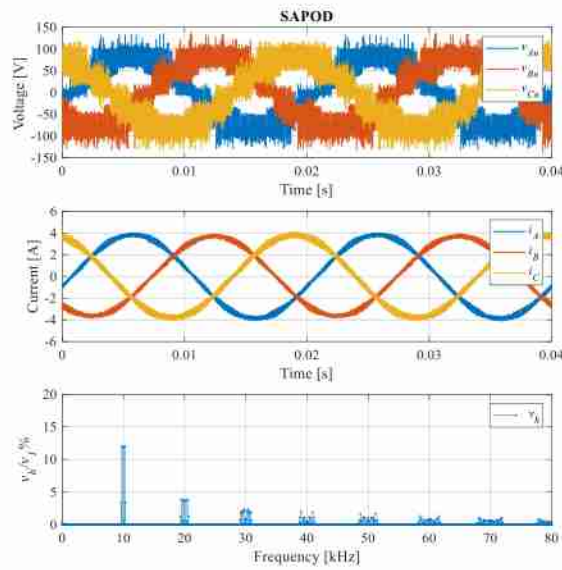
(b)



(c)



(d)



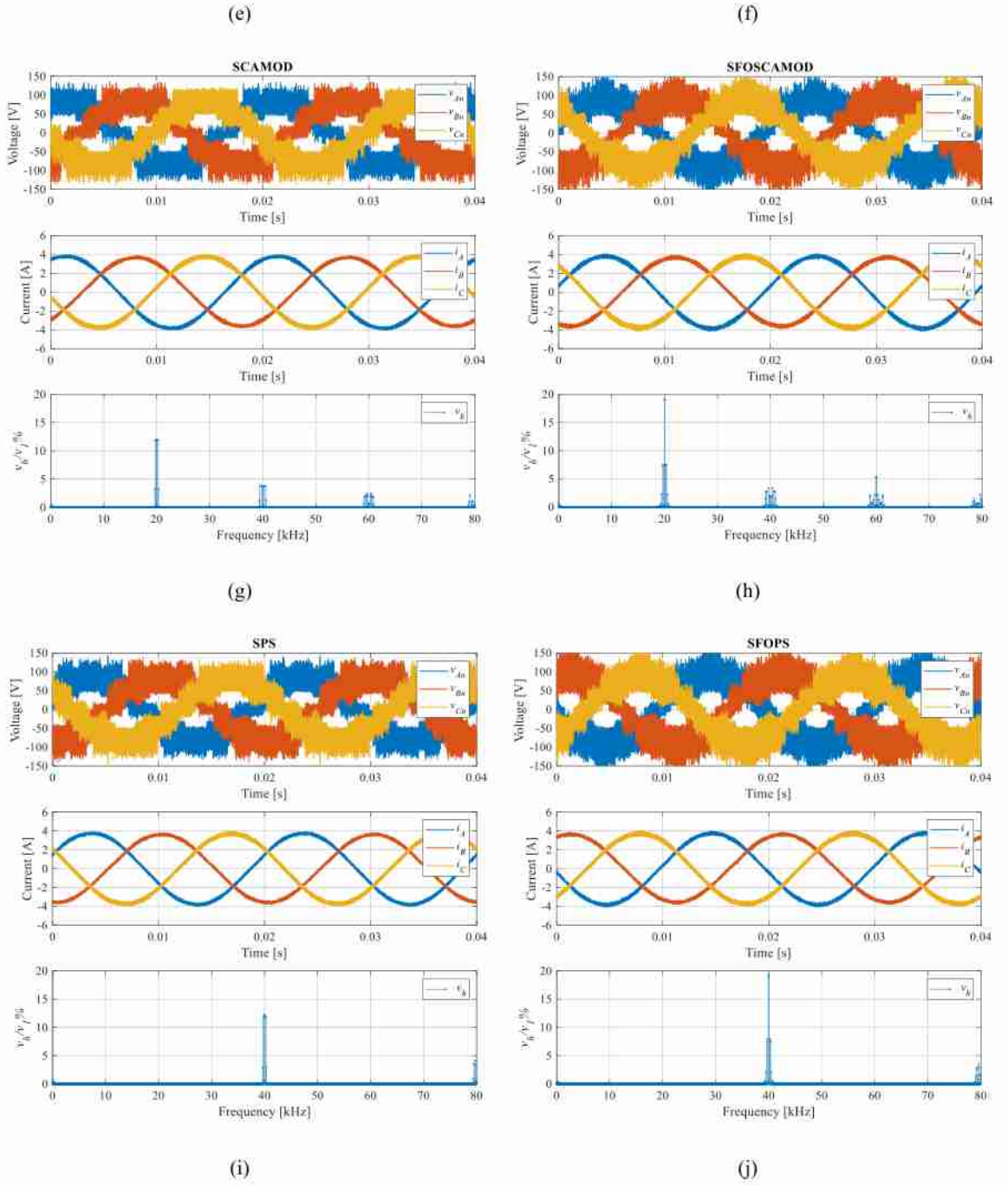
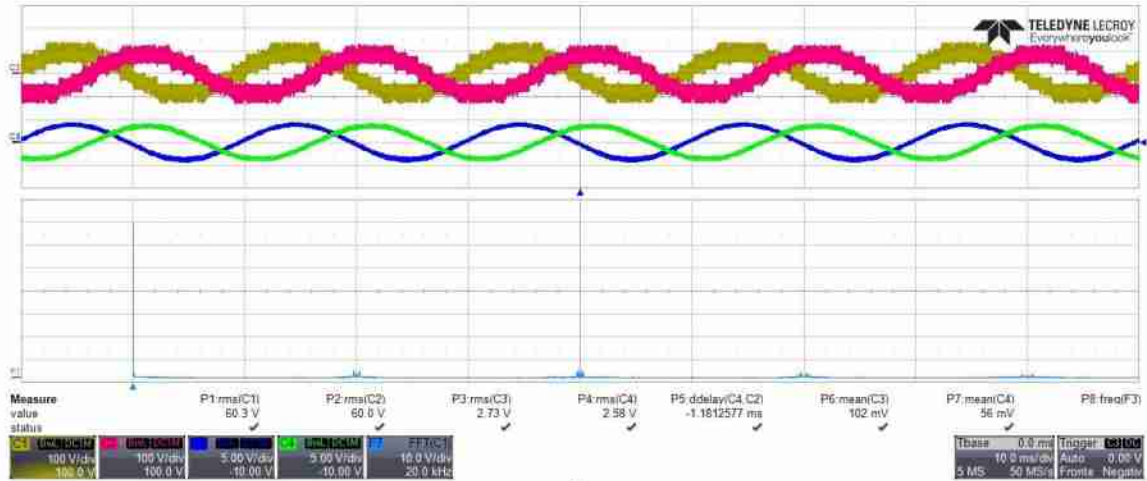


Fig. I. 17: Measured CHB load voltages, phase currents, and voltage spectra of the adopted MC-PWM strategies when $M=0.9$ and $f_{sw}=10$ kHz: (a) SPD, (b) SFOPD, (c) SPOD, (d) SFOPD, (e) SAPOD, (f) SFOAPOD, (g) SCAMOD, (h) SFOSCAMOD, (i) SPS, (j) SFOPS.

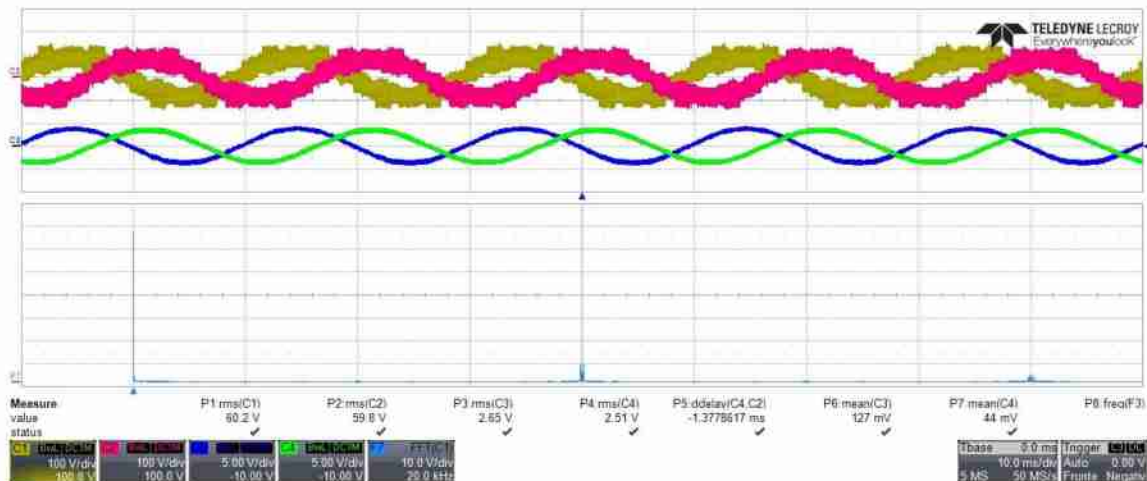
It should be noted that voltages generated with an LS-PWM strategy, shown in Fig. I. 17 (a)-(f), exhibit a spectrum with harmonics centered at the switching frequency, equal to 10 kHz, and its integer multiples. Moreover, more significant harmonics are up to 40 kHz. Voltages generated with the PS-PWM strategy, shown in Fig. I. 17 (g)-(h), exhibit a spectrum with harmonics centered at four times the switching frequency, i.e., 40 kHz, and its integer multiples. More significant harmonics are up to sixteen times the switching frequency, equal to 160 kHz. Voltages generated with the SCAMOD strategy, shown in Fig. I. 17 (i)-(j), exhibit an intermediate behaviour between LS and PS modulation schemes. In detail, the

first harmonics are centered at two times the switching frequency, equal to 20 kHz, and more significative harmonics are up to eight times the switching frequency, equal to 80 kHz.

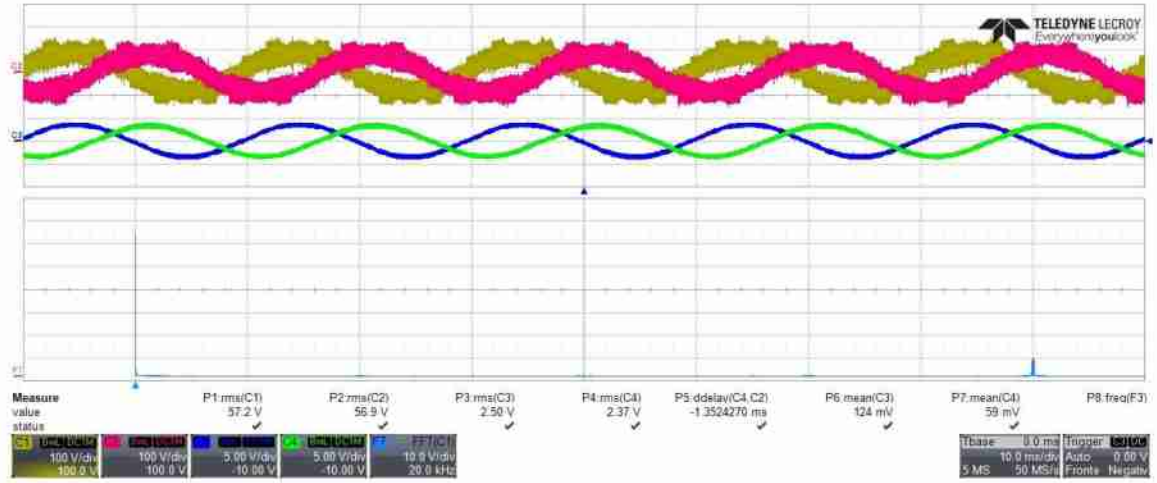
As a way of example, oscilloscope screens of the load voltages, phase currents, and voltage spectra generated by SPD, SCAMOD, and SPS modulation strategies, with $M=0.9$ and $f_{sw}=40$ kHz, are reported in Fig. I. 18 (a), (b), and (c), respectively. In detail, the acquisitions are carried out over an acquisition window of 0.1 s, with the voltage scale set to 100 V/div, the current scale set to 5 A/div, the harmonic spectra in the frequency domain set to 10 V/div and 20 kHz/div. It can be noted that the same phenomena, previously described, are recorded also in this case. Thus, these results confirm that each modulation scheme displaces harmonics in the frequency domain depending on the selected switching frequency, according to the discussion carried out in Section I.3. Moreover, it is possible to demonstrate the effectiveness of the control algorithm implemented and described in the previous section.



(a)



(b)



(c)

Fig. I. 18: Measured CHB load voltages, phase currents, and voltage spectra when $M=0.9$ and $f_{sw}=40$ kHz: (a) SPD, (b) SCAMOD, (c) SPS.

To complete the voltage waveform time-domain analysis, in Table I. 10 some waveform features are summarized; in detail, the number of phase voltage and line-to-line voltage levels, the maximum load voltage instantaneous value, and the frequency with the maximum harmonic amplitude are presented. It is interesting to note that these features depend on the chosen modulation scheme and modulating signals, but they are not affected by the switching frequency.

Table I. 10: Main phase voltage, line-line voltage and load voltage waveforms features for every considered MC-PWM strategies.

Type	Frequency with maximum harmonic amplitude	Number of phase voltage V_{aN} levels	Number of line-to-line voltage V_{ab} levels	Load voltage V_{an} maximum value with S modulating signals	Load voltage V_{an} maximum value with SFO modulating signals
PD	f_{sw}	5	9	$7/3 V_{dc}$	$7/3 V_{dc}$
POD	f_{sw}	5	9	$7/3 V_{dc}$	$8/3 V_{dc}$
APOD	f_{sw}	5	9	$2 V_{dc}$	$8/3 V_{dc}$
PS	$4 f_{sw}$	5	9	$2 V_{dc}$	$8/3 V_{dc}$
SCAMOD	$2 f_{sw}$	5	9	$2 V_{dc}$	$8/3 V_{dc}$

Attention is paid also to the DC side. In detail, with respect to a n_l -level 3P-CHB, it is possible to define n_{HB} triplets, where a triplet is a set of three HB modules sharing the same carriers. Concerning the 3P-5L-CHB scheme reported in Fig. I. 4, it is possible to define the upper and lower HB modules triplets: the upper triplet is composed of three HB modules, whose GCSs are generated trough carriers T_1 and T_4 or, equivalently, HB modules controlled by GCSs named $S_{j,1z}$; the lower tern is composed of three HB modules, whose GCSs are generated trough carriers T_2 and T_3 or, equivalently, HB modules controlled by GCSs named $S_{j,2z}$. Since HB modules belonging to the same triplet share the same carriers, and assuming the three-phase load is balanced, then HB modules belonging to the same triplet lead the

same amount of power to the load, and the total DC power $P_{DC,i}$ absorbed by the i^{th} triplet is defined as:

$$P_{DC,i} = P_{a,HBi} + P_{b,HBi} + P_{c,HBi} \quad (I,39)$$

where $P_{a,HBi}$, $P_{b,HBi}$, and $P_{c,HBi}$ are the DC power absorbed by the HB modules belonging to the i^{th} triplet and to the phase a , b , and c , respectively. Then, it is possible to investigate the DC power distribution among cascaded triplets when MC-PWM strategies are employed over the defined working range, as shown in Fig. I. 19. It is possible to note that LS-PWM strategies result in an uneven DC power absorption among triplets for every modulation index M . Moreover, when M is lower than 0.5, the upper triplet is not leading power to the load at all. This behaviour can be justified by looking at the LS-PWM modulation schemes shown in Fig. I. 16 (a)-(f). Indeed, if $M < 0.5$, the modulating signals never intersect the external carriers and, as a consequence, one of the two triplets is not switching at all. On the other side, PS and SCA PWM guarantee an even DC power distribution over the entire working range.

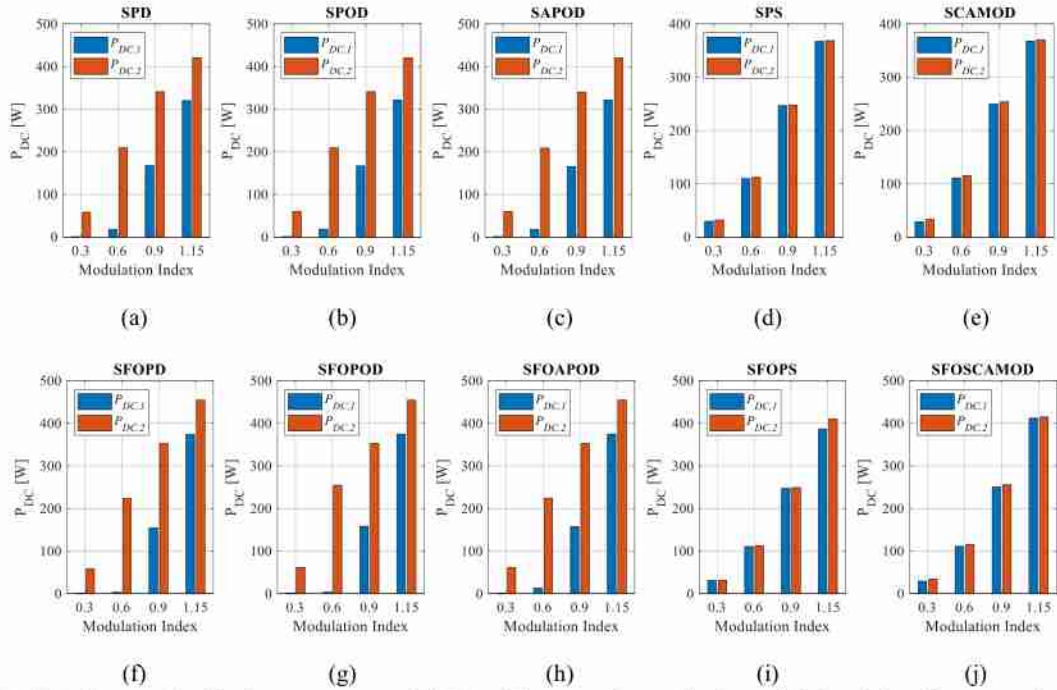


Fig. I. 19: DC power distribution among cascaded HB triplets over the amplitude modulation index, for every adopted MC-PWM strategy, $f_{sw}=10$ kHz.

I.8.2 Voltage Total Harmonic Distortion Analysis

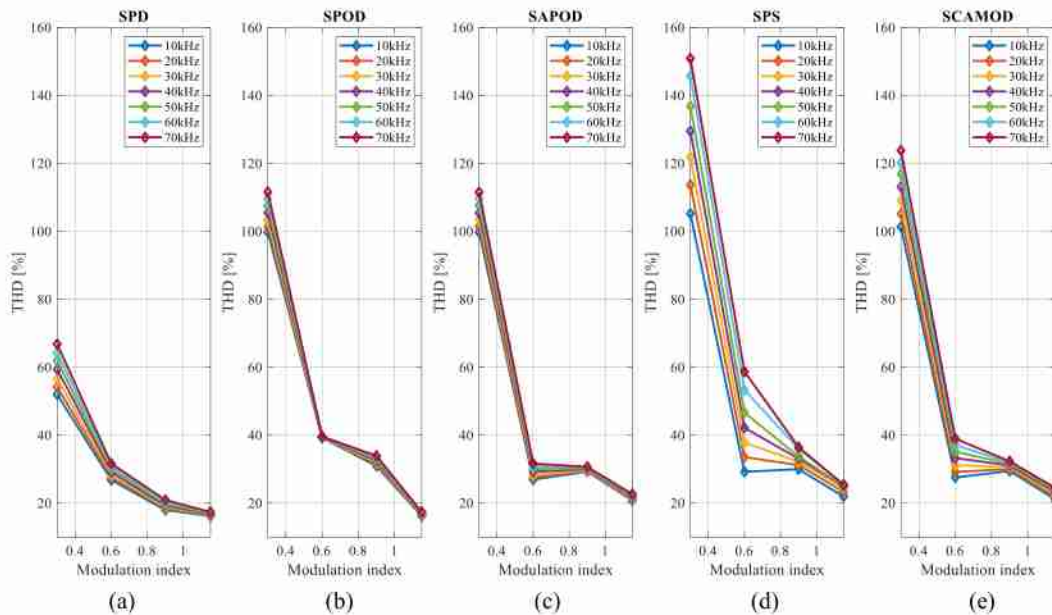
To investigate the performance of the converter, in terms of harmonic distortion, the THD% index is adopted. It is defined as follows:

$$THD_{\%} = 100 \cdot \sqrt{\frac{S_{RMS}^2 - S_{1,RMS}^2}{S_{1,RMS}^2}} \quad (I,40)$$

where S_{RMS} is the RMS value of the generic electric quantity S , and $S_{1,RMS}$ is the RMS value of its fundamental harmonic. By adopting a sampling frequency equal to 10 MS/s, in the $THD_{\%}$ evaluation the harmonics up to 5 MHz can be considered, according to the Shannon theory.

Fig. I. 20 shows the voltage THD trends as a function of the modulation index M for every MC-PWM strategy and every considered switching frequency value. By looking at Fig. I. 20, several considerations can be carried out: generally, an increase in the switching frequency always generates an increase also in the voltage THD. Such a phenomenon is recorded for every considered MC-PWM strategy and for every modulation index value and can be justified by looking at the trend of the fundamental voltage harmonic amplitude over the switching frequency, reported in Fig. I. 21. It is possible to note a slight reduction in the fundamental harmonic amplitude, and even in this case, it is common to every MC-PWM strategy and every modulation amplitude value. However, the fundamental voltage harmonic reduction slope is correlated to the apparent switching frequency. In detail, the higher the apparent switching frequency, the higher the voltage fundamental harmonic reduction slope.

In detail, by increasing the switching frequency the GCSs duration is gradually reduced, becoming similar to the DT. Thus, this phenomenon generates the cancellation of some GCSs and the increase of the overall distortion, if compared to the ideal GCSs without DT. Such a fundamental harmonic reduction is correlated to the DT effect, as will be discussed much more in detail in the next section.



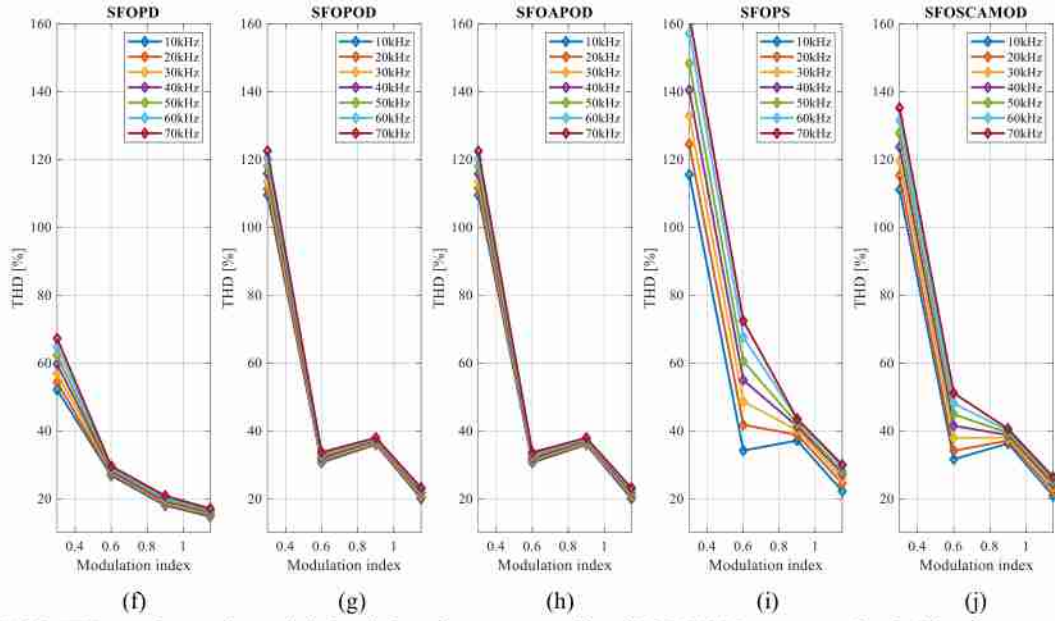


Fig. I. 20: THD trend over the modulation index, for every considered MC-PWM strategy and switching frequency value.

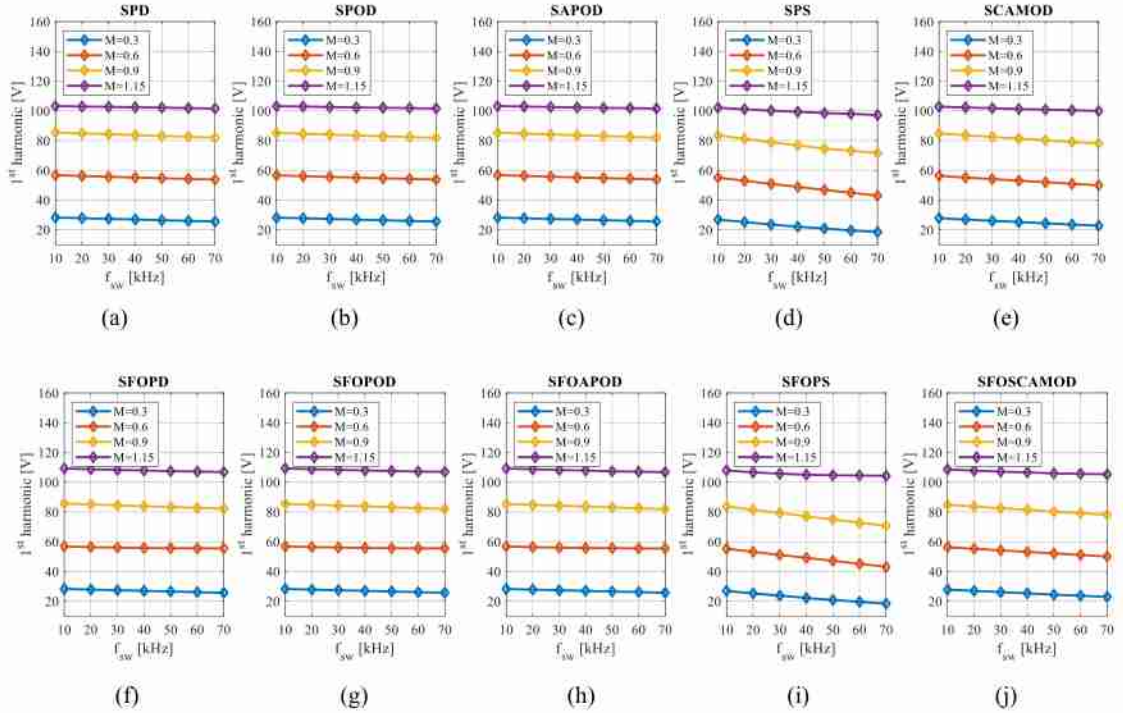


Fig. I. 21: 1st voltage harmonic trend over the switching frequency for every considered MC-PWM strategy and amplitude modulation index value.

In Fig. I. 22, cross-comparison among the adopted MC-PWM strategies is reported. In detail, the THD is reported for fixed amplitude modulation index M over the defined switching frequency range. Indeed, LS-PWM strategies exhibit the least THD growth, among the MC-PWM strategies. Moreover, such a THD increase is more evident at low modulation index values. SPD-PWM strategy exhibits the lowest THD for every value of the modulation index and every switching frequency, with a maximum value equal to about 70% when $M=0.3$, and a minimum value of about 15% in the overmodulation region. SPOD and SAPOD

exhibit similar behavior: in detail, they generate a voltage THD comparable to the SPD only in the overmodulation region (about 20%); over the rest of the working region, they exhibit a much higher voltage THD, with a maximum value of 110% when $M=0.3$. SPS exhibit the worst harmonic behaviour over the entire working range, with a minimum THD value which is higher than 20% and a maximum THD value of about 150%. It can be noted that, for fixed modulation index, increasing the switching frequency causes a drastic voltage THD increase (for example from 30% to 60%, moving from 10 to 70 kHz when $M=0.6$). SCA modulation exhibits an intermediate behaviour between LS and PS PWM strategies, with a minimum THD equal to 21 % and a maximum value equal to 120%.

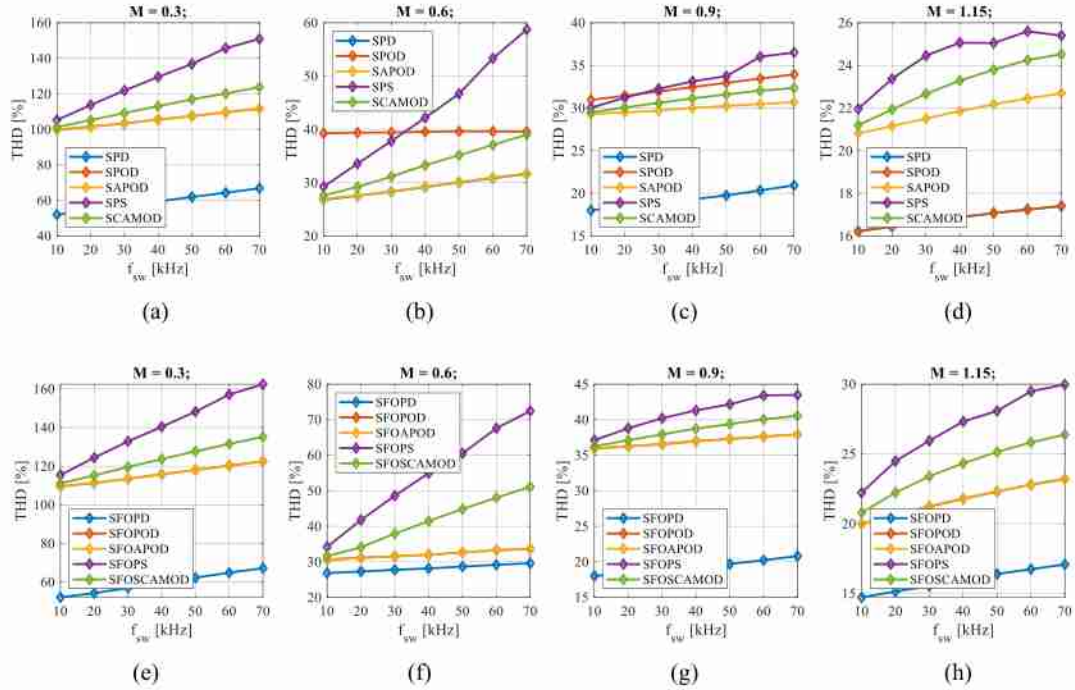


Fig. 1.22: THD trends over the switching frequency, for every considered MC-PWM strategy and every modulation index.

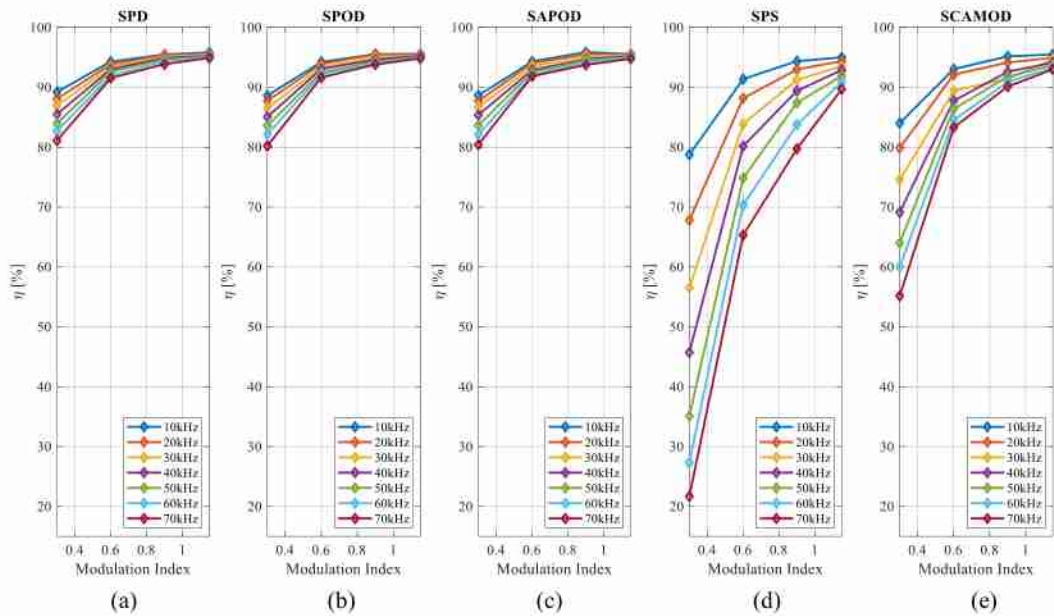
Regarding the choice of modulating signal, similar considerations can be carried out when SFO modulating signals are adopted. In detail, SFO modulating signals cause an increase in voltage THD almost for every MC-PWM strategy and modulation index value, except for APOD PWM when $M=0.6$, where a slight reduction of the THD is recorded.

1.8.3 CHB Inverter Efficiency Analysis

The second quantity analyzed and used for converter performance comparison purposes is the conversion efficiency η , expressed in percent as:

$$\eta = \frac{P_{AC}}{\sum_{i=1}^{n_{HB}} P_{DC,x}} \cdot 100 \quad (I,41)$$

where P_{AC} is the AC output power. Fig. I. 23 shows the conversion efficiency trends as a function of the modulation index M for every MC-PWM strategy and every considered switching frequency value. Generally, an increase in the switching frequency causes a reduction in the conversion efficiency. Such a phenomenon is related to the increase of CHB commutations that generate an increase in the switching losses. It can be noted that, as discussed for the THD trends, the efficiency decrease is strictly correlated to the apparent switching frequency. In detail, the higher the apparent switching frequency, the greater the efficiency decrease. Indeed, LS-PWM strategies exhibit similar behavior and guarantee the maximum efficiency for every modulation index and every switching frequency value, with a minimum value of 80% when $M=0.3$, and a maximum value of 96% when $M=1.15$. On the contrary, PS-PWM exhibits the worst efficiency for every switching frequency and for every modulation index value, with a minimum value of 20% when $M=0.3$, and a maximum value of 95% when $M=1.15$. Anyhow, it is necessary to observe that switching frequencies up to 30 kHz efficiency values are comparable with the LS-based schemes. Moreover, it is necessary to consider that adopting PS-based schemes allows for easier voltage and current filtering if compared to the LS-PWM with the same switching frequency. SCAMOD confirms an intermediate behaviour between LS and PS strategies, with minimum and maximum efficiency values equal to 55% and 96%, respectively.



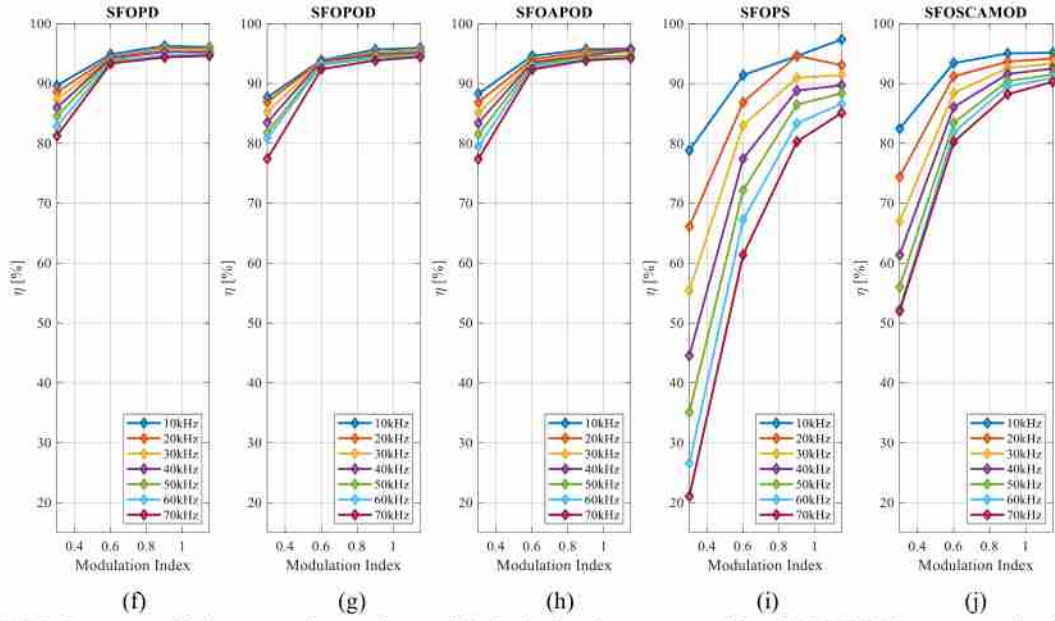


Fig. I. 23: Converter efficiency trends over the modulation index, for every considered MC-PWM strategy and switching frequency value.

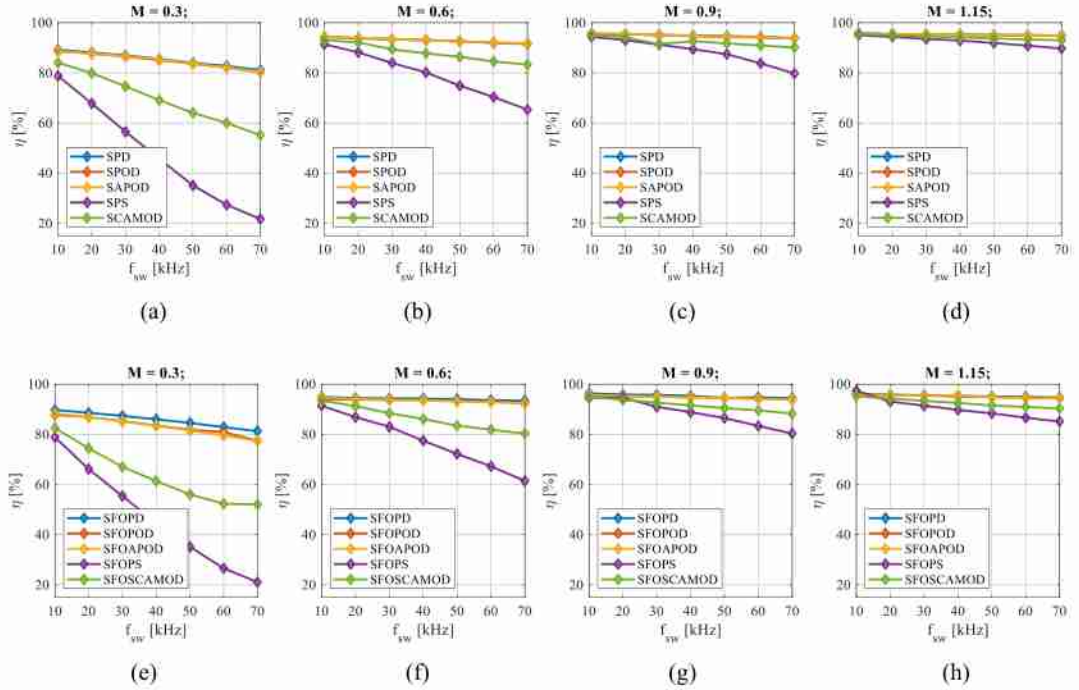


Fig. I. 24: Converter efficiency over the switching frequency, for every considered MC-PWM strategy and for every modulation index value.

In Fig. I. 24, some cross-comparison among adopted MC-PWM strategies as a function of the switching frequency, for fixed values of the modulation index, are shown. It is possible to note that, the efficiency reduction due to the switching frequency increase is also correlated to the modulation index value. In detail, for fixed MC-PWM strategy, the lower the modulation index, the deeper the efficiency reduction. Such a phenomenon can be explained by considering that for high modulation index values, which correspond to high

values of the AC output power, the conduction losses are predominant, and, for this reason, the switching frequency effect on the conversion efficiency is reduced.

Concerning the modulating signals impact on the converter efficiency, it is possible to note that efficiency trends with sinusoidal and SFO modulating signals are comparable, then previous considerations are valid also for SFO modulating signals. However, SFO determines a slight reduction in the converter efficiency.

I.9 Fundamental Harmonic Voltage Drop Due to the Dead Time Effect Mathematical Formulation

Experimental analysis conducted in Section I.8 showed that the increase in the switching frequency is correlated to a reduction of the voltage fundamental harmonic. Such a reduction could be correlated to the DT effect. Then, in this section, the DT effect is deeply investigated to evaluate its impact both on the voltage fundamental harmonic and on the voltage harmonic distortion. The goal is to analytically estimate the fundamental harmonic voltage drop Δv due to the DT effects, for a generic n_l -level CHB, taking into account the adopted MC-PWM strategy. With this aim, the modular modeling approach introduced in Section I.2 is adopted, i.e., the CHB model is obtained as the mathematical linear composition of several HB modules models. In detail, with respect to Fig. I. 1, the HB legs are treated as two paralleled Half Bridges independently controlled by a traditional PWM strategy, whose scheme is reported in Fig. I. 25 (a). The DT is introduced by splitting the modulating signal u into $u+k$ and $u-k$, according to the method discussed in Section I.4. It must be underlined that moving from the Half Bridge to the HB and finally to the CHB over the following discussion, it is supposed that the total DC link voltage U_{dc} is constant.

According to equations (I,27) and (I,28), the Half Bridge GCSs S_1 and S_2 , reported in Fig. I. 25 (b), are generated. DT leads to an output voltage width variation, if compared to the ideal case, which depends on the sign of the load current i_L . In detail, in each switching period T_{PWM} , the Half-Bridge output voltage impulse v_{xo} , is larger when the current is negative and it is shorter when the current is positive, if compared to the theoretical case, as shown in Fig. I. 25 (c). This behavior depends on whether the diodes are involved in the current circulation path. According to [I,34], neglecting the devices turn-on and turn-off times, the mean voltage drop Δv on a switching period T_{PWM} can be expressed as follows:

$$\Delta v = \begin{cases} -\frac{t_{dt}}{T_{PWM}} U_{dc}, & i_L > 0 \\ +\frac{t_{dt}}{T_{PWM}} U_{dc}, & i_L < 0 \end{cases} = -\Delta V \cdot \text{sgn}(i_L) \quad (\text{I,42})$$

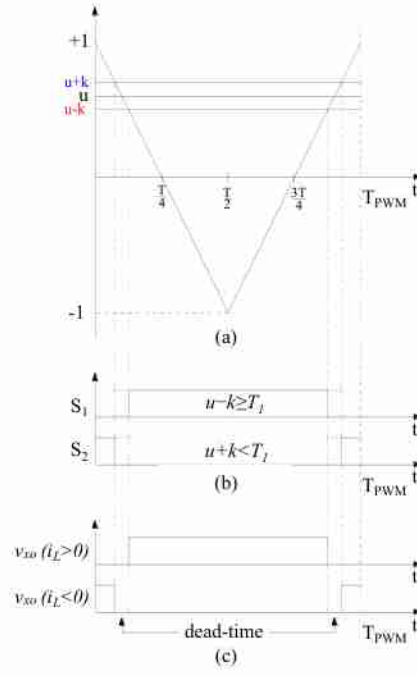


Fig. I. 25: (a) PWM control scheme, composed of one period of the carrier signals, ideal modulating sample u (black) and real modulating samples $u+k$ and $u-k$, split due to the DT; (c) GCSs G_1 and G_2 in the ideal case (dash line) and real case (continuous line) when DT is applied; (d) half-bridge output voltage v_{xo} when the load current i_L is positive and negative.

where t_{dt} is the DT, i_L is the load current, U_{dc} is the total DC-link voltage, and ΔV is the voltage drop module, which can also be expressed as:

$$\Delta V = \frac{t_{dt}}{T_{PWM}} U_{dc} = t_{dt} f_{sw} U_{dc} \quad (I,43)$$

Considering the instantaneous value of the fundamental harmonic v_{xo}^I , due to the DT effects, it is modified as:

$$v_{xo}^I = v_{xo,id}^I - \Delta V \cdot \text{sign}(i_L) \quad (I,44)$$

where $v_{xo,id}^I$ is the output voltage fundamental harmonic in the ideal case with no DT applied. According to the equation (I,44), the output voltage fundamental harmonic is distorted by the superposition of a square wave, whose amplitude depends on the DC link voltage, on the chosen DT and the switching frequency, and whose sign depends on the load current sign and, consequently, on the power factor. When the current is positive, the fundamental harmonic is decreased, when negative, it is increased.

Considering the whole HB module, it is composed of two legs which correspond to two Half-Bridges. Each leg can be independently controlled by assigning independent carrier signals. In this case, the adopted PWM strategy is the traditional Unipolar PWM strategy, whose modulation scheme and GCSs in a switching period T_{PWM} are shown in Fig. I. 26.

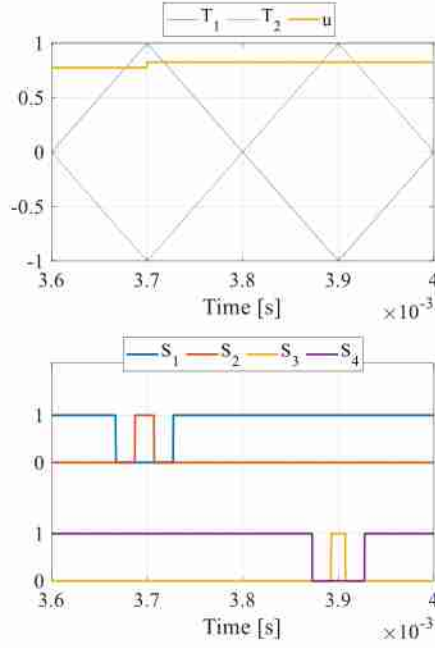


Fig. 1. 26: Traditional Unipolar PWM modulation strategy for single-phase H-Bridge and gate signals in a switching period T_{sw} .

It can be noted that each power switch exhibits only one on-off cycle over a switching period T_{PWM} . This behavior is independent of the modulation index M until the converter works in the linear region. The DT effect on the HB output voltage fundamental harmonic v_{xy}^l is obtained by combining equations (I,5), which express the HB output voltage as a function of the leg voltages, and (I,44):

$$v_{xy}^l = v_{xy,id}^l - 2 \cdot \Delta V \cdot \text{sign}(i_L) \quad (\text{I,45})$$

where $v_{xy,id}^l$ is the output voltage fundamental harmonic in the ideal case with no DT applied.

Now, one phase of a generic n_l -level CHB, where the total DC link voltage U_{dc} is expressed according to (I,20), is considered. Then it is possible to define the voltage drop module $\Delta V_{HB,i}$ as:

$$\Delta V_{HB,i} = t_{dt} f_{sw} V_{dc} \quad (\text{I,46})$$

The output voltage fundamental harmonic v_{aN}^l is obtained by combining equations (I,7), (I,45), and as follows:

$$v_{aN}^l = v_{aN,id}^l - 2 \cdot n_{HB} \cdot \Delta V_{HB,i} \cdot \text{sign}(i_L) \quad (\text{I,47})$$

By replacing (I,46) in (I,47) and by taking into account equation (I,20), it follows:

$$v_{aN}^l = v_{aN,id}^l - 2 \cdot n_{HB} \cdot t_{dt} f_{sw} V_{dc} \cdot \text{sign}(i_L) \quad (\text{I,48})$$

$$v_{aN}^l = v_{aN,id}^l - 2 \cdot t_{dt} f_{sw} U_{dc} \cdot \text{sign}(i_L) \quad (\text{I,49})$$

The second term in equation (I,49) represents the total voltage drop due to the DT on the phase voltage. It can be noted that the voltage drop in relation (I,49) coincides with the voltage drop in equation (I,45). It means that, for fixed DT, fixed switching frequency f_{sw} and fixed total DC link voltage U_{dc} , the total voltage drop module on CHB phase voltage is the same as the traditional single-phase HB. This result can be explained as follows: although CHB is characterized by a higher number of commutations in the considered T_{PWM} due to the higher number of power switches, each of them causes a little voltage drop since each HB module is powered by a fraction of the total DC link voltage U_{dc} .

It must be underlined that relation (I,49) is valid only if each cascaded HB module per phase has the same behavior in terms of the number of commutations per T_{PWM} . In this context, the adopted MC-PWM strategy plays a key role, thus it must be considered. In Fig. I. 27 (a-c) the modulation scheme and GCSs generated in a T_{PWM} , for PS, PD, and SCAMOD strategies, are represented, respectively. Looking GCSs generated by the PS-PWM strategy, reported in Fig. I. 27 (a), it can be noted that each HB module is controlled with the traditional Unipolar PWM strategy. As a consequence, each HB module follows the same switching pattern over a T_{PWM} but properly time-shifted, so the relation (I,49) is valid. Taking into account a PD-PWM strategy, according to the GCSs in a T_{PWM} reported in Fig. I. 27 (b), only one Half-Bridge per T_{PWM} changes its state, which means that Half-Bridge modules are not working in the same way in the considered T_{PWM} , and so relation (I,49) must be modified. For a generic n_l -level CHB, when PD-PWM is adopted, only one Half-Bridge per phase changes its state in a T_{PWM} , this means that $2n_{HB}$ fewer commutations occur in the considered period, if compared to the PS-PWM strategy. Thus, taking into account relations (I,20) and (I,46), equation (I,49) must be modified as follows:

$$v_{aN}^1 = v_{aN,id}^1 - \frac{1}{2n_{HB}} 2 \cdot t_{dt} f_{sw} U_{dc} \cdot \text{sgn}(i_L) = v_{aN,id}^1 - t_{dt} f_{sw} V_{DC} \cdot \text{sgn}(i_L) \quad (\text{I,50})$$

In this case, the voltage drop due to DT is independent of the number of series connected HB modules, since only one Half-bridge is switching per T_{PWM} . According to (I,50), when LS-PWM is adopted, the voltage drop is $2n_{HB}$ times lower than the voltage drop with the PS-PWM strategy. Such considerations are also valid for other LS-PWM strategies (POD, APOD) since the mutual carriers phase shift does not have such influence on the number of commutations per T_{PWM} .

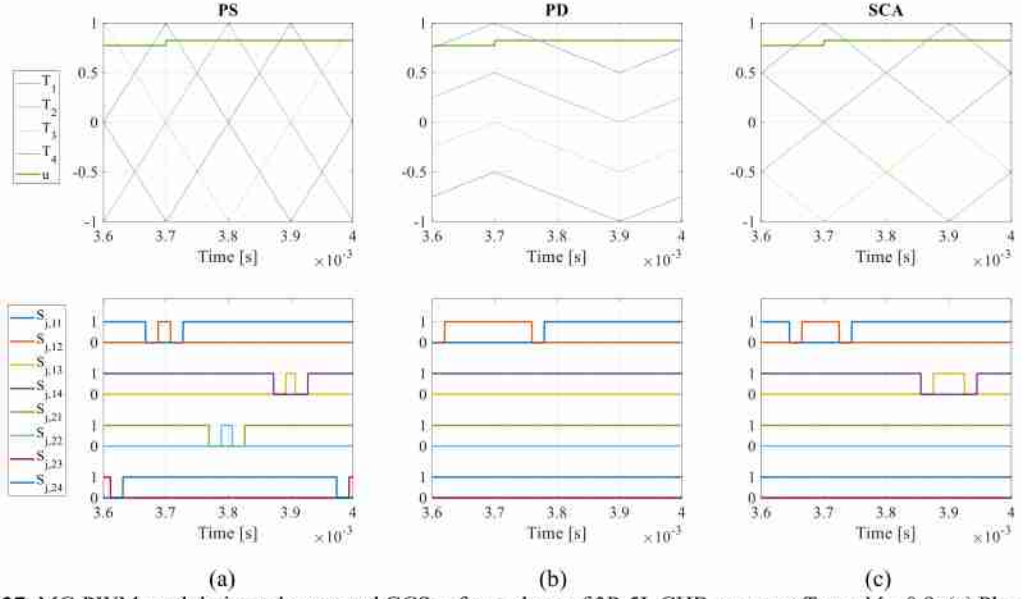


Fig. I. 27: MC-PWM modulation schemes and GCSs of one phase of 3P-5L CHB over one T_{PWM} , $M=0.9$: (a) Phase Shifted (b) Phase Disposition, (c) SCA-PWM.

When SCAMOD is adopted, according to Fig. I. 27 (c), two commutations per T_{PWM} occur. This behaviour is independent of the number of cascaded HB modules per phase since the modulating signal can intercept only two of the n_l-1 carriers signals in a T_{PWM} . Thus, only two Half Bridges are switching. Taking into account such considerations, the relation (I,49) must be modified as:

$$v_{aN}^l = v_{aN,id}^l - \frac{1}{n_{HB}} 2 \cdot t_{dt} \cdot f_{sw} U_{dc} \cdot \text{sgn}(i_L) = v_{aN,id}^l - 2 \cdot t_{dt} \cdot f_{sw} V_{dc} \text{sgn}(i_L) \quad (\text{I,51})$$

According to (I,51), when SCAMOD is adopted, the voltage drop is n_{HB} -times lower than the voltage drop with the PS-PWM strategy.

Unless the converter works in the linear region, all the previous considerations are independent by the amplitude modulation index M , as can be noted in Fig. I. 28, where carriers, modulating signals, and gate control signals of one phase of 3P-5L CHB in a T_{PWM} are represented for $M=0.3$.

In conclusion, according to equations (I,49), (I,50) and (I,51), the phase voltage drop $\Delta v_{MC,N}$ and the CHB output phase voltage v_{aN}^l for the considered MC-PWM strategies can be expressed as follows:

$$\Delta v_{MC,N} = C_{MC} \cdot t_{dt} \cdot f_{sw} V_{dc} \cdot \text{sgn}(i_L) \quad (\text{I,52})$$

$$\Delta V_{MC,N} = C_{MC} \cdot t_{dt} \cdot f_{sw} V_{dc} \quad (\text{I,53})$$

$$v_{aN}^l = v_{aN,id}^l - \Delta v_{MC,N} \quad (\text{I,54})$$

where C_{MC} is a constant parameter that allows for considering the adopted MC-PWM strategy; in detail, $C_{MC}=1$ when LS-PWM is adopted, $C_{MC}=2$ when SCAMOD is adopted, and $C_{MC}=2n_{HB}$ when PS-PWM is adopted. In detail, for 3P-5L CHBML, $C_{MC}=4$ when PS-PWM is adopted.

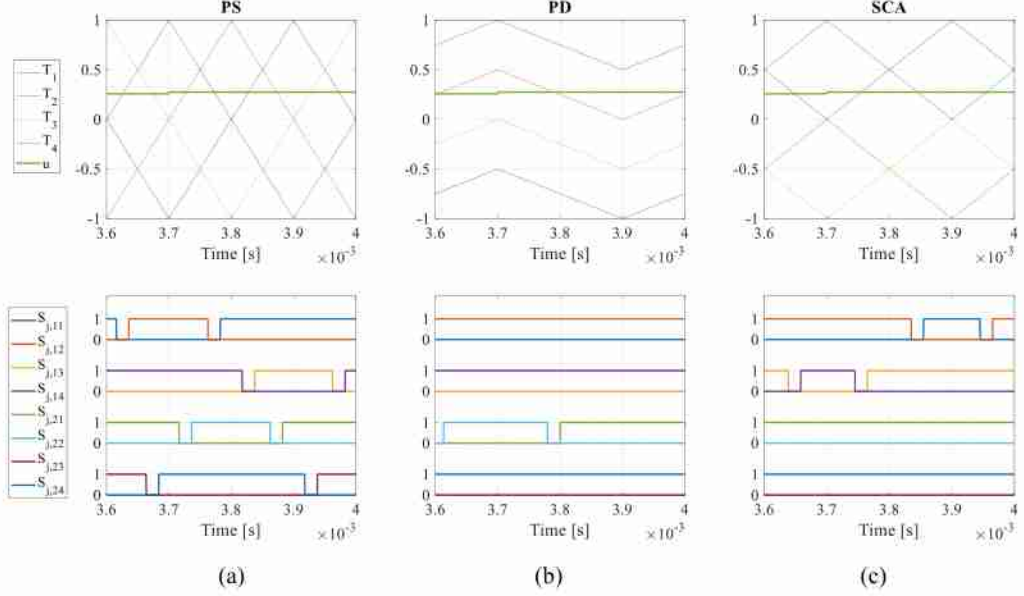


Fig. 1.28: MC-PWM modulation schemes and GCSs of one phase of 3P-5L CHBML in one T_{PWM} , $M = 0.3$: (a) Phase Shifted (b) Phase Disposition, (c) SCA-PWM.

Equation (I,54) is valid for phase voltages v_{jN} measured with respect to the converter star point N . However, it is possible to estimate the DT effect on the load voltages v_{an} , v_{bn} , and v_{cn} , by considering the relation (I,12). In detail, the vector of fundamental load voltages $\mathbf{v}_n^l$ can be expressed as:

$$\mathbf{v}_n^l = \mathbf{v}_{n,id}^l - \Delta \mathbf{v}_{MC,n} \quad (\text{I,55})$$

where $\mathbf{v}_{n,id}^l$ is the ideal vector of fundamental load voltages with no DT applied, and $\Delta \mathbf{v}_{MC,n}$ is the load voltage drop vector due to the DT effect. Through relation (I,12), it is possible to express the load voltage vector $\mathbf{v}_n^l$ as a function of the phase voltage vector $\mathbf{v}_N^l$, as follows:

$$\mathbf{v}_n^l = \mathbf{M} \mathbf{v}_{N,id}^l - \mathbf{M} \Delta \mathbf{v}_{MC,N} \quad (\text{I,56})$$

Then, according to equations (I,12), the load voltage drop vector $\Delta \mathbf{v}_{MC,n}$ can be expressed as follows:

$$\begin{cases} \Delta v_{MC,an} = C_{MC} \cdot t_{dt} f_{sw} V_{dc} \frac{2 \cdot \text{sgn}(i_a) - \text{sgn}(i_b) - \text{sgn}(i_c)}{3} \\ \Delta v_{MC,bn} = C_{MC} \cdot t_{dt} f_{sw} V_{dc} \frac{-\text{sgn}(i_a) + 2 \cdot \text{sgn}(i_b) - \text{sgn}(i_c)}{3} \\ \Delta v_{MC,cn} = C_{MC} \cdot t_{dt} f_{sw} V_{dc} \frac{-\text{sgn}(i_a) - \text{sgn}(i_b) + 2 \cdot \text{sgn}(i_c)}{3} \end{cases} \quad (I,57)$$

According to (I,57), the voltage drop is expressed as a function of all three phase current signs. Since the CHB output voltage system is symmetrical and the load is balanced, the load voltage drop vector represents symmetric and direct term too. As a way of example, the theoretical voltage drop $\Delta v_{MC,N}$ and $\Delta v_{MC,n}$ related to phase a , with PS-PWM modulation strategy, switching frequency $f_{sw}=70$ kHz, $DT=1.5$ μ s are reported in Fig. I. 29 (a) and (b), respectively.

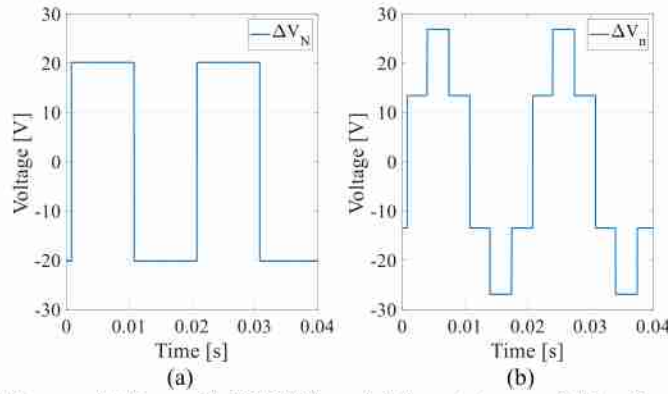


Fig. I. 29: Voltage drop $\Delta V_{MC,N}$ and $\Delta V_{MC,n}$ with PS-PWM modulation strategy, switching frequency $f_{sw}=70$ kHz, $DT=1.5$ μ s.

Looking at equations (I,54) and (I,57), it can be noted that the term $\Delta \mathbf{v}_{MC,N}$ causes a distortion of the fundamental harmonic term $\mathbf{v}_{N}^I$ and similarly $\Delta \mathbf{v}_{MC,n}$ causes a distortion of the fundamental harmonic voltage term $\mathbf{v}_n^I$. For this reason, to analyze only the effect on the fundamental harmonic, the fundamental harmonics voltage drop ΔV_{Ix} must be considered. In detail, looking at Fig. I. 29 (a-b), both waveforms are characterized by an odd and quarter-wave symmetry. Therefore, the even-order harmonics are absent, while the odd-order harmonics have the following amplitudes:

$$\Delta V_{hx,N} = \frac{4}{\pi} \Delta V_{MC} \int_0^{\pi/2} \sin(h\omega t) d(\omega t) = \frac{4\Delta V_{MC,N}}{h\pi} \quad (I,58)$$

$$\begin{aligned} \Delta V_{hx,n} &= \frac{4}{\pi} \frac{2\Delta V_{MC,N}}{3} \left\{ \int_0^{\pi/3} \sin(h\omega t) d(\omega t) + 2 \int_{\pi/3}^{\pi/2} \sin(h\omega t) d(\omega t) \right\} = \\ &= \frac{8\Delta V_{MC,N}}{3h\pi} \left[1 + \cos\left(h \frac{\pi}{3}\right) \right] \end{aligned} \quad (I,59)$$

where h is the harmonic order ($h=1, 3, 5\dots$). Concerning the fundamental harmonic, it results:

$$\Delta V_{1x,N} = \Delta V_{1x,n} = \frac{4\Delta V_{MC,N}}{\pi} \quad (I,60)$$

Looking at equation (I,60), it results that fundamental harmonic voltage drops $\Delta V_{1x,N}$ and $\Delta V_{1x,n}$ are characterized by the same amplitude. This result confirms that is possible to use equations (I,52) and (I,54) also on voltages referred to the point n . Then, in the rest of this chapter, the subscripts n and N will be suppressed and the mathematically estimated voltage drop will be identified using the notation $\Delta V_{1x,t}$, where t stands for theoretical and it is required to distinguish theoretical fundamental harmonic voltage drop $\Delta V_{1x,t}$ and the fundamental harmonic voltage drop $\Delta V_{1x,m}$ obtained from the experimental data.

I.10 Experimental Validation of Dead Time Impact on Fundamental Harmonic Voltage Drop

In this section, the voltage drop mathematical formulation is validated through experimental analysis. Tests are carried out on the same test bench discussed in Section I.7 and according to the same procedures already described. In particular, the previously considered working range is extended, considering three DT values, such that $t_{dt} \in \{0.5 \mu s, 1 \mu s, 1.5 \mu s\}$. For every DT value, the same analysis as a function of the amplitude modulation index M and the switching frequency f_{sw} is carried out, with $M \in \{0.3, 0.6, 0.9, 1.15\}$ and $f_{sw} \in \{10, 20, 30, \dots, 70 \text{ kHz}\}$. Each test is repeated for every MC-PWM strategy. It must be highlighted that the minimum DT value is chosen according to MOSFETs turn-on and turn-off times. Measured quantities are analyzed in the MATLAB environment.

I.10.1 Comparison Between Theoretical and Measured Fundamental Harmonic Voltage Drop

The first analysis deals with the comparison between the theoretical fundamental harmonic voltage drop amplitude $\Delta V_{1x,t}$ and the fundamental harmonic voltage drop amplitude $\Delta V_{1x,m}$ obtained from the experimental data. In detail, the term $\Delta V_{1x,t}$ is evaluated by extracting the first harmonic amplitude from the spectrum of the theoretical voltage drop $\Delta v_{MC,N}$, evaluated according to relations (I,52) and (I,60). The term $\Delta V_{1x,m}$ is evaluated by extracting the first harmonic amplitude from Δv_m^I , defined as:

$$\Delta v_m^I = v_{an,id}^I - v_{an,m}^I \quad (I,61)$$

where $v_{an,m}^1$ is the fundamental harmonic of the measured phase voltage on one phase of CHB, $v_{an,id}^1$ is the ideal fundamental harmonic of the CHB phase voltage, which depends on the amplitude modulation index M and on the total DC link voltage U_{dc} as follow

$$v_{an,id}^1 = M \cdot U_{dc} \cos(2\pi f_1 t + \phi_{1,m}) \quad (1,62)$$

where $\phi_{1,m}$ represents the measured voltage phase.

In Fig. I. 30, a comparison between the theoretical fundamental harmonic voltage drop $\Delta V_{1x,t}$ and the fundamental harmonic voltage drop from the experimental data $\Delta V_{1x,m}$ is presented. In detail, for each modulation scheme and different DT values (0.5 μ s, 1.0 μ s, and 1.5 μ s) the theoretical voltage drop $\Delta V_{1x,t}$ is compared with the corresponding voltage drop obtained by using Sinusoidal $\Delta V_{1x,m,S}$ and SFO $\Delta V_{1x,m,SFO}$ as modulation signals.

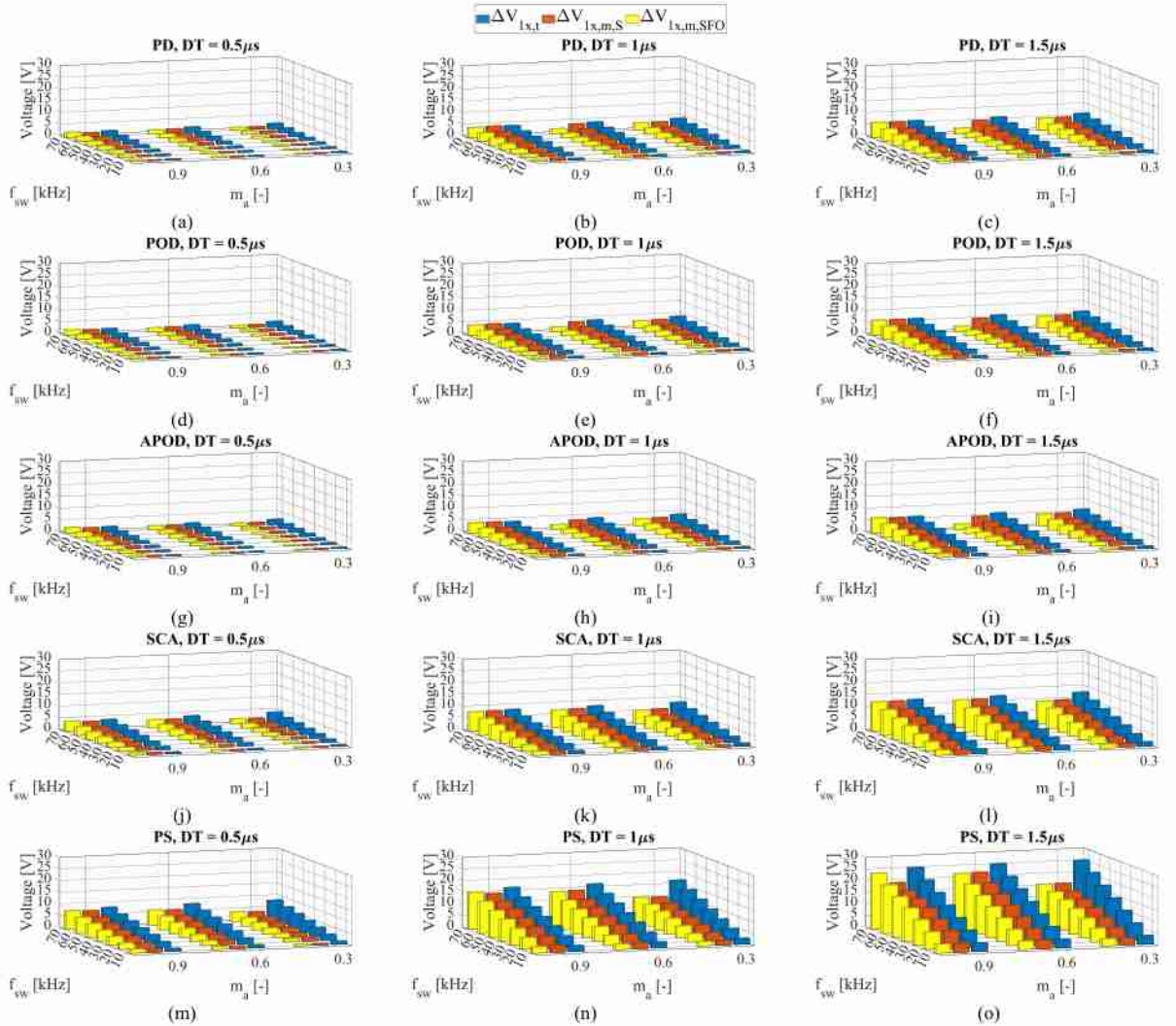


Fig. I. 30: Comparison between the theoretical voltage drop first harmonic $\Delta V_{1x,t}$ (blue bars) and the voltage drop first harmonic from the experimental data $\Delta V_{1x,m}$ (red bars for Sine modulation signal and yellow bars for SFO modulation signals).

Looking at the LS-PWM strategies (PD, POD, and APOD) shown in Fig. I. 30 (a)-(i), the DT causes the lowest voltage drop if compared with other MC-PWM strategies. In detail,

the theoretical voltage drop range of variation is summarized in Table I. 11, for different values of the considered DT. Concerning the theoretical voltage drop, It can be noted that by increasing the switching frequency or the DT, the voltage drop increases; the amplitude modulation index M does not affect the theoretical voltage drop. Moreover, for fixed switching frequency and DT, the analytical voltage drop value is the same, independently of the chosen LS-PWM strategy, since the triangular carrier signals mutual phase has a negligible effect on the voltage drop.

Table I. 11: Theoretical voltage drop $\Delta V_{I_{x,t}}$ range for PD, POD, and APOD-PWM schemes.

Dead Time [μ s]	Voltage Drop $\Delta V_{I_{x,t}}$ [V]		
	<i>PD-PWM</i>	<i>POD-PWM</i>	<i>APOD-PWM</i>
0,5	$0.3 \leq \Delta V \leq 2.15$	$0.3 \leq \Delta V \leq 2.15$	$0.3 \leq \Delta V \leq 2.15$
1	$0.6 \leq \Delta V \leq 4.28$	$0.6 \leq \Delta V \leq 4.28$	$0.6 \leq \Delta V \leq 4.28$
1,5	$0.9 \leq \Delta V \leq 6.40$	$0.9 \leq \Delta V \leq 6.40$	$0.9 \leq \Delta V \leq 6.40$

Regarding experimental results, some considerations must be made: it can be noted that when the amplitude modulation index M increases, also the experimental voltage drop increases. This phenomenon can be justified by considering the switching devices conduction losses: in detail, when the amplitude modulation index increases, the load current increases, and consequently the voltage drop on the conducting switching devices increases too. However, the difference between the theoretical and measured voltage never exceeds 1 V, except when SFO modulating signals are adopted and $M=0.6$, where some non-linearities occur. To properly discuss such converter non-linear behaviour, Fig. I. 31 is presented. In detail, in Fig. I. 31 (a-b), a fraction of the SFOPD-PWM modulating scheme is reported, with the time axis centered at $T_{PWM}/4$, where the modulating signal exhibits a quasi-flat trend. Concerning the ideal case with DT=0 reported in Fig. I. 31 (b), the modulating signal falls between two adjacent carriers signals, and the ideal control signals are generated. The generated signals are consistent with the previous discussion, i.e., control signals are sent only to one Half-Bridge at a time. Moreover, looking at a single Half Bridge, both *upper* and *lower* control signals change state in the considered T_{PWM} . Regarding the case with DT $\neq$ 0 reported in Fig. I. 31 (b), due to the modulating and carriers signals comparison, very small amplitude gate control signals should be ideally produced, but, if the DT is larger than the GCS impulse, the signal impulse is not produced at all.

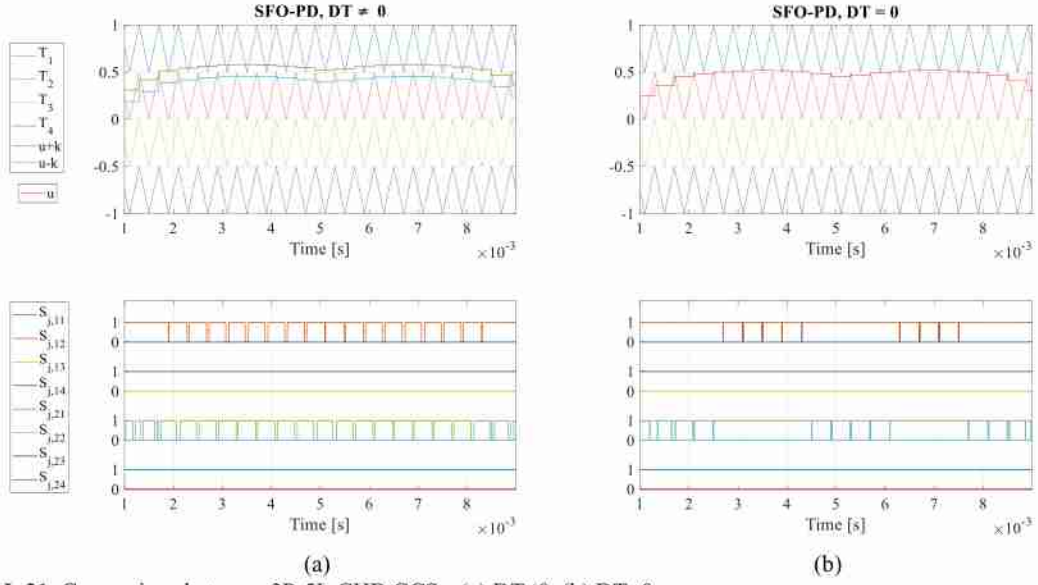


Fig. I. 31: Comparison between 3P-5L CHB GCSs, (a) $DT \neq 0$, (b) $DT = 0$.

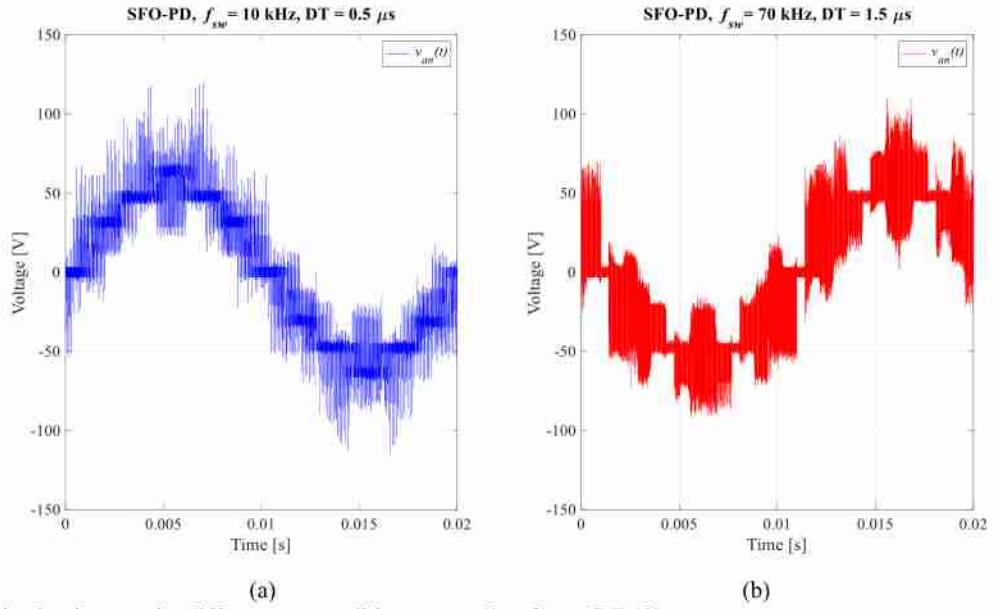


Fig. I. 32: load voltage under different test conditions, saturation due to DT effect.

Due to the DT effects, the GCSs are very different if compared to the ideal case; in detail, the split modulating signals are producing GCSs sent to upper and lower devices of different Half Bridges. This behaviour causes a saturation effect on the output voltage, as can be seen in Fig. I. 32. In detail, PD-PWM is chosen as a way of example and the load voltage v_{an} is reported under two working conditions, obtained with switching frequency $f_{sw}=10$ kHz, $DT = 0.5 \mu s$, and switching frequency $f_{sw}=70$ kHz, $DT = 1.5 \mu s$. In the first working condition, shown in Fig. I. 32 (a), which is the least severe in the adopted working range, the DT effect is negligible and no saturation can be observed; in the second working condition, shown in Fig. I. 32 (a), which is the most severe, the DT causes a saturation effect, such that the CHB stop switching in some fractions of the fundamental period and the output voltage is constant. This behavior leads on one side to a reduced voltage drop, since a reduced number of

commutations occurs, on the other, it causes an increment of harmonic distortion, as will be discussed in the following sections. Since the working region around $M=0.6$ is not linear, in this region, the relations (I,52), (I,54), and (I,60) are not valid anymore; moreover, high DT and switching frequency values result in a wider non-linear operating region around $M=0.6$. It must be noted that a similar situation occurs when sinusoidal modulating signals are chosen and $m_a=0.5$. This behavior is not visible in Fig. I. 30, because tests have not been carried out at this specific working point. Moreover, this phenomenon occurs only when an LS-PWM strategy is adopted since it depends on the mutual carriers disposition; it does not occur when SCAMOD and PS are chosen, as will be illustrated below.

When PS-PWM and SCAMOD schemes are considered, the theoretical voltage drop is doubled and quadrupled, respectively. In detail, the variation range of analytical voltage drop is summarized in Table I. 12, for different values of the dead time considered, and SCAMOD and PS-PWM strategies.

Table I. 12: Theoretical Voltage drop range for SCA-PWM and PS-PWM schemes.

Dead Time [μ s]	Voltage Drop $\Delta V_{Ix,t}$ [V]	
	<i>SCA-PWM</i>	<i>PS-PWM</i>
0,5	$0.6 \leq \Delta V \leq 4.3$	$1.2 \leq \Delta V \leq 8.6$
1	$1.2 \leq \Delta V \leq 8.56$	$2.4 \leq \Delta V \leq 17.12$
1,5	$1.8 \leq \Delta V \leq 12.80$	$3.6 \leq \Delta V \leq 25.60$

Considerations about PS and SCA theoretical and experimental voltage drops partly coincide with previous considerations related to LS-PWM strategies. In this case, the maximum difference between the theoretical and measured voltage drop reaches less than 5 V and 10 V in SCA and PS, respectively. It must be underlined that the coincidence between voltage drops with sinusoidal and SFO modulating signals is more evident, as the previously described non-linearity phenomenon does not occur when $M=0.6$, due to the different carriers disposition. It can be noted that the difference between theoretical and measured voltage drops increases when the switching frequency increases and the amplitude modulation index decreases. The theoretical voltage drop calculation leads to an overestimation, as it is confirmed in [I,32].

I.10.2 Comparison Between Ideal and Expected Load Voltage Fundamental Harmonic Amplitude

The second analysis deals with the comparison between the ideal fundamental load voltage amplitude $V_{an,id}^l$, which is defined as the module of (I,62), and the expected ideal load voltage amplitude $V_{an,ex}^l$, which is evaluated, according to equation (I,55), by extracting the first harmonic amplitude from:

$$v_{an,ex}^l = v_{an,m}^l + \Delta v_{MC,n}^l \quad (I,63)$$

where $v_{an,m}^l$ is the fundamental harmonic of the measured load voltage and $\Delta v_{MC,n}^l$ is the theoretical voltage drop, evaluated according to equation (I,52). The term $v_{an,ex}^l$ is distorted due to the DT voltage drop, so the fundamental harmonic is extracted through the FFT algorithm. To carry out this comparison, the relative percentage error $e\%$ is defined as:

$$e\% = \frac{V_{an,id}^l - V_{an,ex}^l}{V_{an,id}^l} \cdot 100 \quad (I,64)$$

In Figure 12 the relative percentage error $e\%$ over the considered working range is reported.

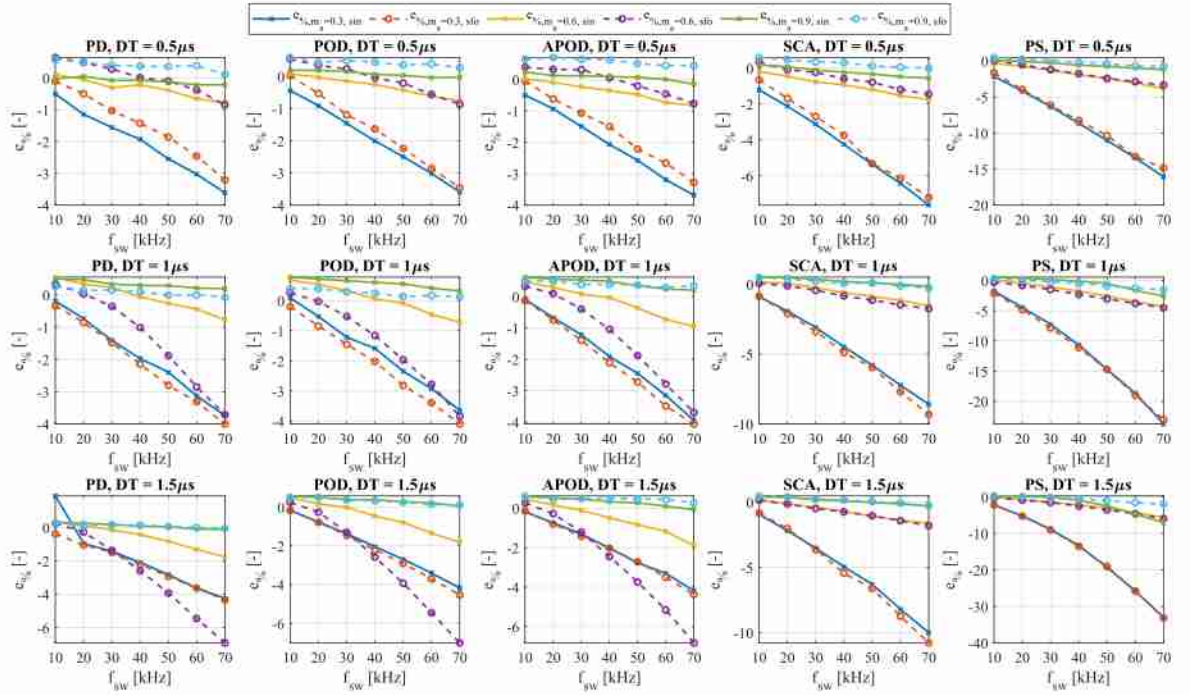


Fig. I. 33: Percentage error $e\%$ under various test conditions.

Taking into account LS-PWM strategies, the maximum $e\%$ is equal to 8% and occurs when $f_{sw}=70$ kHz, $DT=1.5$ μ s, $M=0.6$, and SFO modulating signal is adopted. This specific working is characterized by non-linearities, as previously discussed. In all the other working conditions, $e\%$ magnitude is always lower than 4%, and in most cases is lower than 1%.

Taking into account PS-PWM, the maximum $e\%$ magnitude occurs when $f_{sw}=70$ kHz, $DT=1.5$ μ s, $M=0.3$ and $e\%$ is equal about to 30%. The error sign confirms that when the amplitude modulation index is very low, a voltage drop overestimation occurs. The percentage error is drastically reduced when the amplitude modulation index increases and it does not exceed 5%. Similar considerations can be applied to the SCA-PWM, although the maximum amplitude error is lower than in the previous case, about 10%. Also, in this case, the worst approximation occurs when M is very low.

Experimental results discussed above confirm the DT effects strong dependency on the selected MC-PWM strategy. Indeed, from the comparison between analytical and experimental results, the voltage drop mathematical formulation allows predicting quite well the DT effect on the voltage fundamental harmonic for higher values of the modulation index (in the range from 0.5 to 1). Nevertheless, an overestimation phenomenon occurs for lower values of the modulation index. Thus, this phenomenon must be considered in all cases where a voltage compensation algorithm is employed.

I.11 Experimental Analysis of Dead Time Impact on CHB Performance

In this section, the DT impact on the voltage harmonic distortion and converter efficiency is analyzed through an experimental comparative analysis. In detail, the analysis carried out in Section I.8 is repeated for three DT values considered in this work. With this aim, three distortion indexes, i.e., the THD, the Partial Harmonic Distortion (PHD), and the Low-Frequency Total Harmonic Distortion (THD_{LF}) are adopted. Indeed, according to [I,33], the THD index allows for investigating the overall harmonic content in a voltage or current waveform without providing information on the real distribution in the harmonic spectra and the contribution of each harmonic in the frequency domain. In other words, the THD allows measuring the overall distortion, although it does not allow distinguishing harmonics from inter-harmonics or low-frequency components by high-frequency components. However, knowing the real distribution of the harmonic components and their amplitudes in the frequency domain can be used, for example, in the filter design process for grid-connected applications or to estimate the torque ripple and iron losses for electrical drive applications. Then, PHD and THD_{LF} are adopted to evaluate the DT effect on harmonic groups centered around the apparent switching frequency and its multiples, and on low-frequency harmonics (from the 5th to 23rd), respectively.

I.11.1 Voltage Total Harmonic Distortion Analysis

The THD, defined as in (I,40) is used as a comparison tool of the converter performance. Fig. I. 34 - Fig. I. 38 show the voltage THD as a function of the modulation index M , for every DT value, switching frequency, and considered MC-PWM strategy. It is interesting to note that the previously discussed correlation between the THD and the DT is confirmed. In detail, increasing the DT value leads to an increase in the voltage THD, almost in every considered working condition. Moreover, such an increase is strongly correlated with the adopted MC-PWM strategy. LS-PWM strategies, shown in Fig. I. 34 - Fig. I. 36, exhibit the lowest increase in the THD, when the DT increases, if compared to other strategies. Such an

increase is emphasized when the switching frequency increases and for very low values of the amplitude modulation index.

Looking at Fig. I. 39 and Fig. I. 40, where the THD over the switching frequency for every DT value is reported, it is possible to quantify the THD increase. PD-PWM exhibits the lowest THD increase, moving from 60% to 75% at the worst working point ($f_{sw}=70$ kHz, $M=0.3$). On the contrary, when $M=0.9$ and $f_{sw}=10$ kHz, the DT impact is negligible. Similar considerations can be carried out for POD and APOD-PWM, although THD values are always higher than PD-PWM. When PS is adopted, the DT impact is strongly emphasized: as a way of example, when $f_{sw}=70$ kHz, $M=0.3$, it moves from 125% to 180%. SCAMOD exhibits an intermediate behaviour between LS and PS PWM: when $f_{sw}=70$ kHz, $M=0.3$, increasing the DT the THD does not exceed 150%.

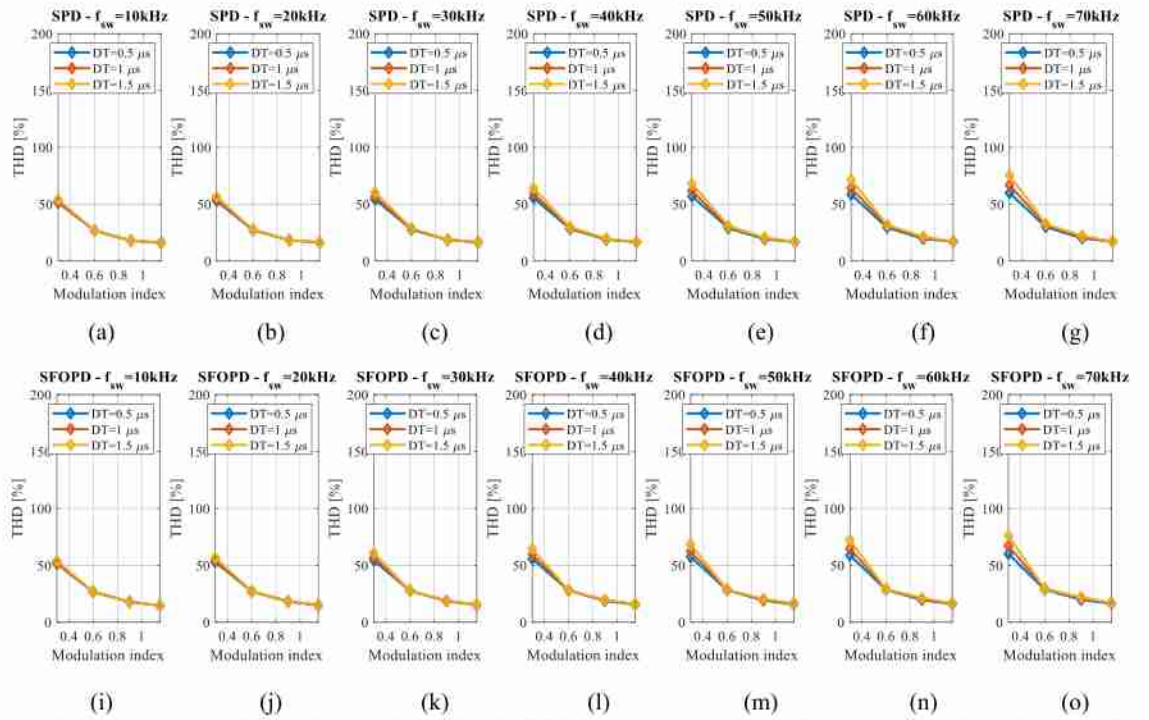
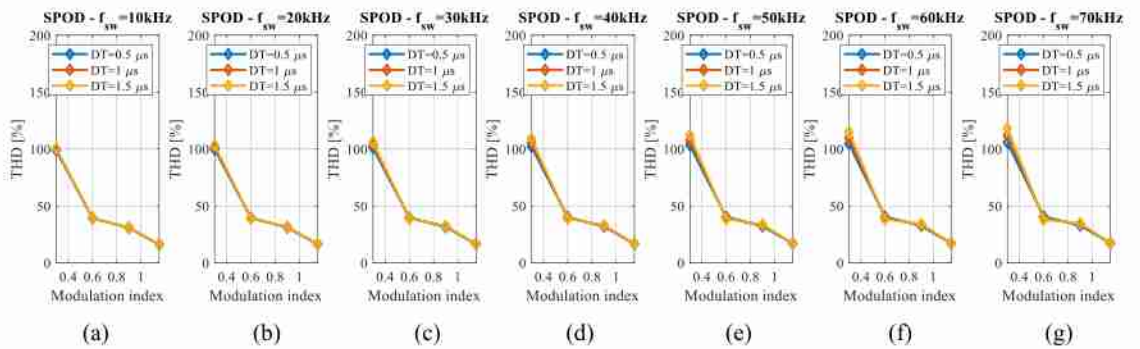


Fig. I. 34: THD trends over the modulation index for PD-PWM strategy, (a-g) sinusoidal modulating signal for f_{sw} in the range 10-70 kHz, (i-o) SFO modulating signal for f_{sw} in the range 10-70 kHz.



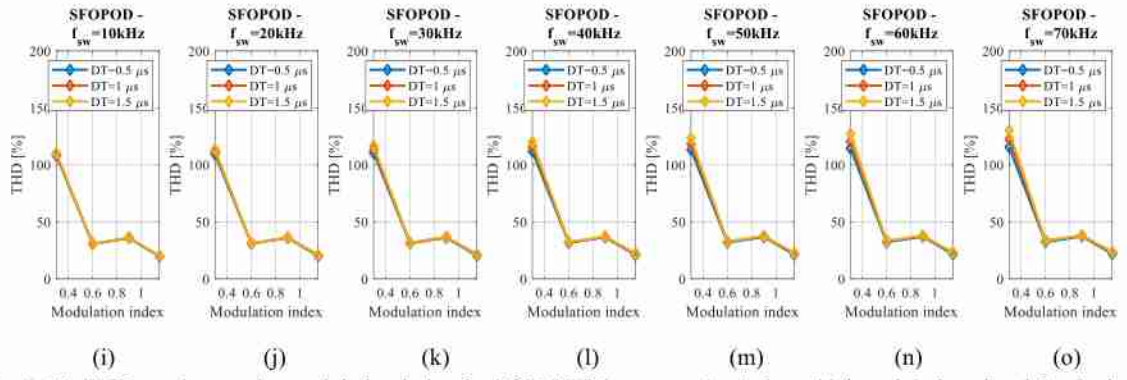


Fig. I. 35: THD trends over the modulation index for POD-PWM strategy, (a-g) sinusoidal modulating signal for f_{sw} in the range 10-70 kHz, (i-o) SFO modulating signal for f_{sw} in the range 10-70 kHz.

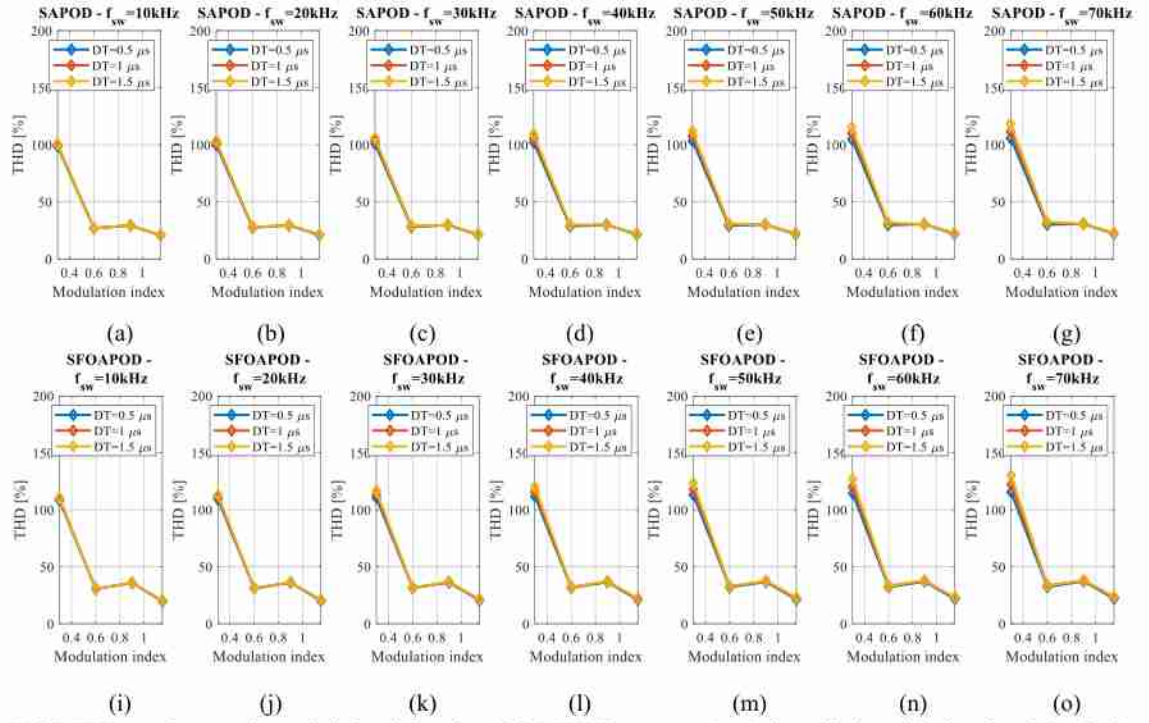
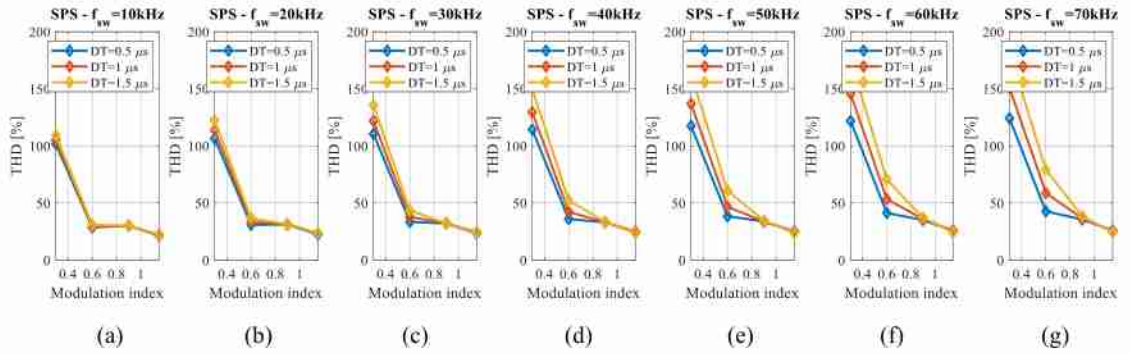


Fig. I. 36: THD trends over the modulation index for APOD-PWM strategy, (a-g) sinusoidal modulating signal for f_{sw} in the range 10-70 kHz, (i-o) SFO modulating signal for f_{sw} in the range 10-70 kHz.



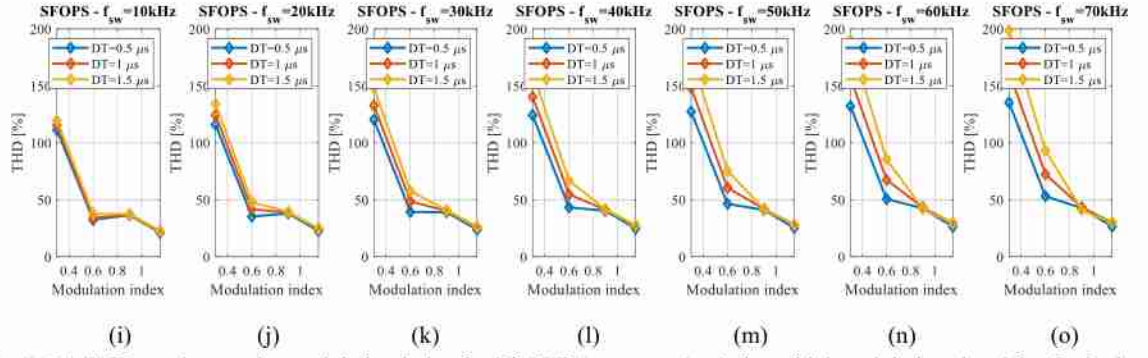


Fig. 1.37: THD trends over the modulation index for PS-PWM strategy, (a-g) sinusoidal modulating signal for f_{sw} in the range 10-70 kHz, (i-o) SFO modulating signal for f_{sw} in the range 10-70 kHz.

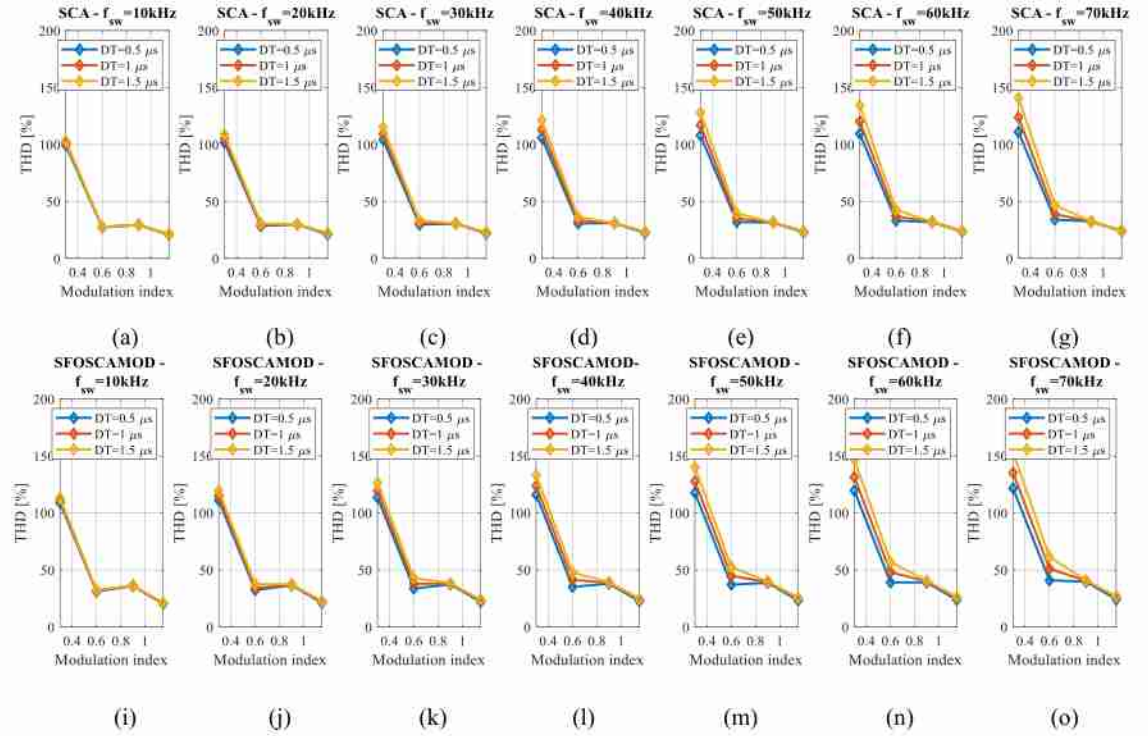


Fig. 1.38: THD trends over the modulation index for SCAMOD strategy, (a-g) sinusoidal modulating signal for f_{sw} in the range 10-70 kHz, (i-o) SFO modulating signal for f_{sw} in the range 10-70 kHz.

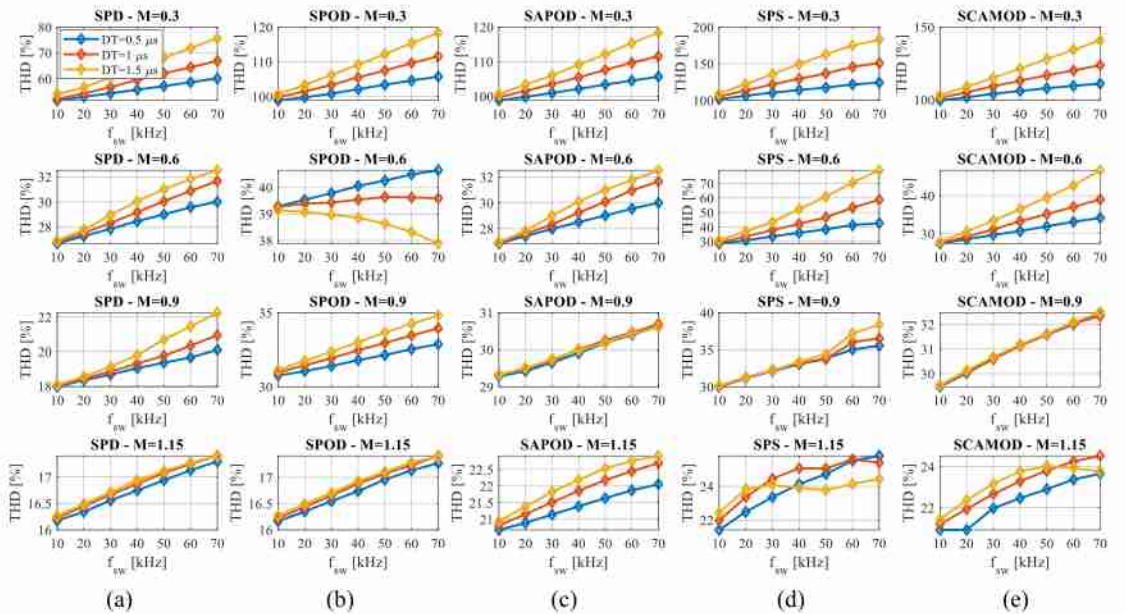


Fig. I. 39: THD trends over the switching frequency with sinusoidal modulating signals, (a) PD, (b) POD, (c) APOD, (d) PS, (e) SCAMOD.

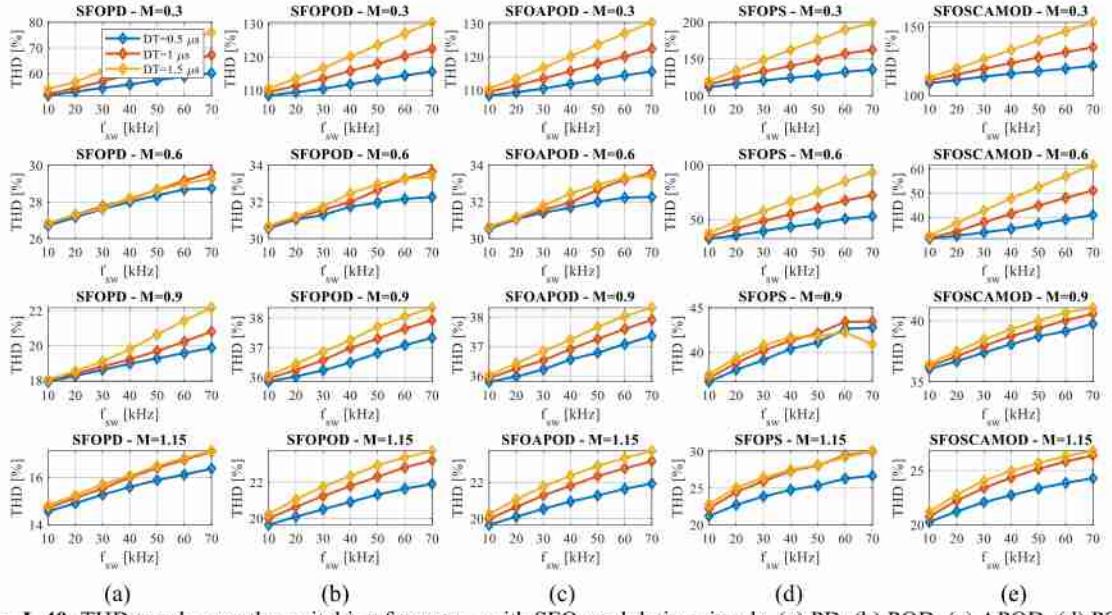


Fig. I. 40: THD trends over the switching frequency with SFO modulating signals, (a) PD, (b) POD, (c) APOD, (d) PS, (e) SCAMOD.

As previously discussed, the THD increase with the switching frequency can be correlated to a reduction of the fundamental harmonic amplitude. THD experimental results presented in this section, combined with the discussion about the fundamental harmonic voltage drop carried out in the previous section, allow for confirmation that the THD increase is strongly correlated to the DT effect.

1.11.2 Voltage Partial Harmonic Distortion Analysis

The PHD is defined as follows:

$$PHD\% = \frac{100}{U_{dc}} \sqrt{\sum_{h=k_h \cdot f_{sw} - B_{sw}}^{k_h \cdot f_{sw} + B_{sw}} V_h^2} \quad (I.65)$$

where V_h is the considered h^{th} voltage harmonic, k_h is a constant integer number, and B_{sw} is the bandwidth which allows for considering the sideband harmonics around the frequency $k_h f_{sw}$; in detail, B_{sw} is equal to 2 kHz. It must be noted that the PHD values are expressed as a percent of the total DC voltage U_{dc} . In this way, the PHD allows the evaluation of the DT impacts in the frequency domain providing information about the distribution and amplitude of the main high-frequency harmonics without considering the previously described first harmonic reduction effect. Concerning k_h , its value is particularized depending on the analyzed MC-PWM strategy, to investigate the most significant harmonics groups. PHD% evaluation points in the frequency domain are summarized in Table I. 13. From the elaboration of the experimental data, by fixing the values of the DT and switching frequency,

it emerges that the PHD% values do not vary over the modulation index. Thus, the PHD% values only for amplitude modulation index $M=0.9$ are reported.

Table I. 13: PHD evaluation points in frequency domain.

Modulation schemes	PHD evaluation points $k_h f_{sw}$				
<i>LS-PWM (PD, POD and APOD)</i>	f_{sw}	$2f_{sw}$	$3f_{sw}$	$4f_{sw}$	$5f_{sw}$
<i>PS-PWM</i>	$4f_{sw}$	$8f_{sw}$	$12f_{sw}$	$16f_{sw}$	$20f_{sw}$
<i>SCAMOD</i>	$2f_{sw}$	$4f_{sw}$	$6f_{sw}$	$8f_{sw}$	$10f_{sw}$

Fig. I. 41 and Fig. I. 42 show the LS-PWM strategies PHD trends over the switching frequency, for every DT value and for every k_h reported in Table I. 13, with sinusoidal and SFO modulating signals, respectively.

Looking at Fig. I. 41, the DT effect is evident only for SPD in the harmonic group centered at the switching frequency ($k_h=1$). In detail, it is possible to observe a stronger increase in the PHD values for higher values of the switching frequency. Whereas, the DT effect is negligible in other analyzed cases. Looking at Fig. I. 42, the DT effect is evident in the harmonics centered at twice ($k_h=2$) the switching frequency in all adopted LS-PWM strategies. In this case, the DT effect generates a stronger increase in the PHD values for higher values of the switching frequency. Moreover, an interesting effect has been observed in the harmonics group centered at three times ($k_h=3$) of the switching frequency, when SFOPD is adopted. In detail, a reduction of the PHD values has been observed when the switching frequency increases.

Fig. I. 43 shows the PHD obtained with SPS and SCAMOD schemes. It can be noted that the DT effect is more evident, if compared to the LS-PWM schemes. In detail, the DT effect generates a reduction of the PHD values in the first harmonic groups centered at four ($k_h=4$) and two ($k_h=2$) times of the switching frequency for SPS and SCAMOD, respectively. Moreover, for the SPS scheme, the DT generates an increase in the PHD values harmonic groups centered at eight ($k_h=8$) and twelve ($k_h=12$) times of the switching frequency. For the SCAMOD scheme, the DT effect is negligible for the other harmonic group, from $k_h=4$ to $k_h=10$, where the PHD values are similar.

Fig. I. 44 shows the PHD trends with SFOPS and SFOSCAMOD. It should be noted that also in this case the DT impact determines a slight reduction of the PHD values as the DT increase. Instead, an increase in the PHD values has been observed in the second harmonic groups, $k_h=8$ and $k_h=4$, for SFOPS and SFOSCAMOD, respectively. In other cases the DT effect is negligible.

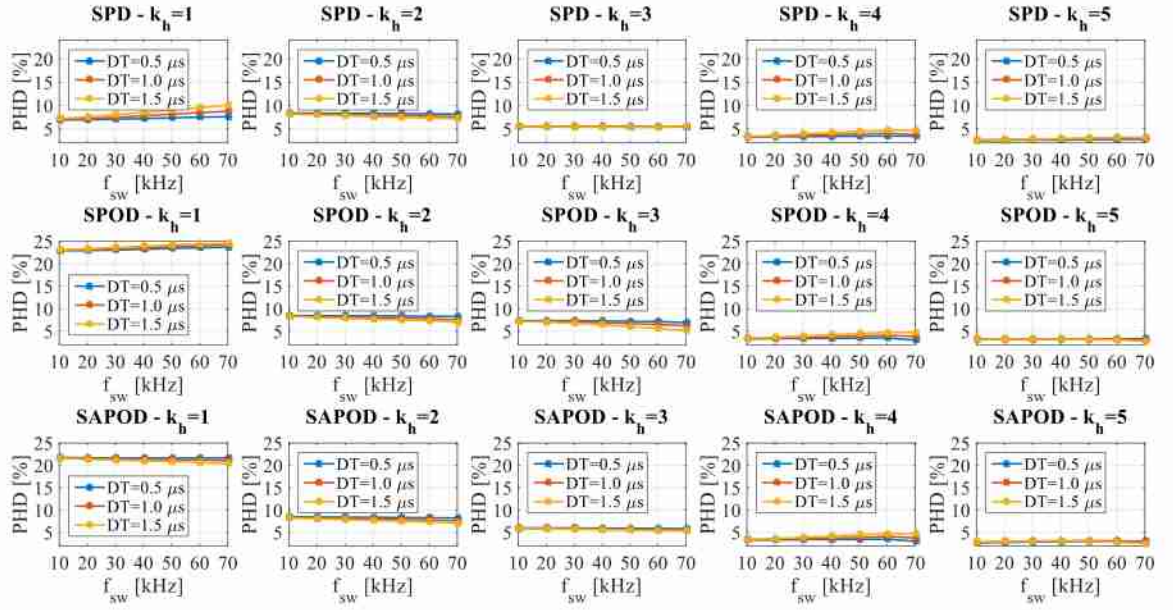


Fig. I. 41: PHD values vs. switching frequency obtained with LS-PWM-based schemes and sinusoidal modulation signals (SPD, SPOD and SAPOD).

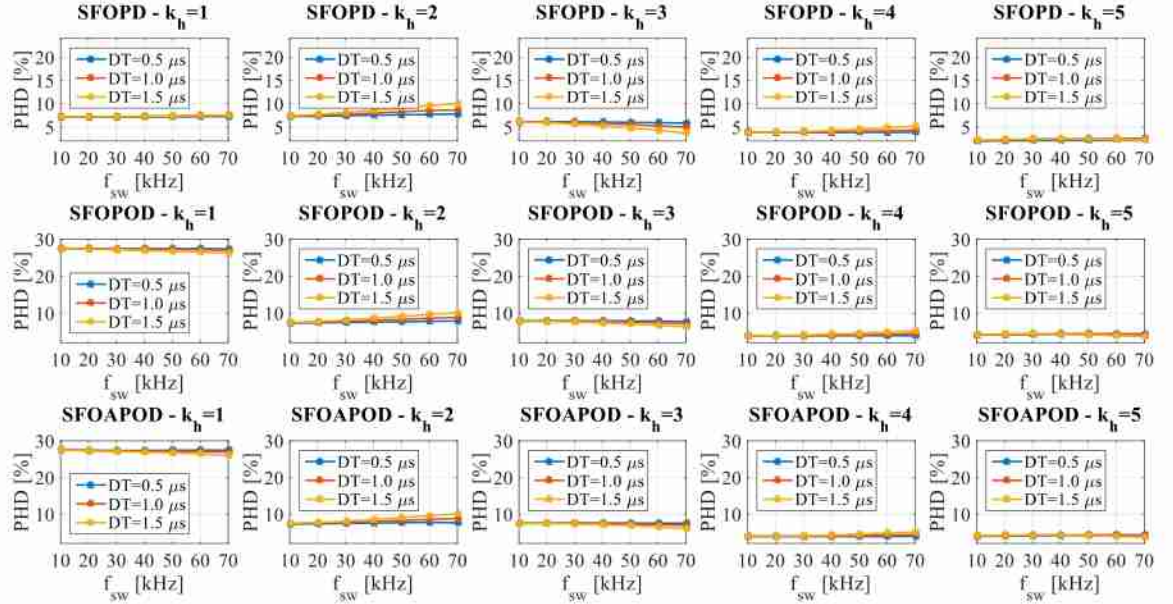


Fig. I. 42: PHD values vs. switching frequency obtained with LS-PWM-based schemes and switching frequency optimal modulation signals (SFOPD, SFOPD and SFOAPD).

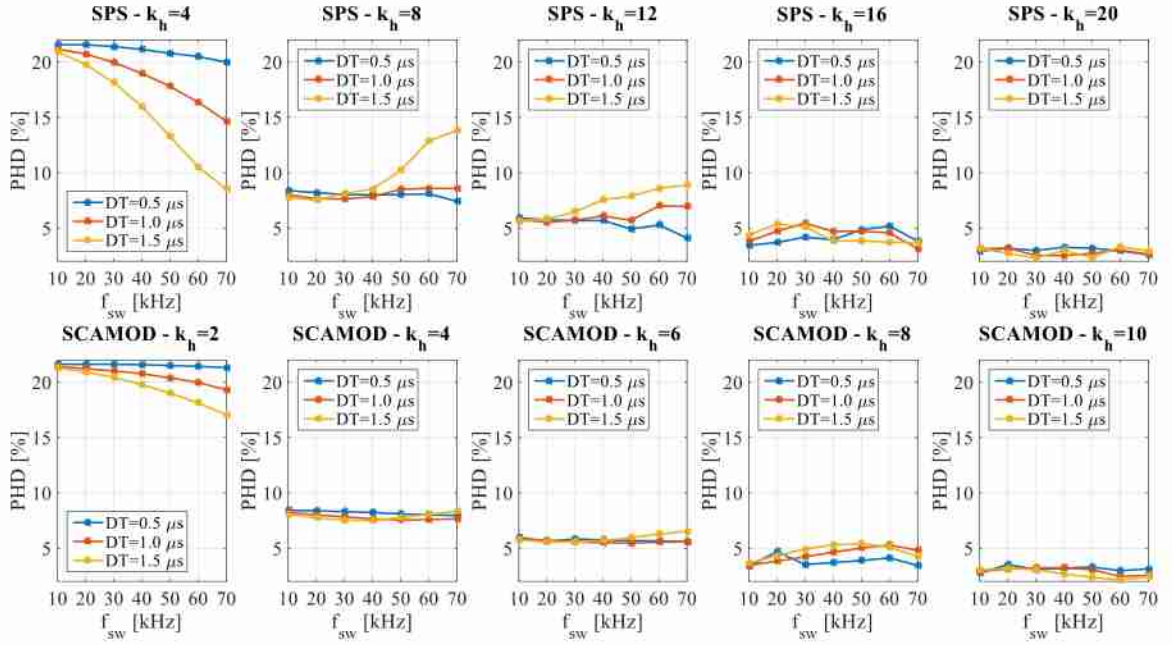


Fig. I. 43: PHD values vs. switching frequency obtained with SPS and SCAMOD schemes.

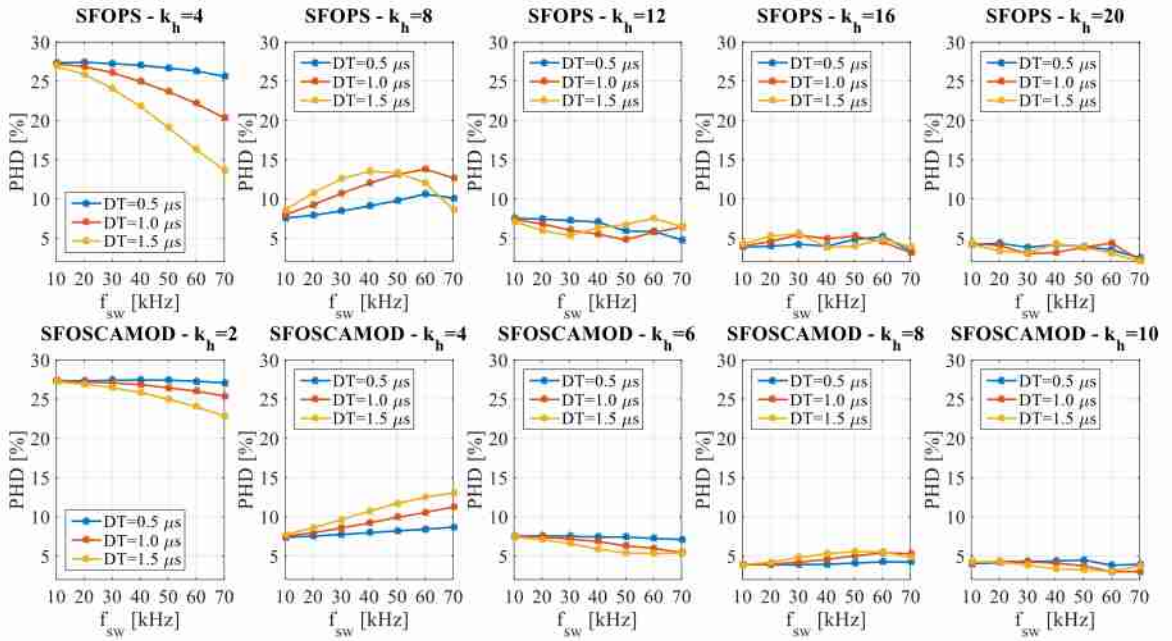


Fig. I. 44: PHD values vs. switching frequency obtained with SFOPS and SFOSCAMOD schemes.

Previously discussed experimental results allow for stating that, generally, the DT effect is negligible in high-frequency harmonics, except for PS-PWM and SCAMOD schemes, where a PHD slight reduction is recorded for the first group of harmonics when the DT and the switching frequency increase.

I.11.3 Voltage Low-Frequency Total Harmonic Distortion Analysis

The $THD_{LF}\%$ is expressed as

$$THD_{LF}\% = \frac{100}{V_1} \sqrt{\sum_{h=5}^{23} V_h^2} \quad (I,66)$$

It must be underlined that the $THD_{LF}\%$ allows for investigating the overall low-frequency voltage harmonics distortion by providing information about the DT impact without considering the real harmonics distribution in the frequency domain.

Fig. I. 45 shows the $THD_{LF}\%$ as a function of the amplitude modulation index M , switching frequency, and DT, for each considered MC-PWM strategy. Looking at Fig. I. 45 (a)-(f), the DT impact is similar among the LS-PWM schemes. In detail, $THD_{LF}\%$ increase with the switching frequency the more the DT. Moreover, such a growth is emphasized when the modulation index is equal to 0.6. When sinusoidal modulating signals are employed, the $THD_{LF}\%$ exhibit a strong increase in the overmodulation region. However, the DT effect is strongly reduced, i.e., the $THD_{LF}\%$ does not vary significantly when the DT increases. On the contrary, when SFO modulating signals are adopted, $THD_{LF}\%$ is comparable to that in the other working points. This is expected, since the SFO allows for extending the converter linear working region up to $M=1.15$. However, the DT effect is emphasized in the overmodulation region.

Fig. I. 45 (g) and (h) show the $THD_{LF}\%$ results obtained with SPS and SFOPS schemes, respectively. As it was expected, the DT effect causes a strong increase of the $THD_{LF}\%$ values when the switching frequency increases. The DT effect is evident even in the overmodulation region: it is interesting to note that the switching frequency is high (i.e., 70 kHz), the $THD_{LF}\%$ reach the same values with sinusoidal and SFO modulating signals. Then, it can be stated that harmonics produced due to the DT have a much bigger amplitude, if compared to harmonics produced due to overmodulation region non-linearities.

Finally, the $THD_{LF}\%$ results for SCAMOD and SFOSCAMOD are depicted in Fig. I. 45 (i) and (l), respectively. It can be noted that, when $M=0.3$, the $THD_{LF}\%$ reaches the highest values, if compared to other MC-PWM strategies, both employing sinusoidal and SFO modulating signals. Over the remaining working points, SCAMOD exhibits an average behaviour between LS and PS-PWM strategies, as expected by the previous considerations.

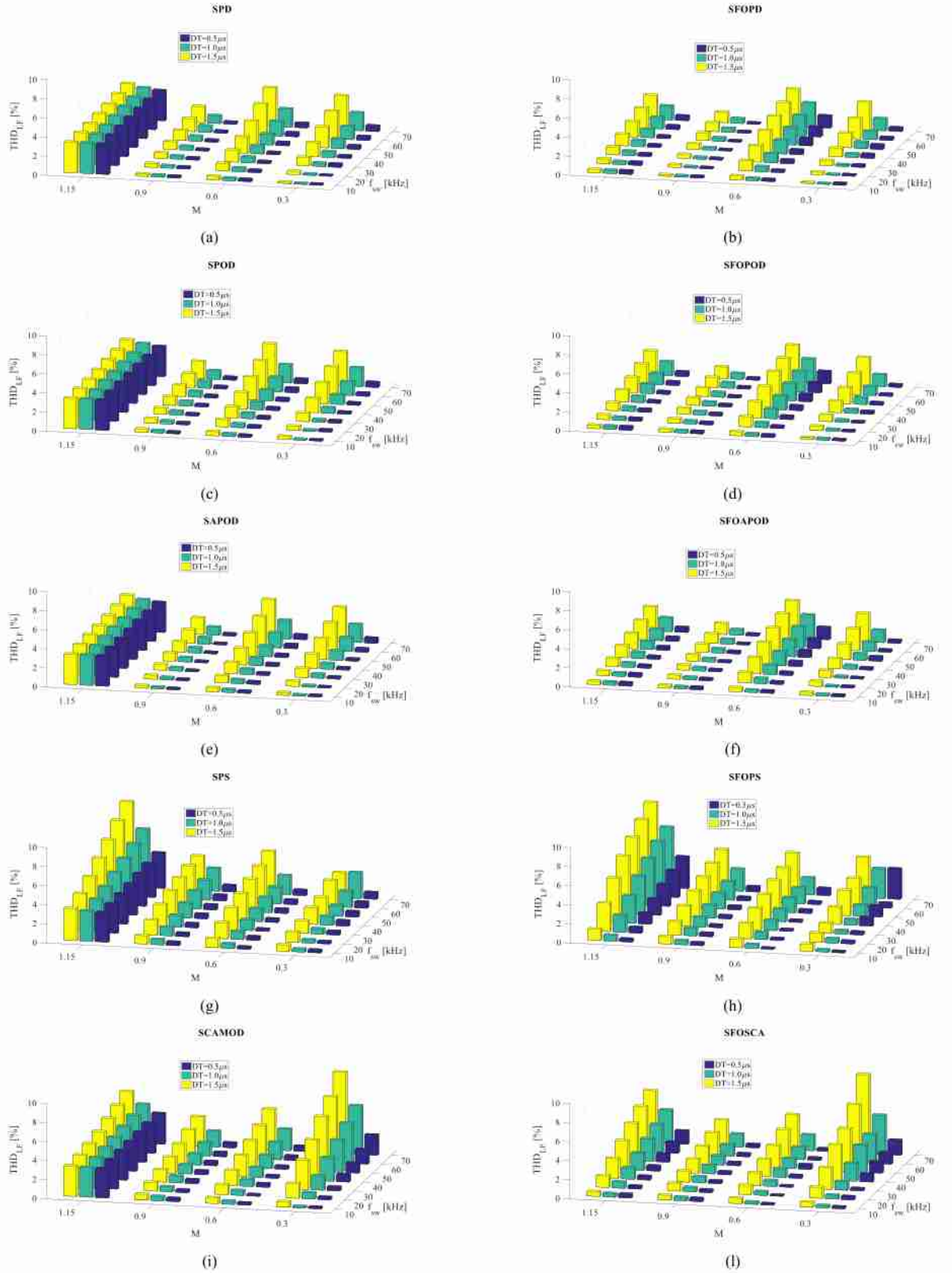


Fig. 1.45: Experimental $THD_{LF}\%$ values: (a) SPD; (b) SFOPD; (c) SPOD; (d) SFOPOD; (e) SAPOD; (f) SFOAPOD; (g) SPS; (h) SFOPS; (i) SCAMOD; (l) SFOSCAMOD.

Finally, by comparing results related to $THD_{LF}\%$ and $PHD\%$, it can be stated that the DT effect causes a strong harmonic increase in the low-frequency spectrum. As a consequence, filtering such harmonic is a trivial task.

1.11.4 CHB Inverter Efficiency Analysis

Finally, the DT effect on the converter efficiency is investigated. The converter efficiency is computed according to (I,41). Fig. I. 46 and Fig. I. 47 show the efficiency trends as a function of the switching frequency, for every adopted DT, for every amplitude modulation index M , and for every MC-PWM strategy, with sinusoidal and SFO modulating signals, respectively. It can be noted that the DT effect also impacts the converter efficiency, by producing an efficiency reduction when the DT increases. Most of the considerations previously carried out are valid also for efficiency trends. In detail, the LS-PWM strategies are poorly affected by the DT, with an efficiency between 96% and 75%, in the worst case. On the contrary, PS-PWM is strongly affected by the DT, and the converter efficiency reaches 20% in the worst case ($M=0.3$, $f_{sw}=70$ kHz, $DT=1.5 \mu s$). Moreover, it reaches the efficiency of 95% only in the overmodulation region, showing always a much lower efficiency in the considered working range, if compared to the LS-PWM strategies. SCAMOD determines similar converter efficiency to PS-PWM when $M=0.3$ and $M=1.15$. However, when $M=0.6$ and $M=0.9$, the efficiency is slightly higher than PS for every considered f_{sw} and DT.

SFO modulating signals produce a slight reduction of the converter efficiency. However, most of the considerations carried out for the sinusoidal modulating signals are valid for SFO modulating signals.

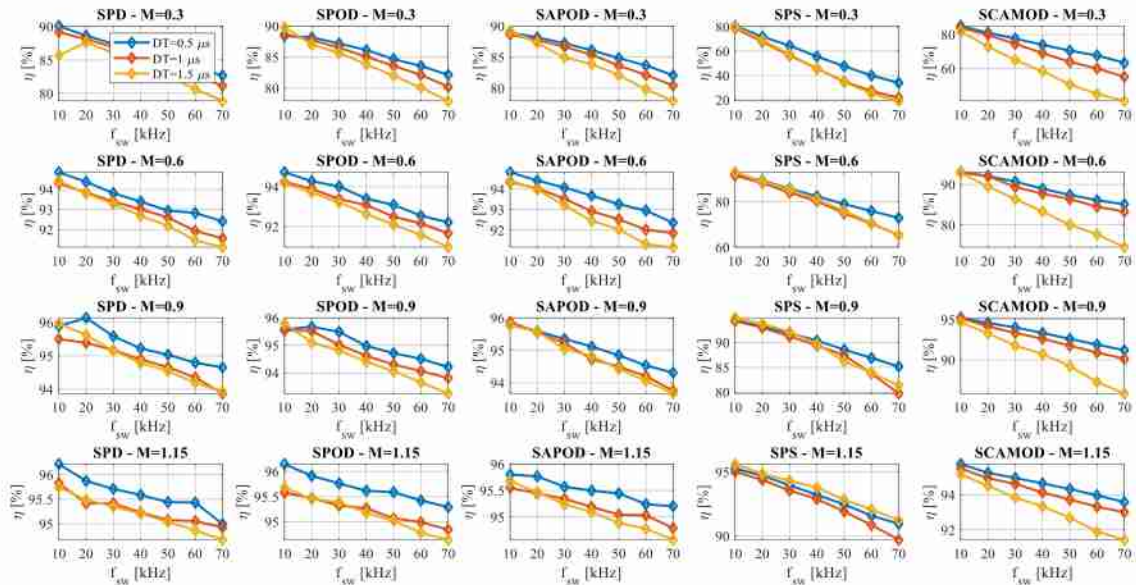


Fig. I. 46: Efficiency over switching frequency trends for every adopted DT, for every modulation index M , and every MC-PWM strategy with sinusoidal modulating signals.

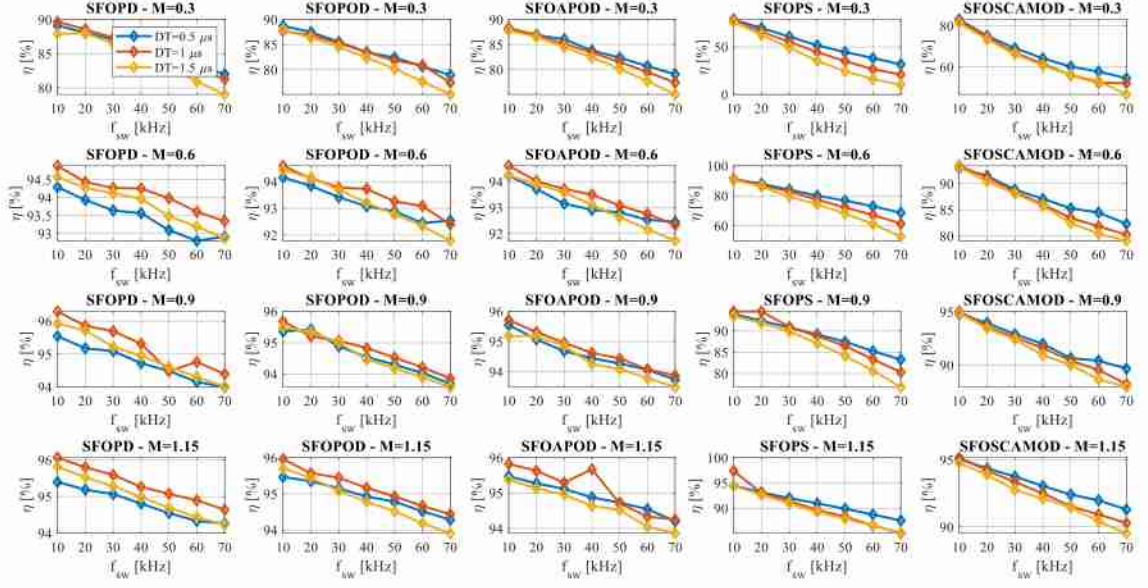


Fig. 1. 47: Efficiency over switching frequency trends for every adopted DT, for every modulation index M , and every MC-PWM strategy with SFO modulating signals.

I.12 References

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Chapter II Cascaded H-Bridge – Fed IPMSM Drive: Design, Implementation, and Performance Analysis

II.1 Introduction

The actual global energy scenario is characterized by a rapid energy electricity consumption increase, mostly due to the electrification of transportation systems and the development of more and more automotive and industrial electric drives. In this context, electric drives represent one of the largest end-consumers of electricity by accounting for nearly 50% of all global electricity consumption [II,1]-[II,2]. As discussed in the Introduction section of this work, the majority of adjustable-speed drives, especially in the e-mobility sector, are fed by 2L-VSIs controlled with the PWM strategy. They introduce non-negligible current harmonics and additional power losses, if compared to sinusoidal grid supply, due to the voltage harmonic content, which reduces the motor efficiency [II,3]-[II,4], and introduces additional vibrations and noise [II,5]. In detail, such power losses are known in the scientific literature as harmonic power losses and several works demonstrated that 2L-VSIs drives are associated with high harmonic power losses, ranging from 5% to 30% of the total motor power losses [II,6]-[II,7]. Indeed, such harmonic power losses compromise the whole drive efficiency, since more than 70% of total drive power losses are located in the motor [II,8]. Then, regulatory bodies released new international standards to improve the minimum efficiency electric drive requirements and define new energy efficiency classification for motors, Complete Drive Modules (CDMs) and Power Drive Systems (PDSs) for energy savings purposes [II,9]-[II,10]. Therefore, the motor efficiency requirements are going to become stricter over time, thus resulting in power losses reduction in both the motor and the whole power drive system.

In this context, MIs are the main candidate for motor power losses reduction. They are currently much more adopted in medium-voltage electric drives rather than in low-voltage drives, due to the additional cost required, if compared to conventional 2L-VSIs. However, concerning the e-mobility applications, it is already proven in the scientific literature that the CHB converter has a higher efficiency than the 2L-VSI, especially at partial load and low-speed working conditions, and determines an overall reduction of the powertrain cost due to its impact on the battery pack design process [II,11]. It is noteworthy to point out the absence of a detailed and expansive examination in the literature regarding the power losses behaviour in CHB-fed PMSM drives. The overwhelming majority of the studies proposed in literature focus on PMSM drives fed by conventional 2L-VSIs controlled with PWM strategy [II,12]-[II,16]. Only a few papers investigate the MIs impact on electrical motor power losses. An evaluation of harmonic losses for an induction motor driven by CHB has been presented and discussed in [II,17], by considering three different modulation strategies at no-load operations. The effect of different converter topologies on the iron loss of non-oriented electrical steel at different switching frequencies has been carried out in [II,18]. In detail, this analysis employs two-level inverters alongside three and five-level T-type NPC configurations. Noteworthy is the observation that the five-level converter, even at a low carrier frequency, exhibits lower iron losses in comparison to the other converters. This analysis is limited only to evaluate the iron losses at no-load conditions. The effect of MIs on power losses of wound-field synchronous machine cores has been studied in [II,19]. Again, this study focuses on iron losses, emphasizing the favorable influence of the number of inverter voltage levels in reducing these losses compared to traditional two-level solutions. An investigation of 60 kW IPMSM losses driven by a 100 kVA seven-level MI is discussed in [II,20].

Scientific literature review shows that only a few works focus on the CHB-fed IPMSM drives and, in any case, a detailed analysis on relationship between harmonic power losses and the chosen inverter topology, modulation strategy, and switching frequency value lacks in-depth exploration. Then, in this chapter, the design, implementation and experimental performance analysis of a 3P-5L-CHB-fed IPMSM drive is carried out. The design and implementation process is carried out at the SDESLAB of the University of Palermo and involves both hardware and software aspects, covering the design and realization of conditioning circuits for current and speed measurement, as well as the control software implementation. The core control strategy is FOC, that it integrated with the modulation

stage detailed in Chapter I, allowing for switching between the mentioned MC-PWM strategies.

Electric drive performance analysis deal with experimentally investigating the impact of MC-PWM strategies on IPMSM current harmonic distortion and harmonic power losses over a wide operating range, defined in terms of motor speed and torque. In detail, to perform accurate current THD and IPMSM loss maps identification, sixteen IPMSM Working Points (WPs) defined in the torque-frequency plane have been defined at a switching frequency value of 4 kHz and for the other switching frequency values nine IPMSM WPs have been selected to analyze the impact of switching frequency. With this aim, taking into account results achieved in the previous chapter, three different MC-PWM strategies, i.e., PD, PS, and SCAMOD, with sinusoidal modulating signals, and four different switching frequency values, ranging from 4 kHz to 16 kHz with a step of 4 kHz, are considered. Each MC-PWM strategy exhibits a distinct harmonic spectrum. A frequency domain power analysis approach is adopted to segregate the total power losses into fundamental and harmonic power losses [II,21]-[II,22]. Furthermore, to quantify the IPMSM efficiency improvement derived by the use of CHB inverter, a comparison with a conventional 2L-VSI is carried out under the same work conditions.

II.2 Field Oriented Control Mathematical Formulation

The FOC allows for regulating the motor torque and magnetic flux independently, by properly controlling the stator currents. In detail, according to [II,23], Park transformation, whose transformation matrix $\mathbf{T}_{dq}$ is reported in (II,1), allows for projecting the main electric quantities represented in the original ABC frame, in the bi-dimensional dq reference frame that is rotating at the synchronous speed ω_e and whose d and q axis are aligned with the motor magnetic direct and quadrature axis, respectively.

$$\mathbf{T}_{dq} = \frac{2}{3} \begin{bmatrix} \cos(p\theta) & \cos\left(p\theta - \frac{2\pi}{3}\right) & \cos\left(p\theta + \frac{2\pi}{3}\right) \\ -\sin(p\theta) & -\sin\left(p\theta - \frac{2\pi}{3}\right) & -\sin\left(p\theta + \frac{2\pi}{3}\right) \end{bmatrix} \quad (\text{II},1)$$

where θ is the rotor angular position and p is the number of machine pole pairs. In order to design the FOC, the standard IPMSM model in the dq reference frame is introduced. According to [II,24] and [II,25], the control model is based on the following hypothesis: the core saturation is neglected; hysteresis and eddy currents are neglected; the electromotive force is sinusoidal. Consequently, the motor parameters, i.e., the stator resistance R , the

direct and quadrature inductances L_d and L_q , and the permanent magnet flux ψ_{PM} are assumed to be constant, and the following equations are obtained:

$$\psi_d = L_d i_d + \psi_{PM} \quad (\text{II},2)$$

$$\psi_q = L_q i_q \quad (\text{II},3)$$

$$v_d = R i_d + L_d \frac{d}{dt} i_d - p \omega_m L_q i_q \quad (\text{II},4)$$

$$v_q = R i_q + L_q \frac{d}{dt} i_q + p \omega_m (L_d i_d + \psi_{PM}) \quad (\text{II},5)$$

$$T_{em} = \frac{3}{2} p (\psi_{PM} i_q - (L_q - L_d) i_d i_q) \quad (\text{II},6)$$

$$T_{em} - T_L = F_m \omega_m + J_m \frac{d}{dt} \omega_m \quad (\text{II},7)$$

where ω_m is the mechanical rotor speed, T_L is the load torque, J_m is the machine inertia, F_m is the friction. Looking at equations (II,2)-(II,6), some considerations can be carried out: according to the flux equations, the IPMSM magnetization depends on the permanent magnet flux ψ_{PM} and the direct current i_d ; the torque equation is composed of two terms, named fundamental and reluctance torque: the former depends on the permanent magnet flux ψ_{PM} and on the quadrature current i_q ; the latter depends on both the direct and quadrature currents i_d and i_q and on the machine saliency. To ensure that the IPMSM is exclusively magnetized by permanent magnets and that the IPMSM torque is exclusively proportional to the quadrature current i_q , the direct current i_d component must be actively controlled to remain zero. As a consequence, it is possible to define two control channels, the d and q channels, that allow for controlling the magnetic flux and the torque independently, through the d and q currents, respectively. Currents are controlled by imposing the stator voltages v_d and v_q . However, looking at equations (II,4) and (II,5), it can be noted that each current depends on both the stator voltages v_d and v_q , making the control of each current independent a challenging task. For this reason, the decoupling equations are introduced, and the voltages $\hat{v}_d$ and $\hat{v}_q$ are defined as:

$$\hat{v}_d = v_d + p \omega_m L_q i_q \quad (\text{II},8)$$

$$\hat{v}_q = v_q - p \omega_m (L_d i_d + \psi_{PM}) \quad (\text{II},9)$$

According to equations (II,4), (II,5), (II,8) and (II,9), the voltages $\hat{v}_d$ and $\hat{v}_q$ depend only on the homonymous currents i_d and i_q , respectively. Then, the obtained FOC block scheme is shown in Fig. II. 1. In detail, the q control channel is characterized by two cascaded control loops. Cascaded control theory is based on the assumption that the electric dynamic of the machine is much faster than the mechanical one; such an assumption allows for implementing two independent speed and current controllers, arranged in a cascade,

designed on mechanical or electrical equations only. Then, the inner control loop allows for controlling the torque or, equivalently, the current i_q through the stator voltage v_q . The reference q current i_q^* can be set by the user or can be imposed by the outer speed control loop. In detail, the mechanical speed ω_m is controlled by imposing the reference current i_q^* at the inner control loop.

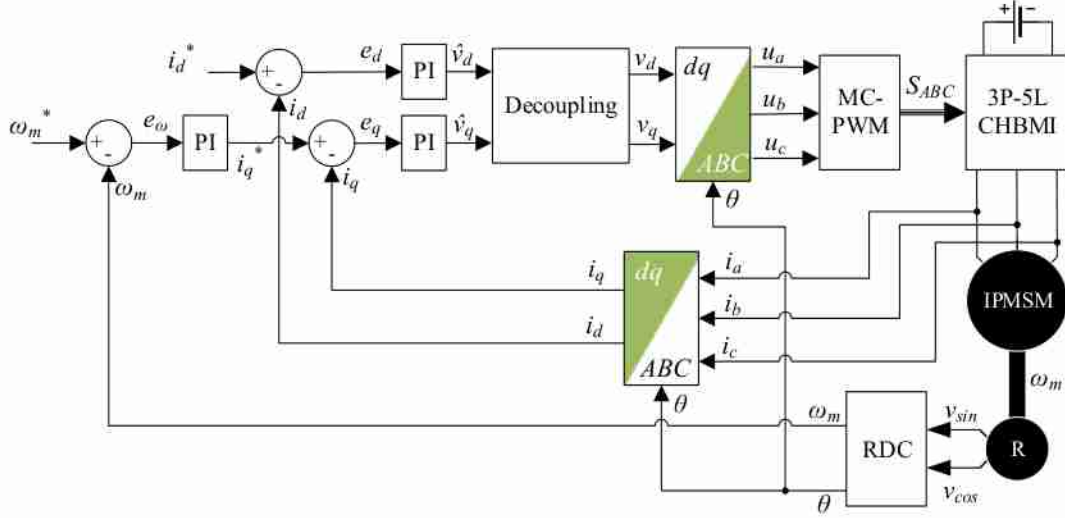


Fig. II. 1: Field oriented control block scheme.

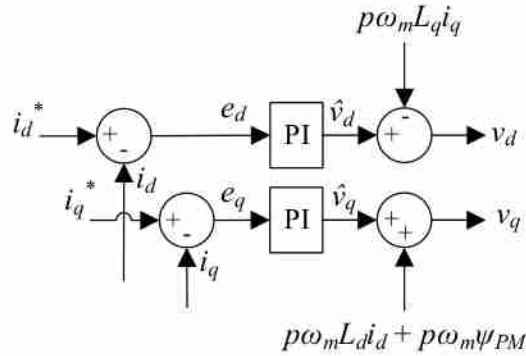


Fig. II. 2: Operations included within the “decoupling” block, shown in Fig. II. 1

Every control loop is based on the Proportional Integral (PI) regulator, whose control law is reported below:

$$y_{PI} = k_p e + \int k_i e dt \quad (\text{II},10)$$

where e is the control error, defined as the difference between the reference and the measured signals, and k_p and k_i are the proportional and integral action gains.

With respect to the d and q current control loops, measured currents i_a , i_b , and i_c are projected in the rotating dq reference frame through the transformation matrix reported in (II,1); similarly, the stator control voltages v_d and v_q are projected in the ABC reference frame through the inverse Park transformation, whose matrix $T_{dq,inv}$ is shown below:

$$\mathbf{T}_{dq,inv} = \begin{bmatrix} \cos(p\theta) & -\sin(p\theta) \\ \cos\left(p\theta - \frac{2\pi}{3}\right) & -\sin\left(p\theta - \frac{2\pi}{3}\right) \\ \cos\left(p\theta + \frac{2\pi}{3}\right) & -\sin\left(p\theta + \frac{2\pi}{3}\right) \end{bmatrix} \quad (\text{II},11)$$

Control voltages in the ABC frame u_a , u_b , and u_c represents the modulating signals to compare to the triangular carrier signals in order to generate the GCSs. It must be underlined that the FOC block scheme shown in Fig. II. 1 is valid for every IPMSM drive, independently of the adopted inverter topology. Indeed, only the modulation stage, represented by the block “MC-PWM” must be properly adapted to the inverter topology. Details related to the modulation stage for a 3P-5L-CHBBI are deeply discussed in Chapter I of this work. Moreover, the adoption of a modulation stage allows for fixing the desired switching frequency.

In the following, the experimental implementation of a FOC for a 3P-5L-CHB-fed IPMSM drive is discussed, both on the hardware and software side.

II.3 Test Bench Description

The test bench of the IPMSM drive fed by the 3P-5L-CHB inverter prototype housed at the SDESLAB at the University of Palermo is depicted in Fig. II. 3.

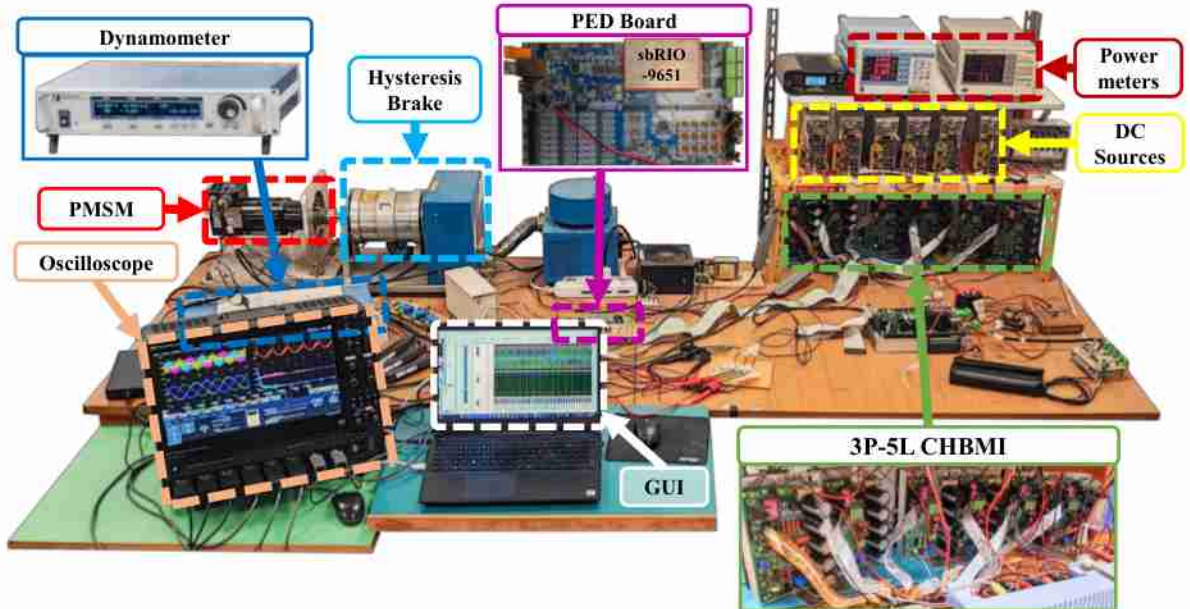


Fig. II. 3: Test bench of the PMSM drive fed by 3P-5L-CHB housed at the SDESLAB laboratory at the University of Palermo, Palermo, Italy.

The electrical drive consists of a DigiPower 3P-5L CHB prototype, composed of six MOSFET-based HB modules powered by six 55 V DC power supply RSO-2400 and 6 poles,

three-phase IPMSM (Magnetic S.r.l., type BLQ-40). Part of this test bench is the same adopted for the CHB open-loop characterization, then, the main technical data of the CHB prototype and DC power supplies are reported in Section I.7 of this work. The main data of the IPMSM are reported in Table II. 1. A MAGTROL HD-715-8NA hysteresis brake is adopted to apply the load torque to the IPMSM, its maximum load torque is 6.2 Nm and the maximum speed is 30000 rpm. The hysteresis brake is controlled by a MAGTROL DSP6001 high-speed programmable dynamometer, which allows direct reading of torque, speed, and mechanical power. The AC-side quantities are measured through a Teledyne LeCroy MDA 8028HD oscilloscope, equipped with three high voltage differential probes Teledyne Lecroy HVD3106A 1 kV, 120 MHz, and three high sensitivity current probes Teledyne Lecroy CP030A AC/DC, 30 A rms, 50 MHz. DC-side measurements are carried out by two current probes Yokogawa 701933 and Yokogawa WT 330 & WT 130 power meters, whose main technical data are reported in Section I.7. The adopted control board is the PED-board equipped with SoM sbRIO 9651 control board, whose technical data are reported in Section I.6.

Table II. 1: Permanent Magnet Brushless Servomotor Main Data.

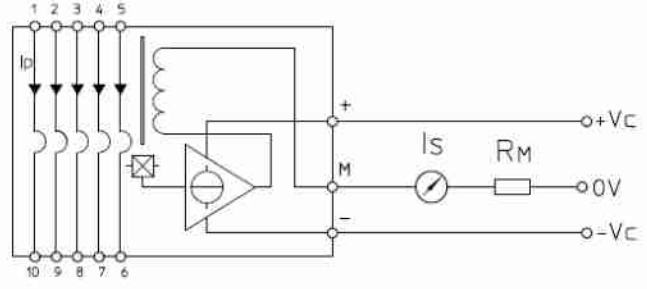
<i>Quantity</i>	<i>Symbol</i>	<i>Value</i>
Rated speed	n_R	4000 rpm
Back EMF	E_p	33 V/krpm
Rated torque	T_R	1,8 Nm
Rated current	I_R	3,6 Arms
Maximum torque	T_p	7,2 Nm
Maximum current	I_p	14.4 A
Pole pairs	p	3

II.4 Field Oriented Control Implementation

In this section, the FOC hardware and software implementation is discussed. In detail, the hardware implementation deals with the design and realization of the conditioning circuits for current and speed measurement, and the software implementation deals with the implementation of the FOC on the adopted control board.

II.4.1 Current Measurement

In order to measure phase currents for control purposes, three Hall effect sensors LEM LA25-NP are adopted. The sensor picture and schematic are shown in Fig. II. 4 and its main data are summarized in Table II. 2.



(a)

(b)

Fig. II. 4: Hall effect sensor LEM LA25-NP (a) picture, (b) schematic.

Table II. 2: Main data of hall effect sensor LEM LA25-NP.

Quantity	Symbol	Value
Primary Nominal current rms	I_{PN}	25 A
Primary current measuring range	I_{PM}	$0 \dots \pm 36$ A
Measuring resistance ($T_a=70^\circ\text{C}$, $I_{PN}=25$ A)	R_M	100-190 Ω
Secondary nominal current rms	I_{SN}	25 mA
Conversion ratio	K_n	1-2-3-4-5:1000
Supply voltage ($\pm 5\%$)	V_c	± 15 V
Current consumption	I_c	$10 + I_S$ mA

The sensor conversion ratio G_{LEM} is chosen as equal to 1/1000. A schematic circuitual representation of the signal conditioning circuit, related to each current sensor, is reported in Fig. II. 5. It consists shunt resistor, a passive filtering stage, and an amplification stage.

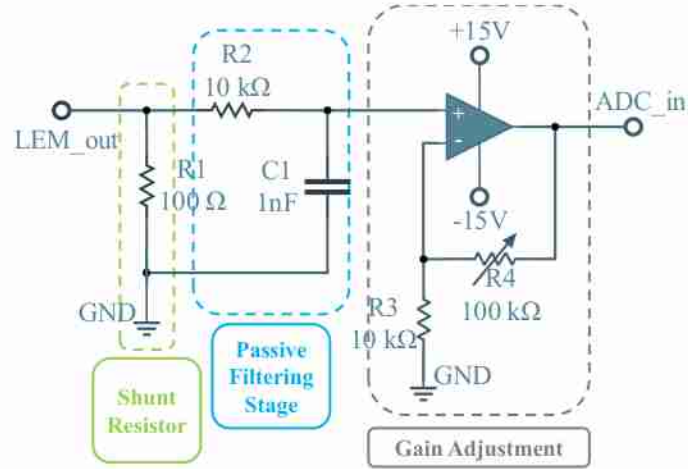


Fig. II. 5: current sensing conditioning circuit.

The shunt resistor allows for assigning to the LEM output current $i_{LEM,OUT}$ a resistance voltage v_{R1} , such that the shunt resistor transfer function G_{shunt} is:

$$G_{shunt} = \frac{v_{R1}}{i_{LEM,out}} \quad (\text{II},12)$$

A 100 Ω shunt resistor is adopted, then G_{shunt} is constant and equal to 100.

The passive filtering stage is realized through a first-order RC filter, whose cut-off frequency $f_{ctf,i}$ is expressed as:

$$f_{ctf,i} = \frac{1}{2\pi R_2 C_1} \quad (\text{II},13)$$

and is equal to 15.92 kHz, according to the R_2 and C_1 values reported in Fig. II. 5. For frequencies lower than $f_{ctf,i}$, the RC filter gain $G_{RC,i}$ is equal to 1.

The amplification stage is realized through an op-amp in a non-inverting configuration, whose amplification gain $G_{op,i}$ is expressed as:

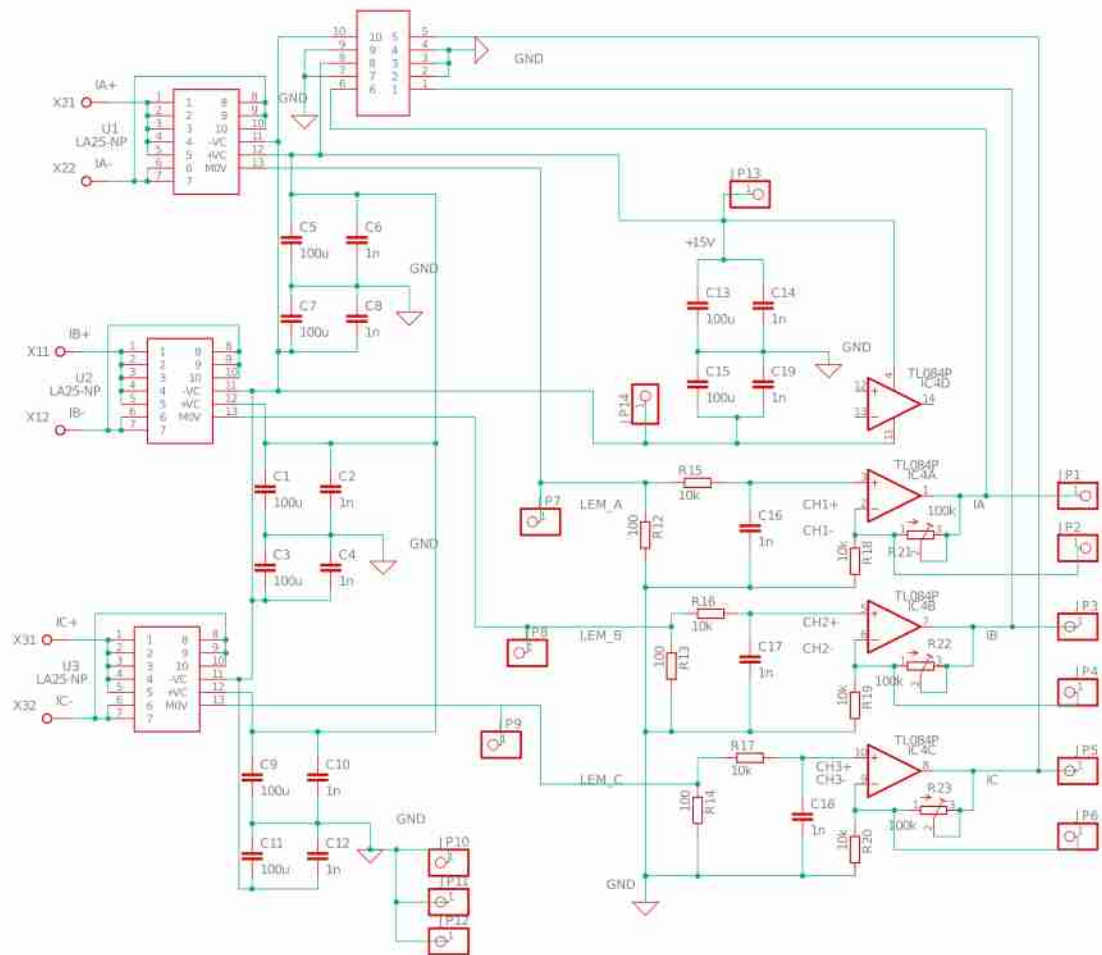
$$G_{op,i} = 1 + \frac{R_4}{R_3} \quad (\text{II},14)$$

The total current transformation ratio $G_{tot,i}$ is defined as:

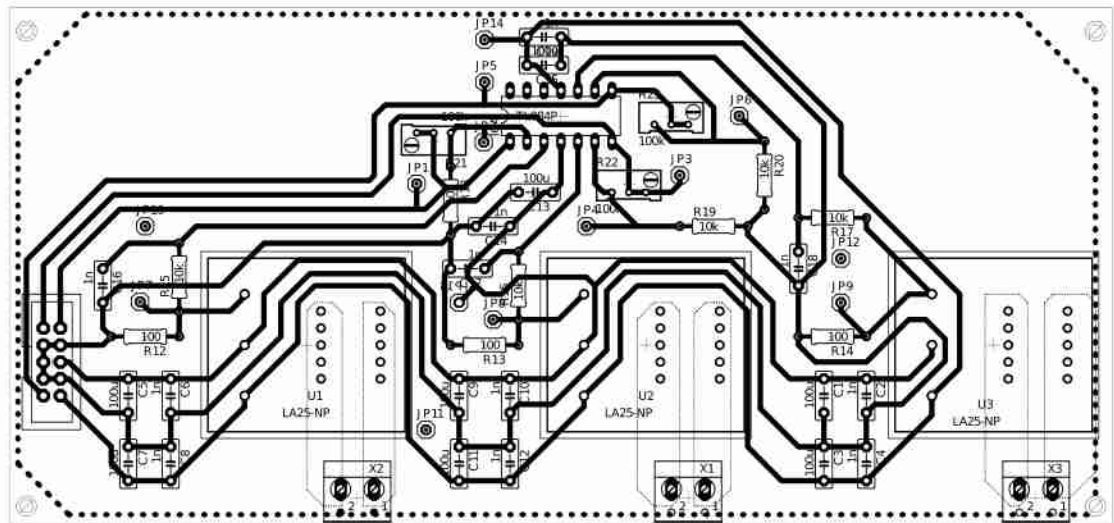
$$G_{tot,i} = \frac{V_{ADC,in}}{i_{LEM,in}} = G_{LEM} \cdot G_{shunt} \cdot G_{RC,i} \cdot G_{op,i} \quad (\text{II},15)$$

where $i_{LEM,in}$ is the measured phase current. $G_{tot,i}$ can be set by the user through the trimmer in the op-amp feedback loop, to match the PED-Board 14-bit Analog to Digital Converter (ADC) input voltage range of ± 5 V, according to data reported in Section I.6. In detail, choosing $R_3=10$ k Ω and setting the trimmer such that $R_4=15$ k Ω , $G_{tot,i}=0.25$. The equation (II,15) must be considered to scale the acquired currents in the software section properly.

The discussed conditioning circuit is designed in the Autodesk Eagle environment. In detail, the current sensors conditioning circuit schematic and Printed Circuit Board (PCB) layout implemented are shown in Fig. II. 6 (a) and (b), respectively. The current conditioning board is realized at the Rapid Prototyping Laboratory (RPLab) at the University of Palermo with LPKF milling machine. The final conditioning board is shown in Fig. II. 7.



(a)



(b)

Fig. II. 6: Current sensing conditioning circuit designed in the Autodesk Eagle Environment : (a) schematic, (b) PCB layout.

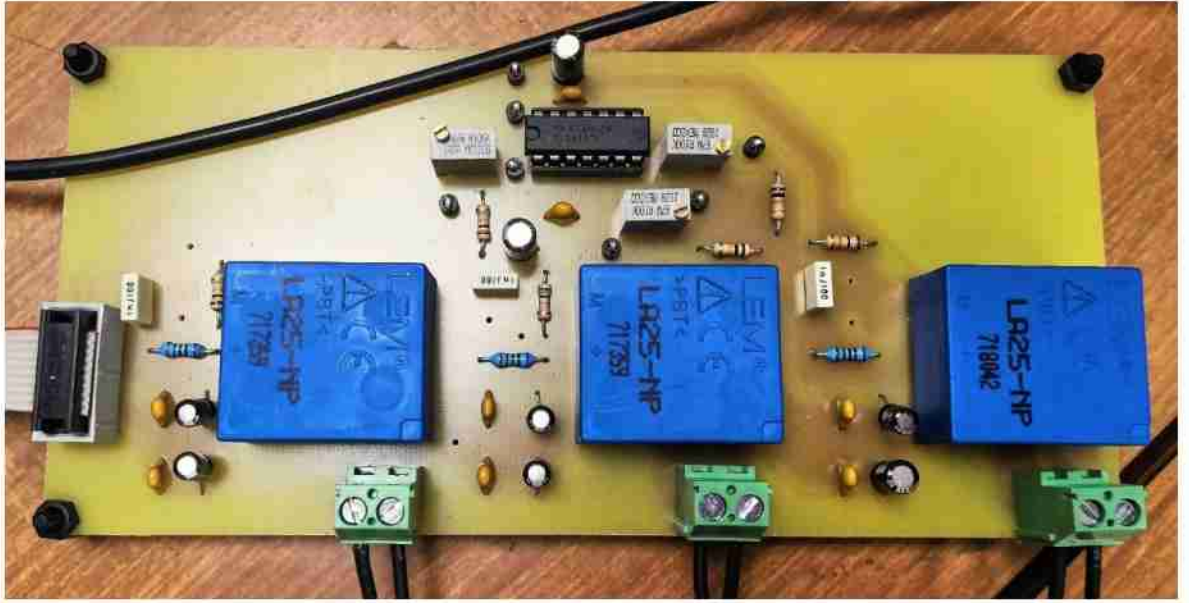


Fig. II. 7: Current conditioning board realized at the Rapid Prototyping Laboratory, at the University of Palermo, Palermo, Italy.

II.4.2 Resolver to Digital Conversion

For rotor speed and position measurement, a Resolver to Digital Conversion (RDC) system is adopted. The resolver is a speed sensor based on the principle of mutual induction; it is a rotating electric machine with a primary rotor winding that allows the sensor excitation, and two secondary stator windings with magnetic axes 90° electrical degrees displaced. The resolver is mechanically coupled with the motor shaft and supplied by a sinusoidal excitation voltage, defined as:

$$v_{ex} = V_{ex} \sin(\omega_{ex} t) \quad (\text{II},16)$$

where V_{ex} is the resolver sinusoidal supply excitation voltage amplitude and ω_{ex} is the excitation voltage angular frequency. When the shaft starts rotating, two amplitude-modulated sinusoidal voltage waveforms $v_{\sin}$ and $v_{\cos}$ are induced in the stator windings. According to [II,26] and [II,27], they can be expressed as:

$$v_{\sin} = k_t V_{ex} \left[\sin(\theta) \cos(\omega_{ex} t) + \frac{1}{\omega_{ex}} \frac{d\theta}{dt} \cos(\theta) \sin(\omega_{ex} t) \right] \quad (\text{II},17)$$

$$v_{\cos} = k_t V_{ex} \left[\cos(\theta) \sin(\omega_{ex} t) + \frac{1}{\omega_{ex}} \frac{d\theta}{dt} \sin(\theta) \cos(\omega_{ex} t) \right] \quad (\text{II},18)$$

where k_t is the resolver transformation ratio. Since the excitation frequency ω_{ex} is chosen such that $\omega_{ex} \gg d\theta/dt$, the second term in (II,17) and (II,18) can be neglected, leading to:

$$v_{\sin} = k_t V_{ex} [\sin(\theta) \cos(\omega_{ex} t)] \quad (\text{II},19)$$

$$v_{\cos} = k_t V_{ex} [\cos(\theta) \sin(\omega_{ex} t)] \quad (\text{II},20)$$

In Fig. II. 8 (a), the resolver excitation voltage and the induced amplitude-modulated voltages in the resolver stator windings are shown.

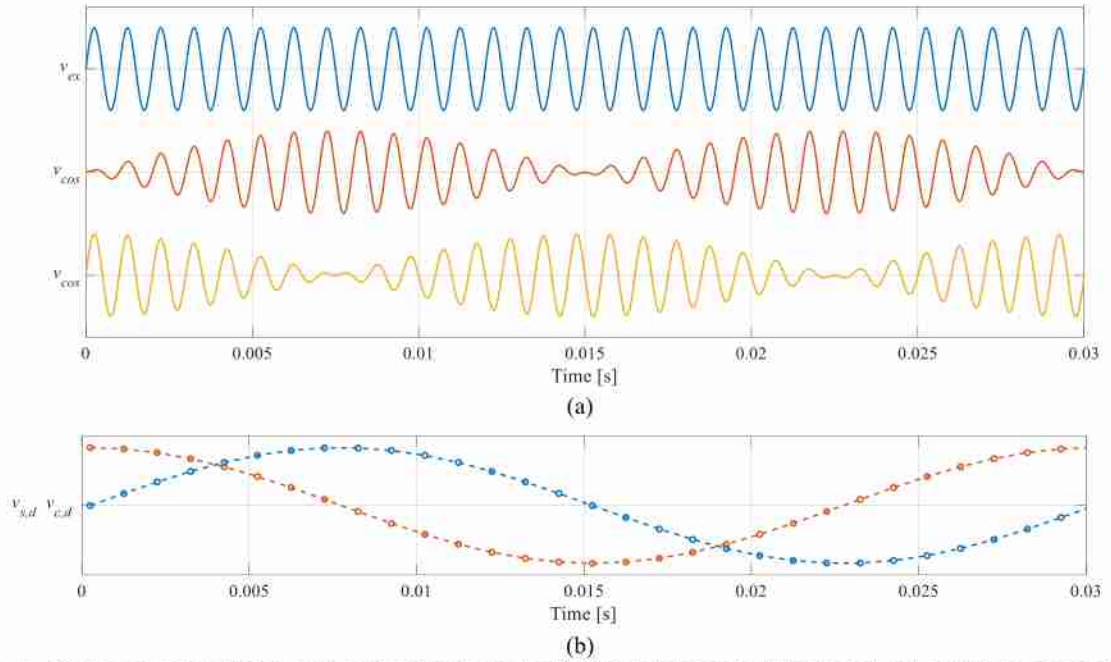


Fig. II. 8: (a) resolver excitation signal and induced amplitude modulated signals, (b) sampled and demodulated signals.

In order to introduce information related to the rotor speed and angular position in the control loop, waveforms v_{sin} and v_{cos} must be properly sampled and elaborated. With this aim, several approaches are proposed in the scientific literature [II,28]-[II,32]. However, in this work, the approach proposed in [II,33] is adopted and expanded. In detail, signals v_{sin} and v_{cos} are sampled by the controller ADC in order to match the following conditions:

- The sampling frequency must be equal to the resolver excitation frequency;
- The sampling instant must coincide with the excitation sinusoidal waveform peak.

If such conditions are matched, the sampled signals $v_{s,d}$ and $v_{c,d}$ represent the amplitude-modulated sinusoidal voltage waveforms v_{sin} and v_{cos} envelopes, whose frequency depends only on the rotor speed ω_m , as it is shown in Fig. II. 8 (b). Then, information related to rotor angular speed and position is obtained by adopting the Angle Tracking observer (ATO) algorithm, whose block diagram is shown in Fig. II. 9. In detail, demodulated signals $v_{s,d}$ and $v_{c,d}$ are multiplied by signals $\cos\varphi$ and $\sin\varphi$, where φ is the estimated rotor angular position at the previous iteration. The obtained signals are compared to each other and the error generated is sent to a PI regulator that returns the speed signal. This signal is filtered by a Moving Average Filter (MAF) to eliminate the ripple; the filtered signal ω_m is integrated and the estimated angular position φ is obtained.

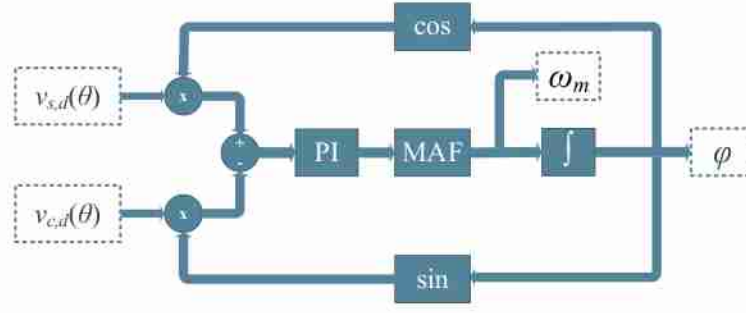


Fig. II. 9: Angle tracking observer algorithm.

The adopted resolver for this application is the ARTUS S26SM19RX452CO1F, whose main data are reported in Table II. 3.

Table II. 3: Main data of the ARTUS S26SM19RX452CO1F.

Data	Value
Input voltage/frequency	10 V at 5 kHz
Transformation ratio	$0.5 \pm 10\%$
Max. electrical error	$\pm 10^\circ$
Max. null Voltage	20 mV _{RMS}
Operating Temperature	$-55^\circ\text{C} + 155^\circ\text{C}$
Max. operating speed	10 000 rpm
Mass	0.34 kg

In Fig. II. 10, the Resolver to Digital Conversion (RDC) block scheme is presented.



Fig. II. 10: Resolver excitation system and Resolver-to-digital conversion stage.

The excitation signal v_{ex} is generated starting from two 5 V PWM signals S_H and S_L , generated by the sbRIO 9651 FPGA controller. For this purpose, the Unipolar PWM scheme, shown in Fig. II. 11, is adopted. Introducing the carrier frequency f_c and the sinusoidal excitation voltage frequency f_{ex} , the excitation frequency modulation index m_f is defined as:

$$m_{f,ex} = \frac{f_c}{f_{ex}} \quad (\text{II},21)$$

Choosing an even m_f value, harmonics of the signal $S_H - S_L$ are placed around twice the carrier frequency and its multiples. This propriety makes the generated signals extremely simple to be filtered.

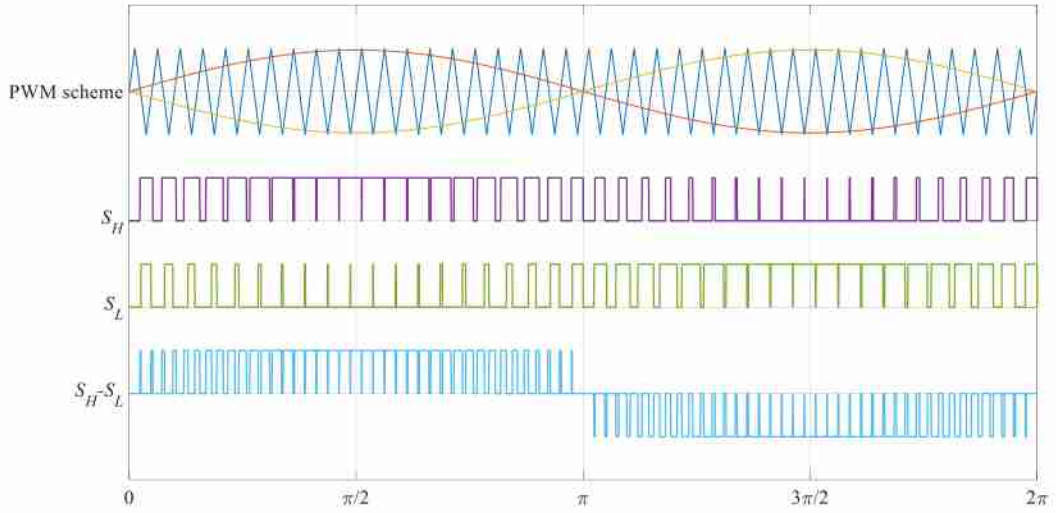


Fig. II. 11: Unipolar PWM Modulation scheme, PWM signals and excitation signal H-L.

Although the resolver rated frequency is 5 kHz, a 10 kHz sinusoidal excitation voltage-modulating signal is generated, for control needs. m_f is chosen equal to 40. then, PWM signals are generated by the comparison of a 400 kHz triangular and two opposite phase 10 kHz sinusoidal modulating signals. Then, harmonics are placed around 800 kHz and its multiples.

Two generated PWM signals S_H and S_L are sent to the resolver excitation signal conditioning circuit, represented in Fig. II. 12. It consists of three different stages: passive filtering, active filtering and pre-amplification, and power amplification.

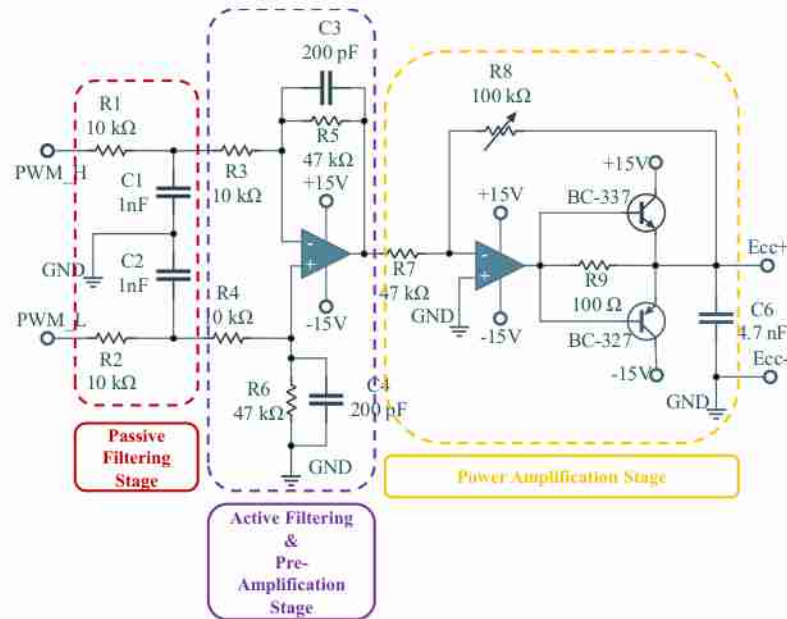


Fig. II. 12: Resolver excitation signal conditioning circuit.

The passive filtering stage is realized through first order RC filter, whose cut-off frequency $f_{cf,r1}$ is computed according to equation (II,13) and is equal to 15.9 kHz, according to the resistance and capacitance values reported in Fig. II. 12. For frequencies lower than $f_{cf,r1}$, the RC filter gain $G_{RC,r}$ is equal to 1. It must be underlined that since harmonics of the signal $S_H - S_L$ are placed around 800 kHz and its multiples, the adopted cut-off frequency allows for a complete harmonic filtration and only the fundamental component at 10 kHz is transmitted.

The active filtering and pre-amplification stage consists of an op-amp in a differential configuration. It allows for electrically subtracting the PWM signals S_H and S_L , and it is characterized by an amplification gain $G_{op,r1}$ expressed as:

$$G_{op,r1} = \frac{R_5}{R_3} \quad (\text{II},22)$$

and it is equal to 4.7, according to the resistance values reported in Fig. II. 12. The cut-off frequency can be expressed according to equation (II,13) and it is equal to 16.9 kHz.

The power amplification stage consists of another op-amp in inverting configuration with adjustable gain and a class B BJT-based power amplifier, which feeds the required current to the excitation circuit and whose amplification gain is equal to:

$$G_{op,r2} = -\frac{R_8}{R_7} \quad (\text{II},23)$$

The output gain is manually tuned acting on the trimmer R_8 , to match the required resolver excitation voltage. Thus, a 10 V 10 kHz sinusoidal excitation signal is obtained, and the final value of R_8 is equal to 38 k Ω . It must be underlined that since the adopted resolver is characterized by a transformation ratio of 0.5, the amplitude-modulated signals exhibit a peak value of 5 V.

The discussed resolver excitation signal conditioning circuit is designed in the Autodesk Eagle environment. In this case, the PCB is designed to be placed on top of the control board and directly connected to it via a snap-fit. Then, it is named PED-Board Shield. Moreover, the PCB is also used to manage various control signals, both analog and digital, such as PWM signals for CHB control, current measurement signals sent to the controller ADC, resolver excitation signals, amplitude-modulated resolver output signals sent to the ADC, ± 15 V PCBs power supply, and 5 V power supply for the HB electronics. The PED-Board Shield schematic and PCB layout are shown in Fig. II. 13 (a) and (b), respectively. The final version of the PED-Board Shield realized at the RPLab is shown in Fig. II. 14.

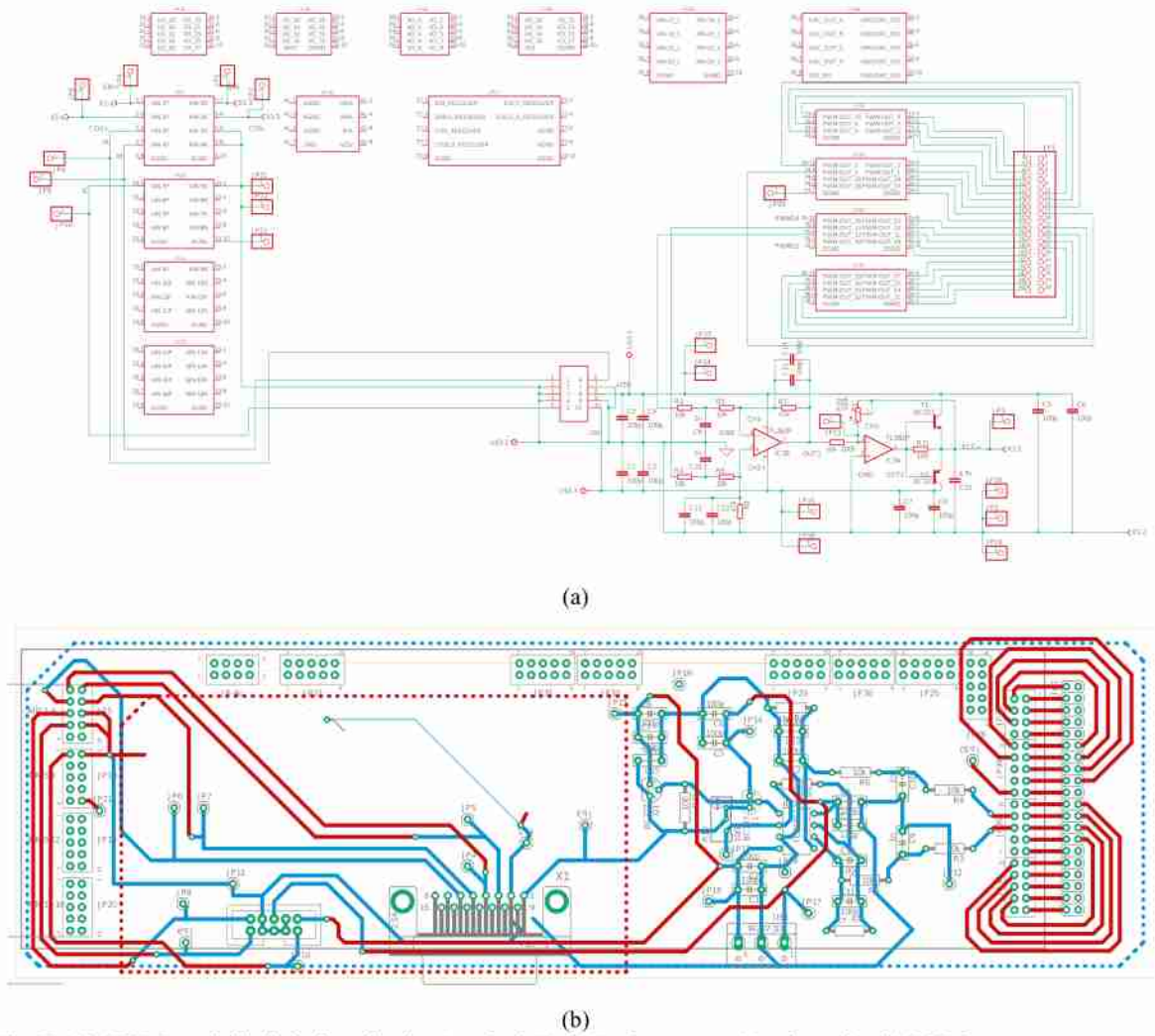


Fig. II. 13: PED-Board shield designed in the Autodesk Eagle Environment : (a) schematic, (b) PCB layout.

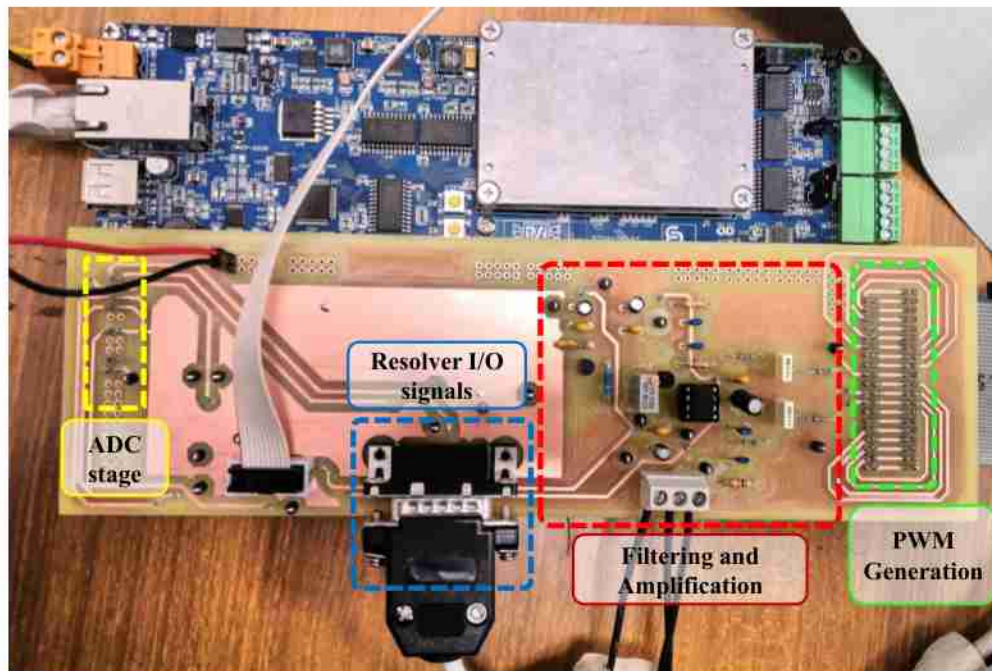


Fig. II. 14: PED-Board shield realized at the Rapid Prototyping Laboratory, at the University of Palermo, Palermo, Italy.

It is interesting to analyze the cost of the proposed resolver conditioning circuit since, both in literature and on the market, the most common solution deals with adopting an integrated RDC system, such as the RDS AD2S1205. This solution presents some disadvantages, i.e., poor versatility, high cost, and low reliability. In Table II. 4, the required electronic components and the total price for the excitation voltage conditioning circuit are summarized. Although the PCB realization of the conditioning circuit is carried out homemade with an LPKF milling machine, the cost analysis includes the commercial cost of required electronic components and PCB board realization. The total cost is equal to € 13.71. In this evaluation, a stock of 100 units has been considered for each component and the PCB board. This price is evaluated as the average price of each electronic component by referring to well-known electronic components sellers, such as [II,34]-[II,36]. Obviously, if an industrial application is considered, the purchase of such components in large quantities results in a further cost reduction. For comparison purposes, the average market cost of an RDS AD2S1210 is € 29.15 [II,37]-[II,38] which is double that of the proposed RDC hardware interface and does not include the costs of the necessary buffer circuits.

Table II. 4: Cost analysis of the proposed resolver excitation circuit.

Electronic component	Required number	Cost per unit [€]
Resistors 10 k Ω	4	0.086
Resistors 47 k Ω	4	0.071
Resistors 100 Ω	1	0.086
Capacitor 1nF	2	0.25
Capacitor 200pF	2	0.163
Capacitor 4.7nF	1	0.34
Trimmer 100 k	1	2.39
Transistor NPN	1	0.254
Transistor PNP	1	0.271
TL 082	1	0.98
D-sub 15 pins	1	2.59
PCB terminal block 3 ways	1	1.66
Connector 72 pins 2.54mm step	1	2.61
PCB board		1.08
Total		13.71

II.4.3 PCBs Power Supply

Analog circuits introduced in the previous sub-sections require ± 15 V supply voltage. For this purpose, an external power supply, whose schematic is presented in Fig. II. 15, is realized. It consists of a transformer with a central socket and nominal transformation ratio of 230V/40V, FB100 voltage rectifier, LM 7815 and 7915 voltage regulators, that guarantee ± 15 V output voltage.

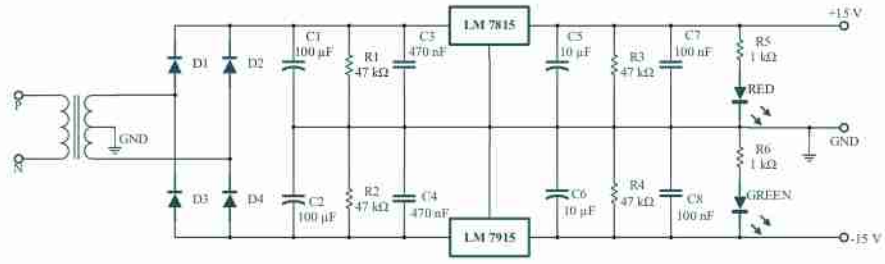


Fig. II. 15: Externa power supply schematic.

The external power supply circuit is designed in the Autodesk Eagle environment and the schematic and PCB layout are shown in Fig. II. 16 (a) and (b), respectively. The final circuit board is shown in Fig. II. 17.

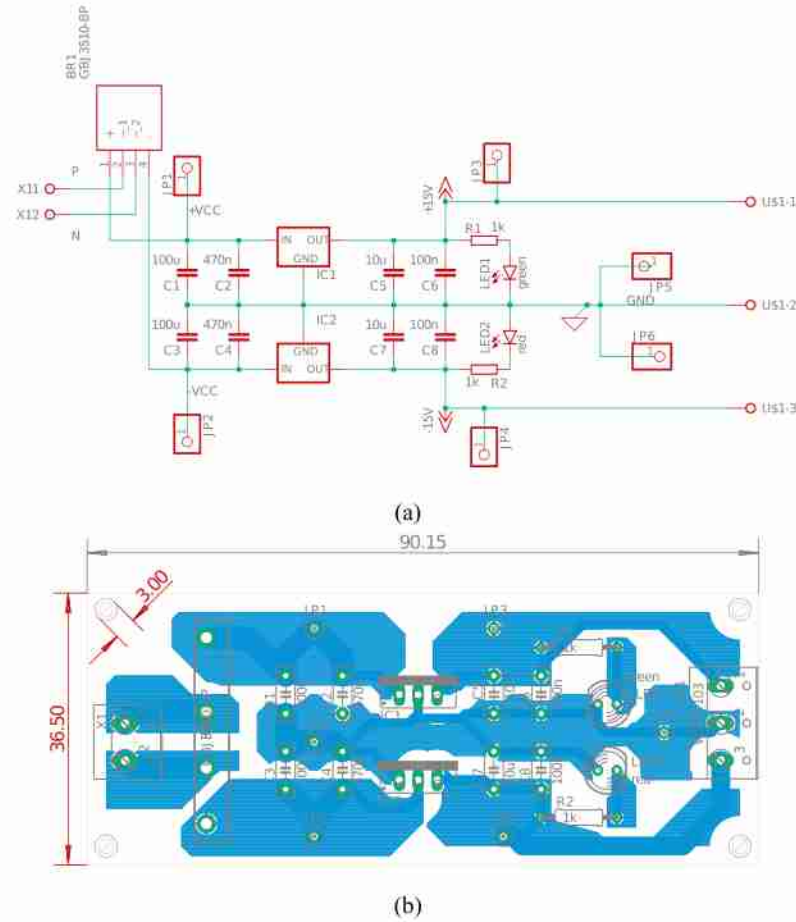


Fig. II. 16: External ± 15 V power supply for current and speed measurement conditioning circuits, designed in the Autodesk Eagle Environment : (a) schematic, (b) PCB layout.



Fig. II. 17: External ± 15 V power supply board realized at the Rapid Prototyping Laboratory, at the university of Palermo, Palermo, Italy.

II.4.4 Field Oriented Control Software Implementation

In Fig. II. 18, the block scheme of the FOC algorithm implemented in the LabVIEW environment is presented. The approach to the control implementation on the sbRIO 9651 controller is similar to that adopted in Section I.6. In detail, three main loops can be identified: the TL, and two WLs, named High Frequency (HF) WL and Low Frequency (LF). These three structures run in parallel and are synchronized with each other.

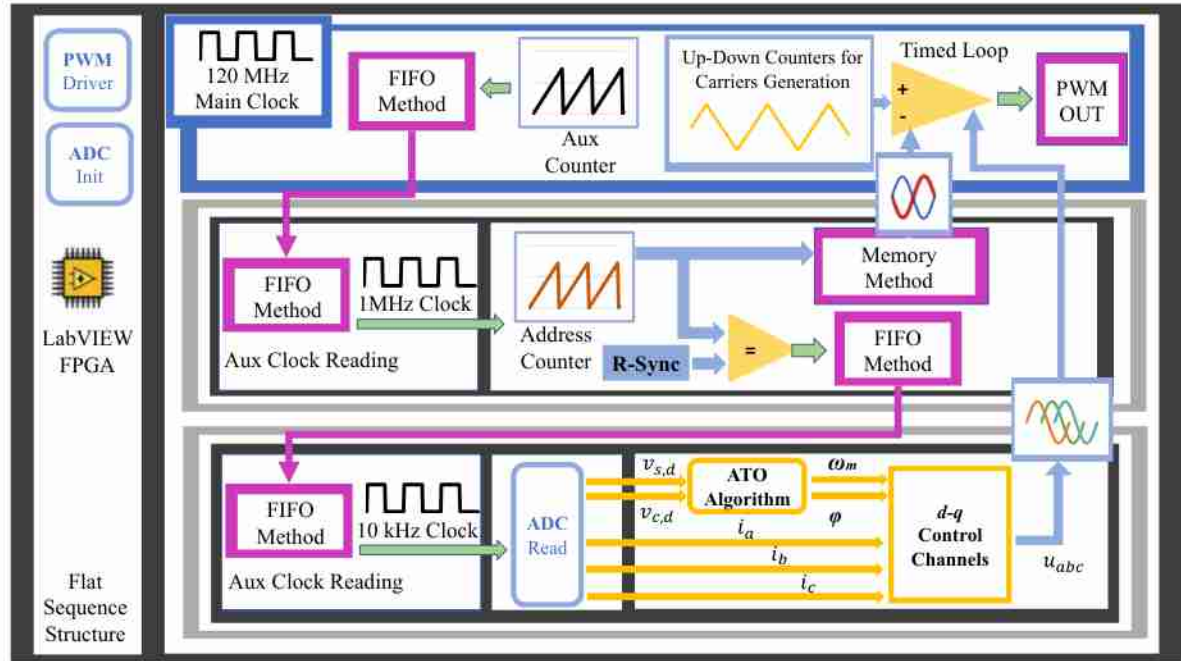


Fig. II. 18: Block diagram of the Field Oriented Control implemented in the LabVIEW environment.

The TL is the main scheduler, i.e., it temporizes the other loops in a cascaded fashion. Operations arranged within the TL are similar to that discussed in Section I.6 and comprehend the MC-PWM carriers generation, the GCSs generation for the CHB inverter control, and the Aux Clock generation. In detail, the Aux Clock is used in this application to trigger the HFWL with a frequency of 1 MHz. Moreover, carrier and PWM signals generation for the resolver excitation signals generation is carried out, according to the discussion in sub-section II.4.2.

The HFWL is triggered with a frequency of 1 MHz clock and it is intended to generate two 10 kHz sinusoidal signals. They are sent to the TL in order to generate PWM excitation signals S_H and S_L . The sinusoidal signals are generated thanks to a sinusoidal 100 elements block memory and an address counter that extracts elements by the memory at each trigger instant. To realize the synchronization between the acquisition stage and the sinusoidal excitation waveform, the address counter is used to generate a 10 kHz auxiliary clock that triggers the LFWL, where the acquisition stage is located. Since the PWM signals are elaborated by an analog conditioning circuit, delays are introduced by the filters. To

compensate for such delays and sample the resolver amplitude modulated voltages according to the conditions discussed in sub-section II.4.2, the LFWL trigger instant is adjusted manually by the user through the GUI, such that the signals $v_{s,d}$ and $v_{c,d}$ match the condition:

$$\sqrt{v_{s,d}^2 + v_{c,d}^2} = V_{\max} \quad (\text{II},24)$$

where $V_{\max}$ must be equal to 5 V, according to the resolver rated excitation voltage and transformation ratio reported in Table II. 3.

The LFWL is triggered with a frequency of 10 kHz and it contains the actual control. In detail, the following operations are executed in series: signals acquisition, ATO algorithm execution, $ABC-dq$ transformation, dq channels control, *decoupling*, $dq-ABC$ transformation, and modulating signals adjustment. All the previously mentioned operations are implemented in single precision floating point data, following the block diagram presented in Fig. II. 1. As a way of example, in Fig. II. 19 a frame of the LFWL, in which position, speed, and currents control with decoupling stage, are implemented.

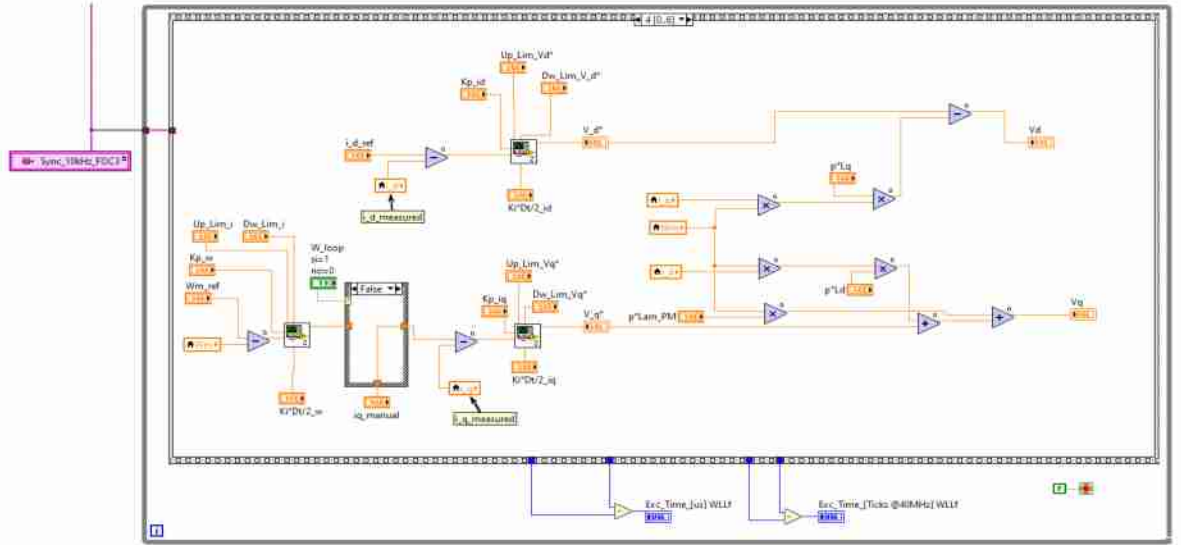


Fig. II. 19: A frame of the WLLF where the dq control is implemented.

PI controllers are implemented by discretizing the equation (II,10) with the trapezoidal integration method, to reduce the integration numerical error. The discrete PI control action $y_{PI}(k)$ at the sampling instant k is expressed as:

$$y_{PI}(k) = k_p e(k) + \frac{k_i T_s}{2} (e(k) + e(k-1)) + y_I(k-1) \quad (\text{II},25)$$

where $e(k)$ and $e(k-1)$ are the control error at the instant k and the previous instant $k-1$, respectively, and T_s is the sampling period. Concerning the speed PI controller, the control action y_{PI} , which corresponds to the reference q -current i_q^* , is saturated to limit the absorbed

stator currents. Such a saturation stage causes the so-called windup phenomenon, i.e., the integral term continues to accumulate, even though the output cannot change. When windup occurs, the controller output may overshoot or oscillate excessively, once the saturation condition is removed. This can lead to poor system performance and even instability. Then, in this application, the adopted anti-windup strategy deals with setting the integral error to zero, when saturation occurs. In this way, the integral state stops varying, i.e., the integral action is constant. The discrete speed PI controller with saturation and anti-windup strategy implemented in the LabVIEW FPGA environment is shown in Fig. II. 20. The q -current is saturated to 10 A, i.e., the peak value of the currents in the ABC is saturated to 10 A, about double the rated PMSM peak current.

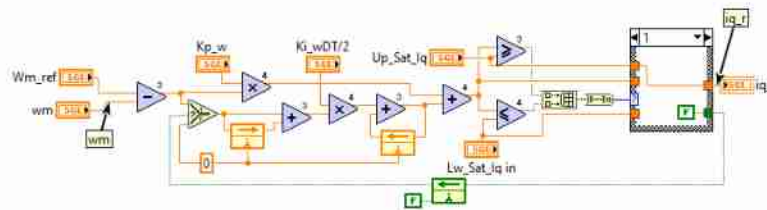


Fig. II. 20: discrete speed PI controller with saturation and anti-windup strategy implemented in the LabVIEW FPGA environment.

Indeed, by assuming that the speed transient is short-lived, it is possible to briefly overload the PMSM to make the speed transient shorter, improving the system dynamic performance.

II.5 PI tuning strategies

According to the discussion carried out so far, four PI controllers, i.e., two current regulator, one speed regulator, and the regulator involved in the ATO observer algorithm, must be tuned. Each regulator is tuned independently due to the cascaded control hypothesis previously mentioned.

II.5.1 Current control loop tuning

The d and q current control channels are summarized through the block scheme reported in Fig. II. 21.

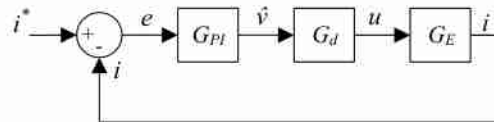


Fig. II. 21: Electric system control scheme.

The block scheme is composed of three cascaded transfer functions, G_{PI} , G_d , and G_E , that allows for modelling the PI controller action, the delay due to the modulation stage, and the

PMSM electric phenomena, respectively. In the Laplace domain, G_{PI} , G_d , and G_E are expressed as:

$$G_{PI} = k_p + \frac{k_i}{s} = k_p \left(1 + \frac{1}{T_i s} \right) \quad (\text{II,26})$$

$$G_d = \frac{u}{\hat{v}} = \frac{1}{1 + T_d s} \quad (\text{II,27})$$

$$G_E = \frac{i}{u} = \frac{1}{R + Ls} \quad (\text{II,28})$$

where T_i is the integral action time constant and T_d is the modulation stage delay. In detail, the transfer function G_E reported in equation (II,28) is derived from the voltage balance equations (II,4) and (II,5) by adopting the decoupling hypothesis reported in (II,8) and (II,9). Such hypothesis allows for obtaining two independent first order transfer functions $G_{E,d}$ and $G_{E,q}$, for the d and q channel respectively. Then, G_E must be particularized depending on the considered control channels. However, equations reported in the following are valid for both d and q control channels. The PI regulator transfer function G_{PI} is derived from (II,10). The transfer function G_d allows for taking into account the adopted modulation strategy through the C_{MC} coefficient, introduced in Chapter I, as follows:

$$T_d = 1.5 \frac{T_{PWM}}{C_{MC}} \quad (\text{II,29})$$

The open loop transfer function F_{ol} and the closed loop transfer function W_E are defined respectively as:

$$F_{ol} = G_{PI} \cdot G_d \cdot G_E = k_p \left(1 + \frac{1}{T_i s} \right) \cdot \left(\frac{1}{1 + T_d s} \right) \cdot \left(\frac{1}{R + Ls} \right) \quad (\text{II,30})$$

$$W_E = \frac{i}{i^*} = \frac{F_{ol}}{1 + F_{ol}} = \frac{k_p \left(1 + \frac{1}{T_i s} \right) \cdot \left(\frac{1}{1 + T_d s} \right) \cdot \left(\frac{1}{R + Ls} \right)}{1 + k_p \left(1 + \frac{1}{T_i s} \right) \cdot \left(\frac{1}{1 + T_d s} \right) \cdot \left(\frac{1}{R + Ls} \right)} \quad (\text{II,31})$$

According to (II,31), W_E is a third order transfer function.

For the current control loop tuning, zero-pole cancellation strategy is adopted. Indeed, by imposing the relation (II,32), i.e., the integral time constant T_i coincides with the electric time constant T_E , it is possible to realize a zero-pole cancellation such that the closed loop transfer function W_E can be rearranged as in (II,33):

$$T_i = T_E = \frac{L}{R} \quad (\text{II},32)$$

$$W_E = \frac{i}{i^*} = \frac{\frac{k_p}{LT_d}}{s^2 + \frac{1}{T_d}s + \frac{k_p}{LT_d}} \quad (\text{II},33)$$

It must be underlined that the integral gain k_i is automatically determined through relations (II,32) and (II,26). Then, it is possible to impose:

$$\frac{1}{T_d} = 2\zeta_E \omega_{n,E} \quad (\text{II},34)$$

$$\frac{k_p}{LT_d} = \omega_{n,E}^2 \quad (\text{II},35)$$

where $\omega_{n,E}$ and ζ_E are the natural pulsation and the damping coefficient of the electrical control loop. By imposing a damping coefficient $\zeta_E=0.707$, it is possible to determine the natural pulsation $\omega_{n,E}$ and the proportional gain k_p as follows:

$$\omega_{n,E} = \frac{C_{MC}}{3\zeta_E T_{PWM}} \quad (\text{II},36)$$

$$k_p = \frac{LC_{MC}}{6\zeta_E^2 T_{PWM}^2} \quad (\text{II},37)$$

II.5.2 ATO PI tuning

Regarding the ATO algorithm reported in Fig. II. 9, for PI tuning purposes it can be simplified by introducing the angle error e_φ as:

$$e_\varphi = k' (\sin \theta \cos \varphi - \cos \theta \sin \varphi) = k' \sin(\theta - \varphi) \quad (\text{II},38)$$

where

$$k' = k_t V_{ex} \quad (\text{II},39)$$

In detail, when $\theta - \varphi$ is lower than 10° , it is possible to assume that:

$$e_\varphi = k' \sin(\theta - \varphi) \approx k' (\theta - \varphi) \quad (\text{II},40)$$

Then, the ATO block scheme can be simplified as:

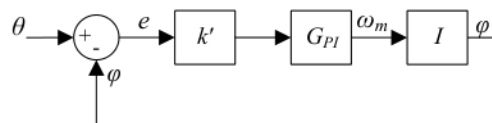


Fig. II. 22: ATO algorithm block scheme.

Where I is the integral action in the Laplace domain. The open loop transfer function F_{ol} , the closed loop transfer function W_{ATO} , and the closed loop error transfer function $F_{e,ATO}$ are defined respectively as:

$$F_{ol,ATO} = k' \cdot G_{PI} \cdot \frac{1}{s} \quad (II,41)$$

$$W_{ATO} = \frac{\varphi}{\theta} = \frac{k'k_p s + k'k_i}{s^2 + k'k_p s + k'k_i} \quad (II,42)$$

$$F_{e,ATO} = \frac{\theta - \varphi}{\theta} = \frac{s^2}{s^2 + k'k_p s + k'k_i} \quad (II,43)$$

Supposing that during an acceleration the mechanical speed varies as a ramp, then the mechanical angle θ is a parabolic input for the system. Under this hypothesis, the steady-state error $e_{\varphi,ss}$ is evaluated through the final value theorem, as follows:

$$e_{\varphi,ss} = \lim_{s \rightarrow 0} s \cdot F_{e,ATO} \cdot \frac{a}{s^3} = s \cdot \frac{s^2}{s^2 + k'k_p s + k'k_i} \cdot \frac{a}{s^3} = \frac{a}{k'k_i} \quad (II,44)$$

Then, by imposing the maximum desired steady state error $e_{\varphi,ss,MAX}$ and the maximum available acceleration, the integral gain k_i can be derived as:

$$k_i = \frac{a_{MAX}}{k' e_{\varphi,ss,MAX}} \quad (II,45)$$

For this application, the maximum steady state error $e_{\varphi,ss,MAX}$ is set equal to 1° and the maximum acceleration a_{MAX} is set thought an experimental test. In detail, a_{MAX} is measured by applying the maximum transient torque, generated by a current $i_q=10$ A, to the PMSM.

In steady state working conditions, the acceleration is zero, the mechanical speed is constant and the mechanical angle θ varies as a ramp. In this context, the steady state error is null, according to (II,46).

$$e_{\varphi,ss} = \lim_{s \rightarrow 0} s \cdot F_{e,ATO} \cdot \frac{\omega_m}{s^2} = s \cdot \frac{s^2}{s^2 + k'k_p s + k'k_i} \cdot \frac{\omega_m}{s^2} = 0 \quad (II,46)$$

Then, with respect to the closed loop transfer function W_{ATO} , it is possible to impose:

$$k'k_p = 2\xi_{ATO}\omega_{n,ATO} \quad (II,47)$$

$$k'k_i = \omega_{n,ATO}^2 \quad (II,48)$$

where $\omega_{n,ATO}$ and ζ_{ATO} are the natural pulsation and the damping coefficient of the ATO algorithm. By imposing a damping coefficient $\zeta_{ATO}=0.707$, it is possible to determine the natural pulsation $\omega_{n,ATO}$ and the proportional gain k_p as follows:

$$\omega_{n,ATO} = \sqrt{k'k_i} \quad (II,49)$$

$$k_p = \frac{2\zeta_{ATO}\omega_{n,ATO}}{k'} \quad (II,50)$$

II.5.3 Speed control loop tuning

The speed control loop block scheme is reported in Fig. II. 23.

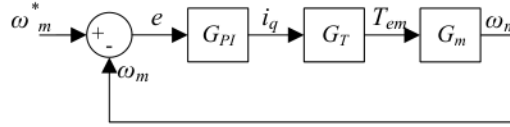


Fig. II. 23: Mechanical system control scheme.

The block scheme is composed of three cascaded transfer functions, G_{PI} , G_T , and G_m : in detail, G_T , and G_m are derived from equations (II,6) and (II,7), that allows for modelling the PMSM electric torque generation and mechanical phenomena, respectively. In the Laplace domain, G_T , and G_m are expressed as:

$$G_T = \frac{T_{em}}{i_q} = \frac{3}{2} p \psi_{PM} \quad (II,51)$$

$$G_m = \frac{\omega_m}{T_{em}} = \frac{1}{J_m s} \quad (II,52)$$

It must be underlined that, concerning (II,52) the friction F_m is assumed to be negligible in this application; concerning (II,51), it is assumed that only the q current produce an electromagnetic torque, since the d is constantly null. The open loop transfer function F_{ol} and the closed loop transfer function W_E are defined respectively as:

$$F_{ol,m} = G_{PI} \cdot G_T \cdot G_m = \left(k_p + \frac{k_p}{s} \right) \cdot \left(\frac{3p\psi_{PM}}{2J_m s} \right) \quad (II,53)$$

$$W_m = \frac{\omega_m}{\omega_m^*} = \frac{F_{ol,m}}{1 + F_{ol,m}} = \frac{\frac{3p\psi_{PM}}{2J_m} (k_p s + k_i)}{s^2 + \frac{3p\psi_{PM}}{2J_m} k_p s + \frac{3p\psi_{PM}}{2J_m} k_i} \quad (II,54)$$

Then, with respect to the closed loop transfer function W_{ATO} , it is possible to impose:

$$\frac{3p\psi_{PM}}{2J_m} k_p = 2\zeta_m \omega_{n,m} \quad (II,55)$$

$$\frac{3p\psi_{PM}}{2J_m} k_i = \omega_{n,m}^2 \quad (\text{II},56)$$

where $\omega_{n,m}$ and ζ_m are the natural pulsation and the damping coefficient of the mechanical control loop. By imposing a damping coefficient $\zeta_m=0.707$, and assuming that the natural pulsation $\omega_{n,m}$ it is possible to determine the natural pulsation $\omega_{n,ATO}$ and the proportional gain k_p as follows:

$$k_i = \frac{2J_m \omega_{n,m}^2}{3p\psi_{PM}} \quad (\text{II},57)$$

$$k_p = \frac{4J_m \zeta_m \omega_{n,m}}{3p\psi_{PM}} \quad (\text{II},58)$$

II.6 Field Oriented Control Experimental Validation

To prove the effectiveness of the discussed control, an experimental dynamic analysis is carried out. As a way of example, system dynamic performance is investigated adopting the PS-PWM strategy with a switching frequency $f_{sw}=10$ kHz. Particular attention is paid to the proposed RDC system. For this purpose, a comparison with an incremental encoder LTN Servotechnik, 1024 ppr, type G36 W is carried out. To perform a dynamic comparative analysis with an accurate speed sensor, an X4 encoding approach is adopted, and 4096 ppr is guaranteed. In Fig. II. 12 (a) and (b), the resolver excitation voltage and stator amplitude modulated voltages at rotor speed equal to 0 rpm 2000 rpm are reported, respectively. It can be seen that, although the excitation signal is made by two PWM signals, the obtained waveforms are sinusoidal. These results validate the effectiveness of the proposed resolver excitation circuit.

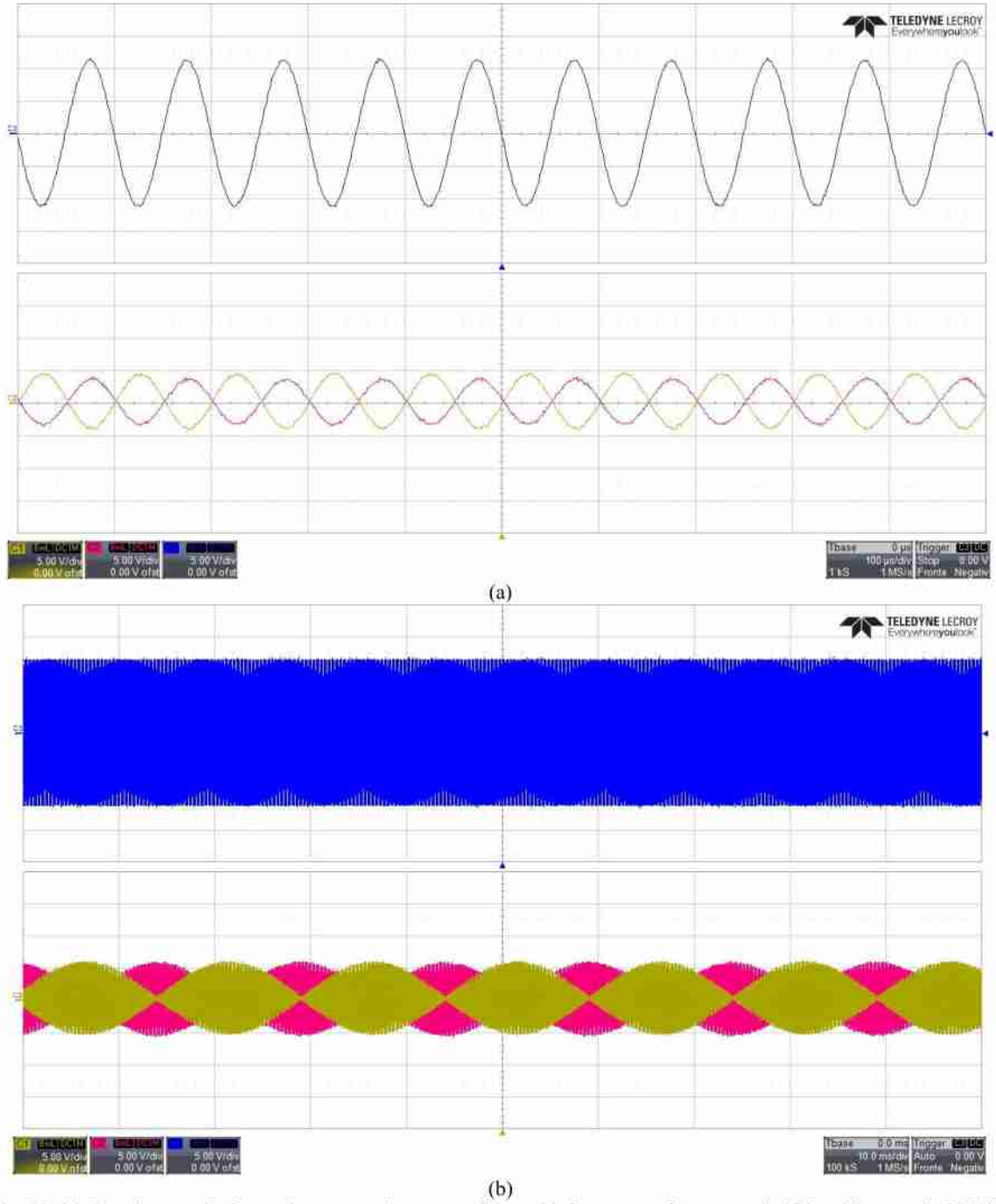


Fig. II. 24: Resolver excitation and output voltage waveforms: (a) 0 rpm speed test, x-axis 100 μ s/div, y-axis 5 V/div, 1MS/s; (b) 2000 rpm speed test, x-axis 10 ms/div, y-axis 5 V/div, 1MS/s.

The FOC effectiveness is tested by investigating the system step-response and disturbance immunity through a 0-3000 rpm acceleration and a 1.5 Nm load torque application and removal, reported in Fig. II. 25 and Fig. II. 26, respectively. Such quantities are acquired through the sbRIO 9651 controller and the sampling frequency coincides with the control sampling frequency, equal to 10 kHz. With respect to Fig. II. 25 (a), demodulated signals $v_{s,d}$ and $v_{c,d}$ are shown. It can be noted that they are characterized by a sinusoidal trend, whose frequency depends on the PMSM rotor angular speed ω_m and with a peak value a bit lower than 5 V. Indeed, the resolver excitation gain is set such that the signals $v_{s,d}$ and $v_{c,d}$ does not

reach 5 V, to avoid exceeding the ADC rated voltage. Such trends prove the effectiveness of the proposed demodulation strategy.

In Fig. II. 25 (b) and (c), the speed and currents trends during the 0-3000 acceleration at no-load working conditions are reported. It can be noted that the d -current is maintained equal to zero over the entire transient, while the q -current reach the saturation value of 10 A and gradually goes to zero when the speed reaches the set point. The PMSM reaches the desired speed after about 0.4 s with an overshoot of about 200 rpm. Moreover, the comparison between resolver-measured speed signal n_{res} and encoder-measured speed signals n_{enc} shows that the encoder-measured speed n_{enc} is significantly affected by noise if compared to the resolver-measured speed n_{res} , and it is characterized by steady-state error. Such a behaviour can be justified by considering the torsional vibrations generated by the hysteresis brake. Such trends prove both the effectiveness of the speed and current control and the superiority of the proposed RDC system.

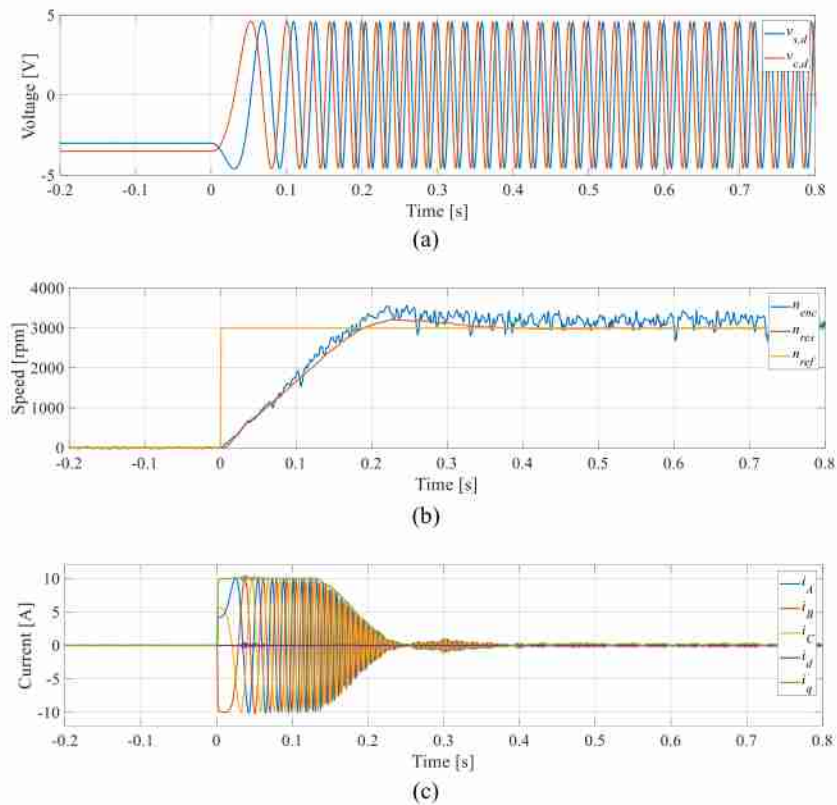


Fig. II. 25: CHB-fed PMSM drive dynamic behavior under a 0–3000 rpm acceleration, (a) comparison between resolver-measured and encoder-measured speed signals, (b) ABC and dq currents, (c) dq voltages, (d) demodulated resolver output signals.

In Fig. II. 26, the resolver- and encoder- measured speed trends during the 1.5 Nm load torque application and removal are shown. It can be noted that, in both cases, the control allows for regulating the speed maintaining the set point of 3000 rpm. Then, such trends confirm the control immunity to external disturbances.

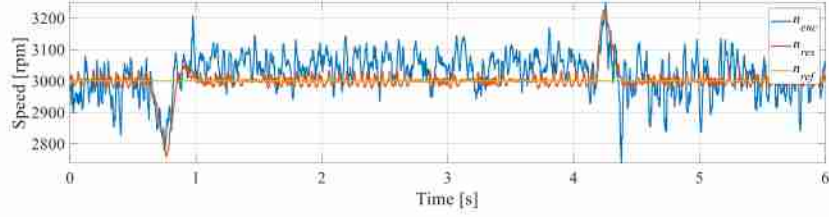


Fig. II. 26: CHB-fed PMSM drive dynamic behavior 1.5 Nm load torque application and removal, reference speed equal to 3000 rpm.

II.7 CHB-Fed IPMSM Drive Steady-State Working Condition Analysis

In this section, the CHB-fed PMSM drive performance analysis in steady-state working conditions is carried out. The main goal of this analysis is to evaluate the MC-PWM strategies impact on the current THD and IPMSM power losses. For this purpose, taking into account results collected in Chapter I regarding the voltage THD and CHB efficiency, only three MC-PWM strategies, i.e., SPD, SPS, and SCAMOD, are investigated. Such a choice is adopted due to the following considerations:

- Regarding the LS-PWM strategies, PD exhibits better performance, both in terms of voltage THD and converter efficiency, if compared to POD and APOD-PWM. Moreover, all LS-PWM strategies displace harmonics over the spectrum in the same way, according to the discussion presented in Section I.3 and with shown experimental results. For these reasons, the PD-PWM strategy is chosen as representative of the LS-PWM strategies.
- In terms of modulating signals, it was noted that S and SFO exhibit similar behaviour. In detail, S guarantees a lower voltage THD, while SFO guarantees an extended linear working range. For these reasons, S is chosen as the representative modulating signal.

The switching frequency is investigated in the range $f_{sw} \in \{4, 8, 12, 16 \text{ kHz}\}$. Electric drive performance are investigated in 16 WPs, identified in the speed n and load torque T plane and summarized in Table II. 5.

Table II. 5: Adopted WPs for CHB-fed PMSM drive steady-state performance analysis.

T [Nm]- n [rpm]	200	1000	2000	3000
1.8	WP4	WP3	WP2	WP1
1.35	WP8	WP7	WP6	WP5
0.9	WP12	WP11	WP10	WP9
0.45	WP16	WP15	WP14	WP13

All the experimental investigations are carried out according to the prescription reported in the international standards IEC 61800-9-1 [II,9] and IEC 61800-9-2 [II,10]. In detail, for every identified WP, measures are carried out only when IPMSM is at thermal equilibrium.

Since achieving IPMSM thermal equilibrium is a very time-consuming task, IPMSM current THD and power losses maps identification for the switching frequency in the range $f_{sw} \in \{8, 12, 16 \text{ kHz}\}$. is carried out by considering only nine WPs, according to standard prescriptions. In detail, the WPs 3-5-6-7-8-11-15 are excluded.

The accurate detection of IPMSM input quantities is performed through the measurement system described in Section II.3. The measurement system manufacturer declares a guaranteed accuracy of 1 % in the measured active power in the whole bandwidth. Since the harmonic power losses, which will be introduced and mathematically described in the following sections, present a small amplitude, it is necessary to perform some observations concerning the correlated accuracy. In detail, it is possible to assess that the determination of harmonic power is only a function of electrical quantities and, thus, the same accuracy can be used for the IPMSM harmonic power losses determination. The Magtrol HD-715-8NA hysteresis brake accuracies are 0.01% of reading for speed measurement and 1.3×10^{-3} N m for torque measurement (0.02% of range). The accuracy data are satisfactory for motor power losses determination and for comparative purposes [II,39].

Particular attention is paid to the determination of fundamental quantities. Consequently, it is crucial to account for the spectral leakage phenomenon and establish the observation window to achieve an optimal frequency resolution. The observation window and relative sampling frequency are set equal to 1 s and 1 MHz, respectively, obtaining a frequency resolution of 1 Hz and synchronous sampling that results in acquiring an integer number of current and voltage waveform periods. Therefore, an optimal window spectrum has been selected to take into account the leakage spectrum phenomenon and accurately evaluate the fundamental quantity.

For comparison purposes, a commercial 3P-2L-VSI DPS 30 A prototype, whose picture and main data are shown in Fig. II. 27 and Table II. 6, respectively, is adopted to feed the IPMSM. Tests on the 2L-VSI-fed IPMSM drive are carried out by setting the 2L-VSI DC-link voltage $V_{dc,2L}$ equal to twice the CHB total DC link voltage U_{dc} , defined according to equation (I,20). In this way, for fixed fundamental harmonic voltage amplitude, both converter topologies work with the same amplitude modulation index M , defined for the CHB and 2L-VSI topologies according to the equation (I,19) and (II,59), respectively:

$$M_{2L} = \frac{U}{V_{dc,2L} / 2} \quad (\text{II,59})$$



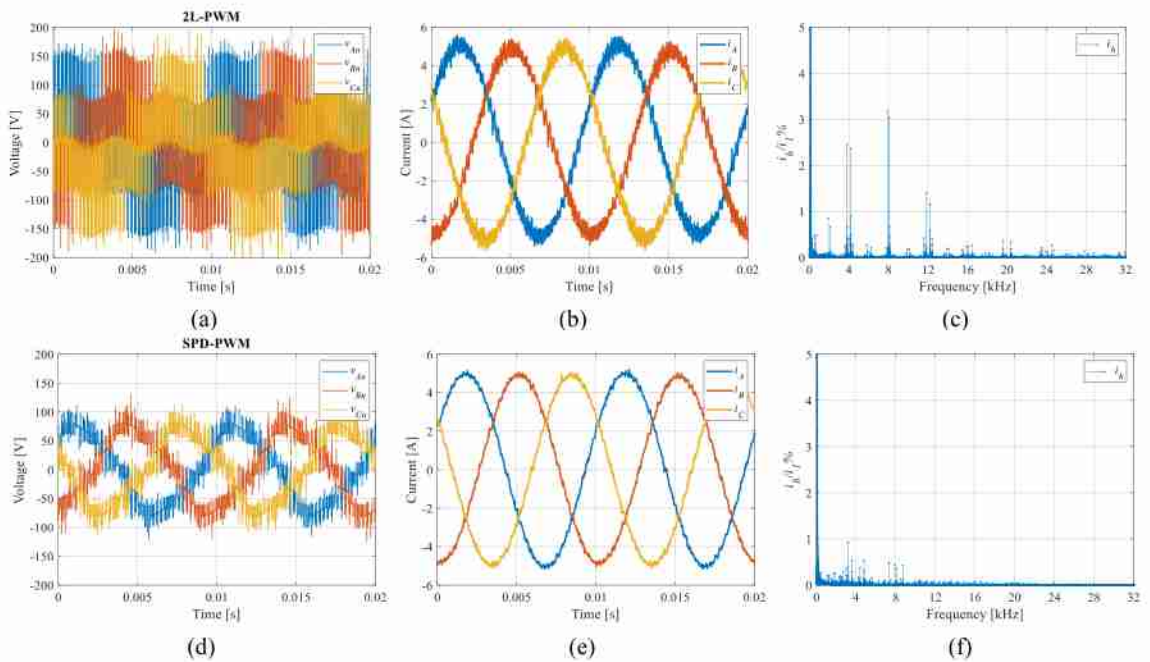
Fig. II. 27: Commercial 3P-2L-VSI DPS 30 A prototype.

Table II. 6: Main data of 3P-2L-VSI DPS 30 A prototype.

<i>Quantity</i>	<i>Symbol</i>	<i>Value</i>
Rated input voltage	V_{in}	240 V
DC-link voltage	V_{DC}	320 V
Minimum input voltage	$V_{in,min}$	70 V
Phase current peak	I_{peak}	30 A
Switching frequency	f_{sw}	2-20 kHz

II.7.1 Current Total Harmonic Distortion

As a way of example, Fig. II. 28 shows the comparison between phase voltages, phase currents, and current spectra obtained with traditional 2L-PWM (a-c), SPD-PWM (d-f), SPS-PWM (g-i), and SCAMOD (j-l), in WP2 (speed $n=2000$ rpm, load torque $T=1.8$ Nm), with the switching frequency $f_{sw}=4$ kHz.



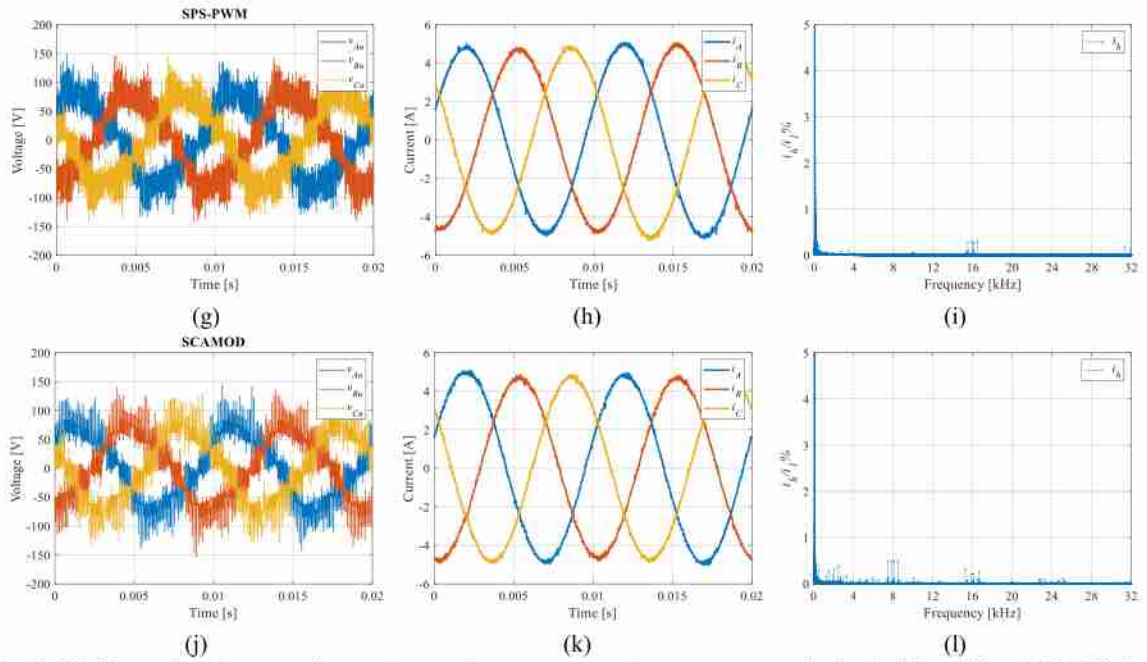


Fig. II. 28: Comparison between phase voltages, phase currents, and current spectra obtained with traditional 2L-PWM (a-c), SPD-PWM (d-f), SPS-PWM (g-i), and SCAMOD (j-l), speed $n=2000$ rpm, load torque $T=1.8$ Nm, and $f_{sw}=4$ kHz.

Concerning the 2L-PWM strategy, the main current harmonic groups are centered around the switching frequency and its multiples; the main harmonic groups, at 4 kHz and 8 kHz, exhibit an amplitude equal to 2.5 and 3%, respectively. SPD-PWM exhibits similar behaviour in terms of harmonic displacement over the spectrum. However, the amplitude of the current harmonics is much lower, if compared to the 2L-PWM strategy, being always lower than 1%. Such a reduced current harmonic content is evident also in the time-domain current trends, that exhibit a lower ripple. Looking at the SPS-PWM strategy, it guarantees the lowest current harmonic distortion, shifting the harmonics in the high-frequency range. SCAMOD strategy main groups of harmonics are centered at 8 kHz and multiples. However, low-frequency current harmonics, centered at a frequency lower than 4 kHz, appear, producing torque ripple with consequent noise and vibrations.

Nevertheless, comparing CHB and 2L-VSI performance, Fig. II. 28 shows that 5L-CHB allows for a drastic current harmonic content reduction, independent of the adopted MC-PWM strategy.

In Fig. II. 29, the current THD maps over the adopted working range, obtained with traditional 2L-PWM, SPD-PWM, SPS-PWM, and SCAMOD (j-l), with switching frequency equal to 4 kHz (a-d), 8 kHz (e-h), 12 kHz (i-l), and 16 kHz (m-p), are reported.

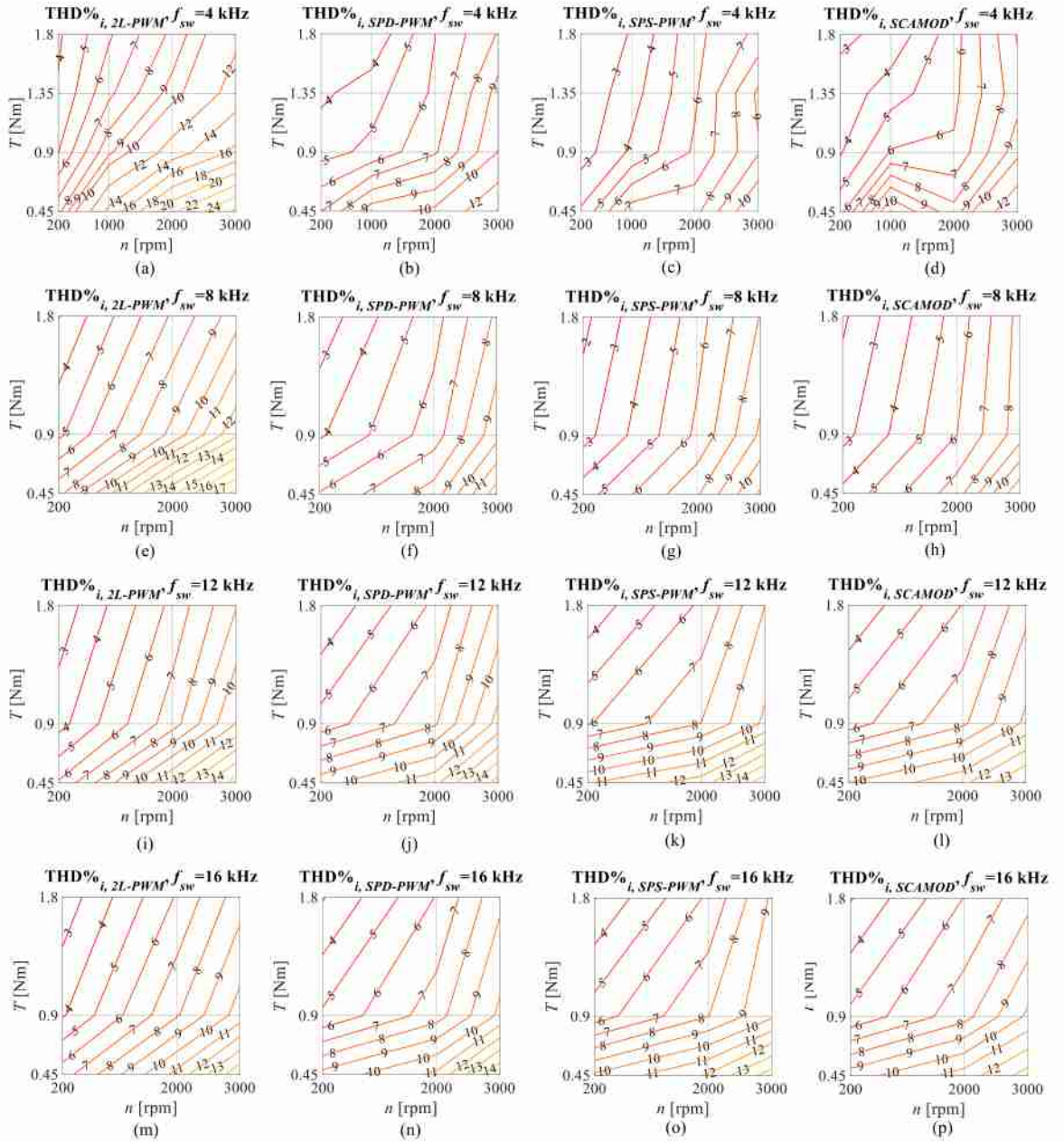


Fig. II. 29: Comparison between current THD maps over the adopted working range obtained with traditional 2L-PWM, SPD-PWM, SPS-PWM, and SCAMOD (j-l), with switching frequency equal to 4 kHz(a-d), 8kHz (e-h), 12 kHz (i-l), and 16 kHz (m-p).

Generally, for fixed switching frequency, inverter topology, and PWM strategy, the lowest current THD value is recorded in WP4, i.e., high-torque low-speed working conditions, and a current THD increment is noted when the speed n increases and when the load torque T decreases. Concerning the dependency on the speed n , such a result can be justified by considering the frequency modulation index m_f , defined as follows:

$$m_f = \frac{f_{sw}}{f_l} \quad (\text{II.60})$$

Where f_l is the fundamental voltage and current frequency, which is correlated to the IPMSM speed n and is equal to 10, 50, 100, and 150 Hz, when the speed n is 200, 1000, 2000, and

3000 rpm, respectively. Indeed, the higher the speed, the lower the frequency modulation index m_f . As a way of example, if $f_{sw}=4$ kHz, m_f varies from $4000/10=400$ to $4000/150=26.67$. Such a parameter indicates the number of control actions over the fundamental frequency. In other words, the higher the speed, the lower the number of voltage pulses which impose the current trend. Moreover, when $n=3000$ rpm, m_f is not an integer number and the voltage waveform symmetries are lost, determining degradation in the voltage and current spectrum.

Regarding the dependency on the load torque T , the higher the load torque, the higher the fundamental current amplitude, which allows for producing the required electromagnetic torque according to (II,6). Then, taking into account the THD, defined as in (I,40), the higher the current fundamental frequency, the lower the THD.

A cross-comparison of the current THD over the switching frequency, for every inverter topology, PWM strategy, and in the 9 main WPs is reported in Fig. II. 30.

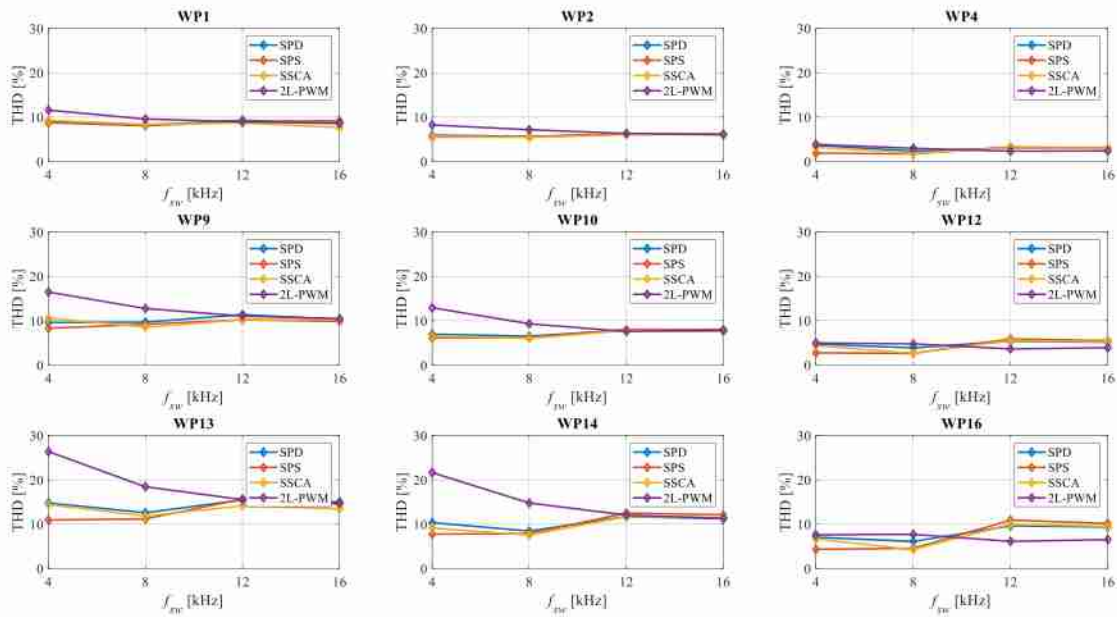


Fig. II. 30: cross-comparison of the current THD over the switching frequency, for every considered inverter topology, PWM strategy, switching frequency, and in the main WPs.

It can be noted that 2L-VSI exhibits a decreasing trend with the switching frequency in every WP, whereas the CHB shows a decreasing current THD trend only when the switching frequency is lower than 12 kHz; then, it starts increasing again, independently of the selected MC-PWM strategy. However, CHB confirms its superiority in terms of harmonic behaviour, if compared to the traditional 2L-VSI, since the CHB guarantees a lower current THD almost in every considered WP, if compared to the 2L-VSI, independently of the adopted MC.PWM strategy. The main difference between 2L-VSi and CHB inverters can be observed in high-

speed and low-torque working conditions, for example in WP13 ($n=3000$ rpm, $T=0.45$ Nm), where the maximum THD value is 26% and 10% for 2LVSI and SPS-PWM driven CHB inverter, respectively. Differences in terms of steady-state performance are less relevant when the switching frequency is increased, and when it is higher than 12 kHz, 2L-VSI and CHB inverter performance are comparable.

Focusing now on the CHB inverter and comparing the adopted MC-PWM strategies, it emerges that differences in terms of current THD are not that evident: PS-PWM guarantees the lowest THD, especially in high-speed low torque conditions with very low switching frequency. Such a behavior is justified by the PS-PWM ability to shift harmonics in the high-frequency range, allowing easy current filtering due to the stator windings. As a way of example, in WP13, PS-PWM guarantees a current THD of about 10%, while PD and SCAMOD exhibit a current THD of about 15%.

Results reported so far allow for stating that the CHB inverter guarantees a drastic reduction of the current THD, if compared to traditional 2L-VSI, independently of the considered WP and adopted MC-PWM strategy. In detail, the lower the switching frequency, the higher the gap between the CHB and 2L-VSI performance. Regarding the MC-PWM strategies, PS-PWM exhibits the best harmonic behaviour, guaranteeing, for fixed switching frequency, the shift of current harmonics in the high-frequency range and, consequently the lowest THD. Looking at the switching frequency impact on the current harmonic distortion, results show that increasing the switching frequency does not guarantee significant improvements in terms of current harmonic content. Furthermore, beyond a certain switching frequency value, an increase in current THD is observed. Under these conditions, the behavior of the traditional VSI converter and the CHB become comparable, and the use of CHB becomes disadvantageous.

II.7.2 Harmonic Power Losses Segregation Mathematical Formulation

The key energy indicators in a motor system are the efficiency η and the power losses ΔP , defined respectively as:

$$\eta = \frac{P_m}{P_{el}} 100 \quad (\text{II},61)$$

$$\Delta P = P_{el} - P_m \quad (\text{II},62)$$

where P_m is the output mechanical power, and P_{el} is the input electrical active power. When a digital measurement system is adopted, the input electrical active power of one phase $P_{el,j}$ is evaluated by employing sampled voltage and current signals, as follows:

$$P_{el,j} = \frac{1}{N_s} \sum_{k=0}^{N_s-1} v_j(k) i_j(k) \quad (\text{II},63)$$

where N_s is the total number of acquired samples, $v_j(k)$ and $i_j(k)$ are the instantaneous voltage and current samples related to the phase $j \in \{A, B, C\}$. Equivalently, by applying the Discrete Fourier Transform (DFT) algorithm to the sampled voltage and current signals, the input electrical active power P_{el} can be evaluated as follows:

$$P_{el,j} = P_{DC,j} + \sum_{h=1}^{h_{\max}} V_{h,j} I_{h,j} \cos(\varphi_{h,j}) \quad (\text{II},64)$$

where P_{DC} is the DC power component, $V_{h,j}$ and $I_{h,j}$ are the voltage and current RMS values related to the h^{th} harmonic and j^{th} phase, $\varphi_{h,j}$ is the respective phase displacement, and $h_{\max}$ is the maximum representable harmonic, which depends on the Nyquist frequency. It must be underlined that the active power is generated only by isofrequential voltage and current harmonics and this approach includes all harmonic, sub-harmonic, and inter-harmonic components. Thus, the total input electrical active power $P_{el,tot}$ of a three-phase electrical motor can be calculated as:

$$P_{el,tot} = P_{el,A} + P_{el,B} + P_{el,C} \quad (\text{II},65)$$

Moreover, according to equation (II,64), supposing that the DC power component is null, the total active power $P_{el,tot}$ can be defined as the sum of the fundamental power P_1 , calculated by considering the voltages and currents fundamental components ($h=1$), and the harmonic power P_h , calculated by considering the sum of the remaining h^{th} voltages and currents harmonic components ($h>1$):

$$P_{el,tot} = P_1 + P_h \quad (\text{II},66)$$

By assuming that the high-frequency harmonics have negligible impact on the torque production, the total power losses ΔP_{tot} , the fundamental power losses ΔP_1 , and the harmonic power losses ΔP_h in the motor can be evaluated respectively as:

$$\Delta P_{tot} = P_{el,tot} - P_m \quad (\text{II},67)$$

$$\Delta P_1 = P_1 - P_m \quad (\text{II},68)$$

$$\Delta P_h = \Delta P_{tot} - \Delta P_1 \quad (\text{II},69)$$

Replacing equations (II,67) and (II,68) in (II,69), the harmonic power losses ΔP_h can be evaluated as follows:

$$\Delta P_h = P_{el,tot} - P_1 \quad (\text{II},70)$$

It must be underlined that comparing (II,70) and (II,66), it follows that the harmonic power P_h coincides with the harmonic power losses ΔP_h . Furthermore, the fundamental and harmonic power losses ΔP_l and ΔP_h can be expressed in percentage value as follows:

$$\Delta P_l \% = \frac{\Delta P_l}{\Delta P_{tot}} 100 \quad (\text{II,71})$$

$$\Delta P_h \% = \frac{\Delta P_h}{\Delta P_{tot}} 100 \quad (\text{II,72})$$

Finally, with the use of the DFT methodology, it is useful to define the cumulative active power P_{cum} , which allows for investigating the electrical active power distribution over the spectrum. Indeed, taking into account the equation (II,64), the cumulative active power P_{cum} in percent of the total electric power P_{el} , is defined as:

$$P_{cum}(\nu) = \frac{100}{P_{el,tot}} \sum_{j=A}^C \left\{ P_{DC,j} + \sum_{h=1}^{\nu} V_{h,j} I_{h,j} \cos(\varphi_{h,j}) \right\} \quad (\text{II,73})$$

where $1 \leq \nu \leq h_{max}$. The adopted power analysis tools allow for carrying out an extended and detailed analysis of CHB impact on IPMSM losses and efficiency.

II.7.3 Power Losses in Frequency Domain: Experimental Results

By way of example, Fig. II. 31 shows the percentage cumulative active power for the IPMSM at WP 2 (speed $n=2000$ rpm, load torque $T=1.8$ Nm), obtained with traditional 2L-PWM (a), SPD-PWM (b), SPS-PWM (c), and SCAMOD (d), with the switching frequency $f_{sw}=4$ kHz. Comparing the cumulative active power trends in Fig. II. 31 with current spectra in Fig. II. 28, it becomes apparent that the discrete changes in input cumulative power align precisely with the harmonic groups of the relative switching frequencies. As expected, the input active power associated with the harmonic quantity cannot be neglected in the case of conventional SPWM modulated 2L-VSI, amounting to about 3%. On the contrary, in the case of CHB inverter, over 99.5% of the IPMSM input active power is centered around the fundamental frequency. Consequently, the contribution of harmonic active power is effectively constrained and it can also be detected and evaluated. In order to provide a general overview of IPMSM performance, the IPMSM efficiency η is reported in Table II. 7. For the sake of repeatability, the measurements of power losses and efficiency in the IPMSM have been conducted multiple times, revealing no significant differences. It is possible to observe a significant IPMSM efficiency improvement with the use of CHB inverter, if compared to the 2L-VSI, in almost all considered WPs. In detail, the IPMSM efficiency improvement varies in the range of 2.5-7% and the margin of efficiency improvement increases as the load

torque decreases for fixed mechanical speed. Comparing the efficiency obtained with MC-PWM strategies, it can be noted that PS-PWM guarantees the maximum efficiency almost in every WP.

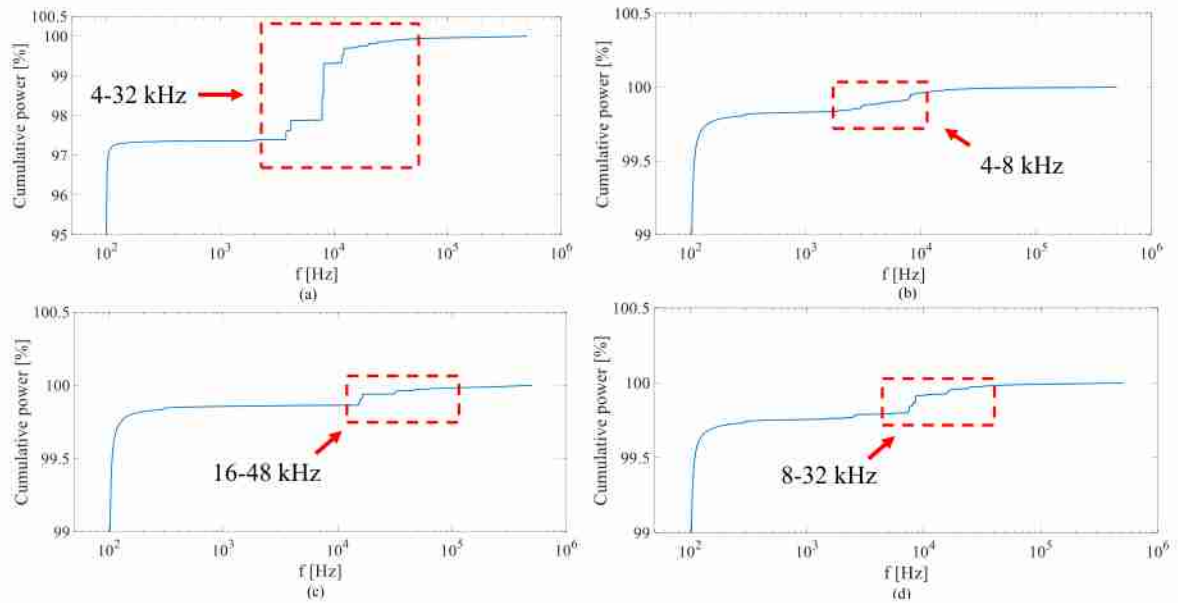


Fig. II. 31: Comparison between IPMSM input cumulative active power obtained with traditional 2L-PWM (a), SPD-PWM (b), SPS-PWM (c), and SCAMOD (d), speed $n=2000$ rpm, load torque $T=1.8$ Nm, and $f_{sw}=4$ kHz.

Table II. 7: IPMSM efficiency detected for every inverter topology, PWM strategy and working condition, $f_{sw} = 4$ kHz.

WPs	Efficiency η [%]			
	2L-PWM	SPD-PWM	SPS-PWM	SCAMOD
1	76.8	79.1	79.4	78.9
2	71.1	73.7	74.1	73.7
3	58.7	61.1	61.3	60.9
4	24.6	25.6	25.7	25.4
5	79.1	81.8	81.9	81.7
6	74.5	77.9	78.1	78.1
7	64.1	67.8	67.9	67.6
8	30.1	32.9	33.2	32.9
9	79.1	82.7	83.1	83.3
10	75.8	80.3	80.7	80.9
11	68.4	73.4	73.4	72.8
12	39.3	42.4	42.8	42.3
13	73.6	78.8	78.9	79.4
14	71.8	78.2	78.4	79
15	68	75	74.2	73.8
16	49	53.6	54	53.4

Fig. II. 32 shows the IPMSM total power losses (a-d), percentage fundamental power losses (e-h), and percentage harmonic power losses (i-l) maps over the adopted working range, obtained with traditional 2L-PWM, SPD-PWM, SPS-PWM, and SCAMOD, with switching frequency equal to 4 kHz. Looking at the total power losses shown in Fig. II. 32 (a-d), it can be noted that the CHB inverter guarantees lower total power losses over the entire working range, if compared to the traditional 2L-VSI, independently of the adopted MC-PWM strategy. Moreover, among MC-PW strategies, PS-PWM guarantees the lowest total power

losses almost in every considered WP. This result was expected since the IPMSM efficiency has been already discussed. However, looking at Fig. II. 32 (e-h) and (e-h), another interesting result is shown, i.e., the CHB allows for segregating a huge amount of power losses at the fundamental frequency, if compared to the 2L-VSI. In detail, results show that fundamental power losses related to the 2L-VSI reach comparable values with the CHB fundamental power losses only at high-torque low-speed working conditions. As a way of example, at WP13 ($n=3000$, $T=0.45$ Nm), the harmonic power losses are 73.55% and 97.62%, for 2L-VSI and PS-PWM driven CHB inverter, respectively. In other words, percentage harmonic power losses related to CHB are extremely low (always lower than 10%) due to the reduced voltages and currents harmonic content.

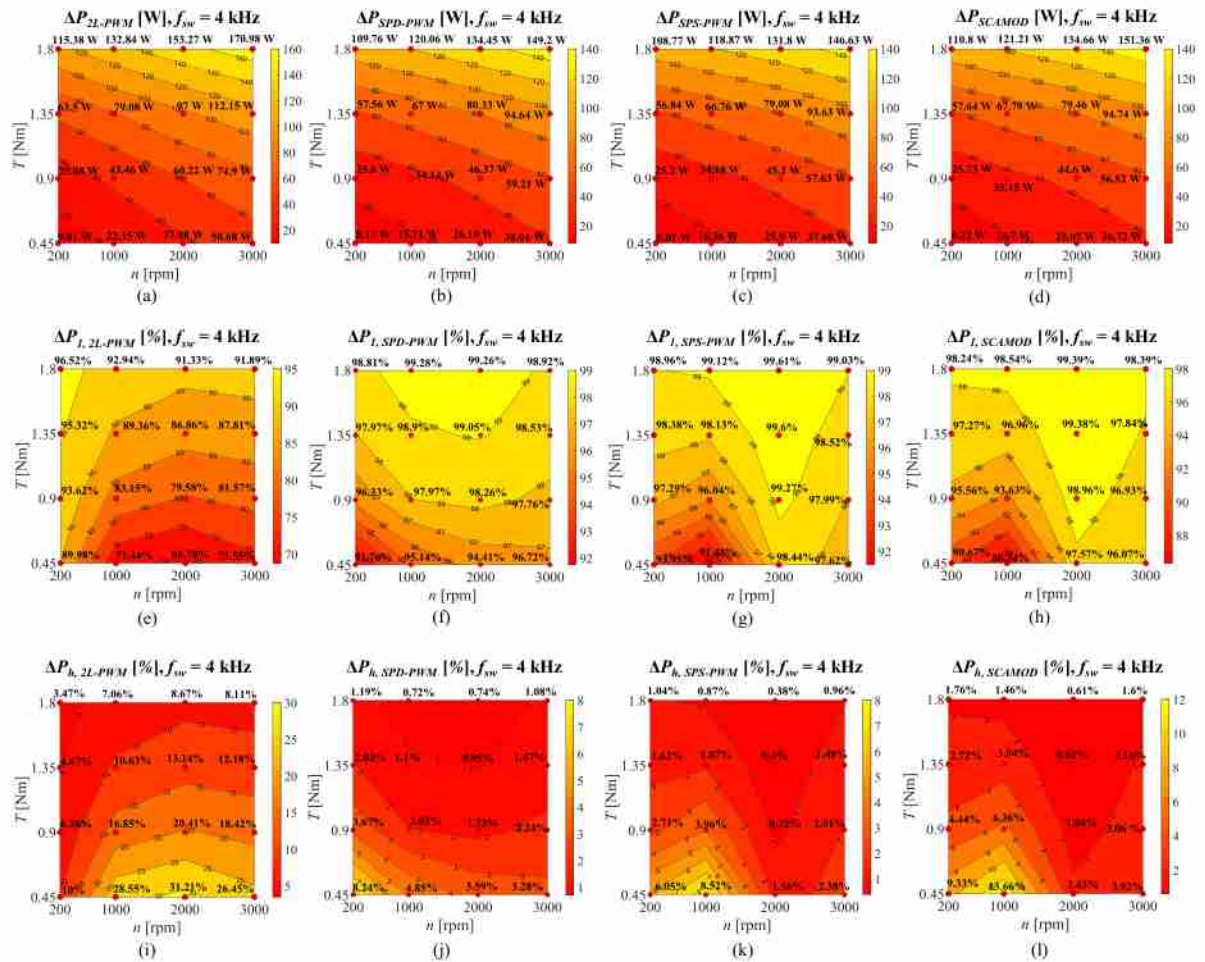


Fig. II. 32: Comparison between IPMSM total power losses (a-d), percentage fundamental power losses (e-h), and percentage harmonic power losses maps (i-l) over the adopted working range, obtained with traditional 2L-PWM, SPD-PWM, SPS-PWM, and SCAMOD, with switching frequency equal to 4 kHz.

Then, it can be stated that CHB inverter not only guarantees a higher IPMSM efficiency but also allows for segregating most of the power losses at the fundamental frequency independently of the considered WP and adopted MC-PWM strategy. This is a very interesting result, since CHB allows for effective power losses control and minimization, for

example through a loss-minimization algorithm. By comparing now MC-PWM strategies behaviors, PS-PWM guarantees the lowest harmonic power losses almost in every WP, if compared to other MC-PWM strategies. Differences among MC-PWM strategies in terms of harmonic power become more evident as the load torque decreases. Such results are related to the ability of the PS-PWM strategy to shift harmonics in the high-frequency range, allowing easy filtration.

Finally, the switching frequency impact on IPMSM power losses is investigated. In detail, since the IPMSM power losses detected with 2L-VSI are higher for all considered switching frequency values, only the IPMSM power losses detected with CHB inverter are analyzed. The IPMSM total power losses, percentage fundamental power losses, and percentage harmonic power losses detected for each WP and considered switching frequency value are reported in Fig. II. 33. In detail, an overall IPMSM total power reduction can be observed in each WP considered as the switching frequency increase. This reduction is more appreciable at high-load IPMSM working conditions.

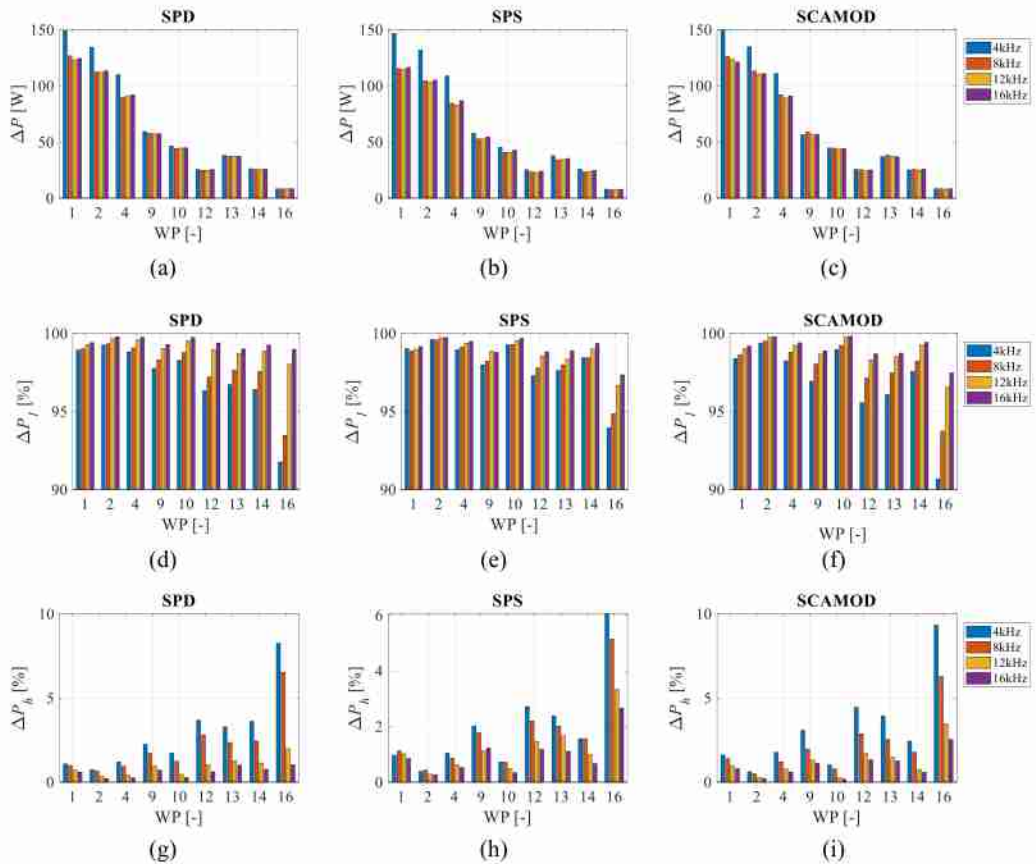


Fig. II. 33: Comparison between IPMSM total power losses (a-c), percentage fundamental power losses (d-f), and percentage harmonic power losses maps (g-i) over a subset of the adopted working range, obtained with, SPD-PWM, SPS-PWM, and SCAMOD, with switching frequency that varies over the range to 4-16 kHz.

This behaviour can be attributed both to a reduction of fundamental and harmonic losses but also to a different power losses distribution. In fact, it is possible to observe an increment of

IPMSM percentage fundamental power losses values as the switching frequency increases. In the case of f_{sw} equal to 16 kHz, the percentage fundamental power losses values vary from a minimum of 97% to a maximum of 99.8% in every considered WPs and for every MC-PWM strategy. In a complementary way, it is possible to observe a reduction of IPMSM percentage harmonic power losses values as the switching frequency increases until values lower than 3% at the maximum switching frequency in all considered WPs and for all MC-PWM strategies. The percentage variations described are more significant at IPMSM low-load operations, where IPMSM harmonic power losses present non-negligible amplitude. Moreover, among all considered MC-PWM strategies, the power losses variations are more significant for the PD modulation scheme.

The experimental analysis carried out on the IPMSM drive fed by CHBMI shows that the vast majority of IPMSM power losses are generated by the fundamental electrical quantities. Furthermore, the increase in switching frequency value generates an overall reduction of percentage harmonic power losses values, but it is necessary to consider that the increase in switching frequency values increases CHB power losses. However, it is necessary to underline that in an electric drive, most of the losses are concentrated on the motor. Since the typical IPMSM control algorithms act on fundamental quantities, only the fundamental power losses are controllable and can be easily reduced. Therefore, the analysis carried out allows to state significant margins for an overall performance improvement of IPMSM drives fed by CHB inverter in terms of power losses compared to the conventional IPMSM drives fed with 2L-VSIs. From an energy-saving point of view, the study conducted shows the use of MIs also in low-voltage drive applications can provide a significant power losses reduction that in long-term operation can justify the additional cost required with respect to conventional 2L-VSI by ensuring optimal power quality, fault-tolerant capability and lower electromagnetic interference.

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Chapter III Finite Control Set Model Predictive Control for CHB-fed IPMSM Drives: Design, Implementation, and Experimental Analysis

III.1 Introduction

In order to maximize the electric drive performance in terms of power losses and control flexibility, the scientific literature efforts focus on new control software solutions such as the MPC. According to [III,1]-[III,2], the scientific community started investigating MPC potentiality in the field of power electronics and drives in the 1980s. However, the control complexity coupled with the short time constants that are characteristic of power electronic systems discouraged the spread of this control strategy. Indeed, as will be discussed more in detail in the following sections, the optimal control action is found by carrying out a number of future system state predictions that depend on the number of available inverter VVs and on the adopted prediction horizon, and comparing the related cost functions in order to find its minimum. In detail, the MPC computational cost grows exponentially with the number of available VVs and on the prediction horizon length. In the last ten years, the spread of high-computational power microprocessors and FPGA controllers has led to the diffusion of MPC both in scientific research and in industrial applications. However, solving online the optimal control problem when MIs are adopted is still a challenging task, due to the high number of available VVs.

Moreover, when the CHB inverter is adopted, VVs and GCSs redundancies entail a further increase in the control complexity. Generally, the main control goals related to CHB-based drives deal with the current reference tracking, converter switching loss minimization, CMV minimization, and CHB SMs power balancing [III,3]-[III,5]. Concerning the SMs power

balancing, this represents a critical control goal, since it affects both the converter, in terms of efficiency and reliability, and the DC sources.

Regarding computational cost minimization, several strategies have been proposed in the literature to reduce the MPC computational complexity for CHB-fed systems. In [III,6], a Cell-by-Cell-Based (CBCB) FCS-MPC for a Cascaded H-Bridge Rectifier (CHBR) is proposed. In detail, per each HB module, the optimal control problem is independently formulated and solved. In [III,7], a hierarchical FCS-MPC is proposed for a grid-connected single-phase CHB inverter. In detail, the candidate GCSs set is selected over a subregion of a 2-D control plane. The control plane allows for the candidate switching state set preselection and additional cost function terms can be deleted. In [III,8], an FCS-MPC for a CHB rectifier with available VV set online variation is formulated. The VVs set is defined depending on the system working conditions (i.e., transients or stationary conditions, faults conditions, and asymmetric loads). In [III,9], the FCS-MPC computational growth reduction from exponential form to polynomial form is addressed by the authors. In detail, the optimal control problem is split into two suboptimization problems, which deal with the current control and the optimal GCSs set selection, respectively.

Regarding the CHB SMs power balancing, bibliographical research shows that this task is not accurately considered and addressed for power drive applications. Aguilera *et al.* propose in [III,10] an FCS-MPC for CHB in photovoltaic applications under interphase unbalanced power generation conditions: the goal is fulfilled by enforcing the CHB to work with a suitable CMV component. It must be underlined that no attention is paid to SMs power unbalance, thus, the same authors propose a PS-PWM-based CCS-MPC for the same application in [III,11]: interphase power unbalance is faced as in [III,10], while the SMs power unbalance is faced by introducing a PS-PWM modulator; in detail, custom duty cycles per each SMs are defined and introduced into the cost function. In both cases, MPC is formulated in the *abc* frame, to directly take into account the CMV. In [III,12], a hierarchical FCS-MPC scheme is proposed where the multi-objective FCS-MPC, which is usually formulated by a unique multi-term cost function, is split into several cascaded FCS-MPCs with one-term cost functions, one of which deals with the SMs power balancing. It must be underlined that hierarchical MPC does not guarantee a computational burden reduction if compared to the traditional FCS-MPC. In [III,13], a modified MPC for a CHB-based BESS is proposed: in detail, the cost function consists of only one term, and a state selector algorithm is introduced to mitigate the unequal power drawn from battery cells. The proposed strategy is validated through Hardware in the Loop (HIL) simulations, moreover,

the SMs power inequality is mitigated but not eliminated. In [III,14], a successive search-based FCS-MPC algorithm is proposed for a CHB-based BESS. The algorithm allows for reducing the control computational burden by adjusting the search direction to find the optimal VV. Although this algorithm is proposed for a BESS application, no attention is paid to the DC-side quantities. In [III,15], a Model Predictive Sliding Control (MPSC) for grid-connected CHB is proposed: control goals (i.e., current and DC link voltages reference tracking) are synthesized into a single cost function to replace the N -PI-based DC link voltage control. By looking at the scientific literature, it can be noted that, when MPC is employed, not always appropriate attention is paid to the SMs power balancing goal. Moreover, the most common approaches to face this problem deal with the adoption of a PS-PWM-based CCS-MPC, which guarantees the SMs power balancing thanks to the modulator stage, or, when the FCS-MPC is adopted, by introducing into the cost function one or more quadratic custom terms, which try to equalize the SMs power.

In this chapter, issues related to MPC implementation for CHB-fed IPMSM drives are faced. In detail, two algorithms named Voltage Vector Based (V^2B) and Split Space Vector-Based (S^2VB)-MPC are proposed: the former strategy is designed in order to fulfill the following goals: computational burden minimization, CMVs minimization, GCS transitions minimization, and phase voltages dv/dt minimization; the latter represents an evolution of the V^2B -MPC. It is properly modified to emulate the PS-PWM switching pattern and guarantee CHB SMs power balancing in every working condition without any modulation stage or dedicated terms into the cost function.

III.2 Model Predictive Control: Classification, Advantages, and Control Formulation

Model Predictive Control is a control strategy that elaborates the control action by solving an optimal control problem, that is formulated based on the controlled system internal dynamic model and on a cost function. The system internal dynamic model is employed in order to carry out future system state predictions over a prediction horizon, using the current system state as the initial state for predictions. The cost function allows for synthesizing the control objectives; in detail, in order to find the optimal control action, the cost function must be minimized subject to the evolution of the internal dynamic model and system constraints. The solution to the optimization problem yields an optimal sequence of manipulated variables over the prediction horizon. Only the first element of such a sequence is applied to the controlled system the remaining elements are discarded. Such an approach is named receding horizon policy.

MPC represents an interesting solution in the field of power electronics and drives control since it allows for overcoming limits of traditional control strategies, such as the FOC, which are briefly resumed below. According to the discussion on the FOC presented in Section II.2, through the decoupling block and the cascaded control theory, the control of power electronics and drive systems, which is generally a Multi Input Multi Output (MIMO) control problem, is simplified in two independent control channels, each one composed of two cascaded Single Input Single Output (SISO) control loops. However, during transients and faults, SISO loops interact, limiting the system bandwidth and robustness. Furthermore, although power electronic converters are inherently nonlinear systems, the adoption of a modulation stage in the control loop allows the masking of system nonlinearities through the use of averaging, i.e., the PWM stage is used to translate the averaged reference quantities into switching signals. Such simplifications allow for the adoption of linear controllers such as PI controllers. However, the adoption of a modulation stage introduces some delays in the control action application, limiting the system bandwidth.

On the contrary, MPC is formulated by adopting the internal dynamic model of the controlled system. Such a model incorporates the power converter model, allowing for taking into account the power electronics switching behaviour. Moreover, the adoption of the internal dynamic model allows for formulating the control problem as a MIMO problem, overcoming the previously discussed FOC limits. Finally, the adoption of a multi-term weighted cost function allows for fulfilling several conflicting control goals.

According to [III,1] MPC control schemes for power electronics are classified into indirect and direct, depending on whether the modulator is adopted or not in the current control loop, respectively. In detail, indirect MPC generates modulating signals to compare with carriers signals. Therefore, the power electronics converter model is not considered in the system dynamic model and the solution to the control problem is the ideal voltage vector reference, i.e., a real-valued vector. On the contrary, direct MPC, known in the literature as Finite Control Set (FCS) MPC, incorporates the power converter model, allowing for directly manipulating the converter GCSs. Then, the solution to the control problem is an integer-valued vector.

In this work, only the FCS-MPC is considered, due to the previously mentioned advantages related to incorporating the power converter model in the controlled system dynamic model. However, the main drawback of FCS-MPC is its computational cost.

For control formulation purposes, the controlled system continuous-time state-space mathematical mode is adopted. Generally, for power electronics and drives applications, the state-space representation is linear, then it can be written in the following matrix form:

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{F}\mathbf{x}(t) + \mathbf{G}\mathbf{u}(t) \quad (\text{III},1)$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) \quad (\text{III},2)$$

Where $\mathbf{x}$ is the state vector, $\mathbf{u}$ is the input vector, $\mathbf{y}$ is the output vector, and $\mathbf{F}$, $\mathbf{G}$, and $\mathbf{C}$ are the system matrix, the input matrix, and the output matrix, respectively. The internal dynamic model must be discretized for digital implementation. Commonly, the Forward Euler approximation is adopted for discretization purposes, due to its reduced computational cost. It follows:

$$\mathbf{x}(k+1) = \mathbf{A}\mathbf{x}(k) + \mathbf{B}\mathbf{u}(k) \quad (\text{III},3)$$

$$\mathbf{y}(k) = \mathbf{C}\mathbf{x}(k) \quad (\text{III},4)$$

where matrices $\mathbf{A}$ and $\mathbf{B}$ are computed as:

$$\mathbf{A} = \mathbf{I} + \mathbf{F}T_s \quad (\text{III},5)$$

$$\mathbf{B} = \mathbf{G}T_s \quad (\text{III},6)$$

The output matrix $\mathbf{C}$ remains the same when deriving the discrete-time system representation.

Constraints related to the inputs, states, and outputs are usually present, making the system non-linear.

$$\mathbf{u}(k) \in \mathcal{U} \subseteq \mathbb{R}^{n_u} \quad (\text{III},7)$$

$$\mathbf{x}(k) \in \mathcal{X} \subseteq \mathbb{R}^{n_x} \quad (\text{III},8)$$

$$\mathbf{y}(k) \in \mathcal{Y} \subseteq \mathbb{R}^{n_y} \quad (\text{III},9)$$

Concerning the input vector $\mathbf{u}(k)$, when FCS-MPC is employed, the set $\mathcal{U}$ is constrained to a subset of integers. As a way of example, for the 5L-CHB inverter, the set available input voltages is $\mathcal{U} = \{-2V_{dc} -V_{dc} 0 V_{dc} 2V_{dc}\}^m$, where $m=3$ for a three-phase system. Constraints on the input vector are defined as *hard* constraints, i.e., they refer to the converter topology and they cannot be relaxed. Constraints related to the state are adopted by the user in order to avoid system overload. They are classified as *soft* constraints, i.e., they can be slightly violated, for example, in dynamic working conditions.

The control goals are synthesized into the cost function. In detail, for power electronics and drives applications, the cost function comprehends two terms and it is defined as follows:

$$J = \sum_{\ell=1}^{k+N_p+1} \left\| \mathbf{x}^*(\ell+1) - \mathbf{x}(\ell+1) \right\|_2^2 + \lambda_u \left\| \Delta \mathbf{u}(\ell) \right\|_1 \quad (\text{III},10)$$

where $\mathbf{x}^*$ is the reference state vector, N_p is the prediction horizon, $\Delta \mathbf{u}(\ell) = \mathbf{u}(\ell) - \mathbf{u}(\ell-1)$, λ_u is a weighting factor, and $\|\cdot\|_1$ and $\|\cdot\|_2$ are the 1-norm and 2-norm, respectively. In detail, the cost function is defined as the sum of the stage costs over the defined prediction horizon N_p ; each stage cost is composed of two terms, the former allows for tracking the state reference vector $\mathbf{x}^*$, and the latter allows for penalizing the converter switching effort. Priority among two control goals can be set by the user through the weighting factor λ_u . It must be underlined that the state error $\mathbf{x}^*(\ell+1) - \mathbf{x}(\ell+1)$ is penalized using the squared 2-norm, which is defined as the sums of the squares of the state error components. According to [III,16], FCS-MPC the vast majority of the literature on MPC with reference tracking is based on 1-norm, defined as the sum of the absolute values of the state error components. However, even if the 1-norm is computationally more efficient if compared to 2-norm, the 2-norm allows for both improving the closed-loop stability and simplifying the weighting factor tuning. It must be underlined that these considerations are not valid for the switching effort penalization term $\Delta \mathbf{u}$, for which is demonstrated that adopting 1- or 2- norm is equivalent in terms of system performance and stability, due to the quantized nature of the input vector in the FCS-MPC.

Minimizing the cost function subject to the system evolution over the adopted prediction horizon N_p and system constraints allows for finding the optimal input sequence over the prediction horizon $\mathbf{U}_{opt} = [\mathbf{u}_{opt}^T(k) \ \mathbf{u}_{opt}^T(k+1) \ \dots \ \mathbf{u}_{opt}^T(k+N_p-1)]$. Then, due to the consideration carried out above regarding to the quantized nature of the system input vector and related to the choice of norm into the cost function, the control problem is formulated as an Integer Quadratic Optimal control Problem (IQOCP), and it is formulated as follows:

$$\begin{aligned} \mathbf{U}_{opt} &= \arg \min J(\mathbf{x}(k), \mathbf{U}(k)) \\ \text{subject to } &\begin{cases} \mathbf{x}(\ell+1) = \mathbf{A}\mathbf{x}(\ell) + \mathbf{B}\mathbf{u}(\ell) \\ \mathbf{y}(\ell+1) = \mathbf{C}\mathbf{x}(\ell+1) \\ \mathbf{u}(\ell) \in \mathcal{U} \quad \forall \ell = k, \dots, k+N_p-1 \end{cases} \end{aligned} \quad (\text{III},11)$$

where $\mathbf{U} = [\mathbf{u}^T(k) \ \mathbf{u}^T(k+1) \ \dots \ \mathbf{u}^T(k+N_p-1)]$ is the sequence of available input vectors over the prediction horizon. In power electronics and drives applications, in order to find the solution to the IQOCP, the future system state and related cost function must be predicted a number

of time that depends on the number of available inverter VVs and on the prediction horizon length. It follows that, for fixed prediction horizon, the number of required predictions drastically grows as the number of inverter voltage levels increases.

Once optimal input vector $\mathbf{U}_{opt}$ is found, only the first element $\mathbf{u}_{opt}^T(k)$ is applied to the controlled system, the remaining elements are discarded and the optimal input vector $\mathbf{U}_{opt}$ is computed again at the next sampling instant. This policy, named receding horizon policy, allows for providing feedback to the control loop.

According to [III,2], due to the lack of a modulator stage and to the adopted control objectives, FCS-MPC does not guarantee fixed switching frequency and voltage waveform symmetries. As a consequence, the sampling frequency f_s does not coincide with the switching frequency f_{sw} and the theoretical maximum switching frequency $f_{sw,max}$ is equal to $f_s/2$. However, the effective switching frequency is much lower than its theoretical limit and depends on several aspects such as the specific MPC algorithm adopted, the system working conditions, and it can be actively limited by the switching effort penalization term into the cost function. Thus, according to [III,2], it is good practice to adopt the highest possible sampling frequency, depending on the controller computational power, to maximize the control granularity, i.e., the ration between the sampling frequency and the effective switching frequency.

III.3 CHB-Fed IPMSM Drive FCS-MPC Mathematical Formulation

In this section, the FCS-MPC is formulated for the CHB-fed IPMSM drive described and discussed over Chapter II. The electric drive control scheme is reported in Fig. III. 1. The speed control loop is synthetized as a PI controller, which generates the quadrature current reference i_q^* ; in this application, the direct current reference i_d^* is set to 0.

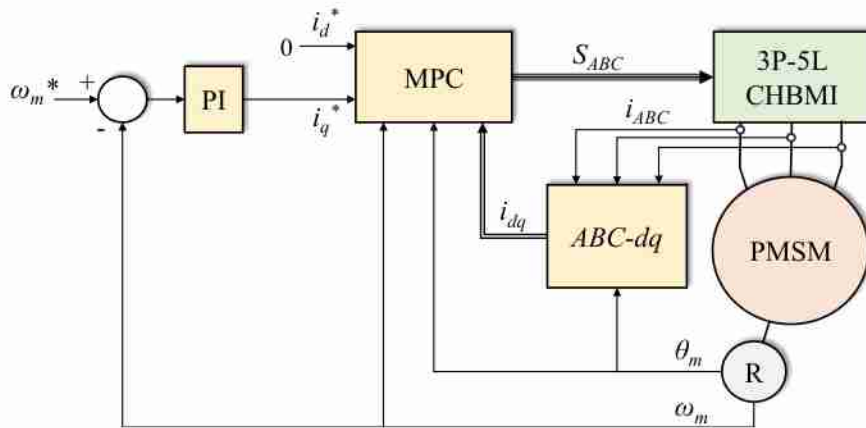


Fig. III. 1: CHB-fed IPMSM drive with FCS-MPC control block scheme.

For the FCS-MPC formulation, the IPMSM and CHB inverter mathematical models are considered. With respect to the IPMSM, the electrical mathematical model formulated in the dq -reference frame, whose equations are reported in Section II.2, is adopted. Here it is reported in the continuous-time state-space form:

$$\frac{d}{dt} \mathbf{i}_{dq}(t) = \mathbf{F} \mathbf{i}_{dq}(t) + \mathbf{G} \mathbf{v}_{dq}(t) + \mathbf{H} \quad (\text{III},12)$$

with:

$$\mathbf{F} = \begin{bmatrix} -\frac{R}{L_d} & \frac{p\omega_m L_q}{L_d} \\ -\frac{p\omega_m L_d}{L_q} & -\frac{R}{L_q} \end{bmatrix}, \mathbf{G} = \begin{bmatrix} \frac{1}{L_d} & 0 \\ 0 & \frac{1}{L_q} \end{bmatrix}, \mathbf{H} = \begin{bmatrix} 0 \\ -\frac{p\omega_m \psi_{PM}}{L_q} \end{bmatrix} \quad (\text{III},13)$$

where $\mathbf{v}_{dq}=[v_d \ v_q]^T$ is the stator voltage vector and $\mathbf{i}_{dq}=[i_d \ i_q]^T$ is the stator current vector. By discretizing equations (III,12) with forward-Euler approximation, the discrete-time state-space model is obtained:

$$\mathbf{i}_{dq}(k+1) = \mathbf{A} \mathbf{i}_{dq}(k) + \mathbf{B} \mathbf{v}_{dq}(k) + \mathbf{K} \quad (\text{III},14)$$

with:

$$\mathbf{A} = \begin{bmatrix} 1 - \frac{T_s R}{L_d} & \frac{p\omega_m T_s L_q}{L_d} \\ -\frac{p\omega_m T_s L_d}{L_q} & 1 - \frac{T_s R}{L_q} \end{bmatrix}, \mathbf{B} = \begin{bmatrix} \frac{T_s}{L_d} & 0 \\ 0 & \frac{T_s}{L_q} \end{bmatrix}, \mathbf{K} = \begin{bmatrix} 0 \\ -\frac{p\omega_m T_s \lambda_{PM}}{L_q} \end{bmatrix} \quad (\text{III},15)$$

The control model of the 3P-5L CHB inverter is obtained by particularizing the state model of the generic n_l -level CHB inverter discussed in Section I.2. In detail, the phase voltage v_{jN} expressed in (I,8) as a function of the GCSs related to the j^{th} phase, with $j \in \{A, B, C\}$ is reported below for a 5L-CHB topology:

$$v_{jN} = V_{dc} (S_{j,11} - S_{j,13} + S_{j,21} - S_{j,23}) \quad (\text{III},16)$$

With respect to the 3P-5L-CHB inverter topology, the relation (I,12), that is reported below, relates the load voltages vector $\mathbf{v}_n=[v_{An} \ v_{Bn} \ v_{Cn}]^T$ with the phase voltage vector $\mathbf{v}_N=[v_A \ v_B \ v_C]^T$ through the matrix $\mathbf{M}$, as follows:

$$\mathbf{v}_n = \mathbf{M} \cdot \mathbf{v}_N \quad (\text{III},17)$$

$$\mathbf{M} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \quad (\text{III},18)$$

In order to incorporate the CHB inverter model in the IPMSM model, the Park transformation matrix $\mathbf{T}_{dq}$, reported below, is applied to the load voltage vector:

$$\mathbf{T}_{dq} = \frac{2}{3} \begin{bmatrix} \cos(p\theta) & \cos\left(p\theta - \frac{2\pi}{3}\right) & \cos\left(p\theta + \frac{2\pi}{3}\right) \\ -\sin(p\theta) & -\sin\left(p\theta - \frac{2\pi}{3}\right) & -\sin\left(p\theta + \frac{2\pi}{3}\right) \end{bmatrix} \quad (\text{III},19)$$

$$\mathbf{v}_{dq} = \mathbf{T}_{dq} \mathbf{v}_n \quad (\text{III},20)$$

By replacing (III,17) in (III,20), it follows:

$$\mathbf{v}_{dq} = \mathbf{T}_{dq} \mathbf{M} \cdot \mathbf{v}_N \quad (\text{III},21)$$

By performing the product between the matrices $\mathbf{T}_{dq}$ and $\mathbf{M}$ it is not difficult to prove that the matrix $\mathbf{T}_{dq}$ is obtained again. Then, (III,21) can be updated as:

$$\mathbf{v}_{dq} = \mathbf{T}_{dq} \mathbf{v}_N \quad (\text{III},22)$$

Equation (III,22) allows for stating that in the dq reference frame, adopting the phase voltage vector or load voltage vector as input vector is equivalent. Then, the implementation of matrix $\mathbf{M}$ can be avoided, allowing for a reduction of the controlled model computational complexity. Then the CHB-fed IPMSM drive model is obtained by replacing (III,22) in (III,14)

$$\mathbf{i}_{dq}(k+1) = \mathbf{A} \mathbf{i}_{dq}(k) + \mathbf{B} \mathbf{T}_{dq} \mathbf{v}_N(k) + \mathbf{K} \quad (\text{III},23)$$

In this work, a prediction horizon $N_p=1$ is adopted. Then, the cost function J , reported in (III,10), is particularized as follows:

$$J = \left\| \mathbf{i}_{dq}^*(k+1) - \mathbf{i}_{dq}(k+1) \right\|_2^2 \lambda_u \left\| \Delta \mathbf{v}_N(k) \right\|_1 \quad (\text{III},24)$$

where $\mathbf{i}_{dq}^*(k+1) = [i_d^*(k+1) \ i_q^*(k+1)]^T$ is the reference currents vector, $\mathbf{i}_{dq}(k+1) = [i_d(k+1) \ i_q(k+1)]^T$ is the future state current vector, $\Delta \mathbf{v}_N = \mathbf{v}_N(k) - \mathbf{v}_N(k-1)$ is the switching effort penalization term. It must be underlined that, at first, the value of the weighting factor λ_u is set to 0.

In order to identify the number of required predictions that must be carried out to solve the IQOCP, VVs and GCSs related to the 3P-5L CHB inverter topology are investigated. For this purpose, VVs in the α - β reference frame are considered. In detail, the voltage vector $\mathbf{v}_{\alpha\beta 0} = [v_\alpha \ v_\beta \ v_0]^T$ is linked to the phase voltage vector $\mathbf{v}_N$ through the Clarke transformation matrix $\mathbf{T}_{\alpha\beta 0}$ as follows:

$$\mathbf{v}_{\alpha\beta 0} = \mathbf{T}_{\alpha\beta 0} \mathbf{v}_N \quad (\text{III},25)$$

with:

$$\mathbf{T}_{\alpha\beta 0} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 1 & 1 \end{bmatrix} \quad (\text{III},26)$$

Since, the inverter phase voltage $v_{jN} \in \{-2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc}\}$, the total number of VVs in the α - β reference frame is obtained as the combination of the three phases inverter voltages, according to:

$$N_{v,\alpha\beta} = n_l^m \quad (\text{III},27)$$

where n_l is the number of phase voltage levels and m is the number of phases. In detail, equation (III,27) is equal to 125 for a 3P-5L CHB. In Fig. III. 2, the available VVs of a 3P-5L-CHB in the α - β reference frame are represented. As can be seen, the total number of non-redundant VVs is equal to 61, thus, most of the 125 VVs are superimposed. By identifying four concentric hexagons and by moving from the outer to the inner one, the Degree of Redundancy (DoR) assigned to the VVs that lie on each hexagon goes from 0 (i.e., no redundant VVs) to 3. The Zero Voltage Vector (ZVV) has a degree of redundancy equal to 4.

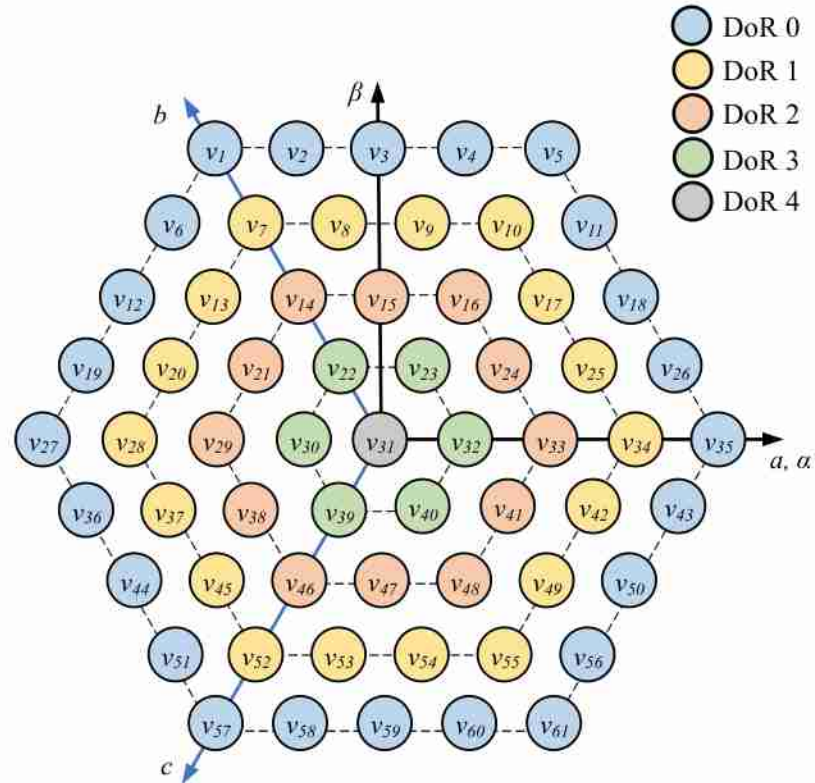


Fig. III. 2: Voltage vectors on the α - β plane related to the 3P-5L-CHBML.

Now, the GCSs are considered. According to (III,16) and (III,25), the number of GCSs combinations N_{GCSs} can be evaluated as the number of states per GCS, which is equal to 2 since $S_{j,iz} \in \{0, 1\}$, to the power of the product between the number of GCSs per phase, which can always be expressed as n_l-1 , and the number of phases m . It follows:

$$N_{GCSs} = 2^{(n_l-1)m} \quad (III,28)$$

which is equal to 4096 when $n_l=5$ and $m=3$. Thus, even considering only 61 non-redundant VVs, most of them can be synthesized by several GCSs combinations.

This analysis highlights the following critical issues in the implementation of FCS-MPC for the 3P-5L CHB-fed IPMSM drive: by initially ignoring redundancies related to GCSs, the total number of VVs is 125. Therefore, the system future state must be predicted a number of times that coincides with the total number of VVs, i.e., 125, and finding the solution to the IQOCP in a sampling interval sufficiently small to be compatible with the electrical time constant of the controlled system is challenging. Moreover, even if this were possible, multiple VVs would return the same value of the cost function J . Therefore, besides simply minimizing the current error, it should also consider a supplementary criterion for selecting the optimal VV. Now, supposing to eliminate redundant VVs and consider the minimum number of available VVs, equal to 61, even non-redundant VVs can be synthesized through different GCSs combinations. Even in this case, it would be necessary to define an additional criterion for selecting the optimal GCSs that provide the same cost function. The worst case takes place when both VVs and all possible combinations of GCSs are considered. In this case, the number of necessary predictions would be 4096, which is an enormous number of predictions for any commercial controller and even for powerful and expensive controllers with scientific research objectives. Finally, it must be considered that the choice of GCSs influences the converter's behavior on both the AC and DC sides. In fact, the presence of multiple isolated DC links significantly complicates the choice of optimal GCSs; indeed, an inappropriate choice of GCSs would cause circulating currents between HB modules and instantaneous power flow inversion towards the DC sources. This could cause the failure of non-bidirectional DC power supplies that, for example, are adopted in this application. In traditional modulation-based control strategies, this issue is solved through the adoption of an appropriate modulation stage, that both allows for synthesizing the reference VV and to impose a certain behaviour on the DC currents.

III.4 Voltage Vector Based-MPC Mathematical Formulation

Looking at the scientific literature, one of the most popular approaches for reducing the FCS-MPC computational cost for MIs deals with solving IQOCP by considering a subset of VVs. With this aim, one of the most interesting solutions is discussed in [III,17], where the VVs candidate set at the current sampling instant is composed of the previous optimal VV and its adjacent VVs. The adopted criterion for eliminating redundant VVs deals with selecting VVs that minimize the CMVs. Indeed, it is a prominent feature in electrical drive applications since high CMV produces bearing currents that determine an early degradation of the bearing and the winding insulation [III,18]. Although the algorithm proposed in [III,17] guarantees both the computational cost reduction and CMV minimization, several issues are left unanswered. Firstly, no attention is paid to GCSs at all; indeed, it is not clear if an extra stage for GCSs selection is adopted, or if redundant GCSs are eliminated, and, if so, what the selection or exclusion criterion is. Moreover, no attention is paid to the CHB DC side behaviour, i.e., SMs DC currents and DC power trends and how GCSs selection influences these patterns. Finally, the FCS-MPC has been designed on a passive RL load, and its impact on an electrical drive is missing. The practical algorithm implementation is not discussed.

This work aims to overcome the main weaknesses of the control strategy presented in [III,17] by designing and implementing a novel multi-objective Voltage-Vector-Based (V^2B) FCS-MPC for CHB-fed IPMSM drive. In detail, the control must fulfill the following goals:

- ❖ Computational burden minimization;
- ❖ CMVs minimization;
- ❖ GCS transitions minimization;
- ❖ Phase voltages dv/dt minimization.

It must be underlined that the control optimization process is carried out offline, to reduce the amount of online computations and, once it is completed, the proposed goals are automatically fulfilled, i.e., no additional cost function terms are required. This feature allows for avoiding the weighting factors tuning process, which is an annoying trial-and-error activity, especially when the cost function comprises many terms [III,7]. The offline optimization process deals with the redundant VVs with high CMVs elimination and optimal GCS set selection, to minimize the switching devices state transitions. An online selection algorithm is implemented to predict the future system state only for the adjacent VVs to the currently applied one. This constraint allows for minimizing both the optimal control problem computational burden since only seven predictions must be carried out at each

sampling period and minimizing the voltage dv/dt since phase voltage instantaneous excursion is limited to one HB DC link voltage.

The offline optimization process and the simplified control algorithm implementation are discussed. To minimize the computational burden, the number of predictions must be minimized. With this aim, the set of available VVs at the k_{th} sampling period consists only of the adjacent VVs to the currently applied one. As a way of example, with respect to the set of available VVs reported in Fig. III. 3, at the k_{th} sampling period, the applied voltage vector is v_{16} , which is identified by the red circle.

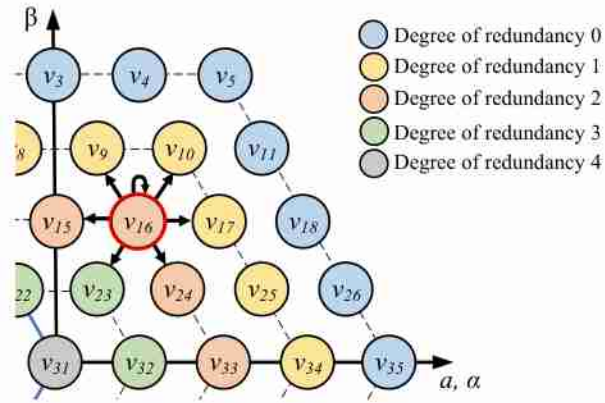


Fig. III. 3: Set of available voltage vectors for predictions when the previous optimal one is v_{16} , identified by the red circle.

At the $k+1^{th}$ sampling instant, the system can move to the adjacent vectors v_{17} , v_{24} , v_{23} , v_{15} , v_9 , and v_{10} or remain in v_{16} . In general, the number of available VVs to be tested in a sampling interval is equal to 7 (i.e., 6 adjacent vectors and the currently applied vector itself), except when the current vector belongs to the outer hexagon; in this case, the number of available input variable sets is equal to 4 when the current vector lies on one of the six edges of the hexagon, and 5 in other cases.

To simplify the control implementation, VV redundancies are eliminated and the adopted criterion to discard redundant vectors is related to CMV minimization. In detail, to minimize the CMVs, per each VV, the Phase Voltages Combinations (PVCs) that minimize the CMV are saved and other combinations are discarded. CMVs are computed according to the following relation:

$$v_{nN} = \frac{v_{aN} + v_{bN} + v_{cN}}{3} \quad (\text{III.29})$$

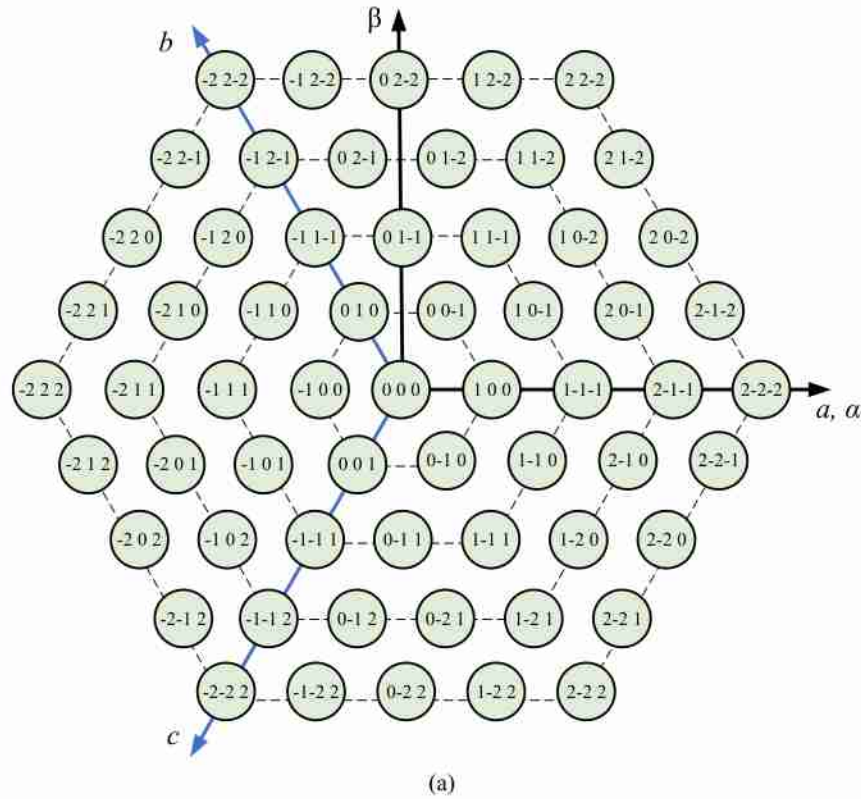
As a way of example, the vector v_7 is considered: it can be obtained by the following PVCs, expressed in the sequence of the phases A , B , and C and in per unit (p.u.) with respect to the voltage V_{DC} : $(-1 \ 2 \ -1)$ and $(-2 \ 1 \ -2)$. These PVCs generate CMVs, expressed in p.u., of 0 V

and -1 V respectively. In this case, the first PVC is saved and the last is discarded. About vector v_{14} , it can be obtained by the PVCs (0 2 0), (-1 1 -1), and (-2 0 -2) which generate CMVs of $2/3$ V, $-1/3$ V, and $-4/3$ V respectively. In this case, the PVC (-1 1 -1) is saved and the others are discarded. Going on with the remaining VVs, it can be noted that there is always only one PVC which minimizes the CMV, this makes the VVs selection very easy. In Fig. III. 4 (a) and (b), the PVCs that minimize the CMVs per each VV and the corresponding CMVs are reported, respectively.

It must be noted that the adopted PVCs reported in Fig. III. 4 (a) allow for fulfilling not only the condition on the CMVs minimization but also the condition on phase voltages dv/dt minimization. Indeed, when moving from a VV to the adjacent one, the following condition is satisfied per each phase:

$$|\Delta v_{jN}| = |v_{jN}(k) - v_{jN}(k-1)| \leq V_{dc} \quad (\text{III},30)$$

Moreover, looking at Fig. III. 4 (a), one or at most two phases change state moving from a VV to the adjacent one.



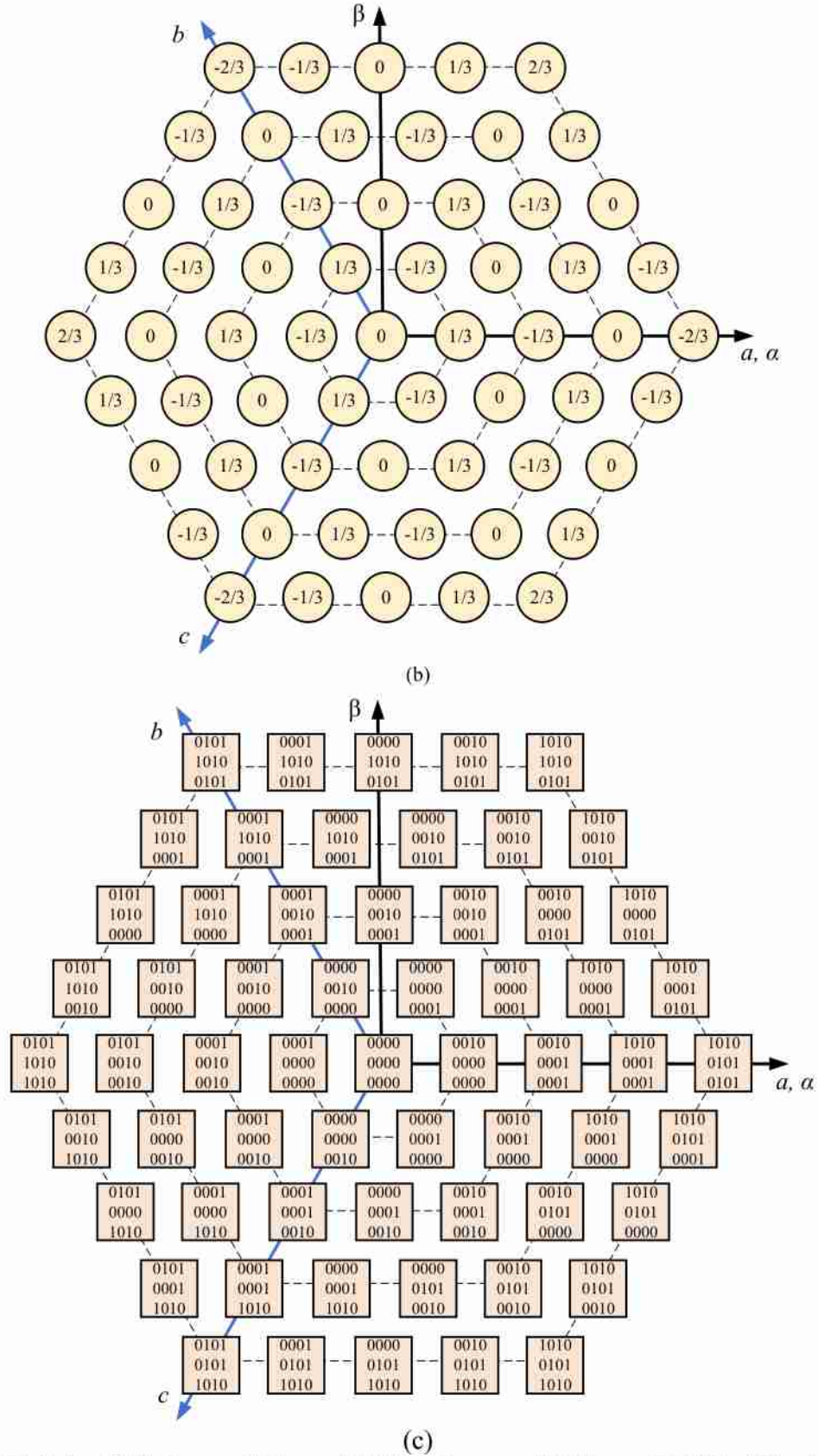


Fig. III. 4: (a) Optimal PVCs for every VV in p.u.; (b) CMV values per each VV in p.u., (c) GCSs which minimize the switching transitions, reported on the α - β plane.

Once the 61 non-redundant optimal VVs are selected, GCSs redundancies are faced. In detail, each VV must be synthesized by only one GCS combination and the adopted criterion to discard redundant GCSs combinations is the minimization of GCSs transitions when

moving from one VV to the adjacent. Indeed, GCSs transitions are correlated to the switching losses. The GCSs assignment procedure is a trial-and-error iterative process, which is briefly discussed below. Considering the generic state transition $v_i \rightarrow v_j$ and assuming that the GCSs set $\mathbf{S}_i$ (expressed as a row of 12 Boolean elements) is always known since it has been assigned previously, the goal is to find the set $\mathbf{S}_j$ which minimizes the transition $\mathbf{S}_i \rightarrow \mathbf{S}_j$, for every VV v_i adjacent to v_j . As a way of example, if the VV v_1 is currently applied, the system can move to vectors v_2, v_6, v_7 . Assuming that $\mathbf{S}_1$ is known, the transition $v_1 \rightarrow v_6$ is considered and it is reported in Table III. 1: it can be noted that the number of transitions is the same and equal to 1 for every $\mathbf{S}_6$. Therefore, the optimal set is chosen arbitrarily (green row in Table III. 1). The same considerations can be applied to the transition $v_1 \rightarrow v_7$, which is summarized in Table III. 2. Now, transition $v_6 \rightarrow v_7$ is considered. In detail, the goal is to verify if the previously selected sets $\mathbf{S}_6$ and $\mathbf{S}_7$ allow also minimizing transitions $v_6 \rightarrow v_7$, which is summarized in Table III. 3. Looking at Table III. 3, the number of transitions is equal to 1 and 3, depending on the considered GCS set. Sets that determine 3 state transitions (red rows in Table III. 3) are discarded. Among the remaining sets, the first one (green row in Table III. 3) coincides with the previously selected set. As can be seen, the selected sets $\mathbf{S}_6$ and $\mathbf{S}_7$ minimize also the transitions $v_6 \rightarrow v_7$. Going on with all the remaining VVs transitions, one GCS set is assigned to each VV. The optimal GCSs are reported in Fig. III. 4 (c). Once a unique match between VVs, PVCs, and GCSs sets is found, the offline optimization process is completed. For control algorithm implementation purposes, the selected sets of PVCs and GCSs are stored in two Look-Up Tables (LUTs), called LUT-1 and LUT-2, respectively. This approach allows for easily defining the set of available PVCs and relative GCSs at the sampling instant k , depending on the previous optimal control action, without affecting the algorithm computational cost, since the access to the elements of LUTs is instantaneous and does not require extra-computations. This aspect is remarked on in Section III.5, where the algorithm implementation is discussed. The final optimal control problem is formulated as follows:

$$\begin{aligned} \mathbf{v}_{dq,opt} = \arg \min J(\mathbf{i}_{dq}(k), \mathbf{v}_{dq}(k)) \\ \text{subject to} \begin{cases} \mathbf{i}_{dq}(k+1) = \mathbf{A}\mathbf{i}_{dq}(k) + \mathbf{B}\mathbf{v}_{dq}(k) + \mathbf{K} \\ |\Delta v_{jN}(k)| \leq V_{DC} \\ \mathbf{v}_{dq}(k) \in \mathcal{U}(k) \end{cases} \end{aligned} \quad (\text{III},31)$$

where $\mathcal{U}(k)$ identifies the available input variables set at the k_{th} sampling instant, which depends on the VV that is currently applied to the system.

Table III. 1: Transition $v_I \rightarrow v_6$

	S_{A11}	S_{A13}	S_{A21}	S_{A23}	S_{B11}	S_{B13}	S_{B21}	S_{B23}	S_{C11}	S_{C13}	S_{C21}	S_{C23}	Number of GCSs transitions
v_I	0	1	0	1	1	0	1	0	0	1	0	1	
v_6	0	1	0	1	1	0	1	0	0	1	0	0	1
	0	1	0	1	1	0	1	0	0	1	1	1	1
	0	1	0	1	1	0	1	0	1	1	0	1	1
	0	1	0	1	1	0	1	0	1	1	0	1	1

Table III. 2: transition $v_I \rightarrow v_7$.

	S_{A11}	S_{A13}	S_{A21}	S_{A23}	S_{B11}	S_{B13}	S_{B21}	S_{B23}	S_{C11}	S_{C13}	S_{C21}	S_{C23}	Number of GCSs transitions
v_I	0	1	0	1	1	0	1	0	0	1	0	1	
v_7	0	0	0	1	1	0	1	0	0	1	0	0	2
	0	0	0	1	1	0	1	0	0	1	0	0	2
	0	0	0	1	1	0	1	0	0	1	1	1	2
	0	0	0	1	1	0	1	0	1	1	0	1	2
	0	1	0	0	1	0	1	0	0	0	0	1	2
	0	1	0	0	1	0	1	0	0	1	0	0	2
	0	1	0	0	1	0	1	0	0	1	1	1	2
	0	1	0	0	1	0	1	0	1	1	0	1	2
	0	1	1	1	1	0	1	0	0	0	0	1	2
	0	1	1	1	1	0	1	0	0	1	0	0	2
	0	1	1	1	1	0	1	0	0	1	1	1	2
	0	1	1	1	1	0	1	0	1	1	0	1	2
	1	1	0	1	1	0	1	0	0	0	0	1	2
	1	1	0	1	1	0	1	0	0	1	0	0	2
	1	1	0	1	1	0	1	0	0	1	1	1	2
	1	1	0	1	1	0	1	0	1	1	0	1	2

Table III. 3: transition $v_6 \rightarrow v_7$.

	S_{A11}	S_{A13}	S_{A21}	S_{A23}	S_{B11}	S_{B13}	S_{B21}	S_{B23}	S_{C11}	S_{C13}	S_{C21}	S_{C23}	Number of GCSs transitions
v_6	0	1	0	1	1	0	1	0	0	0	0	1	
v_7	0	0	0	1	1	0	1	0	0	0	0	1	1
	0	0	0	1	1	0	1	0	0	1	0	0	3
	0	0	0	1	1	0	1	0	0	1	1	1	3
	0	0	0	1	1	0	1	0	1	1	0	1	3
	0	1	0	0	1	0	1	0	0	0	0	1	1
	0	1	0	0	1	0	1	0	0	1	0	0	3
	0	1	0	0	1	0	1	0	0	1	1	1	3
	0	1	0	0	1	0	1	0	1	1	0	1	3
	0	1	1	1	1	0	1	0	0	0	0	1	1
	0	1	1	1	1	0	1	0	0	1	0	0	3
	0	1	1	1	1	0	1	0	0	1	1	1	3
	0	1	1	1	1	0	1	0	1	1	0	1	3
	1	1	0	1	1	0	1	0	0	0	0	1	1
	1	1	0	1	1	0	1	0	0	1	0	0	3
	1	1	0	1	1	0	1	0	0	1	1	1	3
	1	1	0	1	1	0	1	0	1	1	0	1	3

III.5 V²B-MPC Implementation

In this section, the algorithm implementation is discussed. The proposed control algorithm is summarized in Algorithm III. 1. First, operations that can be executed once per sampling period, i.e., the delay time compensation, are implemented. In detail, since the control execution time is always higher than zero, a delay is introduced between the sampling instant

and the control action application instant. Such a delay depends on the algorithm computational complexity and on the adopted controller. In this application, the control action is instantaneously applied when it is available, instead of being stored and applied to the next sampling instant, as is usual when control with a modulator is adopted. As a consequence, the delay time T_d coincides with the execution time. These aspects are illustrated in Fig. III. 5: in detail, the ideal case with a null execution time (i.e. a delay time $T_d=0$) and the real case with a non-null execution time (i.e. a delay time $T_d \neq 0$) are reported in Fig. III. 5(a) and Fig. III. 5(b), respectively. Ignoring the delay time in practical applications can determine non-accurate future system state predictions, which lead to the application of sub-optimal solutions to the controlled system and, as a consequence, current and torque ripple [III,19].

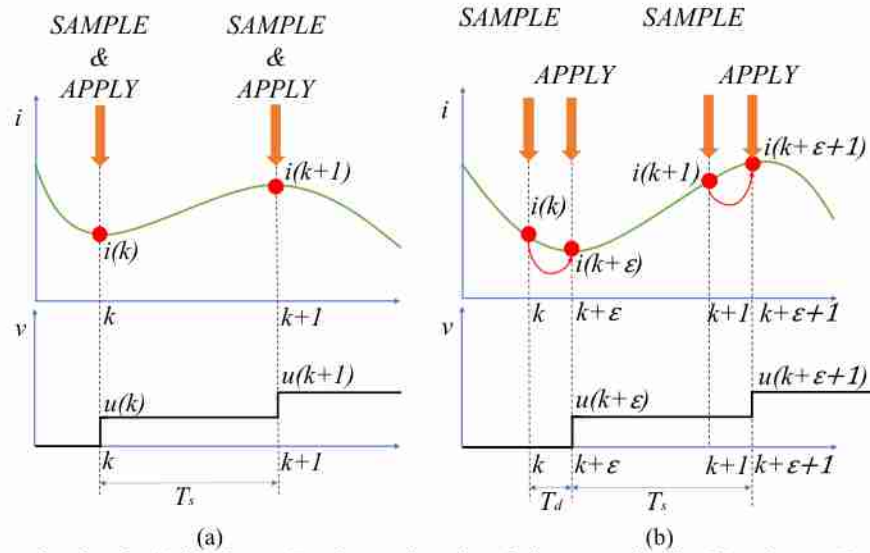


Fig. III. 5: Control actions in (a) ideal case, $T_d = 0$, sample and apply instants coincide; (b) real case, $T_d \neq 0$, sample and apply instants don't coincide.

To take into account such execution time, a delay compensation strategy is adopted. By assuming that the delay time T_d is known and constant for each sampling period T_s , and assuming the speed ω_m and the angular position θ constant over the sampling period T_s , an initial prediction is performed to project the system state from instant k to the instant $k+\varepsilon$, where $k+\varepsilon$ is the control action application instant, which is between the k_{th} and $k+1_{th}$ sampling instants and is correlated with the delay time T_d , according to Fig. III. 5. The system state at the instant $k+\varepsilon$ represents the new current state to adopt for the future state predictions. The initial prediction is performed according to (III,32):

$$\mathbf{i}_{dq}(k+\varepsilon) = \mathbf{A}_d \mathbf{i}_{dq}(k) + \mathbf{B}_d \mathbf{v}_{dq,opt}(k+\varepsilon-1) + \mathbf{K}_d \quad (\text{III,32})$$

with $\mathbf{A}_d$, $\mathbf{B}_d$, and $\mathbf{K}_d$ defined as in (III,15) but replacing the delay time T_d with the sampling time T_s , as follows:

$$\mathbf{A}_d = \begin{bmatrix} 1 - \frac{T_d R}{L_d} & \frac{p\omega_m T_d L_q}{L_d} \\ -\frac{p\omega_m T_d L_d}{L_q} & 1 - \frac{T_d R}{L_q} \end{bmatrix}, \mathbf{B}_d = \begin{bmatrix} \frac{T_d}{L_d} & 0 \\ 0 & \frac{T_d}{L_q} \end{bmatrix}, \mathbf{K}_d = \begin{bmatrix} 0 \\ -\frac{p\omega_m T_d \lambda_{PM}}{L_q} \end{bmatrix} \quad (\text{III},33)$$

and $\mathbf{v}_{dq,opt}$ is the optimal input vector applied to the system at the instant $k+\varepsilon-1$, which is also applied at the sampling instant k and whose value is known. Once the system state at the instant $k+\varepsilon$ is estimated, it is possible to predict the state at the instant $k+\varepsilon+1$, that is, according to Fig. III. 5, the future control action application instant, as follows:

$$\mathbf{i}_{dq}(k+\varepsilon+1) = \mathbf{A}\mathbf{i}_{dq}(k+\varepsilon) + \mathbf{B}\mathbf{v}_{dq}(k+\varepsilon) + \mathbf{K} \quad (\text{III},34)$$

with matrices $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{K}$ defined as in (III,15). Replacing (III,22) and (III,32) in (III,34) and rearranging, the following relation is obtained

$$\mathbf{i}_{dq}(k+\varepsilon+1) = \mathbf{A}\mathbf{A}_d\mathbf{i}_{dq}(k) + \mathbf{A}\mathbf{B}_d\mathbf{T}_{dq}\mathbf{v}_{N,opt}(k+\varepsilon-1) + \mathbf{A}\mathbf{K}_d + \mathbf{B}\mathbf{T}_{dq}\mathbf{v}_N(k+\varepsilon) + \mathbf{K} \quad (\text{III},35)$$

Looking at equation (III,35), it can be noted that only the term $\mathbf{B}\mathbf{v}_{dq}(k+\varepsilon)$ depends on the phase voltage vector $\mathbf{v}_N$. Therefore, the term $\mathbf{i}_{dq,p1}(k+\varepsilon+1)$ can be defined:

$$\mathbf{i}_{dq,p1}(k+\varepsilon+1) = \mathbf{A}\mathbf{A}_d\mathbf{i}_{dq}(k) + \mathbf{A}\mathbf{B}_d\mathbf{T}_{dq}\mathbf{v}_{N,opt}(k+\varepsilon-1) + \mathbf{A}\mathbf{K}_d + \mathbf{K} \quad (\text{III},36)$$

This term can be computed only once per sampling period since it is the same for all 7 predictions. Looking at the matrices $\mathbf{B}_d$ and $\mathbf{K}_d$, it is possible to note that T_d is a common factor and can be put in evidence. By defining the term:

$$\mathbf{A}' = \mathbf{A} \frac{T_d}{T_s} \quad (\text{III},37)$$

the relation (III,36) can be rearranged as:

$$\mathbf{i}_{dq,p1}(k+\varepsilon+1) = \mathbf{A}\mathbf{A}_d\mathbf{i}_{dq}(k) + \mathbf{A}'\mathbf{B}\mathbf{v}_{dq,opt}(k+\varepsilon-1) + (\mathbf{A}'+\mathbf{I})\mathbf{K} \quad (\text{III},38)$$

Then, defining (III,37) allows for supposing that the term $\mathbf{B}\mathbf{v}_{dq,opt}$ is known since it coincides with the optimal $\mathbf{B}\mathbf{T}_{dq}\mathbf{v}_N$ computed at the previous sampling instant, allowing for further reducing the number of required computations. Thus, the expression (III,35) can be rewritten as:

$$\mathbf{i}_{dq}(k+\varepsilon+1) = \mathbf{i}_{dq,p1}(k+\varepsilon+1) + \mathbf{B}'(k)\dot{\mathbf{v}}_N(k+\varepsilon) \quad (\text{III},39)$$

Where $\dot{\mathbf{v}}_N$ is the phase voltage vector expressed in p.u., while $\mathbf{B}'$ is defined as:

$$\mathbf{B}'(k) = V_{dc} \mathbf{B}\mathbf{T}_{dc}(k) \quad (\text{III},40)$$

Next, based on the currently applied VV, the set of available VVs and the corresponding PVCs are defined. This operation is carried out by acceding to a LUT: in detail, each VV is

identified by a number v_x , according to the enumeration in Fig. III. 2, which represents the address to accede to the LUT-1, where PVCs are stored, according to Fig. III. 4 (a). Since the currently applied VV is known, the set of available 7 VVs for future state predictions is identified. It must be underlined that this operation is extremely fast since access to LUTs doesn't affect the computational burden and the algorithm execution time. Once the 7 VVs are known, the 7 corresponding predictions are carried out. The VV which minimizes the cost function J represents the solution to the IQOCP and the corresponding GCSs set is identified through the LUT-2 and applied to the system.

Algorithm III. 1: V²B-MPC for 3P-5L-CHB-fed IPMSM drive.

Voltage Vector Based Model Predictive Control Algorithm	
1:	function V ² B-MPC ($\mathbf{i}_{dq}(k)$, $\mathbf{i}_{dq}^*(k)$, $\mathbf{S}_{opt}(k-1)$, $\omega_m(k)$, $\theta_m(k)$, $M(k-1)$)
2:	Compute $\mathbf{i}_{dq,pt}(k+\varepsilon+1)$, according to (III,38)
3:	Compute $\mathbf{B}'(k)$ according to (III,40)
4:	Access to LUT-1: Define the set of 7 $\hat{\mathbf{v}}_N(k+\varepsilon)$ and v_x , based on $v_{x,opt}(k+\varepsilon-1)$
5:	Initialize cost function J_0
6:	for $y=1: 7$
7:	Compute $\mathbf{i}_{dq}(k+\varepsilon+1, y)$ according to (III,39)
8:	Compute $J(y)$, according to (III,24)
9:	if $J(y) \leq J_0$
10:	$J_0 \leftarrow J(y)$
11:	$v_{x,opt}(k+\varepsilon) \leftarrow v_x(y)$
12:	end if
13:	end for
14:	Access to LUT-2: Define $\mathbf{S}_{opt}(k+\varepsilon)$, based on $v_{x,opt}(k+\varepsilon)$
15:	Apply $\mathbf{S}_{opt}(k+\varepsilon)$ to the system
16:	end function

The test bench adopted to prove the effectiveness of the proposed algorithm is the same as discussed in Section II.3. Indeed, the adopted controller is the SoM sbRIO 9651 and the presented algorithm is entirely implemented on the FPGA target with single-precision floating point data. The RT target is adopted only for the implementation of GUI. In Table III. 4, the control parameters adopted for the V²B-MPC are reported: in detail, the adopted sampling period is equal to 100 μ s, the computational time is experimentally measured and is equal to 23 μ s.

Table III. 4: V²B-MPC control parameters.

Quantity	Symbol	Value
DC Link Voltage	V_{dc}	55 V
Pole pairs	p	3
Stator resistance	R	2.21 Ω
Direct inductance	L_d	0.0088 H
Quadrature inductance	L_q	0.0125 H
PM direct flux	λ_{PM}	0.0913 Wb
Sampling period	T_s	100 μ s
Delay time	T_d	23 μ s

The implementation in the LabVIEW environment is carried out following the same approach discussed in Section II.4. Indeed, the main difference between the FOC and the

proposed MPC is related to the LFWL, where the dq current PI regulators, the decoupling block, and the inverse Park transformation are replaced with the operations reported in Algorithm III. 1. Since the output of Algorithm III. 1 is the set of optimal GCSs $\mathbf{S}_{opt}(k+\varepsilon)$, then counter employed to implement MC-PWM strategies in the TL are removed and GCSs are directly applied to the system. As a way of example, Fig. III. 6 shows some frames of the FSS placed inside the LFWL, where the MPC is implemented. In detail, Fig. III. 6 (a) shows the set of operations required to compute the elements of the vector $\mathbf{i}_{dq,p1}$ according to (III,38), while Fig. III. 6 (b) shows, from left to right, the access to LUT-1 adopted to select the subset of 7 VVs available for predictions, the prediction and cost function minimization stage implemented through a *for* loop, and the access LUT-2 where GCSs combination related to the optimal VV is found. The optimal GCSs combination is sent to the main scheduler TL and, after applying the DT, it is applied to the CHB-fed IPMSM drive.

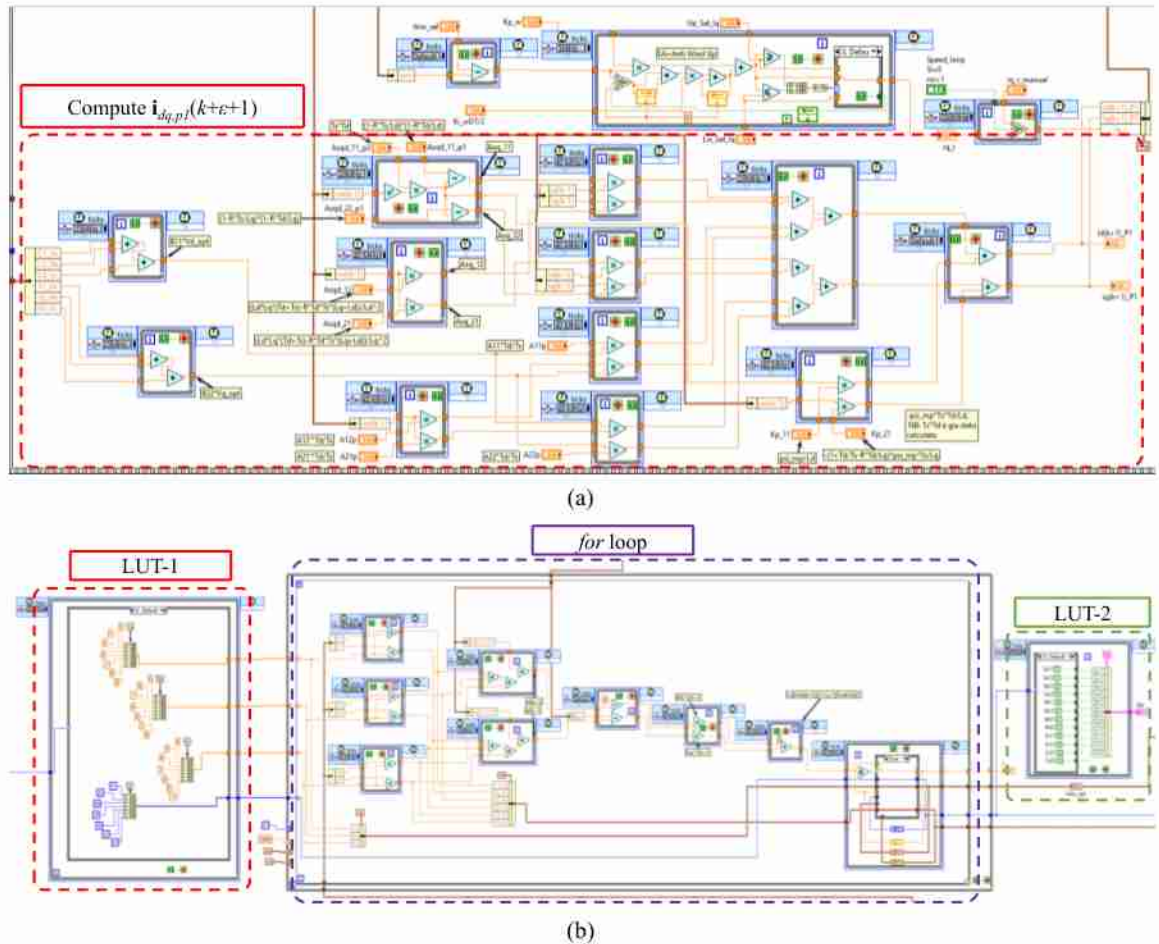


Fig. III. 6: V²B-MPC algorithm in LabVIEW FPGA environment, some frames of the FSS inside the LFWL, (a) Compute $\mathbf{i}_{dq,p1}$, (b) access to LUT-1, *for* loop to predict the future system state and minimize J , access to LUT-2.

III.6 Cell By Cell Based-MPC as the Comparison Target

In order to prove the effectiveness of the proposed V²B-MPC, a comparison with another MPC algorithm for the CHB inverter is carried out. In detail, the Cell-By-Cell-Based

(CBCB) MPC proposed in [III,6] for a single-phase CHB rectifier is adopted as a comparison target. Such a choice is carried out due to the following reasons:

- ❖ the CBCB approach allows for reducing the control computational complexity by introducing some specific switching constraints that exploit the CHB inverter topology;
- ❖ this constraints-based control design approach is homogeneous with the one adopted in this work; moreover, no Branch and Bound (B&B) approach must be adopted to solve the optimal control problem and this makes the control implementation quite easy;
- ❖ although the CBCB algorithm is proposed for a single-phase CHB rectifier, its strong correlation with the converter topology allows for easily adapting the algorithm to a three-phase electric drive application.

Then, the CBCB-MPC algorithm represents a computationally cost-effective, easy-to-implement algorithm that exploits the potentialities of the CHB topology; therefore, it becomes the best available comparison target for the proposed V^2B -MPC. According to [III,6], the CBCB-MPC for the single-phase CHB rectifier is based on predicting the future system state allowing only one HB module at a time to change its state. The algorithm is adapted to the 3P-5L-CHB-fed IPMSM drive by introducing the following rules:

1. Only one HB module per phase must be allowed to change its state;
2. Only one HB leg per module must be allowed to change its state.

With respect to one phase, in order to comply with rule 1, the binary *enabling* variable M is introduced: when $M=1$ the upper HB module is allowed to change state and the lower HB module state is locked; when $M=0$ the upper HB module state is locked and the lower HB module is allowed to change state, as summarized in Fig. III. 7.

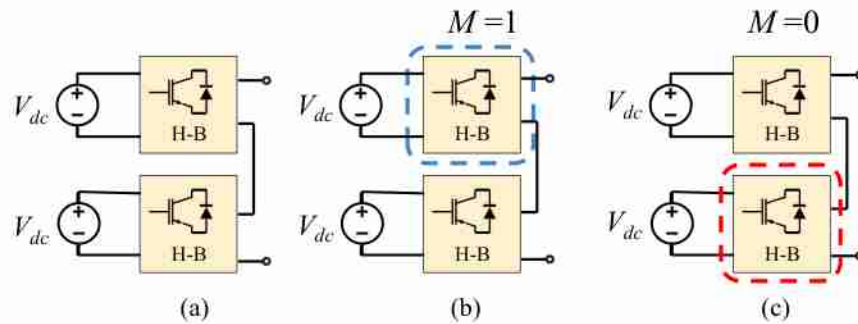


Fig. III. 7: (a) one phase of the 3P-5L-CHB; (b) $M=1$, the upper HB module is allowed to change state, the lower HB module state is locked; (c) $M=0$, the lower HB is allowed to change state and the upper HB state is locked.

The same criterion must be applied to other phases. To comply with rule 2, with respect to the state-unlocked HB module per each phase, the future available states depend on the current state, according to Fig. III. 8. In detail, in Fig. III. 8 (a), all the available state transitions for the state-unlocked HB module are summarized. Available transitions depending on the HB module current state (identified by the red circle) are summarized in Fig. III. 8. (b), (c), (d), and (e).

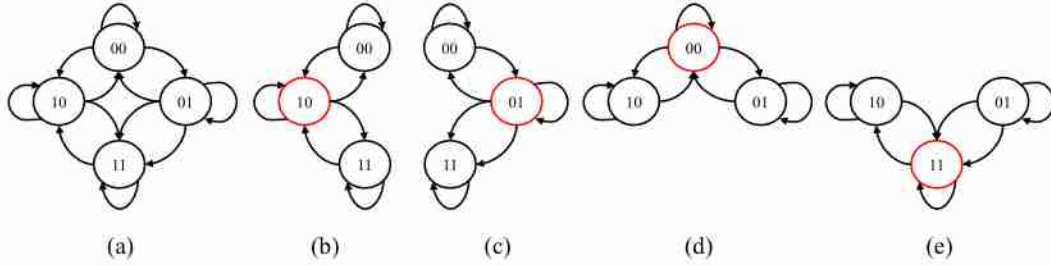


Fig. III. 8: (a) available HB future states when rules 1 and 2 are complied, (b-e), available H-B future states when rules 1 and 2 are complied, taking into account the H-B current state (identified by the red circle).

It can be noted that by complying with rules 1 and 2, GCSs transitions and phase voltage variation $|\Delta v_{jN}|$ are minimized and the relation (III,30) is always satisfied. Moreover, three predictions per phase must always be carried out. To adapt the algorithm for a three-phase electrical drive, the phase-voltage combinations must be taken into account. Thus, the maximum number of predictions becomes $3^3=27$. The IQOCP is formulated as follows:

$$\begin{aligned} \mathbf{v}_{dq,opt} &= \arg \min J(\mathbf{i}_{dq}(k), \mathbf{v}_{dq}(k)) \\ \text{subject to } &\begin{cases} \mathbf{i}_{dq}(k+1) = \mathbf{A}\mathbf{i}_{dq}(k) + \mathbf{B}\mathbf{v}_{dq}(k) + \mathbf{K} \\ |\Delta v_{jN}(k)| \leq V_{dc} \\ \mathbf{v}_{dq}(k) \in \mathcal{U}(k) \end{cases} \end{aligned} \quad (\text{III,41})$$

To make the comparative analysis with the V²B-MPC as fair as possible, the CBCB-MPC implementation is carried out almost in the same way as discussed in the previous sections about the V²B-MPC: in detail, the electric drive control model, the cost function, the delay time compensation strategy, the model parameters, and the sampling frequency are the same as discussed in equations (III,14), (III,16), (III,22), and (III,24), and reported in Table III. 4, respectively. The CBCB-MPC algorithm is summarized in Algorithm III. 2. To minimize the computational cost, also in this case the prediction equation has been split into a term that can be computed only once per sampling period and a term, that depends on the available phase voltages at the current sampling instant, which must be computed several times to carry out the future state predictions, according to equations (III,36) and (III,39). Next, the set of available state functions at the instant $k+\varepsilon$ is defined, according to the two algorithm

rules summarized in Fig. III. 7 and Fig. III. 8, respectively. In detail, these rules depend on the value at the previous iteration of the *enabling* variable M and on the set of optimal switching states at the previous iteration $\mathbf{S}_{opt}(k+\varepsilon-1)$. When the set of available GCSs is defined, the predictions of the system state at instant $k+\varepsilon+1$ for every available GCSs combination are carried out. In detail, 27 predictions must be carried out. However, since the three-phase voltages v_{AN} , v_{BN} , and v_{CN} are mutually independent, operations to compute the second term of (III,39) are organized into three nested *for* loops, thus, v_{AN} and $\mathbf{i}_{dq,p2}(k+\varepsilon+1)$ are computed only 3 times, v_{BN} and $\mathbf{i}_{dq,p3}(k+\varepsilon+1)$ are computed 9 times, and v_{CN} , $\mathbf{i}_{dq}(k+\varepsilon+1)$, and the cost function J are computed 27 times. At every iteration, the computed cost function J is compared with the last minimum J_0 : if $J \leq J_0$, the value of J_0 and $\mathbf{S}_{opt}(k+\varepsilon)$ are updated. At the end of the 27 iterations, J_0 represents the minimum of the cost function and $\mathbf{S}_{opt}(k+\varepsilon)$ is the set of input variables that minimized J . The set $\mathbf{S}_{opt}(k+\varepsilon)$ is applied to the system.

Algorithm III. 2: CBCB-MPC for 3P-5L-CHB-fed IPMSM drive.

Cell-By-Cell-Based Model Predictive Control Algorithm	
1:	function CBCB-MPC ($\mathbf{i}_{dq}(k)$, $\mathbf{i}_{dq}^*(k)$, $\mathbf{S}_{opt}(k+\varepsilon-1)$, $\omega_m(k)$, $\theta_m(k)$, $M(k-1)$)
2:	Compute $\mathbf{i}_{dq,p1}(k+\varepsilon+1)$, according to (III,38)
3:	Compute $\mathbf{B}'(k)$ according to (III,40)
4:	if $M(k-1)=0$
5:	$M(k) \leftarrow 1$
6:	Define the set of available $S_{j,1z}(k+\varepsilon)$, according to Fig. III. 8
7:	$S_{j,2z}(k) \leftarrow S_{j,2z}(k-1)$
8:	else if $M(k-1)=1$
9:	$M(k) \leftarrow 0$
10:	Define the set of available $S_{j,2z}(k+\varepsilon)$, according to Fig. III. 8
11:	$S_{j,1z}(k) \leftarrow S_{j,1z}(k-1)$
12:	end if
13:	Initialize cost function J_0
14:	for $l=1:3$
15:	Compute $\dot{v}_{AN}(l)$, according to (III,16)
16:	$\mathbf{i}_{dq,p2}(k+\varepsilon+1) \leftarrow \mathbf{i}_{dq,p1}(k+\varepsilon+1) + [\mathbf{B}'_{11}\dot{v}_A(l) \mathbf{B}'_{21}\dot{v}_A(l)]^T$
17:	for $m=1:3$
18:	Compute $\dot{v}_{BN}(m)$, according to (III,16)
19:	$\mathbf{i}_{dq,p3}(k+\varepsilon+1) \leftarrow \mathbf{i}_{dq,p2}(k+\varepsilon+1) + [\mathbf{B}'_{12}\dot{v}_B(m) \mathbf{B}'_{22}\dot{v}_B(m)]^T$
20:	for $n=1:3$
21:	Compute $\dot{v}_{CN}(n)$, according to (III,16)
22:	$\mathbf{i}_{dq}(k+\varepsilon+1) \leftarrow \mathbf{i}_{dq,p3}(k+\varepsilon+1) + [\mathbf{B}'_{13}\dot{v}_C(n) \mathbf{B}'_{23}\dot{v}_C(n)]^T$
23:	Compute J , according to (III,24)
24:	if $J \leq J_0$
25:	$J_0 \leftarrow J$
26:	$\mathbf{S}_{opt}(k+\varepsilon) \leftarrow [S_{A,11}(l) S_{A,13}(l) S_{A,21}(l) S_{A,23}(l) \dots$ $S_{B,11}(m) S_{B,13}(m) S_{B,21}(m) S_{B,23}(m) \dots$ $S_{C,11}(n) S_{C,13}(n) S_{C,21}(n) S_{C,23}(n)]$
27:	end if
28:	end for
29:	end for
30:	end for
31:	Apply $\mathbf{S}_{opt}(k+\varepsilon)$ to the system
32:	end function

Implementation of Algorithm III. 2 in the LabVIEW FPGA target is carried out similarly to the V²B-MPC algorithm. The main difference deals with the identification of M and implementation of the three nested for loops, which are shown in Fig. III. 9 as a way of example. The execution time for the CBCB-MPC is equal to 55 μ s. It can be noted that CBCB-MPC requires more than twice the time needed by the VVB-MPC to elaborate the control action, due to the higher number of predictions required. In this case, the V²B approach results in being more efficient than the phase-by-phase-based one. In Table III. 5, the control computational resources employed for the CBCB-MPC and the VVB-MPC are reported. It must be underlined that employed computational resources and computational time deal with the whole control, which consists not only of the current MPC algorithm but also includes the sampling process, the ATO algorithm for the speed and position measurement, and the outer speed control loop, which is synthesized as common PI controller. The rest of the control algorithm has been discussed in Section II.4.



Fig. III. 9: CBCB-MPC algorithm in LabVIEW FPGA environment, one frame of the FSS inside the LFWL, read $M(k-1)$ and set the available GCSs, three nested for loops to predict the future system state and minimize J .

Table III. 5: Employed Computational Resources on SoM sbRIO 9651.

Device Utilization	Available resources	Employed resources [%]	
		CBCB-MPC	V ² B-MPC
Total slices	13300	86.9	86.8
Slice registers	106400	26.7	26.8
Slice LUTs	53200	68.2	67.9
Block RAMs	140	6.4	7.1
DSP48s	220	90.9	88.2

III.7 V²B-MPC Experimental Validation

In this section, experimental results are presented to validate the effectiveness of the proposed control algorithm. Moreover, a detailed comparison between the V²B-MPC and the CBCB-MPC is carried out both in steady state and dynamic working conditions. The test bench consists of the DigiPower 3P-5L CHB prototype powered by six 55 V DC power supply RSO-2400 and the Magnetic S.r.l. BLQ-40 three-phase IPMSM, and it has been deeply described in Section II.3. Such electric drive performance analysis is carried out similarly to the analysis carried out in Chapter II. In detail, for the steady-state performance

analysis, the apparent switching frequency, the current and voltage THD, and the CMV are adopted as performance metrics. To generate thicker maps if compared to that shown in Section II.7, 20 WPs are considered instead of 16, defined as a function of IPMSM working conditions in terms of speed n and load torque T . The considered working points are summarized in Table III. 6. For each identified WP, phase voltages and phase currents are measured with a Teledyne LeCroy MDA 8028HD oscilloscope, with an observation window of 1 s and a sampling frequency of 1 MS/s.

Table III. 6: CHB-fed IPMSM drive working points.

T [Nm]- n [rpm]	200	1000	2000	3000	4000
1.8	WP5	WP4	WP3	WP2	WP1
1.35	WP10	WP9	WP8	WP7	WP6
0.9	WP15	WP14	WP13	WP12	WP11
0.45	WP20	WP19	WP18	WP17	WP16

Concerning the dynamic behaviour analysis, a cycle composed of a 0-3000 rpm acceleration, including no-load and rated-load operations, has been carried out. During dynamic analysis, the maximum allowed transitory currents is set to $i_q=10$ A and $i_d=0$, respectively. IPMSM phase voltages, phase currents, load torque applied by the brake and speed signals are acquired with MDA 8028HD oscilloscope by setting an observation window of 5 s and a sampling frequency of 500 kS/s.

III.7.1 Comparison in Steady-state working conditions

The load voltages v_{An} , v_{Bn} , and v_{Cn} , and phase currents generated with V²B-MPC when the CHB-fed IPMSM drive is in WP2 ($n=3000$ rpm and $T=1.8$) are shown. It must be underlined that in the rest of this chapter the phase voltages v_{AN} , v_{BN} , and v_{CN} measured with respect to the CHB star center N are reported. Such a choice is carried out to easily evaluate the apparent switching frequency. Indeed, load voltages depend on the switching behaviour of all three phases, making the estimation of switching frequency challenging.

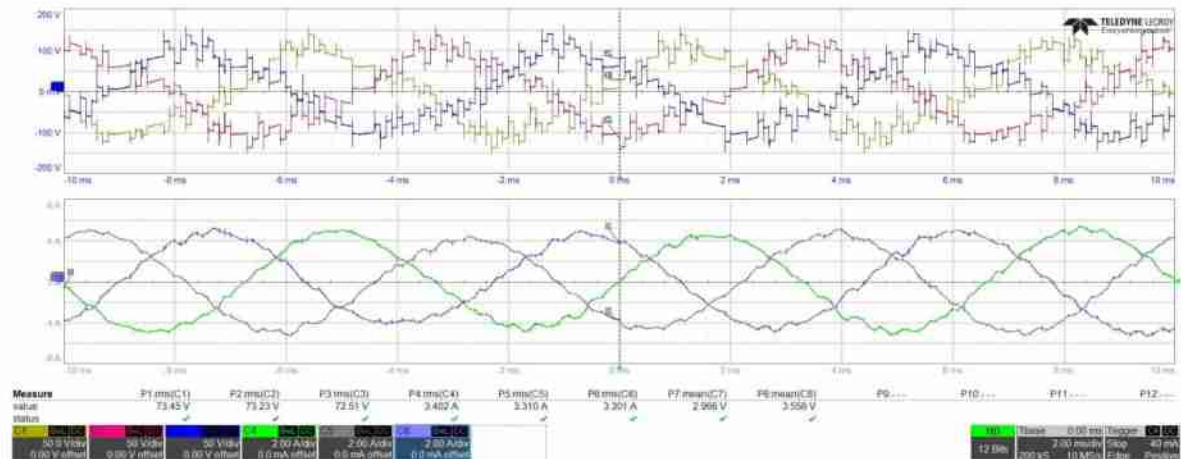


Fig. III. 10: Load voltages and phase current obtained with V²B-MPC, $f_s=10$ kHz, $n=3000$ rpm, $T=1.8$ Nm.

The phase voltages produced by the CBCB-MPC and the V²B-MPC in the time and frequency domain are reported in Fig. III. 11 (a-j) and Fig. III. 11 (k-u), respectively, when the load torque is set to 1.8 Nm and the speed is varied over the defined working range. Concerning the V²B-MPC, phase voltages exhibit three voltage levels when the speed is lower than 2000 rpm, and five levels when the speed is higher than 2000 rpm. Phase voltages with CBCB-MPC are characterized by a more chaotic behaviour and exhibit the fifth level even in the low-speed working range. However, in both cases, phase voltages are characterized by dv/dt at most equal to one HB DC link voltage over the entire working range, as is expected by their mathematical formulation. Voltage spectra with V²B-MPC present harmonics lower than 5% of the fundamental except when the speed is equal to 4000 rpm when the overmodulation region is reached. Concerning the CBCB-MPC, voltage spectra are characterized by higher harmonics amplitude almost in every considered working point, especially in the low-speed range where low-frequency harmonics reach 20% of the fundamental. A comparison between instantaneous CMV trends is reported in Fig. III. 11(v-z): concerning V²B-MPC, the CMVs maximum instantaneous value is equal to 18.33 V, except when the speed is equal to 4000 rpm where it is equal to 36.66 V; a much worse behaviour can be noted with the CBCB-MPC, where the most frequent peak value is equal to 55 V and the maximum peak value is equal to 110 V which occur in the low-speed range. This behaviour is emphasized in Fig. III. 12, where CMV instantaneous peak values over the defined working range are reported. It can be noted that the control goal of minimizing the CMV with the V²B-MPC, which is synthesized in Fig. III. 4 (b), is reached over the entire defined working range, since the CMV peak is always equal to $V_{dc}/3$ (i.e. 18.33 V, when $V_{dc} = 55$ V), except in WPs 1, 6, and 11, where the CMV peak reaches the value of $2V_{dc}/3$ equal to 36.66 V. This behaviour is justified by taking into account that only when the speed is equal to the rated value and the load is higher than half the rated torque, it is mandatory to employ the VVs v_{11} , v_{55} , v_{27} , v_{35} , v_{57} , and v_{61} are employed where a higher CMV peak value cannot be avoided. On the other hand, no attention is paid to CMVs in the CBCB-MPC algorithm design. Only when the speed reaches the rated value, CMV behaviours become similar.

The phase currents in the time and frequency domain, when the CBCB-MPC and the V²B-MPC are adopted, are shown in Fig. III. 13 (a-h) and (i-p), respectively, when the load torque is varied over the defined working range and the speed is constant and equal to 3000 rpm.

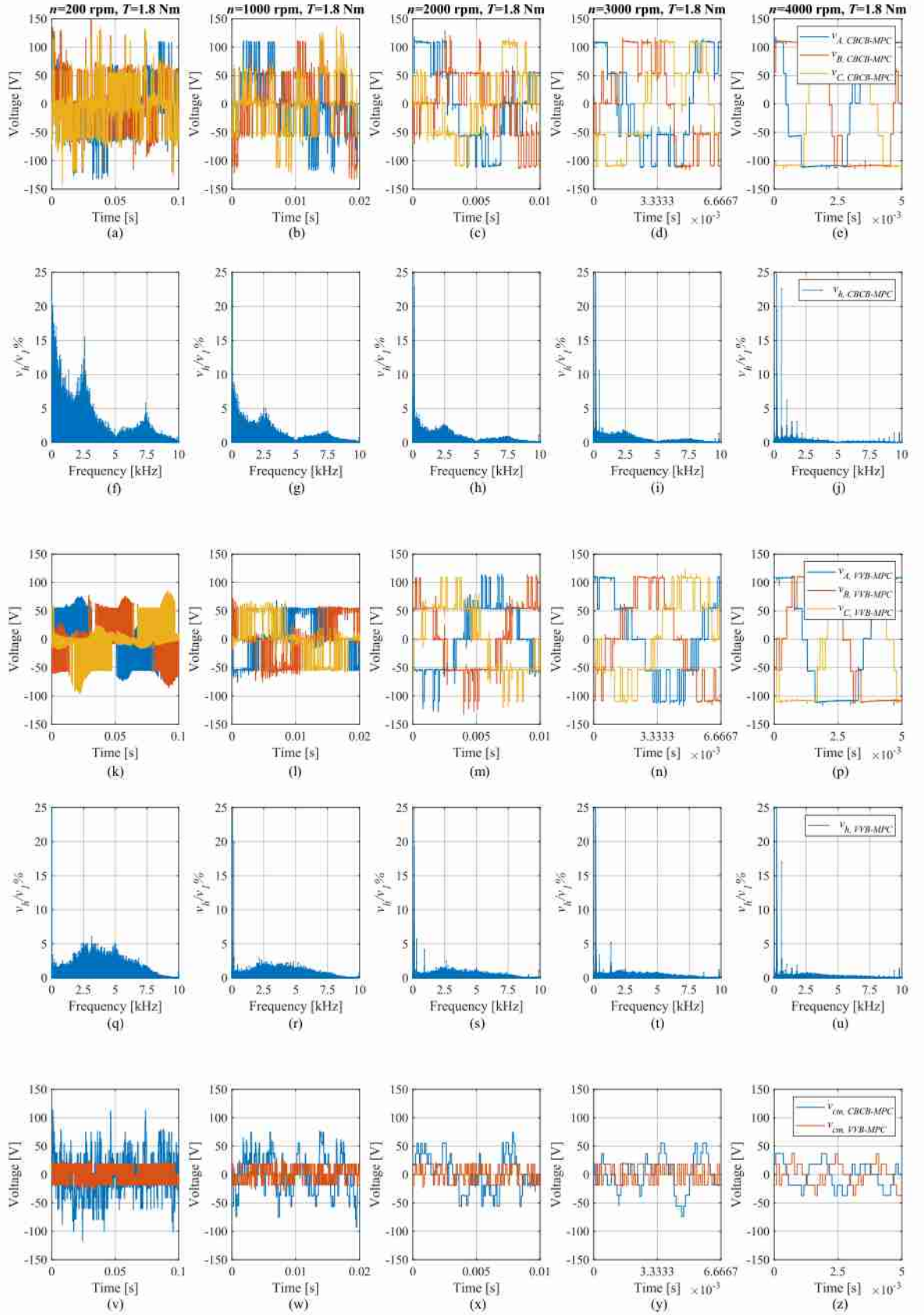


Fig. III. 11: Analysis for fixed load torque (1.8 Nm), varying the speed over the defined working range: (a-e) CBCB-MPC phase voltages, (f-j) CBCB-MPC phase voltage spectra, (k-p) V²B-MPC phase voltages, (q-u) V²B-MPC phase voltage spectra, (v-z) CBCB and V²B-MPC common mode voltages comparison.

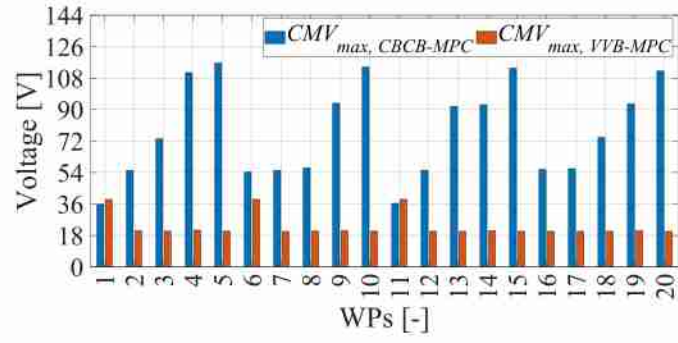


Fig. III. 12: Comparison between peak values of the common mode voltage in each working point with CBCB-MPC and V²B-MPC.

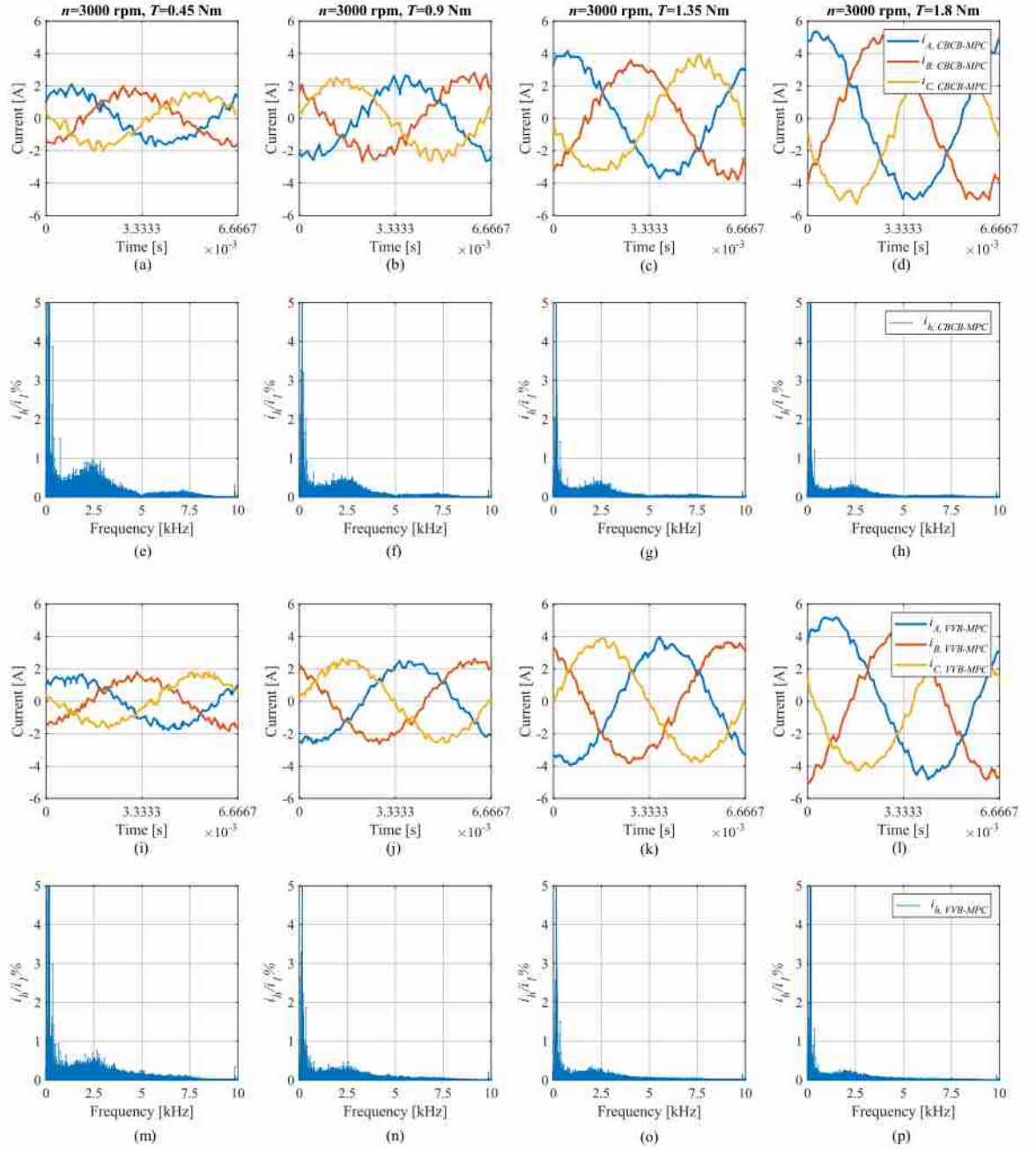


Fig. III. 13: Analysis for fixed speed (3000 rpm), varying the load torque over the defined working range: (a-d) CBCB-MPC phase currents, (e-h) CBCB-MPC phase current spectra, (i-l) V²B-MPC phase currents, (m-p) V²B-MPC phase current spectra.

Comparing CBCB-MPC and V²B-MPC current spectra, it can be noted that also, in this case, V²B-MPC guarantees a lower harmonic content over the entire working range, although the difference is less marked, if compared with voltage spectra: the worst case takes place when speed is equal to 200 rpm and the low-frequency harmonics reach the maximum value of 4% and 3 % when CBCB and V²B-MPC are considered, respectively.

In Fig. III. 14 (a) and (b) the optimal phase voltage, expressed in p.u., and related GCSs with respect to the phase A generated by the CBCB-MPC and V²B-MPC, respectively, are shown. These signals are generated by the respective MPC strategies in the sbRIO 9651 controller, acquisition is carried out with the control sampling period of 100 μ s with the motor speed $n=3000$ rpm at no-load working conditions. It can be noted that, when V²B-MPC is adopted, it is possible to identify a pattern in the GCSs trend. Such a pattern is typical of LS-PWM strategies. Indeed, according to Fig. I. 27 and Fig. I. 28 reported in Section I.9, each cascaded HB module in a phase starts switching only when the modulating signals start intersecting the couple of carriers assigned to that specific HB module. On the contrary, the CBCB-MPC determines a much more chaotic GCSs trend, which is reflected in a higher voltage and current harmonic content. However, looking at both voltage trends, it is easy to see that constraints on the phase voltage dv/dt summarized in (III,30), and GCSs constraints summarized in Fig. III. 4 (c) and Fig. III. 8 for V²B-MPC and CBCB-MPC respectively, are fulfilled.

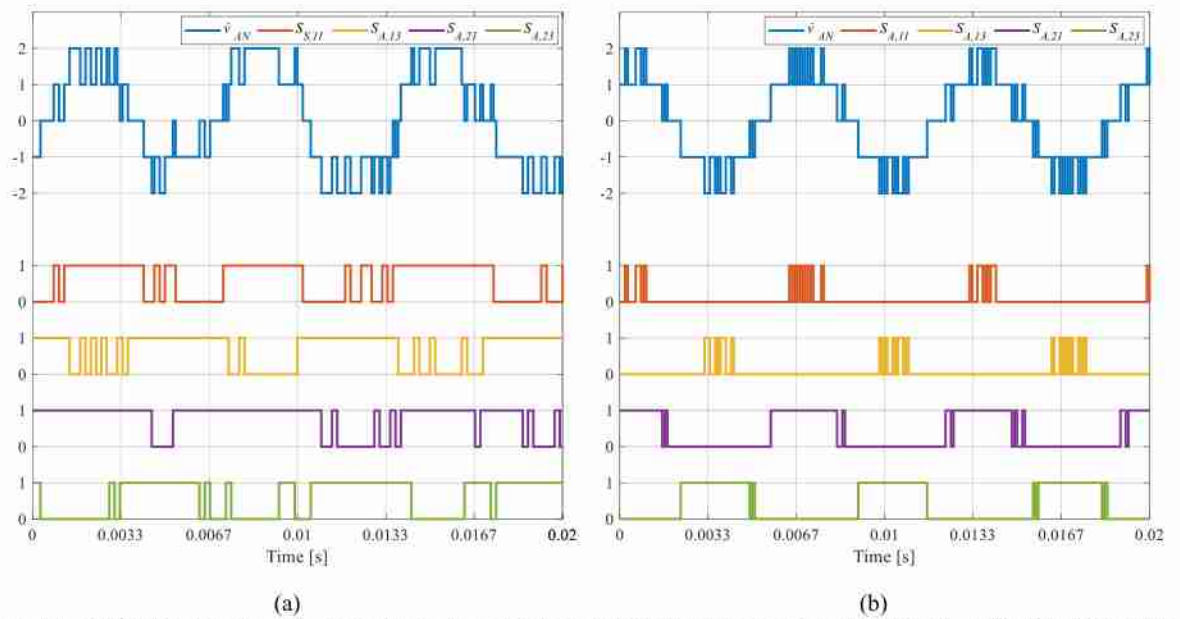


Fig. III. 14: Optimal phase voltage expressed in p.u. and related GCSs with respect to the phase A, (a) CBCB-MPC, (b) V²B-MPC.

The apparent switching frequency f_{sw} over the defined working range for the CBCB-MPC and the V²B-MPC are reported in Fig. III. 15 (a) and (e), respectively. Switching frequency

estimation has been carried out by counting the phase voltage level transitions N_t over the observation window and dividing by double the observation window T_w , according to equation (III,42):

$$f_{sw} = \frac{N_t}{2T_w} \quad (\text{III,42})$$

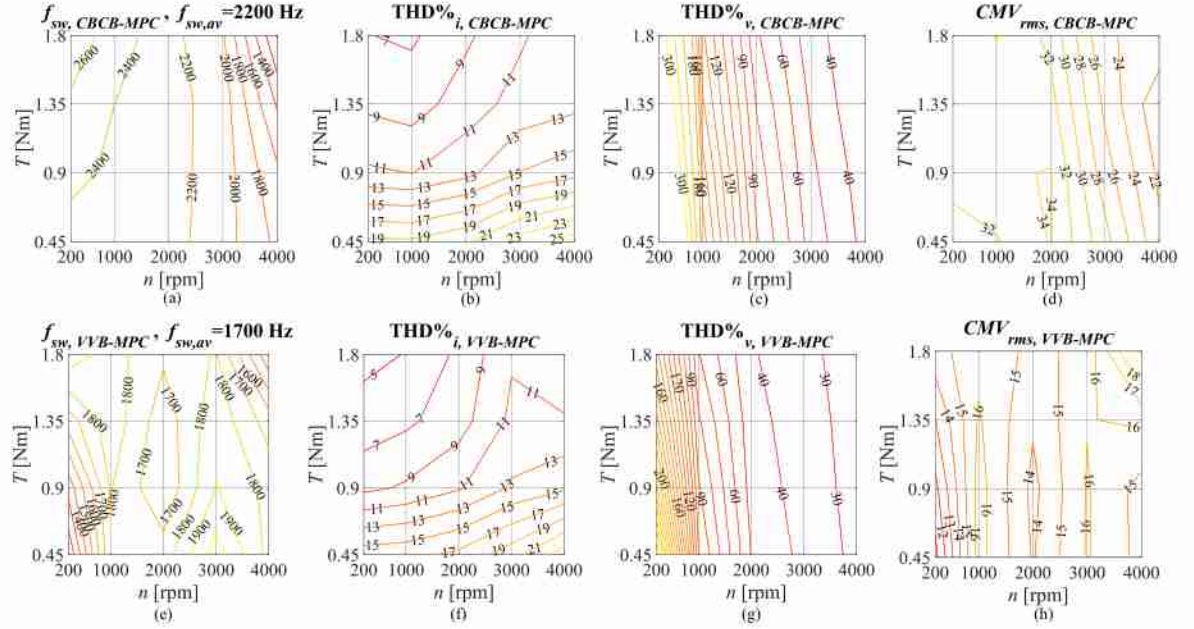


Fig. III. 15: Comparison tools: (a) CBCB-MPC apparent switching frequency, (b) CBCB-MPC current THD, (c) CBCB-MPC voltage THD, (d) CBCB-MPC CMV rms value, (e) VVB-MPC apparent switching frequency, (f) VVB-MPC current THD, (g) VVB-MPC voltage THD, (h) VVB-MPC CMV rms value.

It can be noted that, in the considered working range, the apparent switching frequency varies from 1800 to 2600 Hz with an average apparent switching frequency equal to 2200 Hz when CBCB-MPC is adopted. Instead, the apparent switching frequency varies from 1400 to 1900 Hz with an average apparent switching frequency equal to 1700 Hz when V²B-MPC is adopted. It must be underlined that V²B-MPC guarantees at the same time a lower switching frequency and a better voltage and current harmonic content over the entire working range if compared to the CBCB-MPC. This behaviour is confirmed by the current and voltage THD maps over the adopted working range, reported in Fig. III. 15 (b-c) and Fig. III. 15 (f-g). In detail, it can be noted that the current THD varies in the range of 7-25% and 5-21% when CBCB-MPC and V²B-MPC are adopted, respectively. In both cases, for a fixed speed, the THD drastically decreases when the load torque increases. This behaviour is correlated with an increment of the fundamental frequency. Moreover, it can be noted a correlation between the current THD and the speed, such that the THD slowly increases when the speed increases. This behaviour can be justified by a progressive decrement in the switching frequency when the speed increases. About the voltage THD, it varies in the range of 40-300% and 30-200%, respectively. It can be noted that the THD variation is strictly correlated

to the speed. In detail, when the speed increases, the THD decreases. Moreover, the voltage THD is quite independent of the load torque.

The CMV rms value over the defined working range is reported in Fig. III. 15 (d) and Fig. III. 15 (h), for CBCB and V²B-MPC, respectively. In detail, it can be noted that the CMV rms value over the defined working range is always quite low and the voltage variation over the working range is quite small, 12–18 V, when V²B-MPC is adopted. This analysis confirms that the goal of minimizing the common mode voltage with V²B-MPC has been fulfilled. Moreover, the CMV harmonic content results to be quite independent of the working range. Concerning CBCB-MPC, voltage variation over the working range is 22–32 V, thus, CMV rms values are higher than V²B-MPC over the entire working range, as was expected.

III.7.2 Comparison in Dynamic Working Conditions

In Fig. III. 16, a comparison between the electric drive dynamic behaviour obtained with the two compared strategies is reported. In detail, IPMSM phase voltages, phase currents, speed, and load torque trends during the whole dynamic cycle are reported in Fig. III. 16 (a) and (b), respectively. It is interesting to note that, in both cases, the currents reach the reference values in about 2 ms with a negligible overshoot. The speed transient ends in about 500 ms with about 200 rpm overshoot. The system exhibits also a good rejection of external disturbances, as can be seen when the load torque is applied and next removed. In detail, the speed transient due to the external disturbance ends in about 0.3s.

Fig. III. 17 (a) and (b) show the current trends both in the *ABC* and *dq* reference frames, obtained with CBCB-MPC and V²B-MPC respectively, during a 0-2000 rpm acceleration at no load conditions. In Fig. III. 17 (c), a direct comparison among previously mentioned current trends in the *dq* reference frame is reported. Such trends are sampled through the control board with a sampling frequency equal to the control frequency of 10 kHz. Step response comparison shows no relevant differences among compared MPC strategies. In detail, considering the V²B-MPC the strongly reduced subset of VVs to investigate during transients determines a short overshoot and a few oscillations before reaching the set point of 10 A. With regard to the CBCB-MPC, although the *q*-current reaches the set point slightly faster than the V²B-MPC and with a lower overshoot, it is characterized by a non-negligible current ripple.

The reported trends allow for stating that both algorithms guarantee comparable dynamic performance and no remarkable differences in the must be underlined.

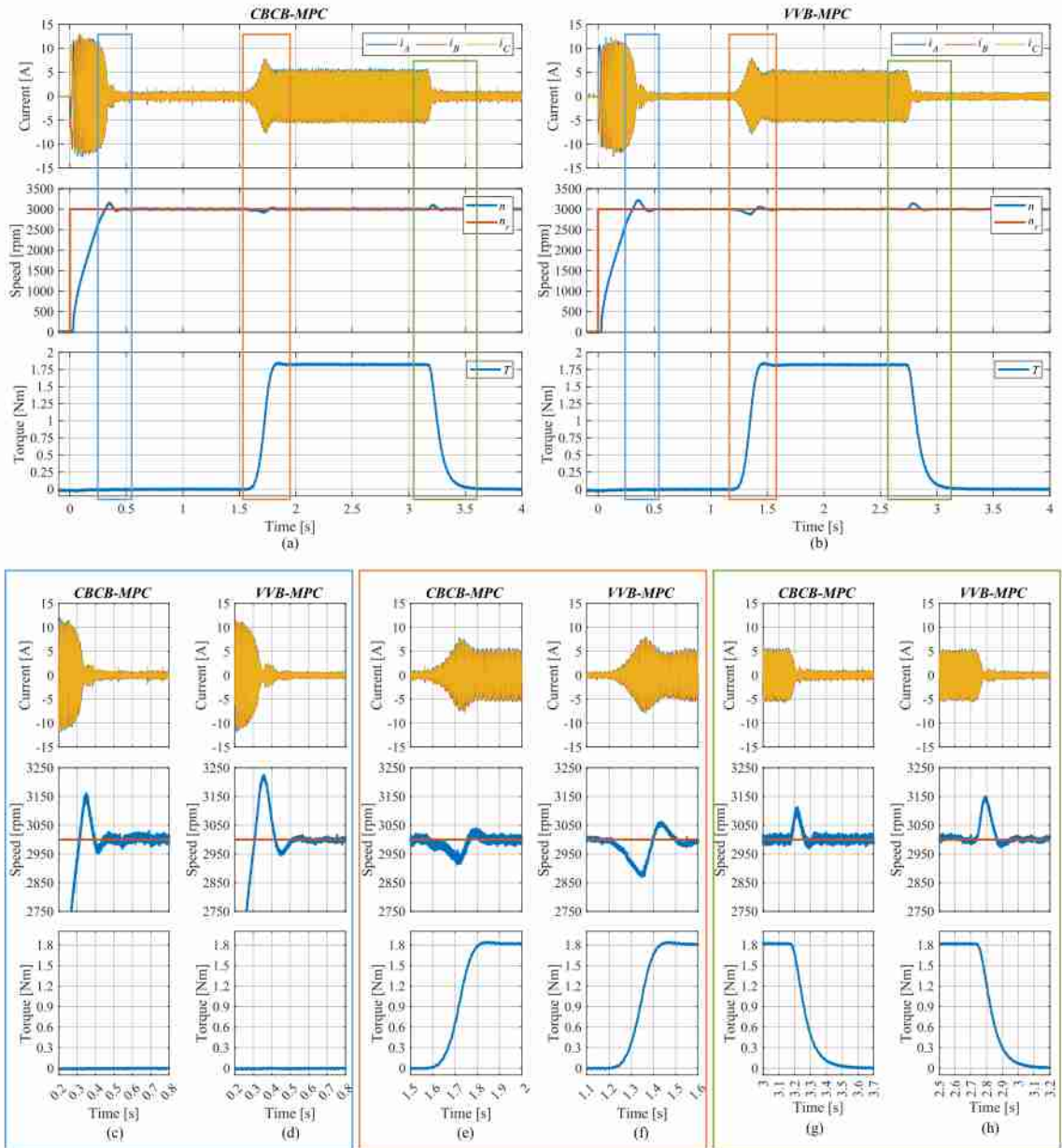
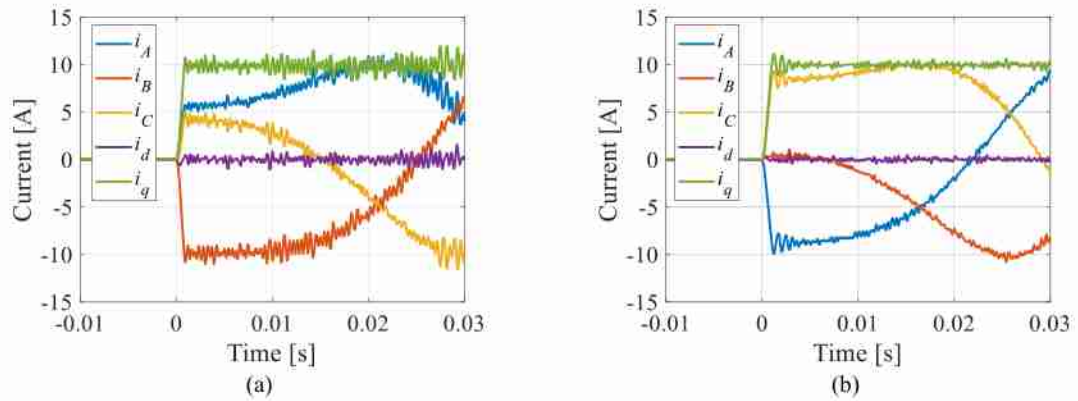


Fig. III. 16: Comparison between electric drive dynamic behaviour under a 0-3000 rpm acceleration and load torque variation: (a) CBCB-MPC , (b) V²B-MPC, (c-d) zoom on acceleration, (e-f) zoom on load torque application, (g-h) zoom on load torque exclusion.



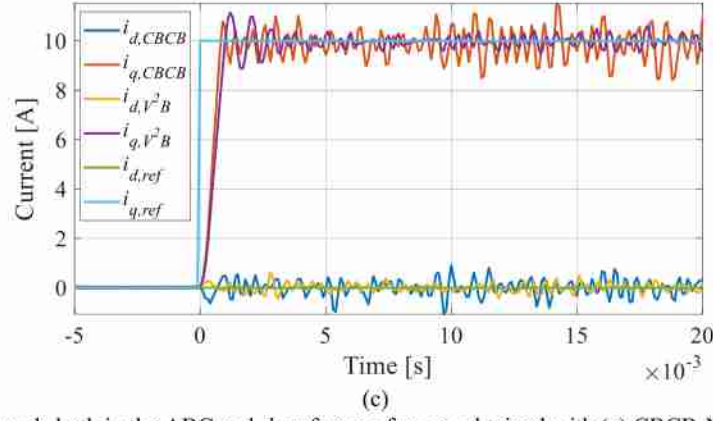
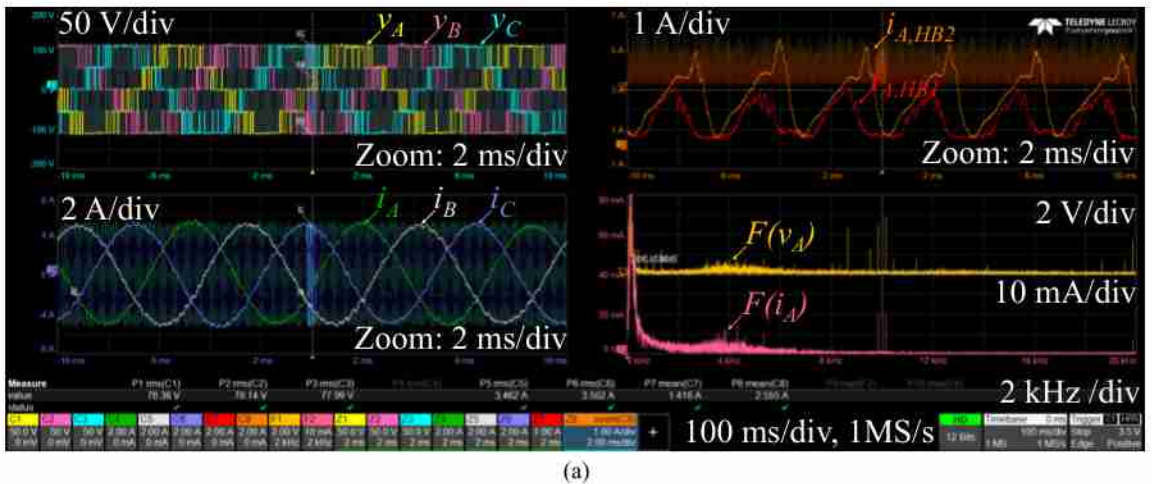
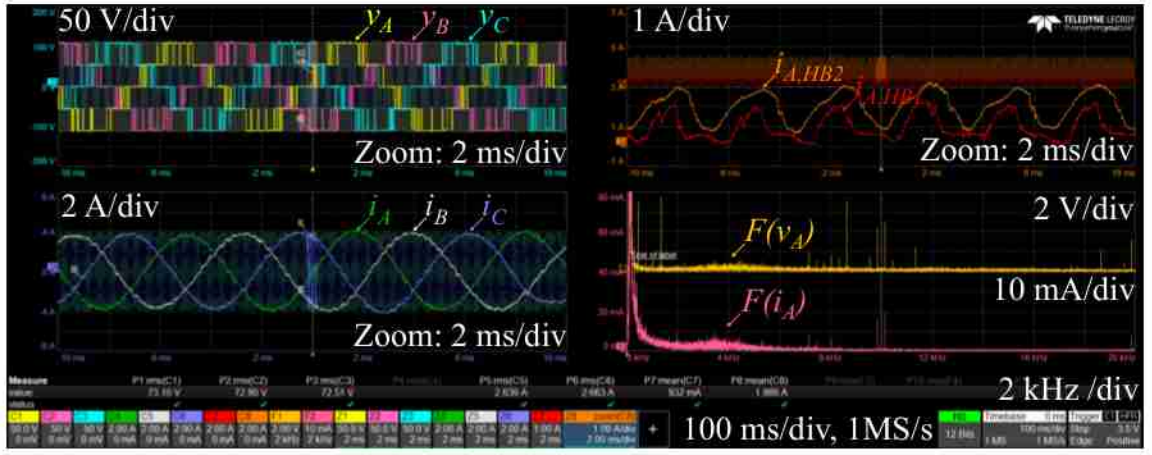


Fig. III. 17: Current trends both in the ABC and dq reference frames, obtained with (a) CBCB-MPC, and (b) V²B-MPC. (c) CBCB-MPC and V²B-MPC current trends comparison in the dq reference frame.

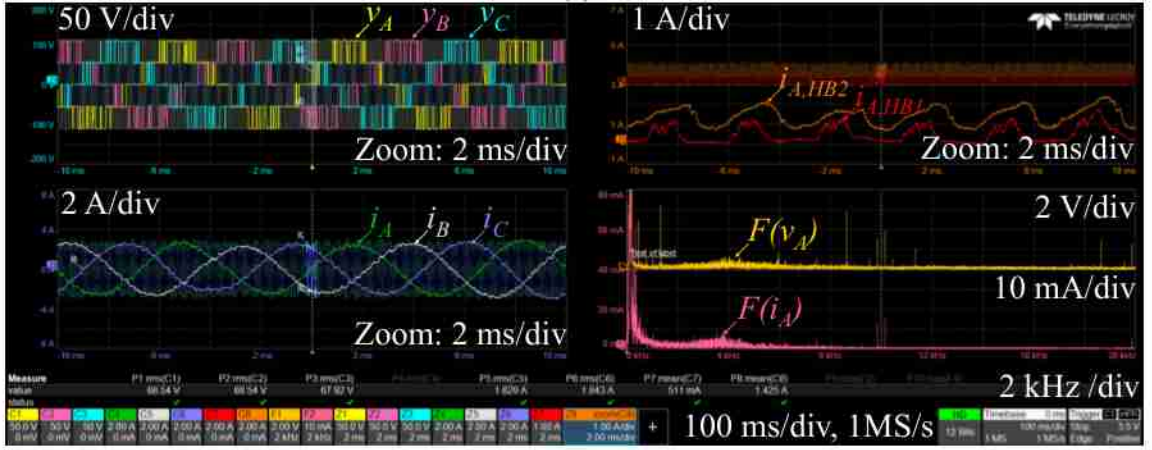
III.8 Similarities Between V²B-MPC and LS-PWM Strategies

As discussed in the previous section, V²B-MPC exhibits very good steady-state performance, guaranteeing quite low voltage and current THD and at the same time a very low switching frequency, overperforming the CBCB-MPC. Comparison among CBCB and V²B-MPC algorithms in terms of electric drive dynamic performance showed a comparable behaviour. Now, attention is paid to the CHB DC side. As a way of example, Fig. III. 18 shows some oscilloscope screens of CHB-fed IPMSM phase voltages, phase currents, related spectra, and a couple of DC currents related to SMs of phase A ($i_{A,HB1}$ and $i_{A,HB2}$), when speed $n=3000$ rpm, and the load torque T is varied over the previously defined working range. Tests are carried out by maximizing the control algorithm sampling frequency, compatible with its execution time. Then, a sampling frequency of 40 kHz is adopted. It can be noted that the V²B-MPC strategy determines an inhomogeneous DC currents absorption among the cascaded SMs over the entire working range. Indeed, DC current trends are not superimposed and present a different average value; moreover, when the load torque is lower or equal to 0.9 Nm, DC current related to the upper SM is different than zero only for a fraction of the current period.

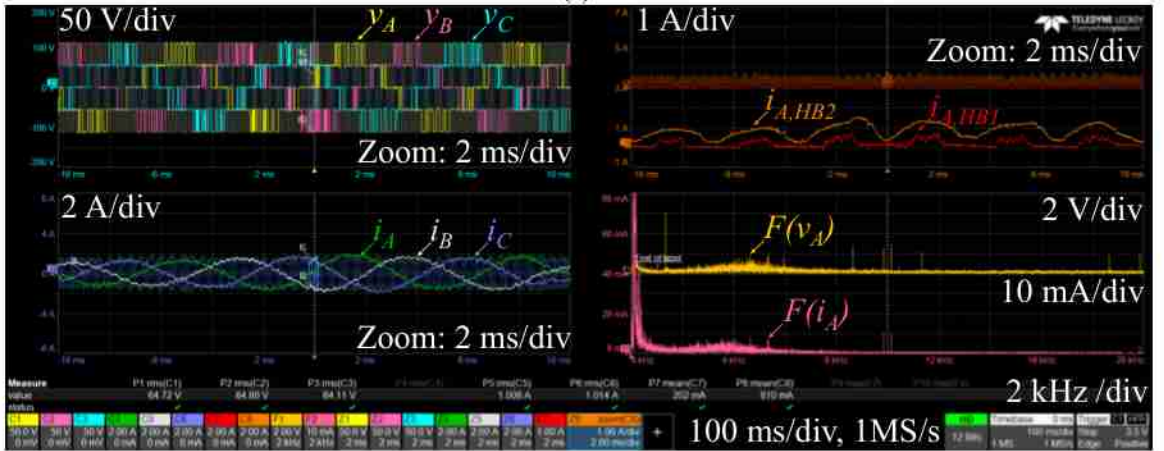




(b)



(c)



(d)

Fig. III. 18: Oscilloscope screens showing phase voltages, phase currents, related spectra, and DC sub-modules currents related to phase A, generated with V²B-MPC when speed $n = 3000$ rpm and varying the load torque over the defined working range (a) $T = 1.8$ Nm, (b) $T = 1.35$ Nm, (c) $T = 0.9$ Nm, (d) $T = 0.45$ Nm.

Such considerations are carried out by looking at the DC currents of phase A, however, they are also valid for phases B and C. Such behaviour is correlated to the adopted control goals that led to the discussed offline optimization process. Indeed, the minimization of the phase voltage dv/dt and GCSs transitions impose to the CHB inverter a switching behaviour that is very similar to that generated by an LS-PWM modulation stage, as can be noted by looking at the GCSs reported in Fig. III. 14 (b). In detail, according to the discussion on MC-PWM strategies carried out in Chapter I, LS-PWM strategies modulation schemes are characterized

by stacked carriers such that over a T_{PWM} only one HB leg per phase changes its state, depending on what carrier is intersected by the modulating signal. Moreover, when the modulating signal exceeds the inner carriers amplitude (T_2 and T_3 according to the carriers nomenclature adopted in Chapter I), HB controlled by the inner carriers remains in a conduction state until the modulating signal amplitude is decreased again and a new intersection with T_2 and T_3 occurs. This behaviour is shown in Fig. III. 19 (a) and (b) for modulating signal $u(k)$ higher and lower than 0.5, respectively.

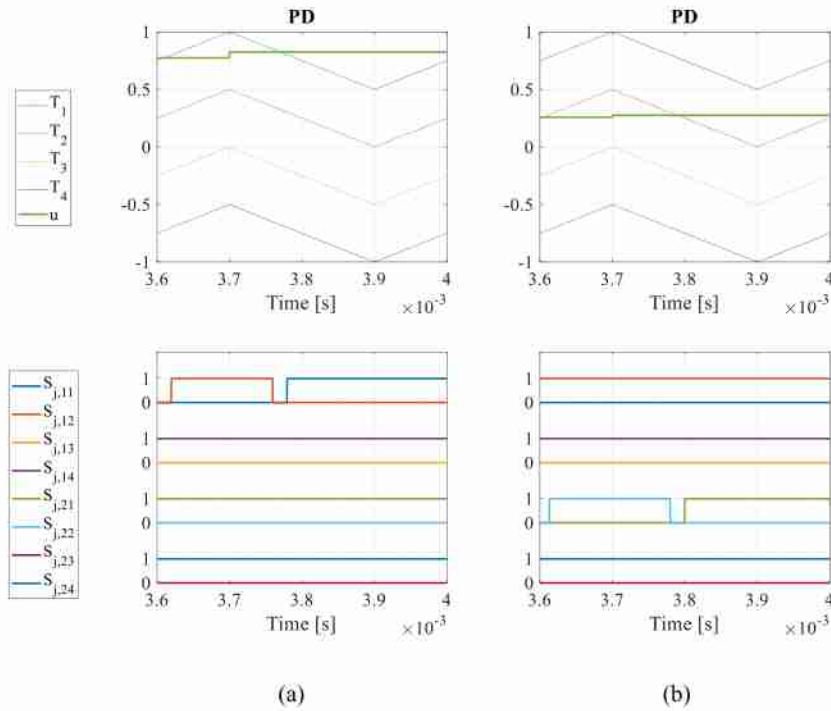


Fig. III. 19: PD-PWM modulation scheme and GCSs related to the generic phase j , (a) $u(k) > 0.5$, (b) $u(k) < 0.5$.

As a consequence, the two cascaded HB in a phase drive a different amount of power to the load, as demonstrated in Fig. I.19, where it is highlighted that when the amplitude modulation index M is lower than 0.5 one of the two cascaded HBs is not driving power to the load at all.

Concerning the V^2B -MPC strategy, this behavior is more pronounced the more the electric drive is operated at low-speed working points, as illustrated in Fig. III. 20, where optimal phase voltage and related GCSs for the phase A are shown when the speed is varied over the defined range. Indeed, at low speed, one of the two cascaded HBs is not switching at all, confirming the strong correlation with the LS.PWM strategies.

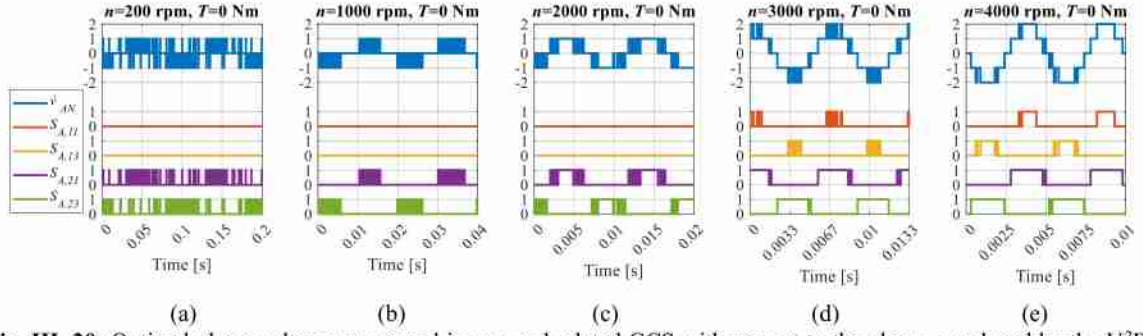


Fig. III. 20: Optimal phase voltages expressed in p.u. and related GCS with respect to the phase α , produced by the V²B-MPC algorithm at no-load conditions, (a) $n=200$ rpm, (b) $n=1000$ rpm, (c) $n=2000$ rpm, (d) $n=3000$ rpm, (e) $n=4000$ rpm.

III.9 Split Space Vector-Based MPC for DC Power Balancing

Main control goals related to CHB-based drives deal with the current reference tracking, converter switching loss minimization, CMV minimization, and CHB SMs power balancing. The latter represents a critical control goal, since it affects both the converter and the DC sources, in terms of efficiency and reliability. In detail, by assuming that each SM is characterized by the same DC link voltage, the fact that each SM drives a different amount of power to the load implies that SMs are interested in different currents and are switching differently. Thus, each SM is interested in different conduction and switching losses. It follows that more stressed SMs will age prematurely and will be more likely to fail, reducing the converter lifetime. Moreover, depending on the applications, driving a different amount of power by each DC link could be undesirable, such as when a Battery Energy Storage System (BESS) is adopted [III,20]-[III,21].

As it has been proven in Section I.8, PS-PWM allows for overcoming this issue, guaranteeing SMs power balancing in every working condition. Indeed, it is based on carriers phase shift, which allows for each carrier to be related to a particular and independent SM. The phase shift among carriers implies that all SMs in a phase follow the same switching pattern with a certain time delay. Moreover, adopting a proper carriers phase shift allows for shifting the voltage harmonics over the spectrum $2n_{HB}$ -times the carriers frequency. It follows that PS-PWM represents the natural choice for the implementation of a CHB control strategy where a modulator must be adopted.

By looking at the scientific literature, it can be noted that, when MPC is employed, not always appropriate attention is paid to the SMs power balancing goal. Moreover, the most common approaches to face this problem deal with the adoption of a PS-PWM-based CCS-MPC, which guarantees the SMs power balancing thanks to the modulator stage, or, when the FCS-MPC is adopted, by introducing into the cost function one or more quadratic custom terms, which try to equalize the SMs power. However, the PS-PWM-based CCS-MPC

solution determines poor dynamic performance, if compared to the FCS-MPC, due to the control delay introduced by the PWM modulator stage; the custom cost function terms of FCS-MPC implies measuring DC voltages and/or DC currents and tuning the cost function weighting factor, which is a tedious trial-and-error activity and can affect the system performance, according to [III,7].

In order to overcome the limits of V²B-MPC discussed in the previous section, a novel Split Space Vector-Based (S²VB) FCS-MPC (named S²VB-MPC) for a 3P-5L-CHB-fed IPMSM drive is proposed. The key novelty of this work deals with the fact that the proposed control allows for guaranteeing CHB SMs power balancing in every working condition without any modulation stage or dedicated terms into the cost function. Such a goal is reached by emulating the PS-PWM strategy switching pattern. With this aim, the 3P-5L-CHB inverter is considered as two cascaded-connected 3P-3L-CHBs, or, in other words, as two SMs triplets, where a triplet consists of three SMs, one per each phase. Such an assumption allows for splitting the 3P-5L-CHB output VV into two VVs, each of which regards a specific SMs triplet. The SMs power balancing is guaranteed by the PS-PWM strategy emulation, i.e., one of the two triplets replicates the switching pattern of the other triplet with a sample time delay. In detail, the triplet that imposes the switching pattern is named Master Triplet (MT), and the triplet that replicates the switching pattern with such a time delay is called Slave Triplet (ST).

III.10 S²VB-MPC Mathematical Formulation

The starting point for the proposed strategy formulation is represented by the PS-PWM modulation strategy, whose modulation scheme is reported in Fig. III. 21. Its main features have been deeply discussed in Section I.3. Now, attention is focused on its digital implementation, which plays a vital role in determining the multilevel inverter performance, both in steady state and dynamic working conditions. For this application, the standard multisampling method described in [III,22] is considered. It deals with dividing the carriers period T_{PWM} into $2n_{HB}$ intervals such that the state variables are sampled when each carrier reaches its maximum value. Thus, the sampling period T_s is related to the carries period T_{PWM} by the relation:

$$T_s = \frac{T_{PWM}}{2n_{HB}} \quad (III,43)$$

For a 3P-5L-CHB inverter, the sampling time T_s is 4 times lower than the carriers period T_{PWM} , as can be seen in Fig. III. 21 (a).

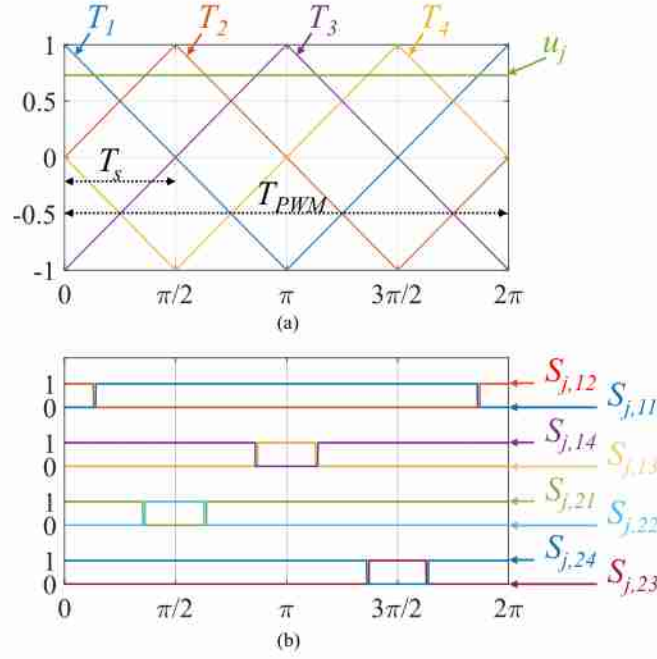


Fig. III. 21: PS-PWM modulation scheme.

Taking into account that the carriers period T_{PWM} is much lower than the modulating signals period, it can be assumed that the modulating signal variations over the T_{PWM} are negligible in steady-state working conditions. Indeed, this hypothesis is also justified by considering that the modulating signal is constant over the entire carriers period T_{PWM} when the standard single-sampling approach is adopted [III,22]. Comparing carriers and modulating signals, the GCSs reported in Fig. III. 21 (b) are generated. The previous assumption allows for stating that the GCSs related to two cascaded SMs are identical and $\pi/2$ displaced. It follows that two cascaded SMs controlled with a PS-PWM strategy follow the same switching pattern with a certain time delay, which coincides with the sampling period T_s . This behaviour guarantees both the SMs to switch the same number of times and, as a consequence, to drive the same amount of power to the load.

Once the PS-PWM key element, i.e., the SMs switching pattern, is identified, to impose this behaviour on the CHB inverter, the VV splitting mathematical formulation must be carried out. Splitting the CHB output VV allows for imposing some switching constraints such that the PS-PWM behaviour is replicated.

First, the 3P-5L CHB available VVs in the $\alpha\beta$ reference frame are considered, through relations (III,25) and (III,26). Taking into account the CHB model, it is possible to rewrite the equation (III,16) explicating the dependency of v_{jN} by the cascaded SMs voltages $v_{j,HB1}$ and $v_{j,HB2}$, as follows:

$$v_{jN} = v_{j,HB1} + v_{j,HB2} \quad (\text{III,44})$$

where:

$$v_{j,HB1} = V_{dc} (S_{j,11} - S_{j,13}) \quad (III,45)$$

$$v_{j,HB2} = V_{dc} (S_{j,21} - S_{j,23}) \quad (III,46)$$

By replacing (III,44) into (III,25) it is possible to express the vector $\mathbf{v}_{\alpha\beta 0}$ as a function of the SMs voltages as follows:

$$\mathbf{v}_{\alpha\beta 0} = \mathbf{T}_{\alpha\beta 0} \{ \mathbf{v}_{HB1} + \mathbf{v}_{HB2} \} \quad (III,47)$$

with $\mathbf{v}_{HB1} = [v_{A,HB1} \ v_{B,HB1} \ v_{C,HB1}]^T$, and $\mathbf{v}_{HB2} = [v_{A,HB2} \ v_{B,HB2} \ v_{C,HB2}]^T$. Distributing the product in (III,47), it follows:

$$\mathbf{v}_{\alpha\beta 0} = \mathbf{v}_{\alpha\beta 0,HB1} + \mathbf{v}_{\alpha\beta 0,HB2} \quad (III,48)$$

with $\mathbf{v}_{\alpha\beta 0,HB1} = [v_{a,HB1} \ v_{\beta,HB1} \ v_{0,HB1}]^T$, and $\mathbf{v}_{\alpha\beta 0,HB2} = [v_{a,HB2} \ v_{\beta,HB2} \ v_{0,HB2}]^T$. According to (III,48), the VVs $\mathbf{v}_{\alpha\beta}$, shown in Fig. III. 22 (a), can be expressed as the sum of $\mathbf{v}_{\alpha\beta 0,HB1}$ and $\mathbf{v}_{\alpha\beta 0,HB2}$, which represent the VVs related to the upper and lower SMs triplets, as shown in Fig. III. 22 (b).

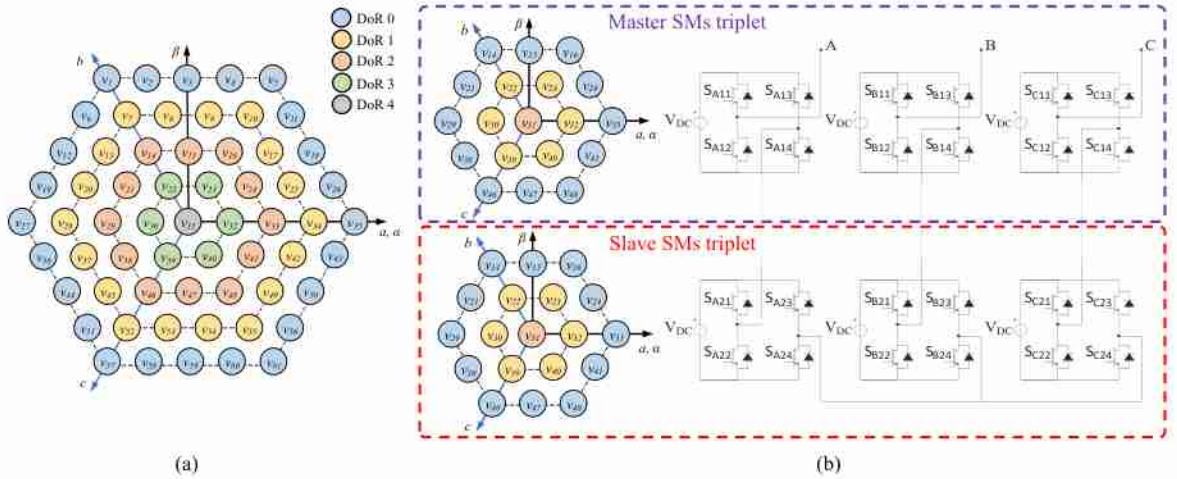


Fig. III. 22: (a) Voltage vectors on the $\alpha\beta$ plane related to the 3P-5L-CHB inverter; (b) Voltage vectors on the $\alpha\beta$ plane related to the two 3P-3L-CHBs.

Upper and lower SMs triplets can be seen as two independent 3P-3L-CHBs, each of which can produce a phase voltage $v_{j,HBx} \in \{-V_{dc}, 0, V_{dc}\}$, and, by applying (III,27) with $n=3$, a number of VVs in the $\alpha\beta$ reference frame equal to 27, of which only 19 are nonredundant. This mathematical formulation allows an easy application of switching constraints to emulate the PS-PWM strategy. For this purpose, according to Fig. III. 22 (b), the upper and lower triplets are chosen as MT and ST, respectively. Once this declaration is made, the following constraint is introduced: at the k_{th} sampling instant, the ST must replicate the MT output VV at the $k-1_{th}$ sampling instant, according to (III,49):

$$\mathbf{v}_{\alpha\beta 0,ST}(k) = \mathbf{v}_{\alpha\beta 0,MT,opt}(k-1) \quad (\text{III},49)$$

Thus, at the k_{th} sampling instant, the solution of the IQOCP deals with finding the optimal VV of the MT by taking into account the VV of the ST, which is imposed by the adopted constraint. It can be noticed that the time delay introduced with the constraint reported in (III,49) is equal to T_s and coincides with the time delay determined by the standard multisampling PS-PWM strategy, according to Fig. III. 21 (a). In other words, such a time delay related to an FCS-MPC which runs with a sampling period T_s is the same carried out by a PS-PWM-based control with a carriers period equal to $4T_s$. It must be underlined that, when FCS-MPC is adopted, GCSs are updated all at the same time, thus it is not possible to strictly replicate the PS-PWM switching pattern. However, to guarantee SMs power balancing, the critical behaviour to emulate regards the fact that both SMs per phase follow the same switching pattern (whatever it is) with a certain time delay, which must be equal to the sampling time.

Adoption of constraint (III,49) implies that the number of predictions to be carried out depends on the number of available VVs of the MT triplet, i.e. 27 VVs, whose 19 are non-redundant. Moreover, through equation (III,28) with $n=3$ and $m=3$, it follows that the number of GCSs combinations is equal to 64. In summary, constraint (III,49) not only guarantees the PS-PWM pattern emulation but also allows for considering 27 VVs (whose 19 are non-redundant), instead of 125 (whose 61 are non-redundant) and then reduces the number of required predictions from 4096 to 64.

Although the proposed algorithm guarantees a drastic reduction in the number of predictions to be performed, 64 predictions are still difficult to implement on common controllers and they can affect the maximum sampling frequency. Therefore, the same switching constraints and offline optimization process discussed in Section III.4 are adopted and properly adapted to the proposed S²VB-MPC. In detail, since the ST VV at the sampling instant k is imposed, switching constraints and selection of PVCs and GCSs must be carried out by considering only the MT VVs, which are shown in Fig. III. 22 (b). Regarding the switching constraint, the solution to the IQOCP at the k_{th} sampling instant must be found by investigating only the adjacent six MT VVs to the currently applied one, i.e., the optimal VV at the $k-1_{th}$ instant, and the previous optimal VV itself, for future state predictions. As a way of example, with respect to Fig. III. 22 (b), if the previous optimal MT VV is v_{32} , the solution to the IQOCP must be found by investigating vectors v_{24} , v_{33} , v_{41} , v_{40} , v_{31} , v_{23} , and v_{32} . Such a constraint allows for reducing the number of VVs to investigate to find the solution to the IQOPC to 7, net of the redundancies.

The optimization process deals with redundancies elimination. The redundancies are eliminated by assigning to each VV unique PVC and GCS combinations, according to the control goals discussed in Section III.4. The PVC is chosen, among the available choices for a single VV, to minimize the CMV related to such VV; the GCS combination is chosen to minimize the GCS state transitions when the system evolves from a VV to another. It can be noted that VVs related to the 3P-3L CHB represent a subset of the 3P-5L-CHB VVs, i.e., the inner VVs; thus, it is sufficient to adopt the PVCs and GCSs combination subsets proposed in Section III.4, related to the 3P-3L CHB, which are summarized in Fig. III. 23.

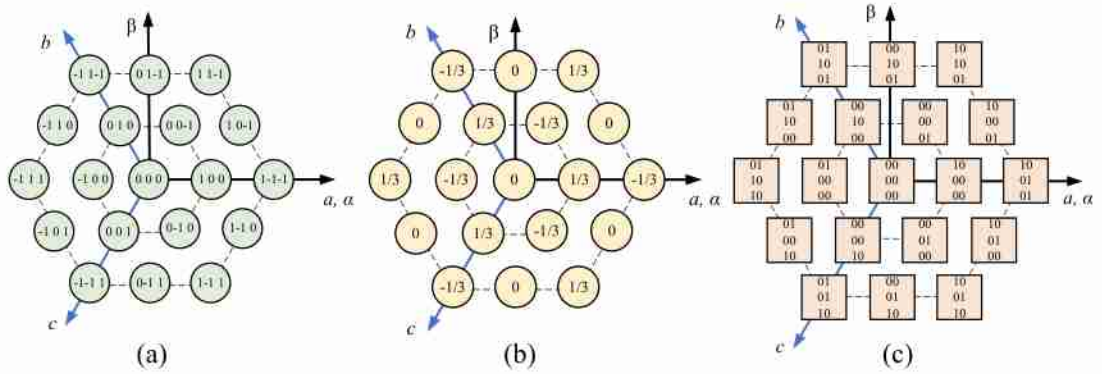


Fig. III. 23: (a) Optimal PVCs for every VV in p.u.; (b) CMV values per each VV in p.u.; (c) GCSs which minimize the switching transitions, reported on the α - β plane.

Once a unique PVCs and GCS combination is assigned to each VV, the number of required predictions goes from 64 to 7. Thus, the IQOCP is formulated as follows:

$$\begin{aligned} \mathbf{v}_{dq,opt} &= \arg \min J(\mathbf{i}_{dq}(k), \mathbf{v}_{ABC}(k)) \\ \text{subject to } &\begin{cases} \mathbf{i}_{dq}(k+1) = \mathbf{A}\mathbf{i}_{dq}(k) + \mathbf{B}\mathbf{v}_{dq}(k) + \mathbf{K} \\ \mathbf{v}_{\alpha\beta,ST}(k) = \mathbf{v}_{\alpha\beta,MT,opt}(k-1) \\ \mathbf{v}_{ABC}(k) \in \mathcal{U}(k) \end{cases} \end{aligned} \quad (\text{III},50)$$

III.11 S²VB-MPC Implementation

The proposed algorithm is summarized in Fig. III. 24. The selected sets of PVCs and GCSs related to the MT VVs are stored in two LUTs, called LUT-1 and LUT-2, respectively. Each VV is identified by a number v_x , according to Fig. 4(b); such a number represents the address to navigate the LUTs. At the sampling instant k , the set of available PVCs for the future state predictions $\mathcal{U}(k)$, which consists of the 7 MT VVs and 1 ST VV, is identified thanks to the optimal VV address at the previous sampling instant $v_{x,opt}(k-1)$. Now, the 7 state predictions are carried out sequentially through a *for* loop and the optimal MT VV, and the relative address $v_{x,opt}(k)$, are found. Addresses $v_{x,opt}(k)$ and $v_{x,opt}(k-1)$ are used to navigate the LUT₂ and find the set of optimal GCSs combination $\mathbf{S}_{opt}(k)$, which is applied to the system. It must

be underlined that adopting LUTs allows for easily defining the set of available PVCs and relative GCSs at the sampling instant k , without affecting the algorithm computational cost.

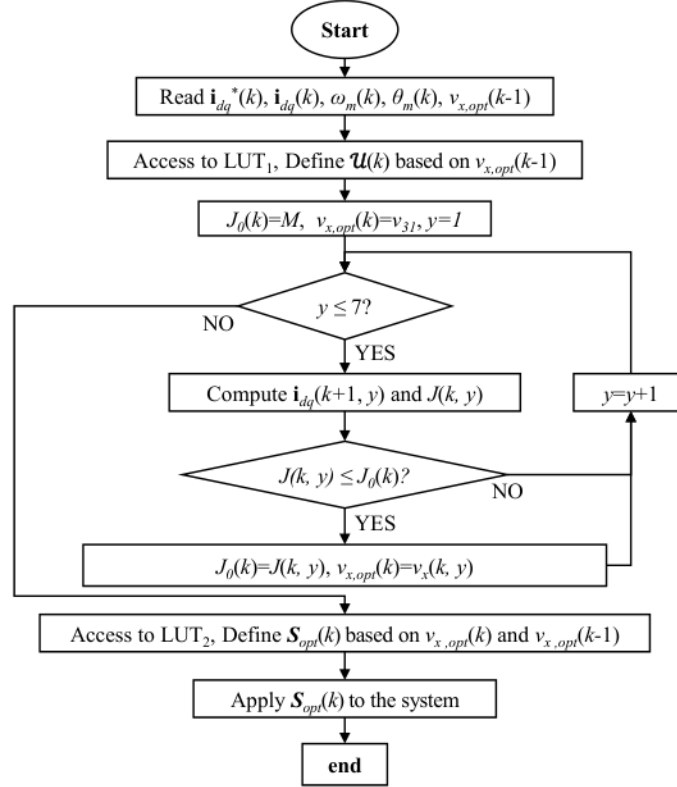


Fig. III. 24: Proposed S²VB-MPC algorithm flowchart.

The algorithm software implementation on the adopted sbRIO 9651 FPGA controller is carried out according to the discussion in Section III.5 related to the V²B-MPC. Indeed, V²B-MPC and S²VB-MPC differ only for the switching constraints (III,49) and for the elements inside LUTs 1 and 2. Then, they employ about the same amount of FPGA resources, as shown in Table III. 7, and require about the same execution time, equal to 23 μ s, to generate the optimal control action. Then, for future algorithms comparison, the adopted sampling frequency f_s in both cases is equal to 40 kHz, which corresponds to a sampling period T_s of 25 μ s. Indeed, 40 kHz represents almost the maximum available sampling frequency for these algorithms with the adopted hardware. Such a choice is carried out in order to maximize the control granularity, as discussed in Section III.2. Moreover, according to the discussion related to the time delay introduced by the constraints adopted in Section III.10, a sampling frequency equal to 40 kHz introduces a time delay between MT and ST switching patterns which is equivalent to the delay introduced by PS-PWM modulation stage with carriers frequency equal to 10 kHz.

Table III. 7: Comparison between employed computational resources on sbRIO 9651 by V²B-MPC and S²VB-MPC.

Device Utilization	Available resources	Employed resources [%]	
		V ² B-MPC	S ² VB-MPC
Total slices	13300	86.8	86.8
Slice registers	106400	26.8	26.8
Slice LUTs	53200	67.9	67.9
Block RAMs	140	7.1	7.1
DSP48s	220	88.2	88.2

III.12 S²VB-MPC Experimental Validation

In this section, experimental results are presented to validate the effectiveness of the proposed control algorithm. In detail, a comparison between the proposed S²VB-MPC and V²B-MPC is carried out, both in steady-state and dynamic working conditions. For steady-state performance analysis, the current and voltage THD%, the apparent switching frequency, the CMV rms value, and SMs DC power are adopted as performance tools. Electric drive performance are investigated in several working conditions, defined according to the standard IEC-61800-9-2 [III,23] and they are reported in Table III. 8.

Table III. 8: electric drive working points for comparison purposes.

T [Nm]- n [rpm]	200	1000	2000	3000	3600
1.8	WP5	WP4	WP3	WP2	WP1
1.35	WP10	WP9	WP8	WP7	WP6
0.9	WP15	WP14	WP13	WP12	WP11
0.45	WP20	WP19	WP18	WP17	WP16

For each identified WP, phase voltages and phase currents are measured with a Teledyne LeCroy MDA 8028HD oscilloscope, with an observation window of 1 s and a sampling frequency of 1 MS/s. With respect to the dynamic behaviour analysis, a cycle composed of a 0-3000 rpm acceleration, including no-load and rated-load operations, has been carried out. During dynamic analysis, the maximum allowed transitory currents were set to $i_q=10$ A and $i_d=0$ A, respectively. IPMSM phase voltages, phase currents, load torque applied by the brake and speed signals are acquired with MDA 8028HD oscilloscope by setting an observation window of 5 s and a sampling frequency of 500 kS/s.

III.12.1 Steady State Analysis

Firstly, attention is paid to the DC SMs currents, to prove the effectiveness of the proposed control strategy. With this aim, Fig. III. 25 shows an oscilloscope screen of phase voltages and currents, both in the time and frequency domain and DC SMs currents of phase A in WP2 (speed $n=3000$ rpm, load torque $T=1.8$ Nm), generated with S²VB-MPC. It can be noted that currents are almost superimposed.

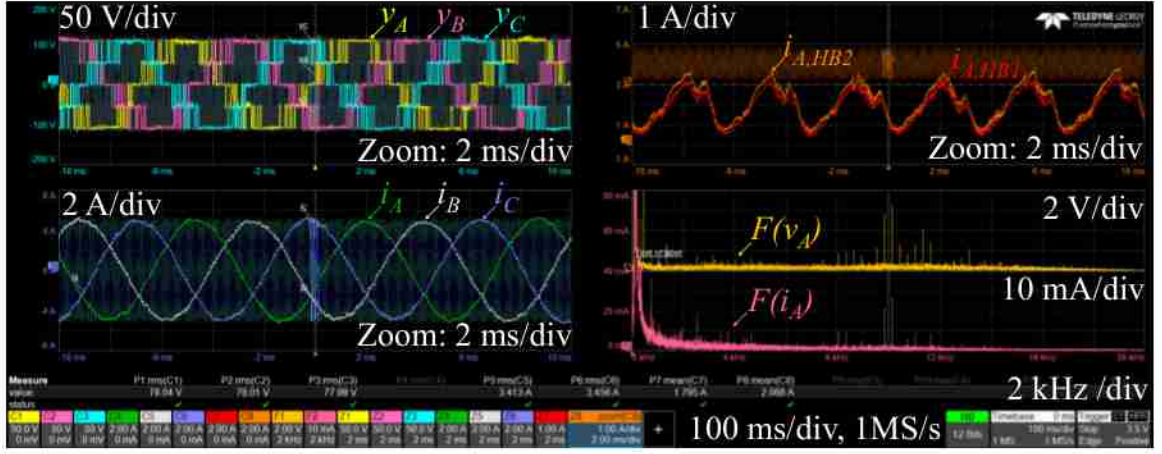


Fig. III. 25: Oscilloscope screens showing phase voltages and currents, both in time and frequency domain, and DC SMs currents of phase A, in WP2 (speed $n=3000$ rpm, load torque $T=1.8$ Nm), generated with S^2VB -MPC.

A detailed comparison in terms of AC and DC currents generated with V^2B -MPC and S^2VB -MPC in WP2, together with WPs 7, 12, and 17 are reported in Fig. III. 26. Indeed, the DC currents behaviour represents the most relevant difference between the two discussed control algorithms. The V^2B -MPC strategy determines an inhomogeneous DC currents absorption among the cascaded SMs over the entire working range. Indeed, DC current trends are not superimposed and present a different average value; moreover, when the load torque is lower or equal to 0.9 Nm, DC current related to the upper SM is different from zero only for a fraction of the current period.

On the contrary, looking at DC currents generated by S^2VB -MPC, it can be noted that trends are superimposed, both SMs conduces for the whole period and DC currents are characterized by the same average value. Such considerations are carried out by looking at the DC currents of phase A, however, they are also valid for phases B and C. Such a DC currents behaviour is equivalent to that determined by the PS-PWM modulation stage, as can be seen in Fig. III. 27. In detail, Fig. III. 27 shows the phase voltages, phase currents, and DC SMs currents related to phase A when the system is in WP 2. Such a test is carried out with a carriers frequency of 2.5 kHz, which determines an apparent switching frequency f_{sw} of 10 kHz.

Such discussion can be extended by taking into account the DC power. In detail, according to the discussion carried out in Section I.8, it is possible to define the total DC power $P_{dc,i}$ absorbed by the i^{th} triplet as in (I,39), that is reported below:

$$P_{DC,i} = P_{a,HBi} + P_{b,HBi} + P_{c,HBi} \quad (III,51)$$

Then, the DC power absorbed by the two SMs triplets $P_{DC,1}$ and $P_{DC,2}$, when V^2B -MPC and S^2VB -MPC are adopted, are reported in Fig. III. 28 (a) and (b), respectively.

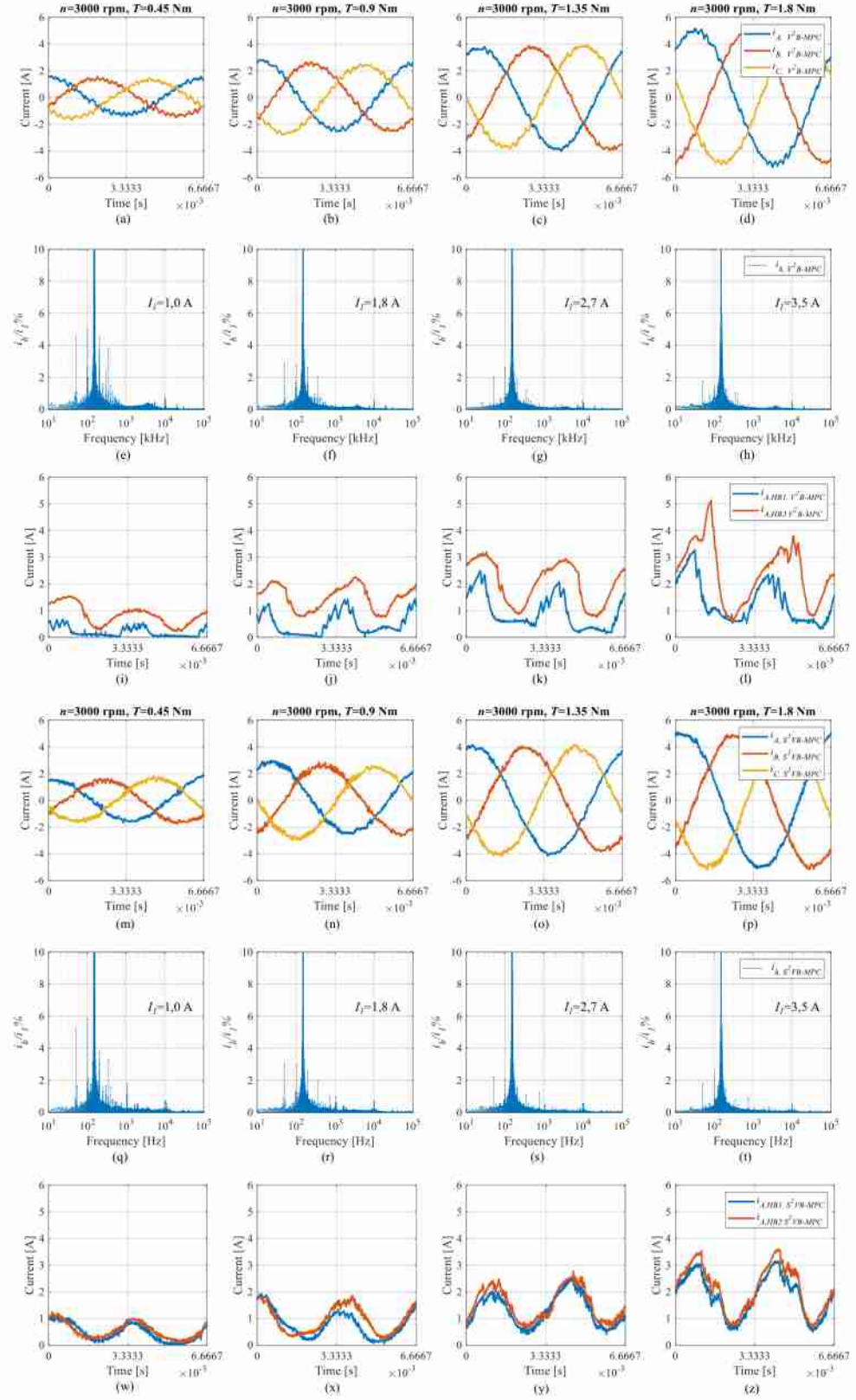


Fig. III. 26: Comparison between V²B-MPC and S²VB-MPC for fixed speed (3000 rpm), varying the load torque over the defined working range: (a-d) V²B-MPC AC phase currents, (e-h) V²B-MPC AC phase current spectra, (i-l) V²B-MPC DC SMs currents of phase A, (m-p) S²VB-MPC AC phase currents, (q-t) S²VB-MPC AC phase current spectra, (w-z) S²VB-MPC DC SMs currents of phase A.

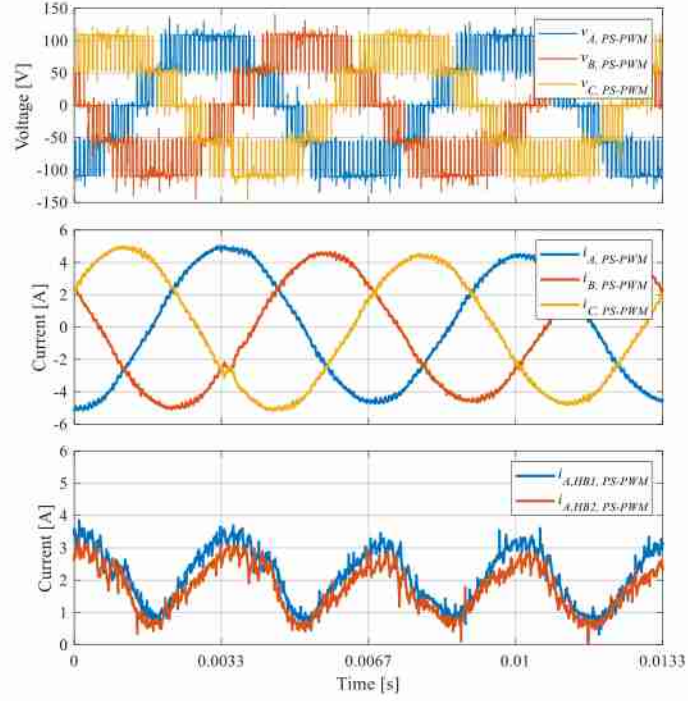


Fig. III. 27: Phase voltages, phase currents, and DC SMs currents related to phase A obtained with a PI-based FOC with PS-PWM modulator. $n_r=3000$ rpm, $T_L=1.8$ Nm, $f_{sw}=10$ kHz.

It can be noted that V^2B -MPC determines a different power absorption between the two triplets over the whole working range. Moreover, in WPs 4, 5, 9, 10, 14, 15, 19, and 20, which are characterized by low-speed working conditions, i.e., low back electromotive force, the whole power is led by only one triplet, which means that the other triplet is not switching at all. Such behaviour is the same as observed in Fig. I.19 of Section I.8 concerning the LS-PWM DC power distribution.

Such behaviour is eliminated when S^2VB -MPC is adopted. Indeed, both triplets lead the same amount of power to the load, since they are following the same switching pattern. To emphasize this aspect, the difference between the power led by the two triplets, expressed in percent with respect to the total power driven to the load, $\Delta P\%_{DC}$ is defined as:

$$\Delta P\%_{DC} = 100 \frac{|P_{DC,1} - P_{DC,2}|}{P_{DC,1} + P_{DC,2}} \quad (III,52)$$

In Fig. III. 28 (c) and (d), a comparison between $\Delta P\%_{DC}$ generated by V^2B -MPC and S^2VB -MPC is reported. When V^2B -MPC is adopted, the more the system moves toward low-speed low-torque operating conditions and the more $\Delta P\%_{DC}$ increases, reaching the value of about 100 % in low-speed operating conditions. The minimum $\Delta P\%_{DC}$ value is reached when the system works in WP1, and it is equal to 8%. When S^2VB -MPC is adopted, $\Delta P\%_{DC}$ is lower than 2% almost over the entire working range, except in WPs 10, 15, 19, and 20, where it reaches the value of 3.7%, 5.7%, 2.8%, and 5.8%, respectively.

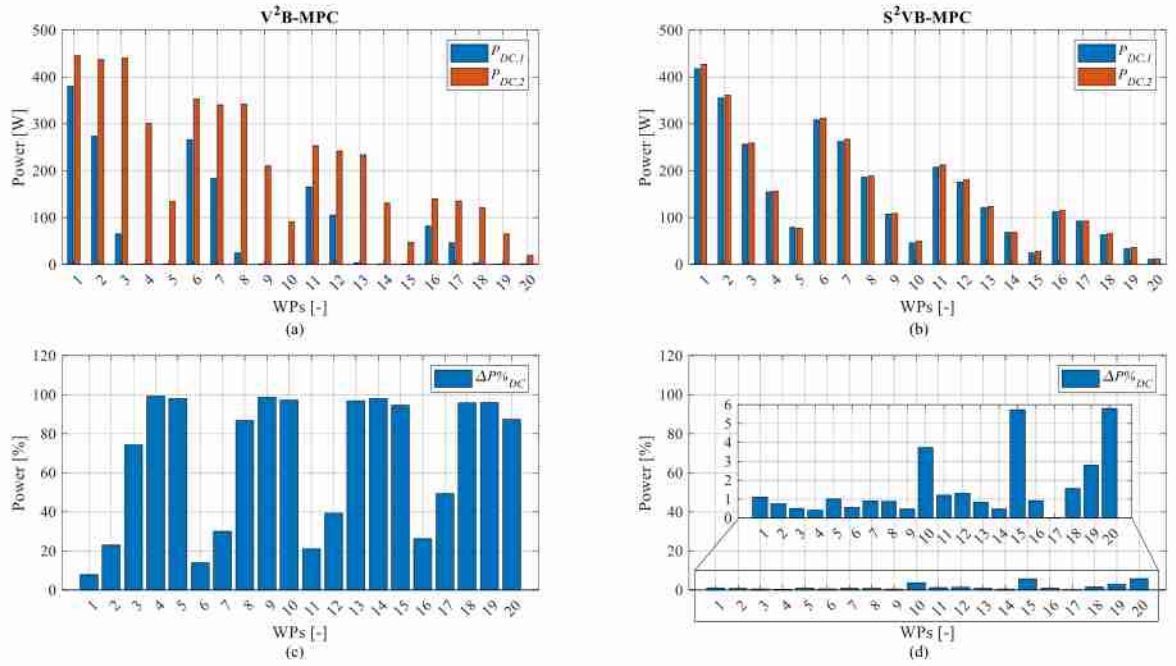


Fig. III. 28: Comparison between power led by the two triplets: (a) $P_{DC,1}$ and $P_{DC,2}$, when V^2B -MPC is adopted; (b) $P_{DC,1}$ and $P_{DC,2}$, when S^2VB -MPC is adopted; (c) $\Delta P\%_{DC}$ when V^2B -MPC is adopted; (d) $\Delta P\%_{DC}$ when S^2VB -MPC is adopted.

These results, together with results related to the DC currents shown in Fig. III. 26 and Fig. III. 27 prove the discussion in Section III.8 concerning the analogies between the V^2B -MPC and the LS-PWM strategies, and confirm that the proposed S^2VB -MPC allows for emulating the PS-PWM strategy behaviour, balancing the DC power absorption.

Looking at the electric drive behaviour on the AC side, both strategies guarantee very good and comparable steady-state performance. The current spectra reported in Fig. III. 26 highlight no significant differences in terms of harmonic content. In detail, in both cases, current spectra exhibit sub-harmonics whose amplitude goes from 6% to 2 % moving from WP2 to WP 17. Other harmonics amplitude is negligible since it is almost always lower than 1%. In Fig. III. 29, a comparison between phase voltages generated by V^2B -MPC and S^2VB -MPC strategies, both in the time and frequency domain, when the speed is varied over the defined working range and the load torque is fixed to the rated torque, is reported. In detail, it can be noted that both strategies exhibit comparable voltage spectra in every WP and the 3rd harmonic represents the predominant harmonic over the entire range. Indeed, in both strategies, it reaches a maximum value of 42% in very low-speed working conditions. However, this harmonic is not present in line-to-line voltages, nor in load voltages, due to its homopolar nature. In fact, this harmonic produces current harmonics with negligible amplitude, as can be seen in the previously shown current spectra. Even in this case, other harmonics exhibit a negligible amplitude, since they are always lower than 10% and, most of the time, lower than 5 % over the considered working range.

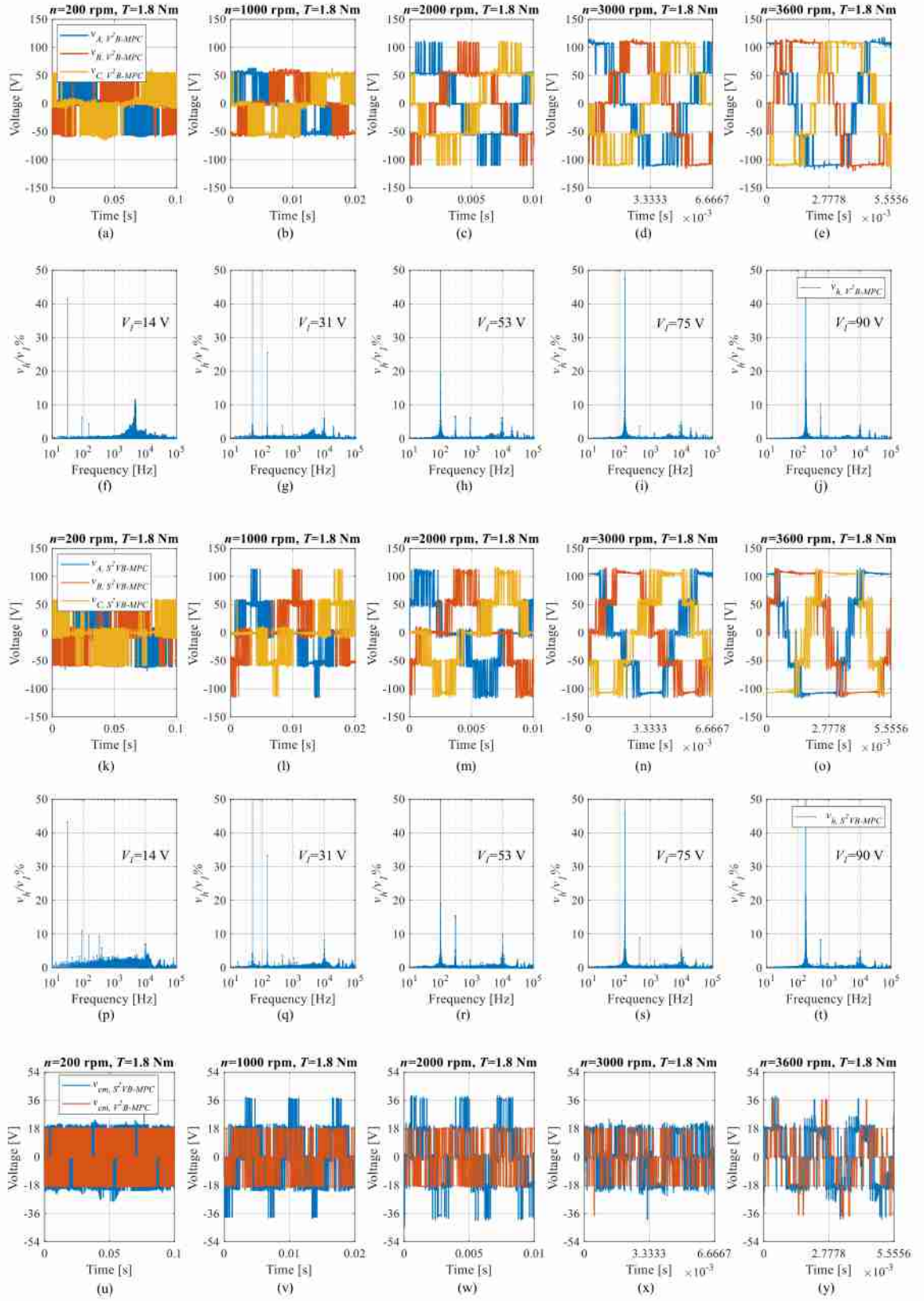


Fig. III. 29: Comparison between V²B-MPC and S²VB-MPC for fixed load torque (1.8 Nm), varying the speed over the defined working range: (a-e) V²B-MPC AC phase voltages, (f-j) V²B-MPC AC phase voltage spectra, (k-o) S²VB-MPC AC phase voltages, (p-t) S²VB-MPC AC phase voltage spectra, (u-y) V²B-MPC and S²VB-MPC CMVs.

Fig. III. 29 (u-y) shows a comparison between CMV trends determined by the two compared strategies. It can be noted that the proposed S^2VB -MPC exhibit a higher CMV peak value if compared to V^2B -MPC only when speed n is equal to 1000 rpm and 2000 rpm, where the peak value is equal to 36.6 V, i.e., the double of the V^2B -MPC. For other speed values, CMVs peak value coincides. This behaviour can be justified by looking at the optimization offline process adopted for the S^2VB -MPC. In detail, the CMV minimization goal is fulfilled concerning one SM triplet. In other words, if only one SM triplet is considered, the its contribution to the CMV is as little as possible, equal to 18.33 V ($1/3 V_{dc}$ according to Fig. III. 23. However, combining the contributions of both SM triplets, the maximum available CMV instantaneous value is equal to 36.66 V ($2/3 V_{dc}$). It must be underlined that, although the S^2VB -MPC exhibits a worst behaviour interms of CMVs in specific working conditions, the generated CMV are lower than that showed concerning the CBCB-MPC in Fig. III. 12 and can be considered acceptable since their peak value does not exceed that reached with traditional SVM and PS-PWM strategies.

To investigate the DC voltage utilization, the maximum modulation index is introduced: it is defined as the ratio between the maximum achievable phase voltage and the total DC link voltage, according to [III,24]. To compare the maximum modulation index related to V^2B -MPC and S^2VB -MPC strategies, the phase voltages in WP1 are considered. In detail, both strategies guarantee an RMS voltage of 90 V, i.e., a peak voltage of 127.3 V. Since the total DC link voltage is equal to 110 V (i.e., the sum of each cascaded SMs DC link voltage), the maximum amplitude modulation index is equal to 1.16. Therefore, both strategies guarantee optimal DC voltage utilization, i.e., the same guaranteed by a space vector modulation strategy. Moreover, it can be stated that the VV split approach does not affect the DC voltage utilization.

Looking at current THD related to the compared strategies, reported in Fig. III. 30 (a) and (e), it can be noted that both strategies determine very similar THD values in every working point. In detail, the current THD in both cases decreases when moving from high-speed to low-speed and from low-load torque to high-load torque working conditions, with a minimum value of 3.3% in WP5 and a maximum value of 20.1% in WP16.

In Fig. III. 30 (b) and (f), voltage THD maps related to V^2B -MPC and S^2VB -MPC are reported respectively. In both cases, voltage THD is strictly correlated to the motor speed, such that the voltage THD decreases when the speed increases. However, voltage THD related to V^2B -MPC decreases a bit faster than S^2VB -MPC voltage THD, reaching a minimum value of 27 %, against 31% of S^2VB -MPC voltage THD. The apparent switching

frequency maps, evaluated according to (III,42), related to the compared strategies are reported in Fig. III. 30 (c) and (g). Maps show that both strategies exhibit a switching frequency increment when the speed increases. However, S²VB-MPC is characterized by higher switching frequency over the entire range, with a minimum value of 3500 Hz to a maximum value of 6000 Hz, against a minimum value of 2000 Hz and a maximum of 4500 Hz, related to the V²B-MPC. Such a behaviour can be justified by looking at the switching constraints related to S²VB-MPC, which impose that the ST pursues the behaviour of the MT and, in turn, the MT looks for the optimal solution to apply by taking into account the future behaviour of the ST that is already defined. Thus, it is very likely that both triplets change state at each sampling instant.

In Fig. III. 30 (d) and (h), maps of CMV rms values, generated by V²B-MPC and S²VB-MPC are reported. Both maps show a strong dependency as a function of the motor speed and the most significant difference between them can be recorded in WPs where $n=2000$ rpm. In detail, in such WPs S²VB-MPC determines a rms value of CMV between 17 V and 19 V, against 13-15 V of V²B-MPC. The differences in terms of CMVs detected with the two control strategies for the other WPs are reduced and, thus, the performance can be considered comparable.

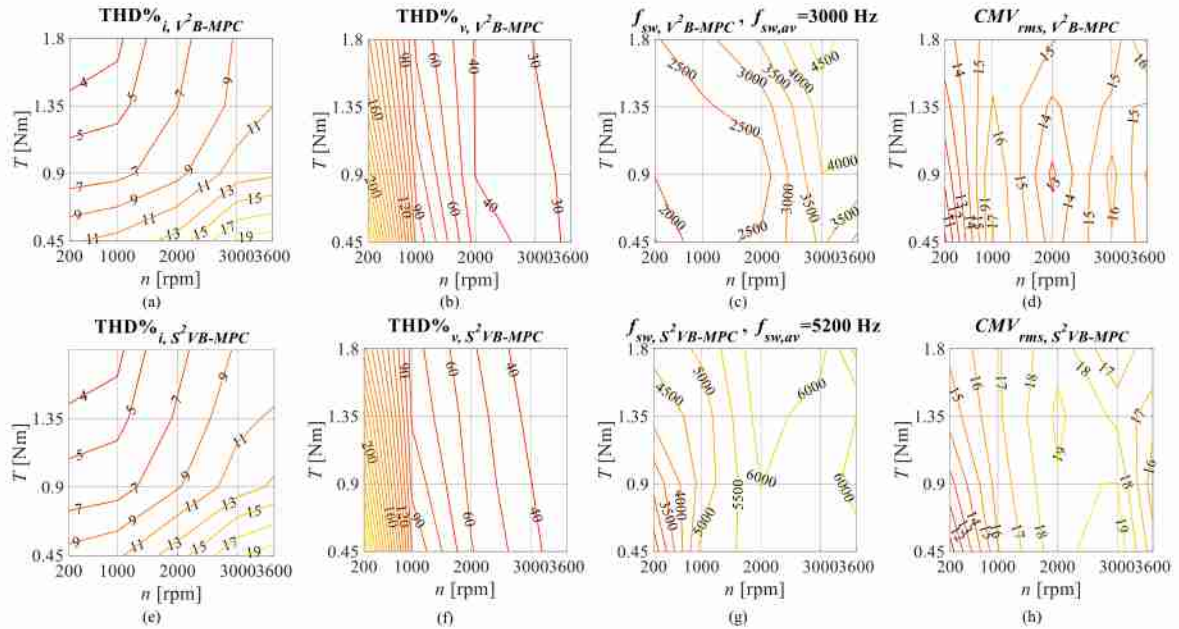


Fig. III. 30: Comparison tools: (a) V²B-MPC current THD, (b) V²B-MPC voltage THD, (c) V²B-MPC apparent switching frequency, (d) V²B-MPC CMV rms values, (e) S²VB-MPC current THD, (f) S²VB-MPC voltage THD, (g) S²VB-MPC apparent switching frequency, (h) S²VB-MPC CMV rms values.

III.12.2 Dynamic Analysis

To investigate the impact of V²B-MPC and S²VB-MPC on the electric drive dynamic performance, a cycle composed of a 0-3000 rpm acceleration, application, and removal of

rated load torque is carried out. IPMSM phase currents, speed, and load torque trends during the whole dynamic cycle are reported in Fig. III. 31 (a) and (b), when V²B-MPC and S²VB-MPC are adopted respectively.

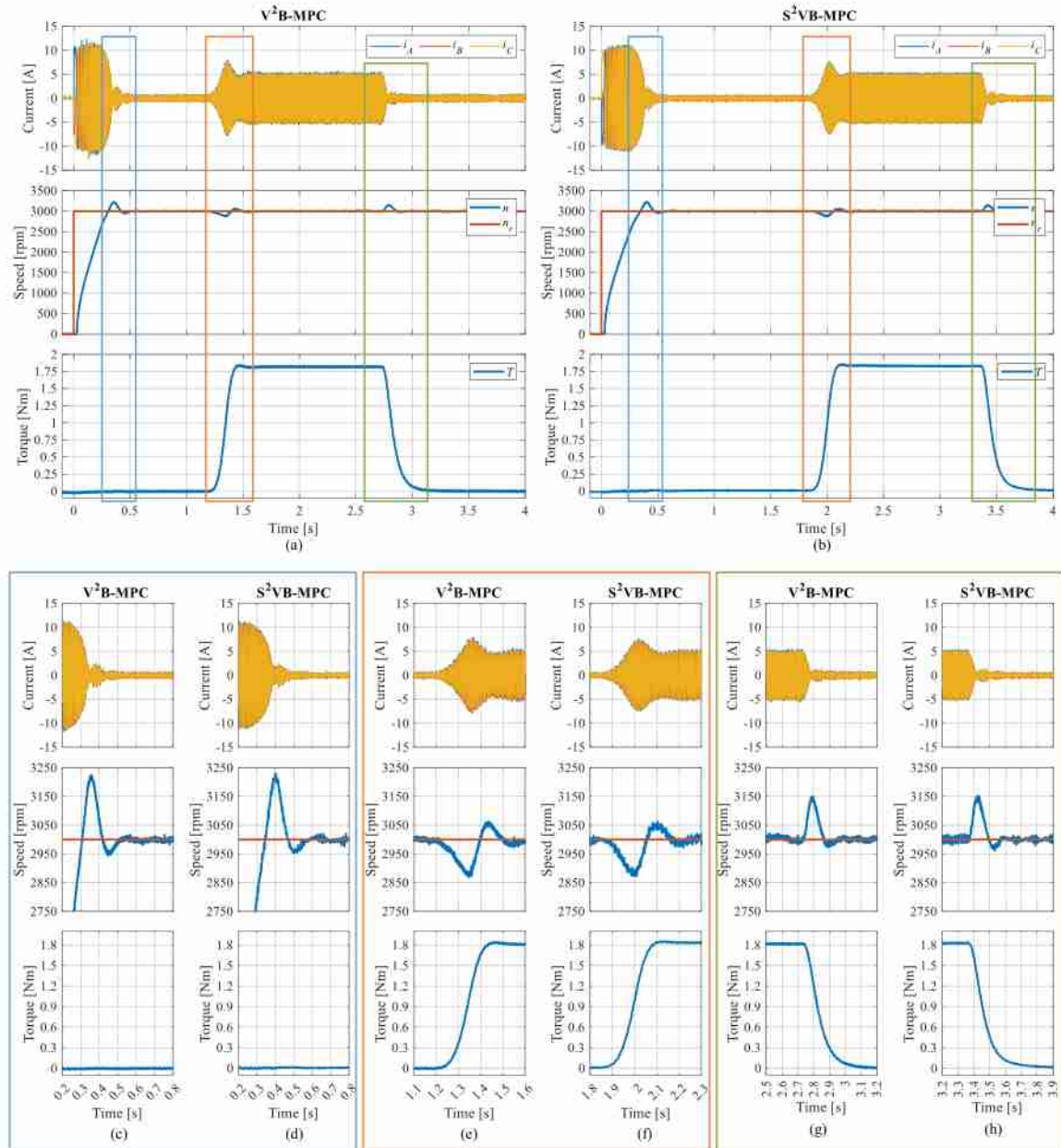


Fig. III. 31: Comparison between electric drive dynamic behaviour under a 0-3000 rpm acceleration and load torque variation: (a) V²B-MPC , (b) S²VB-MPC, (c-d) zoom on acceleration, (e-f) zoom on load torque application, (g-h) zoom on load torque exclusion.

Couples of figures Fig. III. 31 (c) and (d), Fig. III. 31 (e) and (f), and Fig. III. 31 (g) and (h) allow for carrying out a detailed comparison between currents and speed trends. It can be noted by looking at Fig. III. 31 (c) and (d) that in both cases the speed transient ends after about 500 ms with about 200 rpm overshoot. The system exhibits also a good rejection of external disturbances, as can be seen in Fig. III. 31 (e) and (f), and Fig. III. 31 (g) and (h), where the load torque application and removal are shown, respectively. In detail, in both

cases, the speed transient due to the external disturbance ends in about 0.3 s. As a result, the adoption of V²B-MPC or S²VB-MPC has a negligible impact on system dynamic performance: both algorithms guarantee good dynamic performance, with a reduced speed and torque ripple. Thus no remarkable differences in the dynamic response have to be underlined.

III.13 Weighting Factor Impact on Steady-State and Dynamic Performance

In this section, the impact on the steady-state and dynamic working conditions of the weighting factor λ_u is reported. In detail, regarding the steady-state analysis, the CHB-fed IPMSM drive is analyzed only in WP2 ($n=3000$ rpm, $T=1.8$ Nm) and the weighting factor λ_u is varied over the range $0 - 9.36 \cdot 10^{-5}$ with a step of $2.6 \cdot 10^{-6}$. Indeed, 37 values of λ_u are investigated. Concerning the electric drive dynamic behaviour analysis, 0-3000 acceleration at no-load initial working condition is considered. It must be underlined that, in order to maximize the control granularity, the control has been further optimized and the sampling frequency has been increased up to 50 kHz. As a way of example, Fig. III. 32 shows an oscilloscope screen of phase voltages, phase currents, and related spectra, with a weighting factor $\lambda_u=9.36 \cdot 10^{-5}$. It can be noted that, although the apparent switching frequency is very low (890 Hz for this weighting factor value), the current trends are quite sinusoidal and the no relevant distortions are noted, as it is confirmed by the current spectrum, where the 7th harmonic exhibits the highest amplitude, that is lower than 40 mA (about 1.1% of the fundamental amplitude).

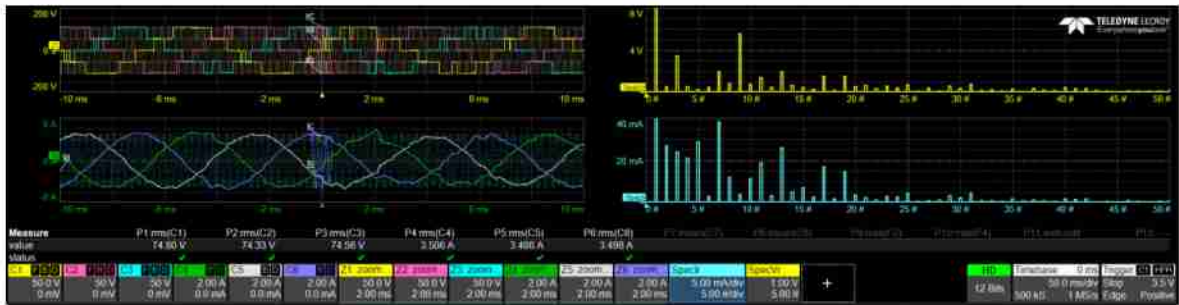


Fig. III. 32: Oscilloscope screen of phase voltages, phase currents, and related spectra when $n=3000$ rpm, $T=1.8$ Nm, $\lambda_u=9.36 \cdot 10^{-5}$, control sampling frequency $f_s=50$ kHz, switching frequency $f_{sw}=890$ Hz.

In Fig. III. 33, the current THD trend over the switching frequency is presented. Varying the weighting factor λ_u over the defined range allows for reducing the switching frequency from about 8 kHz to 900 Hz. In this range, the current THD varies from a minimum value of 6.5% to 10.35%. Despite the THD variability, it is possible to recognize a decreasing trend when the switching frequency increases. Moreover, it is possible to state that the current THD assumes values between 7% and 9% almost in the entire range. Then, varying the switching

frequency determines a modest variation of the current THD, encouraging the adoption of very low switching frequency values to minimize the switching losses.

For comparison purposes, current THD trends generated by traditional FOC with MC-PWM strategies in the same working conditions and shown in Section II.7 are reported. An extra THD point per each strategy, with $f_{sw}=5$ kHz, has been added. It can be noted that V²B-MPC guarantees a lower current THD over the entire range, proving the MPC superiority over the traditional electric drives control and modulation strategies.

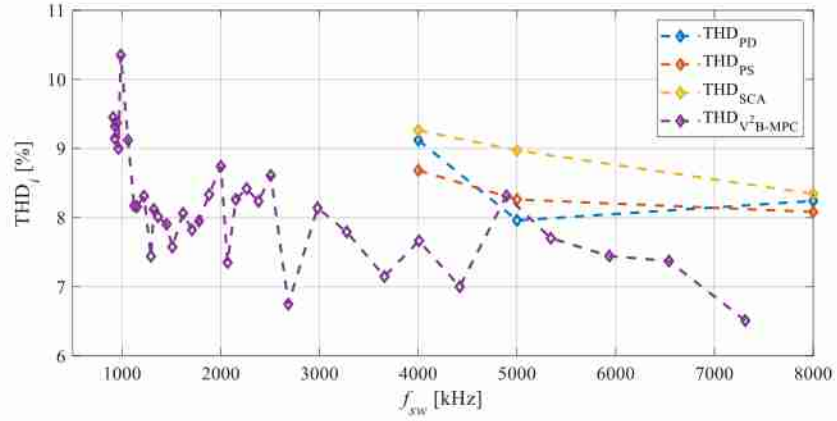


Fig. III. 33: Comparison between current THD trends over the switching frequency, generated by V²B-MPC and traditional FOC with most common MC-PWM strategies.

CHB-fed IPMSM drive speed and dq current trends during a 0-3000 rpm acceleration at no-load conditions, obtained by V²B-MPC with $\lambda_u=0$ and $\lambda_u=5.72 \cdot 10^{-5}$, are reported in Fig. III. 34.

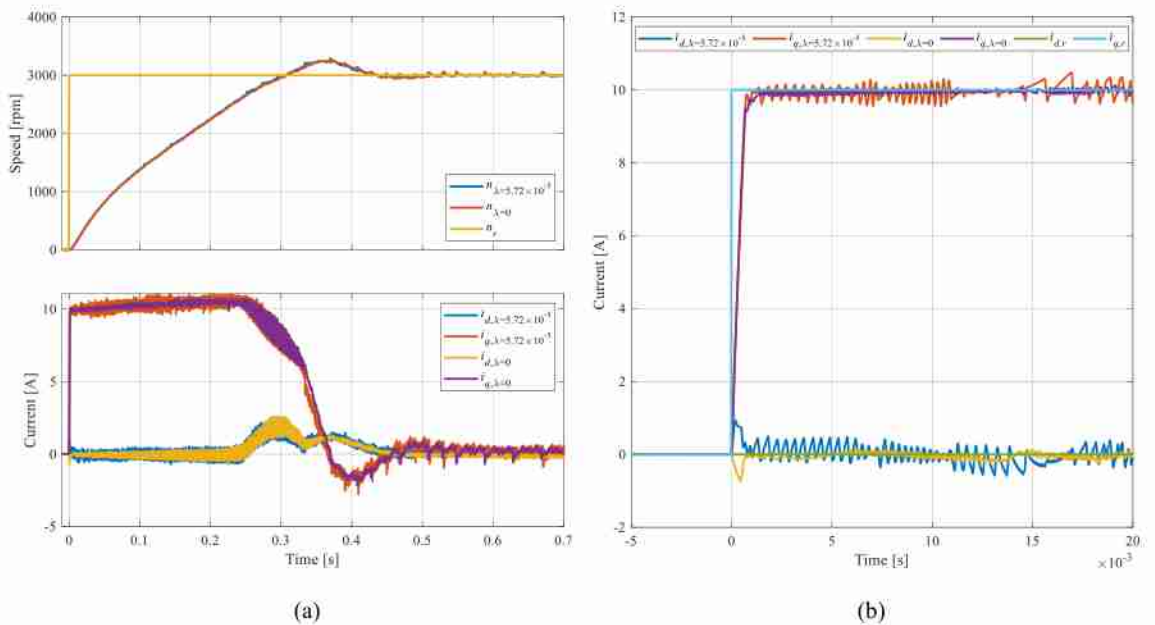


Fig. III. 34: (a) comparison between 0-3000 rpm acceleration at no load conditions with V²B-MPC when weighting factor $\lambda_u=0$ and $\lambda_u=5.72 \cdot 10^{-5}$, (b) zoom on dq current trends when the current q reference is varied.

The latter weighting factor value is chosen since it is considered a good compromise between low current THD and low switching frequency. The comparison shows that increasing the weighting factor does not affect at all the electric drive dynamic behaviour, since both speed and current trends are almost superimposed. Main difference among such trends is related to the higher current ripple recorded when λ_u is higher than zero, due to the lower switching frequency.

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Chapter IV Finite Control Set Model Predictive Control for Six-Phase Asymmetric PMSM Drives: Design, Implementation, and Simulation Analysis

IV.1 Introduction

Multi-phase machine drives are gaining attention both in the scientific and industrial community due to the several advantages they offer, if compared to traditional three-phase drives. In detail, they guarantee lower torque ripple, especially when soft-switching strategies are adopted, lower magnetic induction field space harmonics, power splitting among phases, and fault-tolerant capability [IV,1]-[IV,2]. For such reasons, multi-phase machine drives find applications in electric ship propulsion, railway traction, EV propulsion, more electric aircraft, and wind power generation [IV,3]-[IV,6]. In detail, asymmetric six-phase machines represent the preferred choice in most of the previously listed applications, due to their compatibility with commercial three-phase power converters.

The FCS-MPC has been extensively discussed in Chapter III, regarding the three-phase electric drive application. Nevertheless, its distinctive features, including the adoption of the state-space dynamic model of the controlled system, the ability to pursue multiple and conflicting control objectives, and finally, the direct control of command signals without the adoption of a modulation stage, make MPC appealing even in the field of asymmetric six-phase drives [IV,7]-[IV,8].

However, as discussed in Chapter III, the main drawback of FCS-MPC is represented by its computational burden that grows exponentially not only with the number of the inverter voltage levels, but also with the number of phases. For a 2L-VSI-fed Six-Phase Asymmetric

Permanent Magnet Synchronous Machine (6P-APMSM) drive, 64 predictions must be carried out. Then, FCS-MPC computational burden reduction is a hot topic in the literature and several researchers made efforts to fulfill such a goal. Barrero *et al.* compare in [IV,9] traditional and restrained search (RS)-MPC for a 6P-APMSM drive; in detail, concerning the RS-MPC, only 13 VVs, i.e., the outer VVs, which exhibit the biggest amplitude, and the zero vector, are considered. Such an assumption is frequently adopted in the literature and finds its origin in PWM-based controls [IV,10]. The same authors propose in [IV,11] other two RS-MPC strategies, named RSPC7v and RSPC16v, which are based on some switching rules: concerning RSPC7v, at most one phase leg can change state per sampling period, concerning RSPC16v, at most two phases legs can change state per sampling period. Authors of [IV,12] and [IV,13] propose similar strategies, which deal with finding the unconstrained optimal VV through a deadbeat control and synthesizing it by the application of multiple VVs (three and four VVs, respectively), each one with a certain duty cycle. Both strategies consider only the outer 12 VVs and the zero vector. In [IV,14], the concept of Virtual Voltage Vectors (V3) is adopted to minimize the xy currents: in detail, two parallel VVs on the $\alpha\beta$ subspace, which corresponds to two opposite VVs on the xy frame, are applied at each sampling period with a fixed duty cycle.

In this work, a novel Voltage-Vector-Subset-Based (V^2SB) FCS-MPC for a 6P-APMSM drive is proposed. In detail, the IQOCP is solved by investigating a subset of the VVs; which is selected online depending on the currently applied VV, i.e., the previous optimal solution. Indeed, the approach for reducing the computational complexity adopted for 5L-CHB-fed IPMSM drives discussed in Chapter III is applied to APMSM drives. The key novelty of this work and the main difference with the V^2B -MPC proposed in Chapter III deal with identifying subsets not only of adjacent VVs, but also quasi-adjacent VVs to the previous optimal one. Such subsets are defined by analyzing the most frequent VV paths selected by a traditional FCS-MPC. Indeed, transitions to quasi-adjacent VVs are much more frequent than adjacent VVs. By adopting such constraints, the number of required tests to find the solution of the IQOCP is equal to 14. Indeed, a remarkable reduction of the computational cost is fulfilled, if compared to the traditional FCS-MPC which requires 64 tests for a 6P-APMSM drive, without drastically affecting the system steady state and dynamic performance. This activity was carried out in collaboration with the Institute of Power Electronics System (ELSYS) of the Technische Hochschule Nürnberg Georg-Simon Ohm during the PhD visiting period.

IV.2 FCS-MPC Formulation for 6P-APMSM Drive

In this section, the FCS-MPC is formulated. In detail, the 6P-APMSM drive control model is introduced and the cost function is defined. In Fig. IV. 1 the 2L-VSI-fed 6P-APMSM drive scheme is reported. The electric drive mathematical model is formulated by adopting the Vector Space Decomposition (VSD) approach proposed in [IV,10], which allows for projecting the original six-dimensional space into three two-dimensional orthogonal subspaces, identified as $\alpha\beta$, xy , and o_1o_2 .

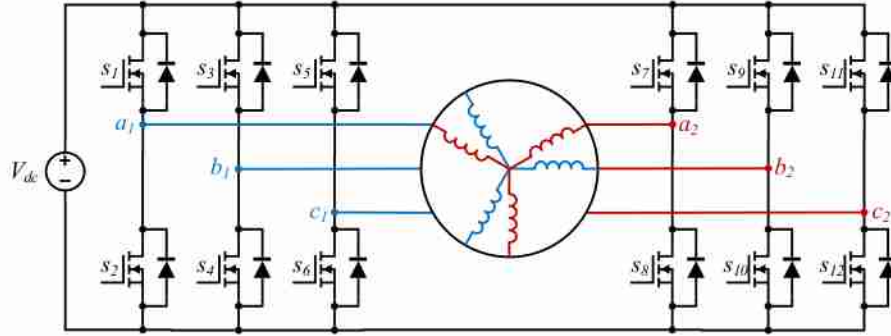


Fig. IV. 1: 2L-VSI-fed asymmetric six-phase PMSM drive scheme.

Such an approach allows for mapping machine variables harmonics into specific subspaces, such that the fundamental components and harmonics with order $12m \pm 1$ are mapped into the $\alpha\beta$ subspace, harmonics with order $6m \pm 1$ are mapped into the xy subspace, and zero-sequence harmonics are mapped into the o_1o_2 subspace. By assuming the magnetomotive force in the air gap is sinusoidal, harmonics mapped into the xy and o_1o_2 subspaces do not contribute to torque generation. As a consequence, current harmonics mapped into the xy subspace determine harmonic distortion and copper losses, thus minimization of such harmonics represents an essential control objective. Moreover, due to the floating neutral points, no currents appear in the o_1o_2 subspace, thus for current control purposes, it can be ignored. The VSD matrix $\mathbf{T}_{VSD}$ is reported in (IV,1):

$$\mathbf{T}_{VSD} = \frac{1}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{2} & \frac{1}{2} & -1 \\ 1 & -\frac{1}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & 0 \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{1}{2} & \frac{1}{2} & -1 \end{bmatrix} \quad (\text{IV},1)$$

The $dqxy$ transformation matrix $\mathbf{T}_{dqxy}$, is reported below:

$$\mathbf{T}_{dqxy} = \begin{bmatrix} \cos(p\theta_m) & \sin(p\theta_m) & 0 & 0 \\ -\sin(p\theta_m) & \cos(p\theta_m) & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad (\text{IV},2)$$

where θ_m is the rotor mechanical angular position and p is the number of pole pairs. It must be noted that only the $\alpha\beta$ subspace is projected in a rotating reference frame. Thus, electrical machine variables $\mathbf{i}_{dqxy}=[i_d \ i_q \ i_x \ i_y]^T$ and $\mathbf{v}_{dqxy}=[v_d \ v_q \ v_x \ v_y]^T$ in the $dqxy$ reference frame are obtained according to (IV,3) and (IV,4):

$$\mathbf{i}_{dqxy} = \mathbf{T}_{dqxy} \mathbf{T}_{VSD} \mathbf{i}_{abc12} \quad (\text{IV},3)$$

$$\mathbf{v}_{dqxy} = \mathbf{T}_{dqxy} \mathbf{T}_{VSD} \mathbf{v}_{abc12} \quad (\text{IV},4)$$

where $\mathbf{i}_{abc12}=[i_{a1} \ i_{b1} \ i_{c1} \ i_{a2} \ i_{b2} \ i_{c2}]^T$ and $\mathbf{v}_{abc12}=[v_{a1} \ v_{b1} \ v_{c1} \ v_{a2} \ v_{b2} \ v_{c2}]^T$ represent the electrical machine variables in the original six-dimensional state. The 6P APMSM model is based on the same hypothesis mentioned in Chapter II concerning the 3P-IPMSM, that are reported below: the core saturation is neglected; hysteresis and eddy currents are neglected; the electromotive force is sinusoidal. Then, according to [IV,15], the following stator voltage balancing equations in the $dqxy$ reference frame are obtained:

$$v_d = Ri_d + L_d \frac{d}{dt} i_d - p\omega_m L_q i_q \quad (\text{IV},5)$$

$$v_q = Ri_q + L_q \frac{d}{dt} i_q + p\omega_m (L_d i_d + \psi_{PM}) \quad (\text{IV},6)$$

$$v_x = Ri_x + L_x \frac{d}{dt} i_x \quad (\text{IV},7)$$

$$v_y = Ri_y + L_y \frac{d}{dt} i_y \quad (\text{IV},8)$$

$$T_{em} = 3p(\psi_{PM} i_q - (L_q - L_d) i_d i_q) \quad (\text{IV},9)$$

with L_d, L_q, L_x, L_y are the absolute inductances, R is the stator winding resistance, ω_m is the mechanical rotor speed, ψ_{PM} is the permanent magnet flux linkage. Such equations allow for formulating the forward-Euler discretized prediction model in the $dqxy$ reference frame as follows:

$$\mathbf{i}_{dqxy}(k+1) = \mathbf{A} \mathbf{i}_{dqxy}(k) + \mathbf{B} \mathbf{v}_{dqxy}(k) + \mathbf{K} \quad (\text{IV},10)$$

where matrices $\mathbf{K}$, $\mathbf{B}$, and $\mathbf{A}$ are defined as follows:

$$\mathbf{A} = \begin{bmatrix} 1 - \frac{T_s R}{L_d} & \frac{p\omega_m T_s L_q}{L_d} & 0 & 0 \\ -\frac{p\omega_m T_s L_d}{L_q} & 1 - \frac{T_s R}{L_q} & 0 & 0 \\ 0 & 0 & 1 - \frac{T_s R}{L_x} & 0 \\ 0 & 0 & 0 & 1 - \frac{T_s R}{L_y} \end{bmatrix}, \mathbf{B} = \begin{bmatrix} \frac{T_s}{L_d} & 0 & 0 & 0 \\ 0 & \frac{T_s}{L_q} & 0 & 0 \\ 0 & 0 & \frac{T_s}{L_x} & 0 \\ 0 & 0 & 0 & \frac{T_s}{L_y} \end{bmatrix}, \mathbf{K} = \begin{bmatrix} 0 \\ -\frac{p\omega_m T_s \psi_{PM}}{L_d} \\ 0 \\ 0 \end{bmatrix} \quad (\text{IV},11)$$

where T_s is the sampling interval.

With respect to the 6P-2L-VSI scheme reported in Fig. IV. 1, by taking into account that switch on the same leg must work in complementary way, the phase voltage v_j , with $j \in \{a1,$

$b_1, c_1, a_2, b_2, c_2\}$ is related to the leg top device GCS s_x , with $x \in \{1, 3, 5, 7, 9, 11\}$, according to (IV,12):

$$v_j(k) = \frac{V_{dc}}{2} (2s_x - 1) \quad (IV,12)$$

where V_{dc} is the DC link voltage.

A prediction horizon $N_p=1$ is adopted and the control goals are synthesized into the cost function J , which is formulated by taking into account the current reference tracking term and the switching effort penalization term, as follows:

$$J = \|\mathbf{i}_{dqxy}^*(k+1) - \mathbf{i}_{dqxy}(k+1)\|_2^2 + \lambda \|\Delta \mathbf{v}_{abc12}(k)\|_1 \quad (IV,13)$$

where $\mathbf{i}_{dqxy}^*(k+1) = [i_d^*(k+1) \ i_q^*(k+1) \ i_x^*(k+1) \ i_y^*(k+1)]^T$ is the reference currents vector, $\mathbf{i}_{dq}(k+1) = [i_d(k+1) \ i_q(k+1) \ i_x(k+1) \ i_y(k+1)]^T$, $\Delta \mathbf{v}_{abc12} = \mathbf{v}_{abc12}(k) - \mathbf{v}_{abc12}(k-1)$, and λ is the weighting factor.

IV.3 Voltage Vector Subset-Based MPC Formulation

In this section, the proposed V^2SB -MPC is presented. Taking into account the VSD matrix and the 6P-2L-VSI mathematical model, reported in (IV,1) and (IV,12) respectively, the VVs in the $\alpha\beta$ and xy subspaces, whose representation is reported in Fig. IV. 2 (a) and (b) respectively, are obtained.

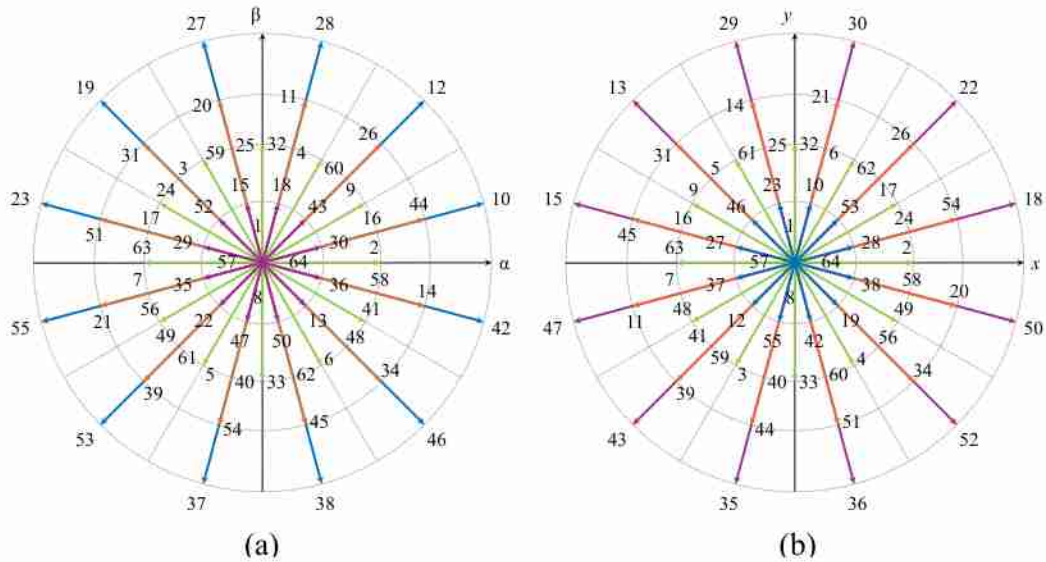


Fig. IV. 2: VVs related to 2L-6P VSI (a) $\alpha\beta$ subspace, (b) the xy subspace.

According to (III,27), the number of available VVs is equal to $2^6 = 64$. By looking at Fig. IV. 2, it can be noted that, both in the $\alpha\beta$ and xy subspaces, VVs are arranged on four concentric circles with the zero vector as the center. The VVs which lie on the second inner circle, i.e., the green VVs, and also the zero vector are characterized by a degree of

redundancy equal to one and three, respectively. This means that only 49 non-redundant VVs can be identified. Considering now the GCSs combinations, by applying the equation (III,28), it is easy to prove that the number of GCSs combinations coincides with the number of available VVs. It follows that a 6P-2L-VSI is characterized by redundancy of VVs, i.e., several PVCs produces superimposed VVs, but each VV can be generated by only one GCSs combination.

Thus, to solve the IQOCP, the future system state must be predicted 64 or 49 times, depending on whether the redundancies are considered. To reduce the number of predictions, the traditional FCS-MPC behaviour is investigated. The goal is to identify the most common VV paths selected by the traditional FCS-MPC; such analysis allows for defining subsets of VVs within which the optimal solution of the IQOCP is very likely to fall, especially in steady-state conditions. Such analysis is carried out by simulating the 6P-APMSM drive in the Matlab\Simulink environment in several Working Points (WPs), defined for the 90%, 75%, 50%, 25%, and 4% of the rated speed and for the 100%, 75%, 50% and 25% of the rated load torque. In Table IV. 1 and Table IV. 2, the simulation data and the investigated WPs are reported, respectively. Simulations are carried out with a maximum step size equal to 1 μ s, the simulation window T_W is varied over the working range to sample 10 electrical periods in steady-state conditions.

Table IV. 1: Simulation data.

Quantity	Symbol	Value
Pole pairs	p	5
Stator resistance	R	0.27 Ω
d -inductance	L_d	1.7 mH
q -inductance	L_q	3.8 mH
x -inductance	L_x	2.4 mH
y -inductance	L_y	2.5 mH
PM direct flux	Ψ_{PM}	0.19 Vs
Rated eff. line-line voltage	V_r	400 V
Rated eff. phase current	I_r	7.1 A
Rated mechanical speed	n_r	3000 rpm
Rated mechanical torque	T_r	28 Nm
DC link voltage	V_{DC}	565 V
Control sampling frequency	f_s	100 kHz
Simulation max step size	T_{mss}	1 μ s

Table IV. 2: Simulated working points.

T [Nm]- n [rpm]	120	750	1500	2250	2700
28	WP5	WP4	WP3	WP2	WP1
21	WP10	WP9	WP8	WP7	WP6
14	WP15	WP14	WP13	WP12	WP11
7	WP20	WP19	WP18	WP17	WP16

As an example, the VVs paths determined by the traditional FCS-MPC, when the system is in WP15, WP8, and WP1, are reported in Fig. IV. 3 (a), (b), and (c), respectively. The VV

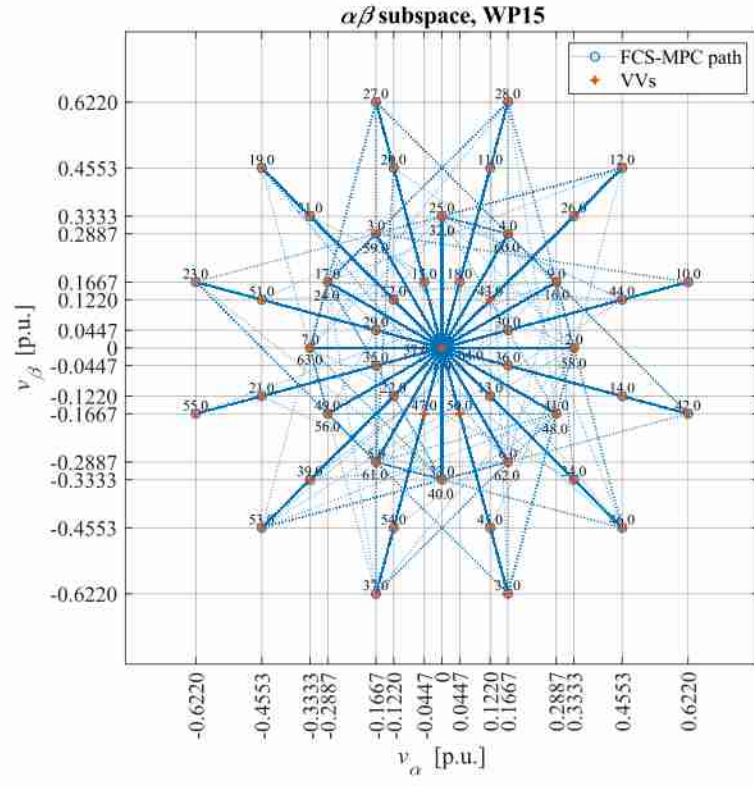
path is drawn by a dotted line, thus as the path is been run more frequently, the thicker the line becomes. Such analysis leads to the following considerations:

- VVs that lie on the inner circle are rarely used, even at low-speed conditions. Such behaviour can be explained by noticing that such vectors on the $\alpha\beta$ subspace correspond to the biggest VVs in the xy subspace, which are most of the time naturally discarded to minimize the xy currents;
- most of the time, the system moves to non-adjacent VVs to the currently applied one. For example, by adopting VV3 as representative of VVs which lie on the same circle, transitions 3-1, 3-28, 3-23, 3-19 and 3-27 are carried out frequently; similarly, by adopting 19 as representative of VVs which lie on its same circle, transitions 19-23, 19-27, 19-28, 19-55, 19-7, 19-25 are very frequent.

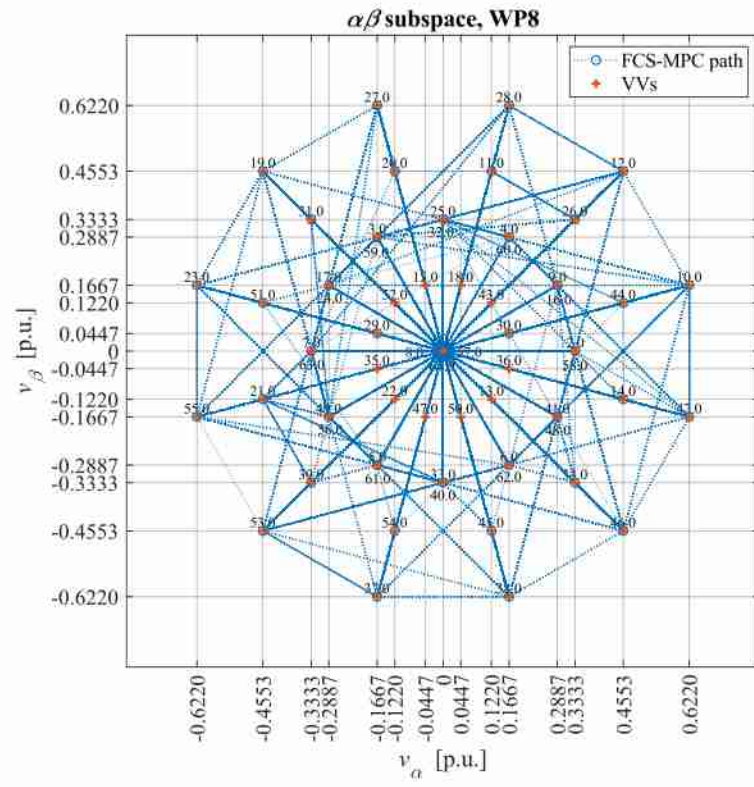
Taking into account such considerations, the VVs subsets reported in Fig. IV. 4 are identified. In detail, concerning Fig. IV. 4 (d), the VVs that lie on the inner circle are never considered, thus the green VVs are adopted as an intermediate step between the outer VVs and the zero vector. The subsets reported in Fig. IV. 4 (a), (b), (c), and (d) are shown by adopting VVs 19, 21, 3, and 1 as previous optimum vectors, however, such subsets are valid for all the other VVs which lie on their same circle, after an appropriate subset rotation. By taking into account the proposed subsets, the number of required tests to solve the IQOCP is equal to 14, except when the previous optimal VV is the zero vector, then only 13 tests are required. Thus, the proposed strategy allows for a drastic computational cost reduction, if compared to the standard FCS-MPC: indeed, at most 14 against 64 or 49 tests are required, depending on whether redundancies are considered or not, respectively. The IQOCP can be formulated as follows:

$$\begin{aligned} \mathbf{v}_{abc12,opt}(k) &= \arg \min J(\mathbf{i}_{dqxy}(k+1), \mathbf{v}_{abc12}(k-1)) \\ \text{subject to } &\begin{cases} \mathbf{i}_{dqxy}(k+1) = \mathbf{A}\mathbf{i}_{dqxy}(k) + \mathbf{B}\mathbf{v}_{dqxy}(k) + \mathbf{K} \\ \mathbf{v}_{abc12}(k) \in \mathcal{U}(k) \end{cases} \end{aligned} \quad (\text{IV},14)$$

where $\mathcal{U}(k)$ represents the subset of available VVs at the sampling instant k , which depends on the previous optimal VV.



(a)



(b)

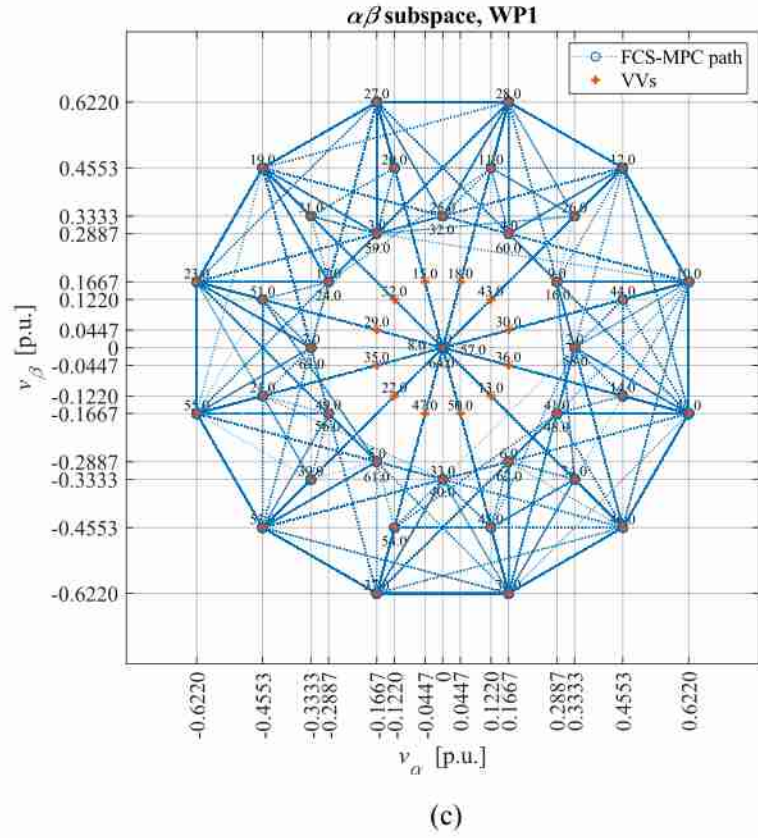
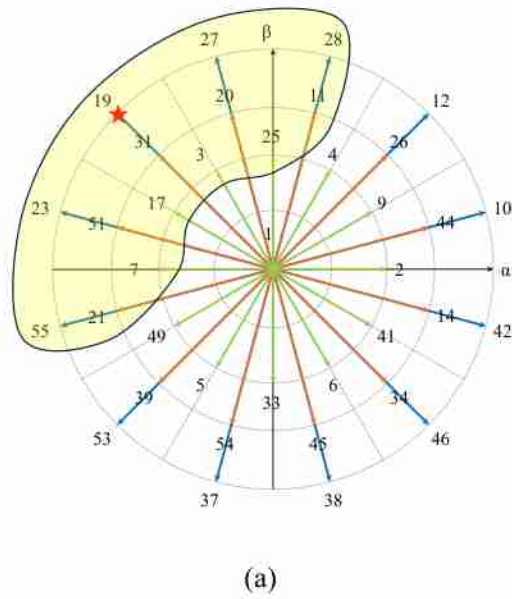
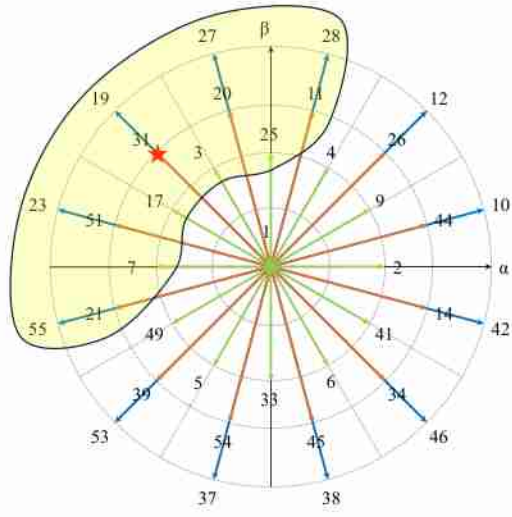
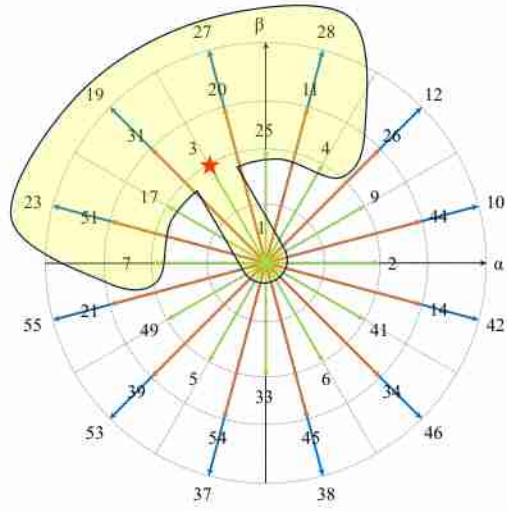


Fig. IV. 3: VV path in the $\alpha\beta$ subspace carried out by traditional FCS-MPC in steady state conditions during different simulated working points: (a) WP15, (b), WP8, (c) WP1.

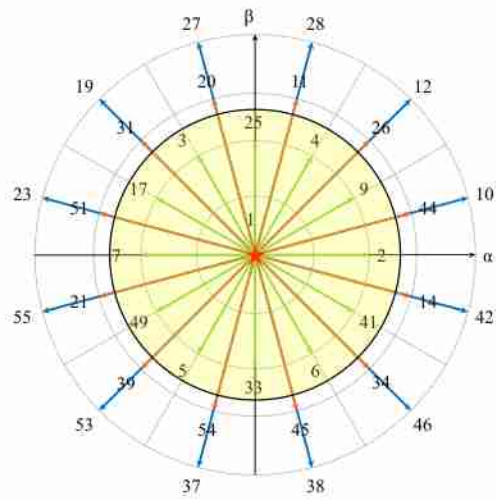




(b)



(c)



(d)

Fig. IV. 4: Proposed VVs subsets related to previous optimal VV (labeled with ★) which lies on one of the concentric circles: (a) VVs subset when the previous optimal VV is 19, (b) VVs subset when the previous optimal VV is 31, (c) VVs subset when the previous optimal VV is 3, (d) VVs subset when the previous optimal VV is 1.

IV.4 Voltage Vector Subset-Based MPC Implementation

Implementation of the proposed V²SB-MPC is carried out similarly to the procedure discussed in Chapter III regarding the V²B-MPC. In detail, the proposed control algorithm is implemented according to the control scheme reported in Fig. IV. 5.

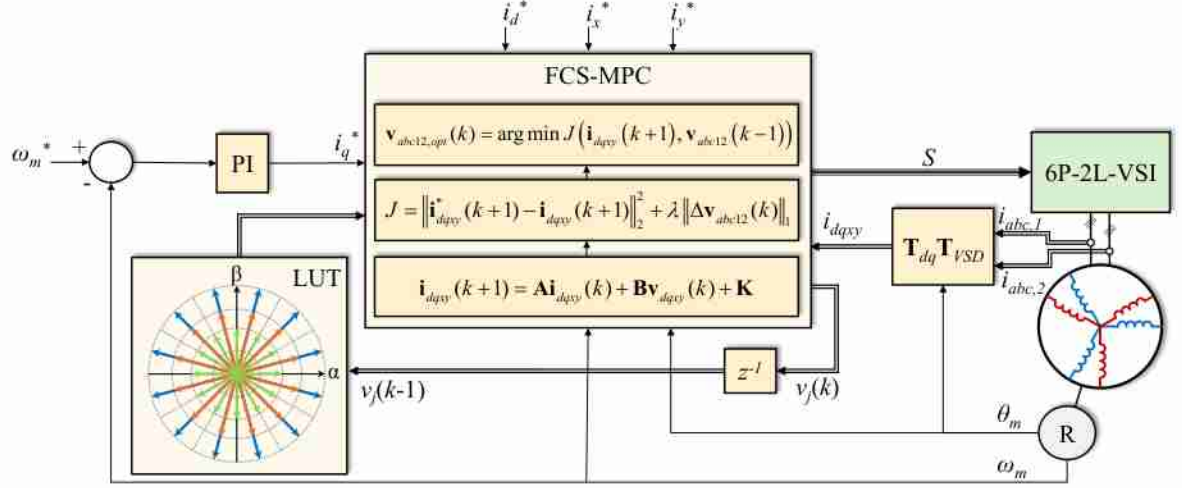


Fig. IV. 5: Proposed V²SB-MPC block scheme.

To simplify the algorithm implementation, redundancies are eliminated, thus each VV is identified by one PVC and one GCSs combination. The set of subsets is stored in a LUT. Each VV is identified by an index j , according to the enumeration reported in Fig. IV. 4; such an index is used to identify the optimal VV at the previous sampling instant $v_j(k-1)$ and navigate the LUT to find the subset of available VVs at the current sampling instant. Then, the future system state is predicted 14 times, and the optimal VV $v_j(k)$, which minimizes the cost function J , is identified and the related GCSs combination is applied to the system.

IV.5 Simulation Results

In this section, the proposed V²SB-MPC strategy is validated through simulation analysis. In detail, the 6P-APMSM drive performance is investigated in steady-state and dynamic working conditions. In both cases, the proposed V²SB-MPC is compared with the traditional FCS-MPC and with the RS-MPC strategies proposed in [IV,9] and [IV,11]. Over the following discussions, each strategy will be identified by the number of tests t required to solve the IQOCP: the traditional FCS-MPC is identified as $64t$ -MPC; the strategy proposed in [IV,9] which takes into account only the outer VVs in the $\alpha\beta$ subspace, is identified as $13t$ -MPC; the strategies proposed in [IV,11] which are based on switching rules such that only one or two VSI legs can change state per sampling period, are identified as $7t$ -MPC and $16t$ -MPC, respectively. Concerning the steady state performance analysis, at first, the electric drive performance over the working range defined in Table IV. 2 is carried out. Such

analysis is carried out without penalizing the 6P-2L-VSI switching effort. As comparison tools, the current THD and the switching frequency f_{sw} are adopted. The THD is evaluated according to equation (I,40). The switching frequency is f_{sw} is evaluated as the mean value of the GCSs transitions over the simulation window T_w , according to:

$$f_{sw} = \frac{1}{6} \cdot \sum_{n=0}^5 \frac{N_{sw,2n+1}}{2T_w} \quad (\text{IV},15)$$

where $N_{sw,2n+1}$ is the number of gate control signals transitions, $n \in \{0, 1, 2, 3, 4, 5\}$ allows for identifying the top device leg gate control signal s_x , with $x \in \{1, 3, 5, 7, 9, 11\}$.

Subsequently, the 6P-2L-VSI switching effort is penalized to investigate the current THD- f_{sw} trend: the weighting factor λ is varied over the range 0-0.004 with a step size of $8.16 \cdot 10^{-5}$, i.e., 50 values of λ are considered. Per each considered MPC strategy, the electric drive simulation is carried out in WP1 varying λ over the defined working range.

Finally, the dynamic performances are evaluated by imposing a 0-20 A step variation of the reference current i_q^* . Every simulation is carried out with d -, x -, and y -reference currents set to 0.

IV.5.1 Steady state analysis

With respect to the cost function reported in (IV,13), the first set of simulations are carried out with the weighting factor $\lambda=0$, i.e., the switching effort is not penalized. In , a comparison between current trends in time and frequency domain related to the discussed MPC strategies is shown, when the controlled system is in WP2 ($n=2250$ rpm and $T=28$ Nm). It can be noted that the proposed 14t-MPC strategy exhibits a comparable spectrum with traditional 64t-MPC, which determines the lowest harmonic content over the entire spectrum. Indeed, current harmonics amplitude is always lower than 1%. Moreover, 13t-MPC presents the worst harmonic content, since it is characterized by 5th and 7th harmonics with remarkable amplitude, equal to 5% and 3.3%, respectively.

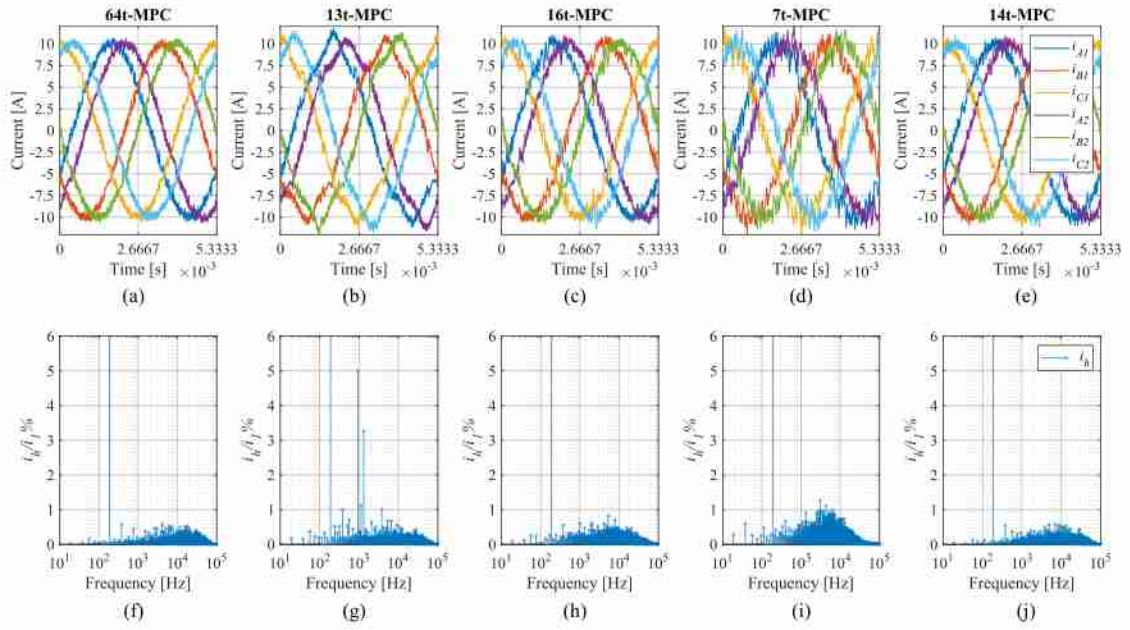


Fig. IV. 6: Comparison between current trends produced by the discussed MPC strategies in the time domain (a-e) and frequency domain (f-j) when the system is in WP2.

In Fig. IV. 7, the adopted comparison tools are reported over the defined working range. With respect to the THD, the proposed control strategy determines a lower THD, if compared to the other RS-MPCs, with a THD that goes from about 6% to 24%. However, the traditional 64t-MPC shows the lowest THD over the entire working range, it goes from 5% to 20%. Such results show that all RS-MPCs and the proposed V²SB-MPC always lead to suboptimal solutions since not all the VVs are available. However, the proposed strategy represents a good compromise between computational cost and harmonic distortion. Concerning the switching frequency, it can be noted that it grows with the mechanical speed, independently of the adopted MPC strategy. 64t-MPC and 13t-MPC exhibit the highest switching frequency, whose maximum values are 20 kHz and 18 kHz, respectively. 7t-MPC and 16t-MPC exhibit the lowest switching frequency over the entire range, whose maximum values are 12 kHz and 7.752 kHz, respectively. Such behaviour is linked with the inverter legs-based constraints. The 14t-MPC exhibits a maximum switching frequency equal to 16 kHz, which is in between the other strategies.

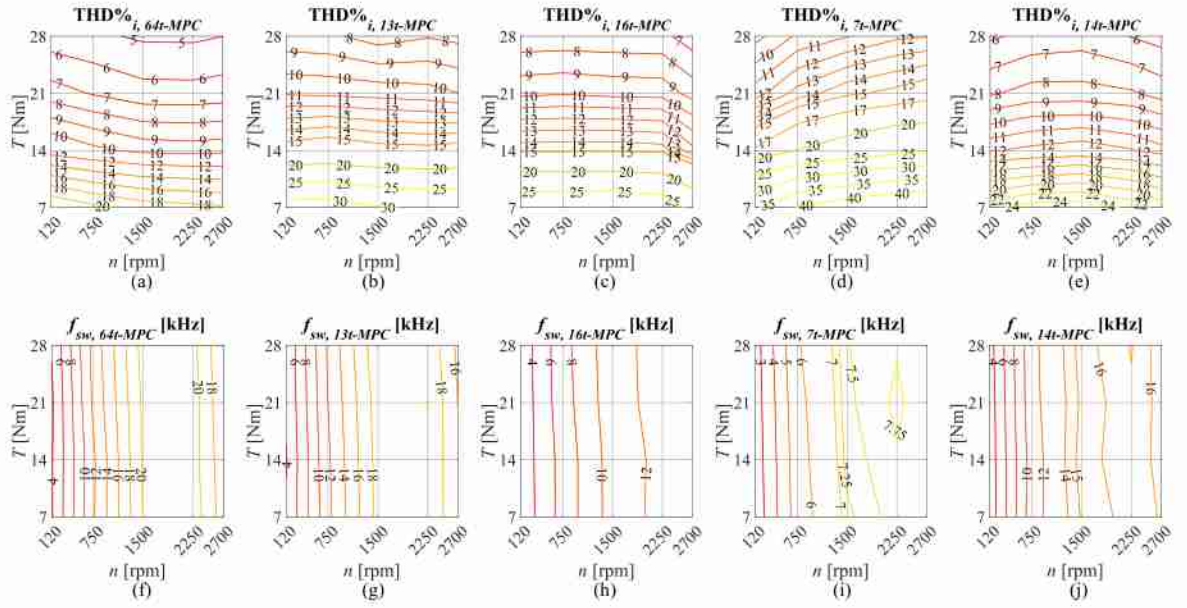


Fig. IV. 7: Comparison between the current THD (a-e) and the switching frequency (f-j) related to the discussed MPC strategies over the defined working range.

To complete the steady-state condition analysis, the 6P-2L-VSI switching effort is penalized to investigate the current THD- f_{sw} trends: in detail, per each considered MPC strategy, 50 values of the weighting factor λ in the range 0-0.004 are considered. In Fig. IV. 8, a comparison between the current THD- f_{sw} trend related to each considered MPC strategy is reported. Such trends confirm that the RS-MPC strategies and the proposed V²SB-MPC lead to a suboptimal solution, if compared to the traditional FCS-MPC strategy, since the traditional MPC exhibit always the lowest current THD for fixed switching frequency. However, the proposed 14t-MPC strategy exhibits a comparable behaviour with the 64t-MPC strategy in the high switching frequency range. Indeed, when f_{sw} is higher than 12 kHz, the proposed 14t-MPC strategy guarantees a current THD of around 6%, outperforming the 13t-MPC, which is the only RS-MPC able to reach such switching frequency range and which exhibits a current THD of around 8%. In the range 6-12 kHz, the proposed 14t-MPC and the 16t-MPC strategies exhibit a comparable current THD, which goes from 7% to 12%.

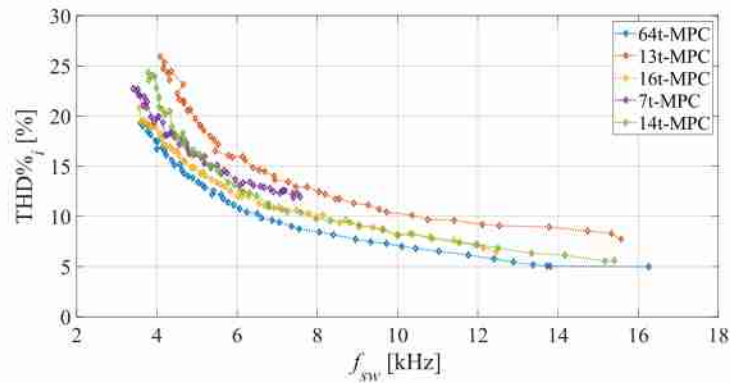


Fig. IV. 8: Comparison between the current THD- f_{sw} trends related to the discussed MPC strategies.

IV.5.2 Dynamic Performance Analysis

In , a comparison between 6P-APMSM drive step responses related to the discussed MPC strategies is reported. In detail, a 0-20 A step variation of the q -reference current is applied, while d -, x -, and y -reference currents are set to 0. Such comparison shows that 7t-MPC determines a remarkable current overshoot if compared to other strategies; moreover, the 13t-MPC strategy is not able to track the y -current reference, since the y current is different than zero even when the q -current reaches the desired value. Such behaviour causes 5th and 7th harmonics over the current spectrum, as discussed in section IV.A. With respect to the q -current step response, to carry out an accurate comparison, the q -current step responses related to the discussed strategies are overlapped in Fig. IV. 10. The comparison shows no remarkable differences among the discussed strategies. Indeed, it can be stated that the proposed V²SB-MPC strategy guarantees a good dynamic response, which is comparable with the traditional FCS-MPC strategy.

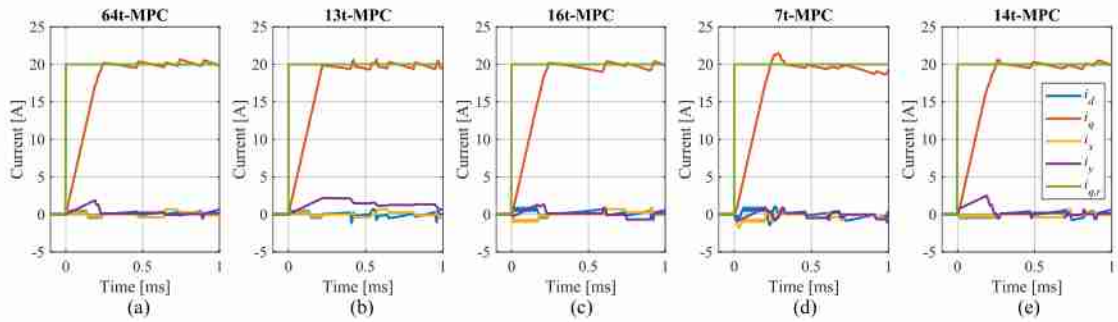


Fig. IV. 9: Comparison between 6P-APMSM drive step responses related to the discussed MPC strategies under a 0-20 A q -reference current step variation.

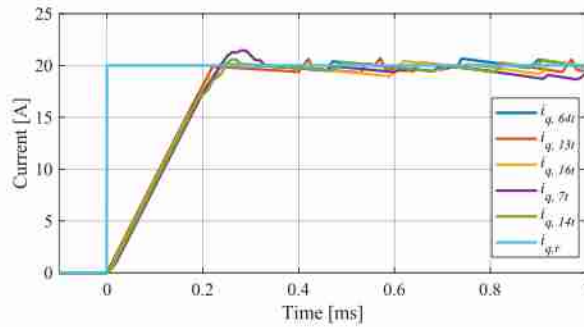


Fig. IV. 10: Direct comparison between q -current step responses produced by the discussed MPC strategies under a 0-20 A q -reference current step variation.

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Conclusions

In this thesis work, the research activities carried out within the PhD project in “Energy” entitled "*Development of an innovative electric drive with multilevel inverter for e-mobility applications*" is presented. Such a research activity was carried out by the author of this work in the period from November 2021 to October 2024 at the SDESLAB and LEAP laboratories of the University of Palermo. Part of the research activity was carried out during a visiting period at the Institute of Power Electronics System (ELSYS) of the Technische Hochschule Nürnberg Georg-Simon Ohm, from November 15, 2023 to May 29, 2024.

After an accurate bibliographic research, reported partly in the introduction of this work and partly in the incipit of the various chapters, it was highlighted that the CHB multilevel converter offers numerous opportunities in the field of sustainable mobility: it, through its modular structure, allows for following the market trend of increasing the EVs battery pack rated voltage, thus determining the increase in power density and allowing XFC and, at the same time, allows for overcoming the limits of a traditional 2L-VSIs, such as high harmonic content of voltages and currents, EMIs issues, and high dv/dt . Furthermore, it offers new and unique possibilities related to its circuit topology, such as increased vehicle reliability thanks to fault tolerant operation and easy HESS management thanks to its modular structure. Despite the opportunities previously discussed, electric drives fed by CHB inverters are little investigated in the literature and their diffusion on the market is severely limited.

Therefore, this PhD project aims to design, implement and analyze the performances of a 3P-5L-CHB-fed IPMSM drive for electric mobility applications. Particular attention is paid to the implementation of modulation and control strategies of the electric drive, aimed at maximizing the system efficiency and dynamic performances. In fact, although the CHB inverter represents a consolidated technology, its performances are strongly influenced by the adopted modulation and control strategies. Indeed, analyzing and developing control

strategies for MI-fed electric drives is currently an open topic and a research area of strong interest in industry and in the scientific community.

With this aim, Chapter I presents an experimental performance analysis of the CHB inverter controlled by several MC-PWM strategies. In detail, analysis is devoted to investigate the impact of the MC-PWM strategies and the switching frequency on the CHB inverter performance in terms of voltage THD and converter efficiency. Experimental results show that PD-PWM strategy guarantees the lowest voltage THD and the highest inverter efficiency, independently of the considered amplitude modulation index and switching frequency. Its main drawback is related to the uneven power distribution among CHB SMs, which is a major issue in vehicular applications, since it determines an uneven discharge of battery modules. On the contrary, PS-PWM strategy guarantees the same power absorption among CHB SMs, almost in every working conditions. Moreover, for fixed carriers frequency, It allows for shifting the voltage harmonic in the high frequency range, allowing for an easy current filtering. However, it exhibit the worst voltage THD and the worst inverter efficiency over the investigated working range, especially at low amplitude modulation index. SCAMOD exhibit an intermediate behaviour among PD-PWM and PS-PWM strategies, both in terms of voltage THD and efficiency. However, it guarantees even power distribution among SMs only when the number of cascaded SMs per phase is equal to two.

Generally, it can be noted that when the switching frequency increases, an increase of the voltage THD and a reduction of the converter efficiency are recorded. This behavior is common to all investigated MC-PWM strategies, albeit to varying degrees. Regarding the voltage THD, its decrement is correlated to a progressive decrement of the fundamental harmonic amplitude with the switching frequency. In order to investigate this behaviour, the DT is adopted as a modulation parameter. In detail, a generalized mathematical model that allows for estimating the fundamental harmonic voltage drop is proposed. Such a mathematical model allows for taking into account the specific behaviour of each considered MC-PWM strategy through a proper correction coefficient. The model is experimentally validated, showing that the PS-PWM strategy determines the highest fundamental voltage drop. Then, the previous experimental investigation is repeated by considering the DT as a modulation parameter. Such analysis confirmed the previous results in terms of voltage THD and converter efficiency, showing a general increase in voltage THD and a reduction in converter efficiency when the DT increases. Moreover, the PHD and the THD_{LF} are adopted to investigate the DT impact on the high-frequency and low-frequency harmonics

respectively. Results show that the DT strongly affects the low-frequency harmonics, determining their progressive increase when the DT increases.

The Chapter II deals with the implementation and performance analysis of the 3P-5L-CHB-fed IPMSM drive. For this application, the FOC is adopted, since it is the most commonly adopted control strategies in several electric drives applications. Even in this case, experimental analysis deals with investigating the MC-PWM strategies impact on electric drive performance in terms of current THD and IPMSM efficiency. With this aim, only three of the previously adopted MC-PWM strategies are selected, i.e., PD, PS, and SCAMOD, and the investigated switching frequency range is modified compared to the previous chapter to select lower switching frequency values, in the range 4-16 kHz, commonly used in vehicular applications to reduce the inverter switching losses. In order to highlight the benefits related to the adoption of the CHB inverter, a comparison with a traditional 2L-VSI-fed IPMSM drive is carried out. Concerning the current THD, experimental results show that the CHB guarantees a much lower current THD if compared to the 2L-VSI almost in every considered WP and for every MC-PWM strategy, especially at low speed and low torque working conditions and for low switching frequency values. Moreover, CHB guarantees the highest IPMSM efficiency if compared to the 2L-VSI, independently of the adopted MC-PWM strategy. Finally, harmonic power loss analysis is carried out: in detail, through the harmonic power segregation approach, fundamental power losses and the harmonic power losses are identified. Experimental results show that, when CHB is adopted, the majority part of the IPMSM power losses are segregated at the fundamental frequency. In detail, percentage fundamental power losses are always higher than 90% over the entire working range, while are about 70% with 2L-VSI. Such results allow for stating that, not only the CHB guarantee a higher IPMSM efficiency, but also, power losses are segregated at the fundamental frequency, allowing for their active control, for example through a devoted loss minimization algorithm, and drastically improving the overall powertrain efficiency. Comparing the MC-PWM strategies impact on IPMSM efficiency, PS-PWM guarantees the highest motor efficiency, although differences among MC-PWM strategies are negligible. Discussing the switching frequency impact on harmonic segregation, it can be noted that the higher the switching frequency, the higher the percentage fundamental power losses, especially at low-torque and low-speed working conditions.

Results presented so far allow for stating that the adoption of CHB inverter implies a drastic improvement of the IPMSM efficiency. In detail, the CHB outperforms the 2L-VSI in partial load and low-speed working conditions. This represents a killer feature for vehicular

applications, where the vehicle speed and load change depend on the traffic conditions and on the number of passengers and it results in a drastic increase of the EV autonomy.

Chapter III is devoted to designing and implementing novel control strategies for CHB-fed IPMSM drives. In detail, FCS-MPC is adopted since it allows for overcoming standard control limitations due to its multi-variable approach and multi-objective capability, improving the system performance and fulfilling several conflicting control goals. In detail, in electric drive applications, a multi-variable cost function reduces the current THD and the switching frequency, through proper terms devoted to tracking the current reference and limiting the switching frequency. Indeed, sampling frequency and switching frequency are independent control parameters and the last one can be actively controlled by properly weighting each cost function term. Indeed, such a feature makes the FCS-MPC an appealing candidate for vehicular applications, especially for heavy-duty trucks where high-power converters must be employed and the switching frequency must be minimized. Its main drawback is the high computational cost required to find the solution to the optimal control problem, due to the high number of required predictions. Indeed, when a CHB inverter is employed, solving the optimal control problem online and managing the converter redundant states is an issue. For this reason, a novel V^2B -MPC for a 3P-5L-CHB-fed IPMSM drive is proposed. It is designed to match the following control goals: computational burden minimization, CMVs minimization, GCS transitions minimization, phase voltages dv/dt minimization. Such goals are fulfilled through an offline procedure that aims to manage state redundancies. Indeed, such goals represent the criterion to select or discard a certain redundant VV or GCS combination. Once a unique match between VVs and GCSs is reached, the optimal control problem is solved online by looking for the optimal solution among a subset of VVs, which consists of the previous optimal one and its adjacent VVs. For comparison purposes, the proposed control strategy is compared to the CBCB-MPC strategy which is selected by the scientific literature. Experimental results showed that the V^2B -MPC outperforms the CBCB-MPC in steady-state working conditions, guaranteeing lower voltage and current THD, lower CMVs, and lower switching frequency over the investigated working range. Moreover, a comparison between f_{sw} - current THD trends with FOC and V^2B -MPC showed that the proposed strategy allows for reducing the current THD for fixed switching frequency, if compared to standard FOC strategy. Investigation on the CHB DC side showed that V^2B -MPC exhibits a similar behaviour to the LS-PWM strategies previously discussed, i.e., it does not guarantee homogenous power distribution among CHB SMs. Then the V^2B -MPC is improved to reach the SMs power balancing goal and the S^2VB -

MPC is designed. In detail, it allows for reaching the SMs power balancing goal by emulating the PS-PWM switching pattern. With this aim, the 3P-5L-CHB topology is treated as the composition of two SMs triplets, such that the slave triplet replicates the master triplet switching pattern with a sampling period delay. Once this switching constraint is introduced, the control is formulated according to the offline optimization procedure described for the V²B-MPC such that the same computation burden is reached. Experimental comparison between S²VB-MPC and V²B-MPC showed that, on the AC side, the two strategies guarantee similar electric drive performance both in steady state and dynamic working conditions. Concerning the DC side, S²VB-MPC guarantees SMs power balancing in every working condition, outperforming the V²B-MPC.

Chapter IV presents the activity carried out during the visiting period at the Institute of Power Electronics System of the Technische Hochschule Nürnberg Georg-Simon Ohm. Indeed, the design of low-computational burden FCS-MPC is extended to the Six-Phase drives, which represent an interesting solution in vehicular applications due to their high power density and reliability. Even in this case, the standard FCS-MPC exhibits a high computational burden due to the higher number of available VVs related to the higher number of phases. To overcome this limit, a V²SB-MPC for a 6P-APMSM drive is proposed. It allows for finding the solution to the optimal control problem by investigating a subset of VVs, composed of the previous optimal one and some adjacent and non-adjacent VVs, such that the number of required predictions is reduced from 64 to 14. Such VVs subsets are identified offline by emulating the standard FCS-MPC switching pattern, and they are selected online depending on the previous optimal VV. A comparative analysis is carried out in MATLAB/Simulink environment. In detail, the proposed strategy is compared with standard FCS-MPC and with some restrained search MPC strategies selected by the scientific literature. Simulation results prove the effectiveness of the proposed strategy, which represents a good compromise between system performance optimization and computational burden.

List of Publications

Articles

1. G. Schettino, G. Sorrentino, G. Scaglione, C. Nevoloso, A. O. Di Tommaso and R. Miceli, "A General Analytical Formulation for LCL Filter Design for Grid-Connected PWM-Driven Cascaded H-Bridge Inverters," in *IEEE Open Journal of Power Electronics*, vol. 5, pp. 1129-1148, 2024, doi: 10.1109/OJPEL.2024.3432990.
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3. C. Nevoloso, A. O. Di Tommaso, R. Miceli, G. Scaglione, S. Foti and A. Testa, "Impact Analysis of FOC-Based Synchronous PWM Strategy on Traction Induction Motor Drives Performance," *2024 International Conference on Electrical Machines (ICEM)*, Torino, Italy, 2024, pp. 1-7, doi: 10.1109/ICEM60801.2024.10700225.
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